TECHNICAL MANUAL

FOR

3 GHz FREQUENCY COUNTER

MODEL FRO-212-1

Astro Communication Laboratory

9125 Gaither Road
Gaithersburg, Maryland

WARNING

High voltages present within this instrument may cause serious injury or death.

NOTE

The instrument is equipped with a filtered cooling fan. The plastic filter should be removed, cleaned, and sprayed with a commercial filter-coat solution every 60 days. More frequent cleaning may be necessary in dusty environments.

INITIAL TESTING OF UNHEATED CRYSTAL OSCILLATORS

(Non-Ovenized)

Extensive testing of the aging rates of the unheated type crystal oscillators has recently been completed. Based on this research, verification of the published aging rate can be accurately determined within a reduced time interval. The following procedure will validate the initial aging specifications.

1. Attach a thermometer or temperature sensing device to the crystal case.

2. Apply instrument power for a twenty four hour period.

3. Measure the crystal's external temperature to within 1° C.

4. Measure the crystal oscillator's frequency to within 1 part in 10^7 (0.1 Hz).

5. After one week's continuous operation again measure the crystal temperature and output frequency.

6. The two frequencies will be within 2 parts in 10^6 (2 Hz), taking into consideration a temperature coefficient of $\pm 0.5 \times 10^{-6}$/° C.

7. The above test confirms the published oscillator specifications.

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INTRODUCTION

SECTION 1

INTRODUCTION

1.1 SCOPE

This manual describes the installation, operation, theory of operation, maintenance, calibration, and repair of the Astro Communications Laboratories Model FRO-212-1 Frequency Counter. It includes complete specifications and electrical drawings for the unit and a parts list.

Section 1.2 is a brief functional description of the instrument. Section 1.3 is an introduction to its theory of operation. Tables 1-1 and 1-2 list its electrical and mechanical specifications respectively.

1.2 GENERAL INFORMATION

The ACL Model FRO-212-1 is an electronic digital frequency meter capable of measuring frequencies from 1 kHz to 3GHz in three overlapping bands, offsetting a frequency measurement by any of twelve preset constants, and, with the addition of DAC (Digital-to-Analog Converter) circuitry, the ability to control an external receiver oscillator. No operator adjustment beyond band selection is necessary. The high frequency measurements use no heterodyne or transfer oscillator techniques and no calculations are necessary - the measured frequency is displayed directly on a row of gas display tubes on the front panel. The trigger level is set automatically, and a reading on an incorrect band gives a virtually error-free zero reading.

The instrument has fifteen channels and a remote mode selectable by two switches on the front panel. Channels 1A, 1B, and 1C are frequency-meter bands, covering the ranges of 1 kHz - 120 MHz, 110 MHz - 600 MHz, and 550 MHz - 3 GHz respectively. In these modes the frequency-offset functions of the instrument are disabled and it functions as a direct-reading frequency meter.

Channels 2 through 13 select different frequency ranges and offsets to make the FRO-212-1 compatible with a variety of ACL communications receivers. In each channel, the instrument monitors the local oscillator of a particular receiver and adds or subtracts a

quantity equal to the receiver's intermediate frequency. Thus it displays the frequency of a received signal directly.

In the REMOTE mode, the channel is selectable remotely. The front panel controls and the remote inputs are discussed in Section 2.

When the instrument is equipped with ACL's special logic and DAC boards, it produces an analog output proportional to any change in the instrument's reading from an original value. When the SET/LOCK switch on the front panel is placed in the SET position, the analog output is zero. When the switch is moved to LOCK, the DAC logic memorizes the value in the counter. If a subsequent frequency measurement shows any change from the set frequency, the analog output voltage changes. This voltage can be used to control the input oscillator, thus "closing the loop" and keeping the oscillator at its original frequency. This output is particularly useful for controlling ACL communications receivers.

The DAC logic is made by an independent subcontractor and is discussed in this manual only in terms of its inputs and outputs.

1.3 INTRODUCTION TO THEORY OF OPERATION

A frequency counter is an electronic instrument that counts the cycles of an unknown input signal for a known interval of time. The known time interval is usually a decimal fraction of a second, so that the frequency can be measured directly in GHz, MHz, kHz, or Hz, by correctly locating the decimal point.

The basic components of any frequency counter are a count chain, a time base, and a gate. The count chain is a register designed to count input pulses or cycles and to store a quantity equal to the number of counts received. The count chain counts and stores data in BCD form. Display circuitry is usually included in make the reading more available to the operator. Its contents can be "reset" to zero, and in this case "preset" to any given value. The time base is simply an electrical signal of accurately known duration. In this instrument, the time base is derived from a precise 1 MHz

crystal oscillator. The gate allows the count chain to count the input signal for the length of time set by the time base.

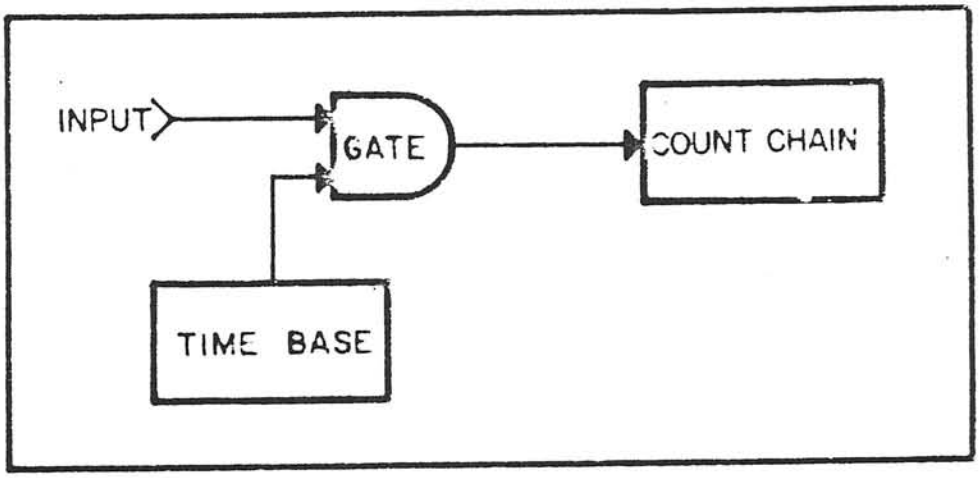


FIGURE 1-1

BASIC FREQUENCY COUNTER

The accuracy of frequency measurement is limited by the accuracy of the time base, which is dependent on the stability of the instrument's master oscillator and a "gating" error which is equal to plus or minus 1 count. The gating error is present because the incoming signal passing through the count gate is not synchronized with the time base pulses which control the gate. As illustrated in Figure 1-2, the first or last cycle may or may not pass through the gate during the selected measurement interval.

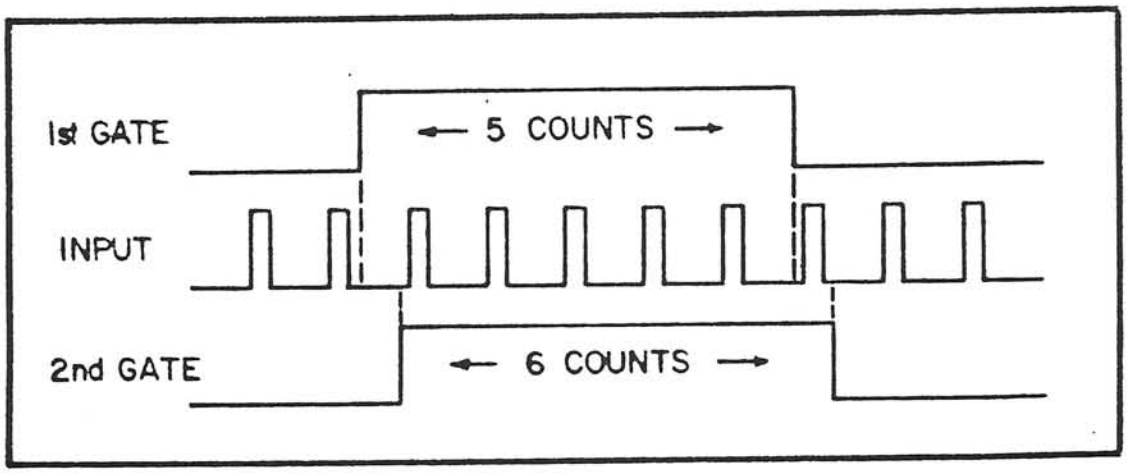


FIGURE 1-2

GATING ERROR

If the count chain is "preset" to some value P, the value of the final reading will be increased by P. If the count chain is preset to $\overline{P}$, the BCD complement of P, the

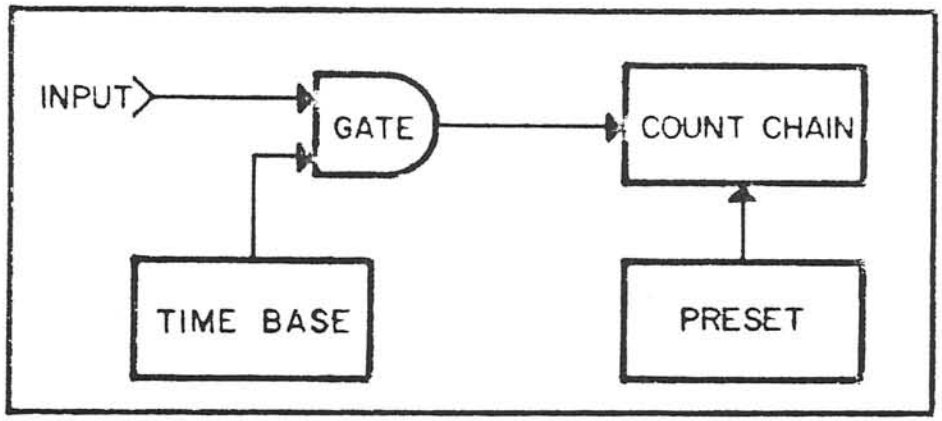


FIGURE 1-3
PRESET COUNTER

value of the final reading will be decreased by P. Thus, we can add or subtract any constant from the indicated frequency simply by presetting the count chain.

Flip-flop counting circuits become impractical above about 200 MHz. The counters in the FRO-212-1 in fact, are rated at 120 MHz, and are used directly only in the low-frequency channels (1A, and several preset channels). In the higher-frequency channels a unique sampling technique is used. Very simply, the counter generates a subharmonic of the input frequency. For an input frequency f, this quantity may be called f/N. The

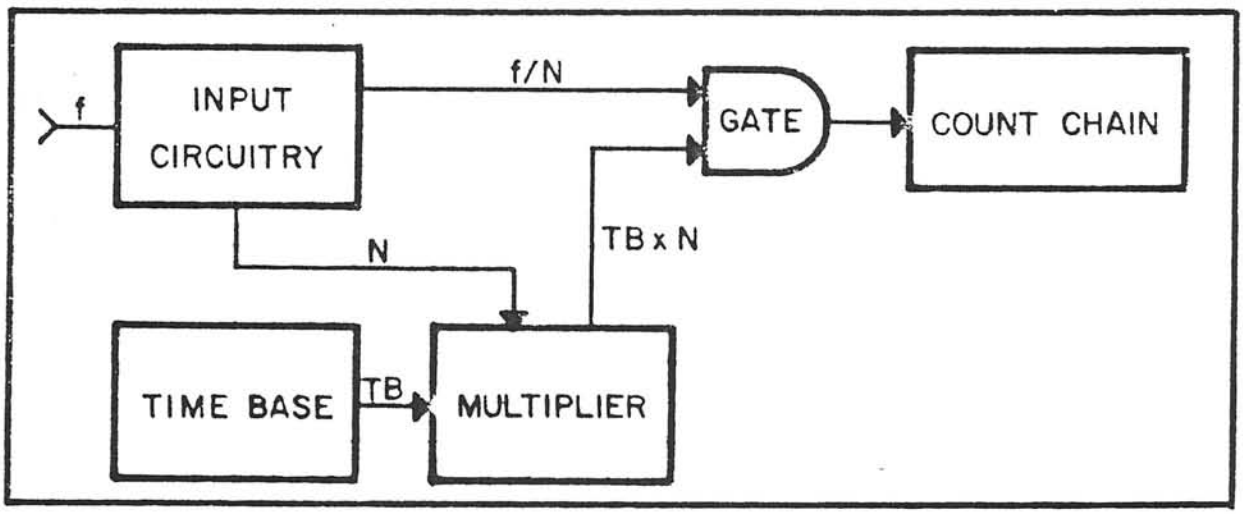


FIGURE 1-4
SAMPLING COUNTER

instrument then discovers the value of N, multiplies the duration of the time base by N, and counts f/N as if it were a normal input signal. Since it effectively counts f/N times the value of N, the final value in the count chain is equal to f.

Even in the sampling channels, the instrument appears to function as an ordinary frequency counter. The theory of the sampling technique is discussed in Section 3.

1.4 SPECIFICATIONS

Table 1-1 and 1-2 list the electrical and mechanical specifications respectively for the Astro Communications Laboratories Model FRO-212-1.

TABLE 1-1

ELECTRICAL SPECIFICATIONS

FUNCTION	Digital frequency meter, basic range 1 kHz - 3 GHz, with remote control, selectable preset, and optional automatic frequency control.

CHANNEL FUNCTIONS

Channel	Count	Display	Offset
1A	0.001 - 120 MHz	000.0010 - 120.0000 MHz	none
1B	110 - 600 MHz	110.0000 - 600.0000 MHz	none
1C	550 - 3000 MHz	0550.000 - 3000.000 MHz	none
13	2130 - 3100 MHz	030.000 - 999.999 MHz	-2100 MHz
2	2.455 - 6.455 MHz	2.00000 - 6.00000 MHz✓	-.455 MHz
3	10.300 - 24.300 MHz	06.0000 - 20.0000 MHz✓	-4.300 MHz
4	25.8 - 50.8 MHz	20.0000 - 45.0000 MHz	-5.800 MHz
5	51.4 - 121.4 MHz	30.0000 - 99.9999 MHz	-21.4 MHz
6	111.4 - 321.4 MHz	090.000 - 300.000 MHz✓	-21.4 MHz
7	310 - 560 MHz	250.000 - 500.000 MHz✓	-60 MHz
8	550 - 1060 MHz	490.000 - 999.999 MHz✓	-60 MHz
9	65.5 - 95 MHz	00.5000 - 30.0000 MHz✓	-65 MHz
10	550 - 1055 MHz	0990.00 - 2000.00 MHz*✓	-110 MHz
11	915 - 1920 MHz	1990.00 - 4000.00 MHz*✓	+160 MHz
12	2.303 - 2.800 MHz	003.000 - 500.000 kHz	-2.3 MHz

* The local oscillator frequency in the receivers used with bands 10 and 11 is doubled before it is fed to the mixer. Therefore the measured frequency is doubled by the FRO-212-1.

INPUT	
Impedance:	50Ω nominal.
Sensitivity:	-13 dBm (dB below 1 mW) to 120 MHz; -10 dBm to 2 GHz; -6 dBm to 3 GHz. Data showing sensitivity versus frequency will be supplied for each instrument.

TABLE 1-1 (Continued)

Connectors:	Type N connector on front and rear panel. Front or rear input selectable internally.
ACCURACY	
Basic Accuracy:	± one count ± oscillator stability.
Oscillator:	1 MHz temperature-compensated crystal oscillator with long term stability of 1 part in 10^6 per month after 30 days continuous operation. Temperature stability of 2 parts in 10^7 per ° C between +16 and +32° C after 30 minutes operation; ± .002% over entire operating range.
Resolution: (cycles per count)	Channel: 1A: 100 Hz 1B: 100 Hz 1C: 1 kHz In bands 2-11 and 13 the least significant digit of the output display is blanked to decrease display jitter and operator confusion. The internal resolution of the instrument is therefore a tenth of the display. The output of the least significant digit is fed to the auto frequency control circuit. 2: 10 Hz (display) 3: 100 Hz 4: 100 Hz 5: 100 Hz 6: 1 kHz 7: 1 kHz 8: 1 kHz 9: 100 Hz 10: 10 kHz 11: 10 kHz *12: 1 Hz 13: 1 kHz * On channel 12, the most significant display tube is blanked.
RF INTERFERENCE	The worst case RF output of the input connector is a 1 ns 20 mV pulse at a repetition rate of 40 MHz. Output is less than 800 μV rms. The case and display are gasketed and screened for RF interference.

TABLE 1-1 (Continued)

HARMONIC REJECTION	The meter will not display any harmonics of the input signal when the total rms harmonic energy is 6 dB or more below the fundamental input signal. For frequencies below 500 MHz, the equivalent limit is -12 dB. Confidence level of this limit is greater than 99%.
AUTO FREQUENCY CONTROL	When the auto frequency control cards are fitted, the unit supplies an analog output voltage of -0.1V/count drift with a range of ±99 counts. This circuitry is not described in this manual.
RELIABILITY	MTBF is 10,000 hr. or better.
FRONT PANEL CONTROLS	CHANNEL SELECT - two rotary switches. SET/LOCK - Toggle switch POWER - On-Off switch GATE - Indicator lamp
POWER REQUIREMENTS	115/230Vac, switch selectable, 50-60 Hz, 70 watts.

TABLE 1-2

MECHANICAL SPECIFICATIONS

ENVIRONMENTAL TOLERANCE	
Temperature:	Storage, -35° C to +75° C. Operating, 0 to +52° C.
Humidity:	0 to 95% relative humidity. The instrument will perform correctly under frost and condensation conditions.
SHOCK AND VIBRATION	
Vibration:	The unit will tolerate vibration levels of 0.06" double amplitude at 5 to 55 Hz.
Shock:	The unit will survive 18 10G impact shocks, including 3 shocks in each direction in three mutually perpendicular axes.

TABLE 1-2 (Continued)

SIZE	3-1/2" x 17-3/4" x 15" (HxWxD). Two rack handles are included for mounting in a standard 19" rack panel.
WEIGHT	Approximately 15 pounds.

SECTION 2

INSTALLATION AND OPERATION

2.1 SCOPE

This section discusses the unpacking, incoming inspection, installation, and operation of the ACL Model FRO-212-1 Frequency Counter.

2.2 UNPACKING

The counter is packed with its accessory items in a specially-designed corrugated cardboard carton. Unpack it carefully and check for the following accessories:

Instruction Manuals (2 each)
Line Cord (1 each)
Rack Handles (2 each)
Extender Board (1 each)
REMOTE Mating Connector (1 each)

Inspect the instrument and the shipping carton for obvious physical damage. If the instrument is obviously damaged, or if the carton shows evidence of unusual abuse, (dents, tears, etc) notify the carrier immediately to assure your warranty.

If any accessory items are missing and the shipping package was not broken, notify the factory.

2.3 INCOMING INSPECTION

Inspect the instrument, using whatever procedures you normally use to check new test equipment. It is not practical to remove the printed-circuit cards for inspection of their contacts or solder joints. They are fitted with cables which are tied to the chassis, and are thus semi-permanently installed. If removal becomes necessary, be sure to replace the cards and cables exactly as they were. Be careful not to disturb any lead dress or trimmer adjustments. Look the instrument over closely. See that the switches turn and that they are aligned with their markings. If the proper mating connectors are available, test-fit them with the input and remote-control connectors. Remove the top cover if you have not already done so. Check the inside of the chassis carefully for broken components

or loose screws. See that the printed-circuit cards and the display tubes are seated well in their sockets. Spin the fan with your finger and see that it rotates smoothly and quietly and does not foul on its filter. See that the fan filter is clean. If all seems in order, replace the top cover. Do not skip any screws - all 30 are needed for proper RF shielding.

2.4 POWER REQUIREMENTS

The instrument is equipped with a standard 3 prong (NEMA) power cord that automatically grounds the instrument chassis when connected to a standard grounded power receptacle. An adapter providing an instrument ground must be used whenever termination to a bi-terminal outlet is necessitated.

The Model FRO-212-1 is capable of operating from either a 115 or 230 volt ac, 50-60 Hz primary power source. The instrument is normally shipped from the factory in the 115 volt configuration. If operation from a 230 volt source is desired, follow the steps outlined in Table 2-1, 230 Volt Operation.

TABLE 2-1

230 VOLT OPERATION

STEP	ACTION
1	Slide the rear panel 115/230 switch to the position revealing the numerals 230.
2	Remove the existing 1.0 ampere (MDL) fuse (rear panel) and replace with a 0.5 ampere SLO-BLO (MDL) type.
3	Conspicuously label the instrument for 230 volt operation.

2.5 INCOMING CONFIDENCE CHECK

Prior to packaging the instrument for shipment, extensive operational, alignment and calibration checks were performed. To satisfy electrical integrity of the instrument at the receiving bench, a simple self-test procedure can be undertaken. The self-check requires no additional equipment and is intended only to verify basic operation. Prior to performing the self-check, it is recommended that the operator become familiar with the basic operating controls described in paragraphs 2.7 and 2.8.

1. Connect the instrument to appropriate power source and verify proper positioning of the 115/230 volt line switch.
2. Rotate the POWER switch clockwise to the ON position. The display will illuminate.
3. Rotate the CHANNEL SELECTOR switch to the 1A position. The display will indicate 000.0000 MHz.
4. While observing the display, rotate both CHANNEL SELECT switches according to the following table and verify correct display.

LEFT SWITCH	RIGHT SWITCH	READING
1A	--	000.0000 MHz
1B	--	000.0000 MHz
1C	--	0000.000 MHz
2-12	2	9.54500 MHz
2-12	3	95.7000 MHz
2-12	4	94.2000 MHz
2-12	5	78.6000 MHz
2-12	6	000.000 MHz
2-12	7	000.000 MHz
2-12	8	000.000 MHz
2-12	9	35.0000 MHz
2-12	10	0000.00 MHz
2-12	11	0000.00 MHz
2-12	12	700.000 kHz
13	--	0000.00 MHz
REM*	--	0000000

* With no remote control connected.

5. If a remote control unit for the FRO-212-1 is available, complete the necessary interconnection to the REMOTE connector on the instrument's rear panel and set the left switch to the REM position. Perform the previously mentioned checks from the remote location. Instructions reguarding the operation and interconnection of the remote control unit are included in its operating manual.

2.6 INSTALLATION

The Model FRO-212-1 is operable upon receipt requiring only the connection of a suitable input, termination of the line cord to a proper ac power source and the interconnection of the remote cable between the instrument and remote control unit.

2.6.1 Installation Consideration

Cooling is provided by a rear panel mounted fan. The air intake duct must remain unobstructed and sufficient rear panel clearance must be maintained to assure adequate air circulation.

2.6.2 Input Connector Location

The FRO-212-1 is equipped with two type N connectors, one located on the front panel and one located on the rear panel. The instrument is factory wired with the rear panel input operable. If the front panel input is to be employed, follow the instructions outlined in Table 2-2.

TABLE 2-2

FRONT INPUT OPERATION

STEP	ACTION
1	Remove the bottom cover panel by extracting the 30 #4 phillips-head screws which secure the panel to the chassis.
2	Unfasten the internal input cable from the rear panel input connector.

TABLE 2-2 (Continued)

3		Carefully clip the cable ties securing the cable to the bottom (circuit side) of the mother board.
4		Route the input cable along the front panel and secure the fitting to the front panel input connector.
5		Cap or label the rear panel connector to indicate that it is no longer operable.

2.6.3 Remote Control Function

The REMOTE control connector (rear panel) is an Amphenol or Bendix type MS3102A-24-28S. The mating connector (supplied) is an Amphenol or Bendix type MS3102A-24-28P fitted with an MS3057-16A cable clamp to relieve unnecessary strain on soldered connections.

When the REMote mode is selected (front panel CHANNEL SELECT switch), the remote line (Terminal A) of the connector is grounded. Cross connecting any of the channel select control lines to the grounded remote line selects the corresponding channel.

NOTE

If more than one channel select control line is grounded or if a channel select control line is grounded when the REMote mode is NOT selected, the instrument will not function correctly.

Table 2-3 lists the REMOTE control connector pin assignments and corresponding functions.

TABLE 2-3

REMOTE CONNECTOR PIN ASSIGNMENTS

TERMINAL	FUNCTION
A	Remote
B	Channel 1A
C	Channel 1B
D	Channel 1C
E	Channel 2
F	Channel 3
G	Channel 4
H	Channel 5
J	Channel 6

TERMINAL	FUNCTION
K	Channel 7
L	Channel 8
M	Channel 9
N	Channel 10
P	Channel 11
Q	Channel 12
R	DAC Output
S	Channel 13
Z	Ground

2.6.4 DAC Installation

Provision is made within the FRO-212-1 for the installation of two DAC printed circuit boards. These boards perform the digital-to-analog control function as previously described in Section 1. Both cards are manufactured and documented by the Systron-Donner Corporation. The DAC LOGIC card (SPC577) is fitted into the connector nearest the rear panel (J1) directly in front on the rear panel mounted oscillator board. The DAC card (SPC579) is fitted into the remaining connector (J2) on the same DAC adapter. Table 2-4 lists the connector pin assignments and corresponding functions.

TABLE 2-4

DAC PIN ASSIGNMENTS

CONNECTOR J1 (SPC577)	CONNECTOR J2 (SPC579)	FUNCTION	CONNECTOR J1 (SPC577)	CONNECTOR J2 (SPC579)	FUNCTION
J, R	-	"4" bit	N, 6	-	"2" bit
M, 11	-	"1" bit	L	-	"80" bit
K	-	"40" bit	D	-	"20" bit
C	-	"10" bit	B	-	"100" bit
E, P	-	Set-Lock Sw.	-	E, X	-12V
U	-	Storage Transfer Pulse	-	D	+12V
3, 12, 19	-	+Vcc	-	C	DAC OUTPUT
4, 22	-	Gnd	2	-	RESET
S, 5	-	"8" bit	A	-	1 MHz Clock

2.7 FRONT PANEL DESCRIPTION

Figure 2-1 and Table 2-5 describe the front panel controls and functions.

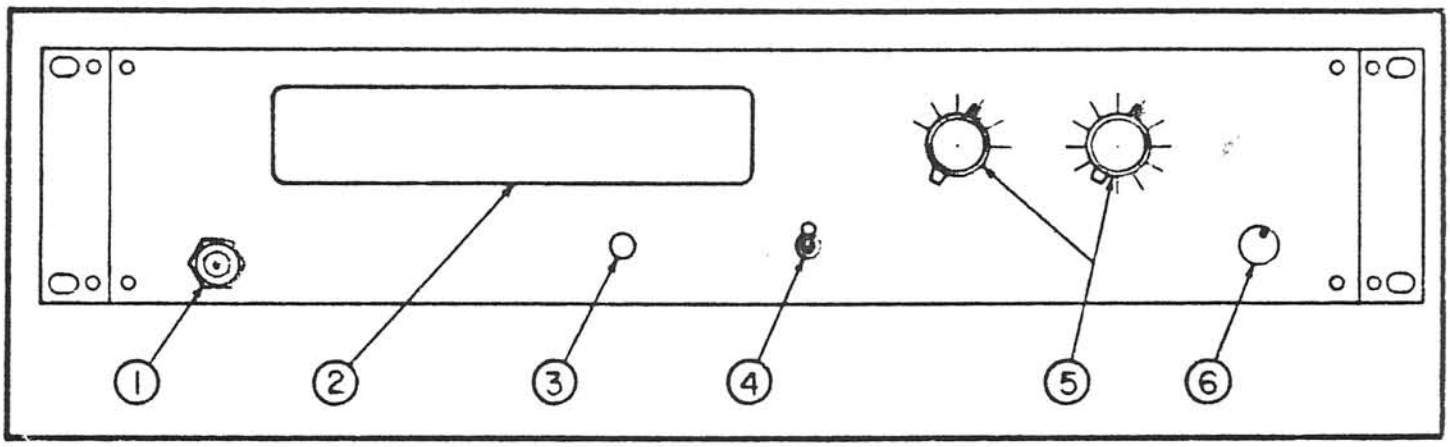


FIGURE 2-1

FRONT PANEL

TABLE 2-5

FRONT PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	INPUT Connector	A type N connector which receives the applied input when the instrument is modified to accept a front panel input.
(2)	Display	Seven numerical indicator tubes with automatically positioned decimal points and an illuminated units annuciator (MHz, kHz). Decimal point position and unit annuciation are determined by the CHANNEL SELECT switch position. During operation employing channels 2 through 11 and 13, the least significant digit is blanked. On channel 12 the most significant digit is blanked.

TABLE 2-5 (Continued)

(3)	GATE Lamp	An indicator which illuminates during the measurement interval indicating a measurement in progress.
(4)	SET-LOCK Switch	A toggle switch employed with the DAC function. In the SET position, the analog output at the rear panel REMOTE connector is zero. In the LOCK position the analog output voltage will shift for subsequent frequency changes.
(5)	CHANNEL SELECT Switch	Two rotary switches which determine the range or channel of operation. The left CHANNEL SELECT switch selects either the range (1A, 1B or 1C), REMote function, channel 13 or enables the right CHANNEL SELECT switch when placed in the 2-12 position. The right CHANNEL SELECT switch is an 11 position rotary switch which selects channels 2 through 12 when the left CHANNEL SELECT switch is in the 2-12 position.
(6)	POWER OFF-ON	Provides ac power to the instrument when rotated in a clockwise direction to the ON position.

2.8 REAR PANEL DESCRIPTION

Figure 2-2 and Table 2-6 describe the rear panel controls and functions.

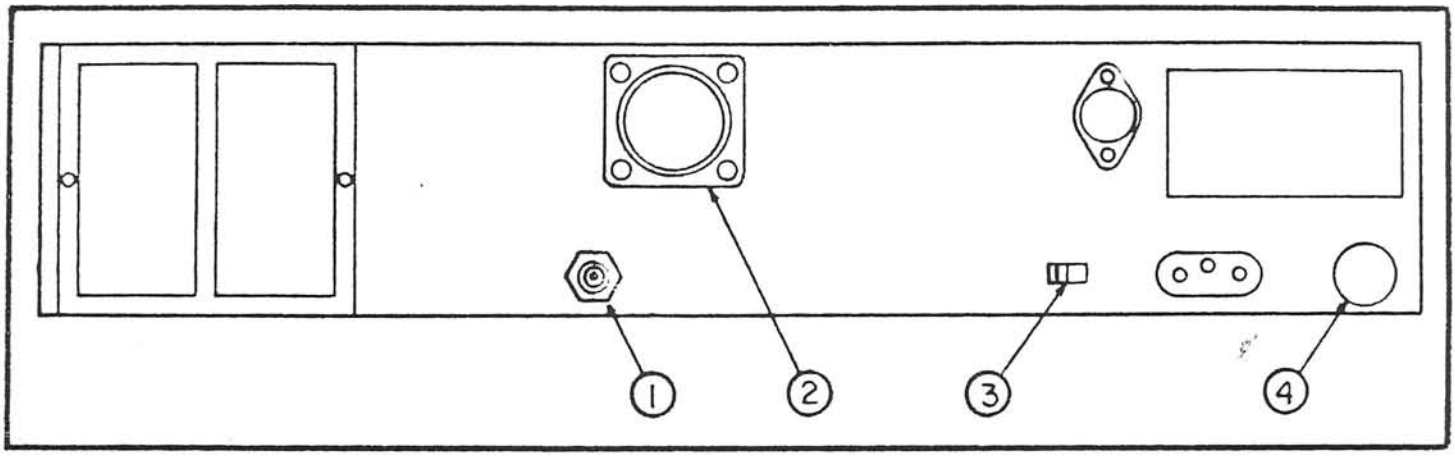


FIGURE 2-2

REAR PANEL

TABLE 2-6

REAR PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	INPUT Connector	A type N connector which accepts the applied input.
(2)	REMOTE Connector	A Military Standard type 24 contact connector employed to interconnect instrument and remote control unit.
(3)	115-230 Line Switch	A recessed slide switch permitting instrument operation from either a 115 or 230 volt ac source.
(4)	1A.S.B. Receptacle	The primary power fuse holder containing a 1 ampere SLO-BLO (MDL) type fuse (115 volt operation). When operating from a 230 volt source, the fuse should be replaced with a 0.5

TABLE 2-6 (Continued)

(4) (Cont'd.)		ampere SLO-BLO (MDL type fuse) to adequately protect the instrument.

2.9 OPERATION

The FRO-212-1 is completely automatic in operation requiring only the application instrument power and selection of the desired channel.

2.9.1 Operation As A Frequency Meter

1. Connect the unknown frequency to the appropriate INPUT connector using 50Ω cable with a type N fitting. Be certain that the source under test has a 50Ω output impedance and sufficient signal amplitude to effect counter operation (Refer to Table 1-1).

2. Select the appropriate frequency range (Channel 1A, 1B or 1C).

3. The unknown frequency will be displayed directly in MHz with proper decimal location.

2.9.2 Operation As A Receiver Monitor

1. Select the preset channel (2-13) with corresponding offset equal to the receivers local oscillator frequency.

2. Connect the receivers local oscillator output to the appropriate counter INPUT connector.

3. The display will indicate the input frequency directly with corresponding units annunciation and decimal location.

2.9.3 Operation As A Receiver Control (DAC Function)

1. Connect the remote control cable to the receiver and REMOTE connector (rear panel).

2. Place the CHANNEL SELECT switch to the REMote position.

SR-212 FINE TUNE VOLTAGE

V	F	
15.17	162.578	$\frac{.0835}{.99} = .084$ MHz/V
15.00	162.5647	
14.35	162.5100	
14.18	162.4945	

AS V GOES UP, F GOES UP

15.01	94.70300	$\frac{.007}{.81} = .008$ MHz/V
14.80	.70134	
14.70	.70044	
14.50	.69884	
14.20	.69643	
15.06	453.8628	$\frac{2.686}{1.63} = 1.65$ MHz/V
13.43	451.176	
14.96	854.963	$\frac{.984}{1.98} = .496$ MHz/V
12.98	853.979	

3. Place the SET-LOCK switch in the SET position.

4. Tune the receiver to the desired frequency.

5. Place the SET-LOCK switch to the LOCK position.

6. A subsequent change in the input frequency will cause an analog voltage shift which can, in turn, be used to control the receiver's input oscillator, holding the frequency constant.

1 V / KHz OF DRIFT
GOES 0 to -9V AS FREQ DRIFTS HIGHER
0 to +9V " " " LOWER

SECTION 3

THEORY OF OPERATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes and explains the theory of operation of the Astro Communications Laboratories Model FRO-212-1 Frequency Counter from three increasingly detailed perspectives. The sampling technique is first discussed followed by a block diagram approach to the overall theory of operation. In conclusion, a detailed description at the circuit level is undertaken to furnish the reader with a comprehensive understanding of the individual circuits which constitute the Model FRO-212-1 Frequency Counter.

3.2 SAMPLING PRINCIPLE

A sampling technique is utilized to achieve the high frequency measurements common to the Model FRO-212-1. By generating an integral subharmonic of the applied input frequency and consequently solving for the harmonic multiple, the instrument is capable of realizing measurements in excess of 3 GHz. Once the harmonic number is discerned, the time base is expanded by the harmonic number while the subharmonic is counted directly by the count chain. Since the frequency of the subharmonic is counted for a duration multiplied by the harmonic number, the resulting solution is equal to the applied input frequency.

3.3 SAMPLING TECHNIQUE

The purpose of the sampling technique is to reduce the input frequency to enable ordinary counter circuits to count very high frequencies. Referring to Figure 3-1, the unknown frequency (f) is split into two equal signals and consequently directed to a "countdown" circuit and an "input sampler" circuit.

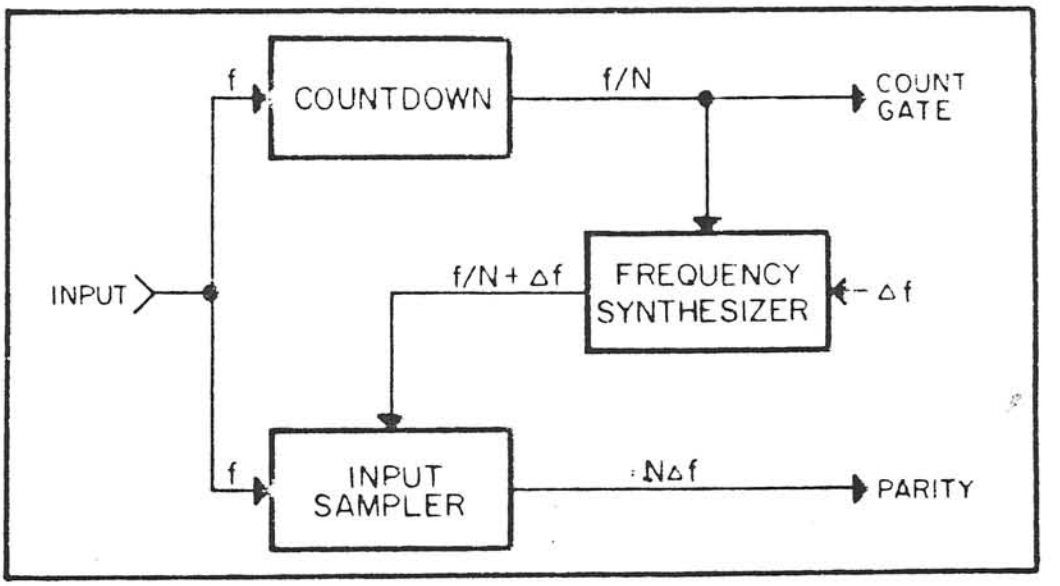


FIGURE 3-1

INPUT BLOCK DIAGRAM

The countdown circuit consists of a tunnel diode astable multivibrator. This circuit free-runs at a frequency compatible with the digital counting circuitry (below 120 MHz). An input signal higher than this natural frequency will drive the multivibrator at some integral sub-multiple of the applied input. Mathematically, the countdown circuit's output is the input frequency (f) divided by the harmonic number (N) or f/N. Figure 3-2 illustrates the countdown output with N equal to six.

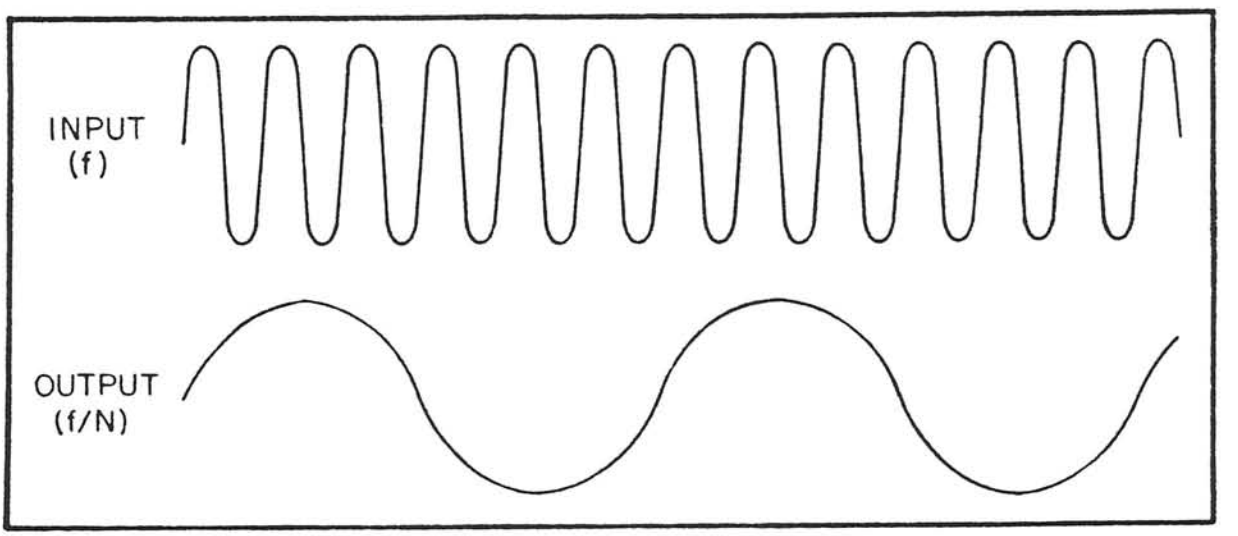


FIGURE 3-2

COUNTDOWN OUTPUT

The input sampler circuit observes (samples) the input signal for an "instant" on command. If the countdown circuit's output (f/N) were used directly to strobe the sampler, no information would be gained in the determination of the harmonic multiple. As an example, assume that the countdown circuit is synchronized to the fourth sub-multiple of the input frequency. The strobe pulses, at the countdown output's rate, occur at 1/4 the input frequency. Since the strobe pulse and the input are in phase, the sample occurs at the same point on the input waveform each time resulting in a dc level output proportional to the amplitude at the point on the input waveform at which sampling occurs (refer to Figure 3-3).

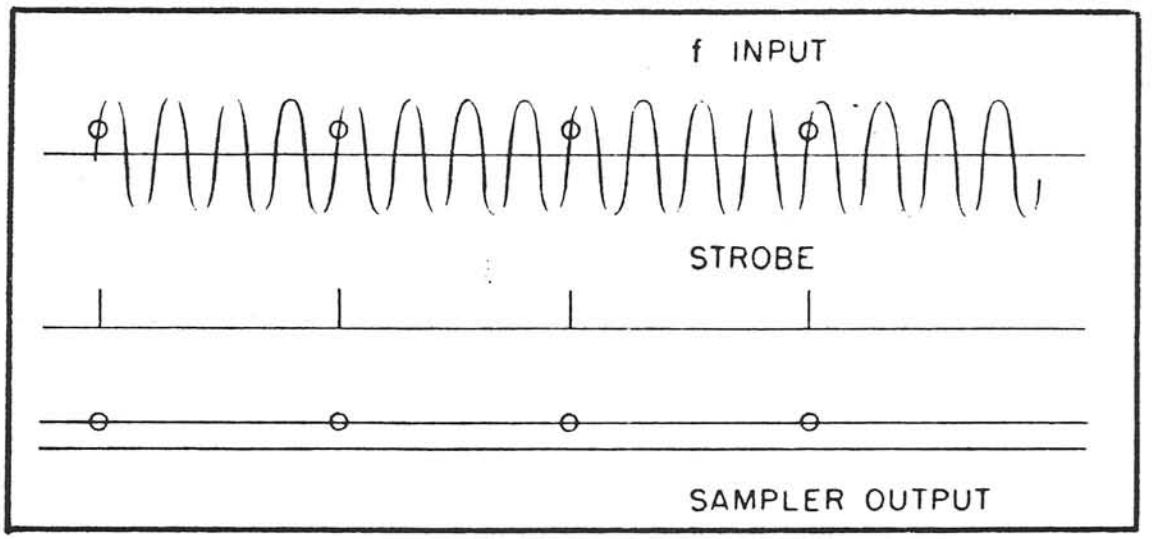


FIGURE 3-3
SAMPLER OUTPUT WITHOUT SLEWING

If the sampling frequency were "slewed", that is, each sample occuring slightly ahead or behind in time, each successive sample would coincide with different points on the input waveform. As illustrated in Figure 3-4, the sampler's output is a low frequency reproduction of the input frequency.

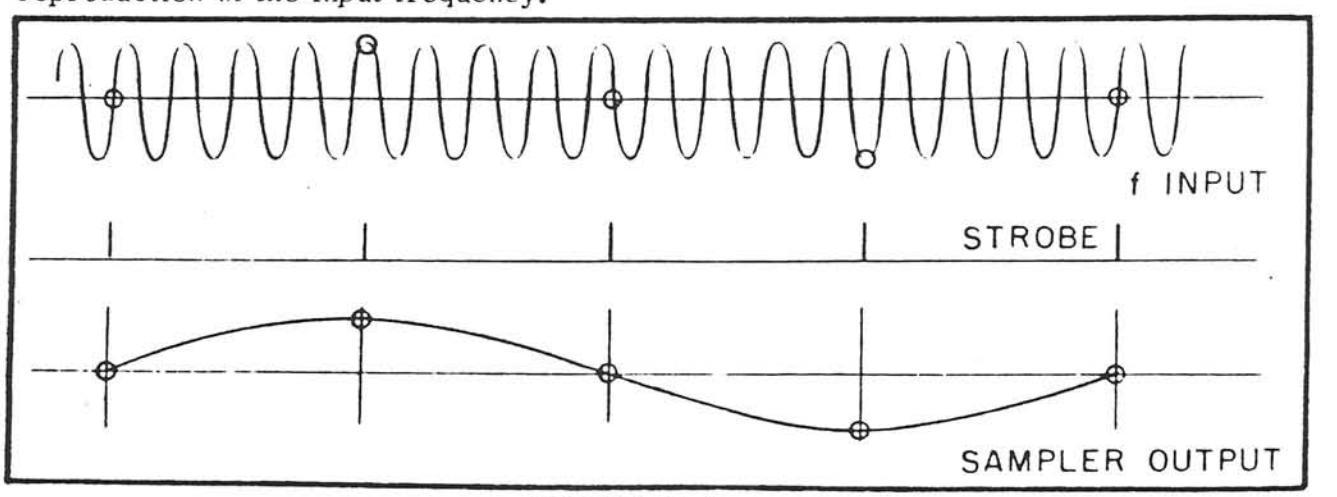


FIGURE 3-4
SAMPLER OUTPUT WITH SLEWING

To provide the necessary offset, the countdown circuit's output is first mixed with a low frequency signal within the frequency synthesizer. The synthesizer's output is the countdown circuit's output (f/N) plus the low frequency signal (Δf) or, mathematically, f/N + Δf.

The addition of f/N + Δf can be shown vectorially.

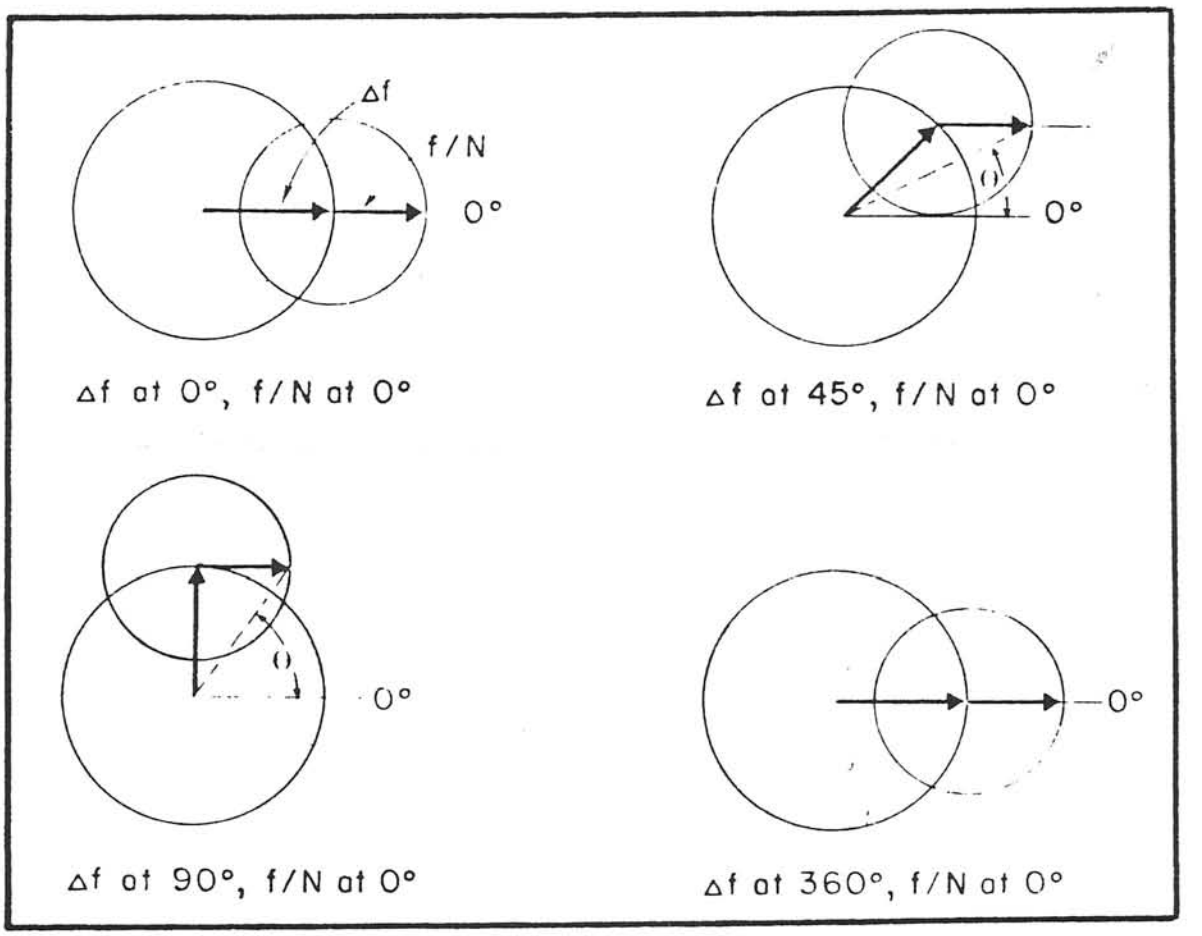


FIGURE 3-5
VECTOR ADDITION OF f/N AND Δf

The two vectors rotate in a counter clockwise direction at a rate determined by their respective frequencies. In the examples shown, the resultant (dotted vector) is shown to be a progressive phase change as the Δf vector rotates through 360°. In respect to the original 0° reference, we have progressively advanced the point of initial reference of the f/N vector through 360° as the Δf vector completes one revolution.

As an example, assume the countdown circuit's output frequency to be exactly 10 megahertz (f/N = 10 MHz). The slewing frequency is 5 kilohertz (Δf = 5 kHz). In the vector representation then, the Δf vector makes 5,000 counter clockwise revolutions per second while the f/N vector completes 10,000,000 revolutions per second.

In respect to time, the Δf vector makes one complete revolution in 200 microseconds while the f/N vector completes 1 revolution in 100 nanoseconds. The resultant phase of the f/N vector changes 360° for one revolution of the Δf vector. Since 360° of the f/N vector is 100 nanoseconds, a total change of 100 nanoseconds in 200 microseconds is realized. The problem now becomes how much change occurs in the time of f/N passing the initial zero reference over a period of 100 nanoseconds of Δf if 100 nanoseconds of change occurs in one complete period of 200 microseconds of Δf? Expressed as a mathematic ratio we have:

$$\frac{\text{X change}}{100 \text{ ns}} = \frac{100 \text{ ns}}{200 \ \mu\text{s}}$$

Solving for the unknown change (X) we have:

$$\text{X change} = \frac{10^{-7} \times 10^{-7}}{2 \times 10^{-4}} = \frac{10^{-14}}{2 \times 10^{-4}} = 5 \times 10^{-11} \text{ or 50 picoseconds}$$

The slewing rate per period of f/N is 50 picoseconds. Therefore each 100 nanosecond period of f/N will lose an additional 50 picoseconds. Since the f/N + Δf signal from the synthesizer is used to strobe the input sampler, each successive sample will occur at 100 nanoseconds minus 50 picoseconds. That is, if the first sample were at 100 nanoseconds (100,000 picoseconds) the succeeding strobe pulses would occur at 100,000 -50 picoseconds or at 100000, 199950, 299900, etc, picoseconds respectively.

Referring to the vector summation, it will be noted that for one revolution of Δf, the f/N vector is advanced in phase by 360°. Since 360° is one cycle, for every cycle of Δf there will be precisely one additional cycle of f/N.

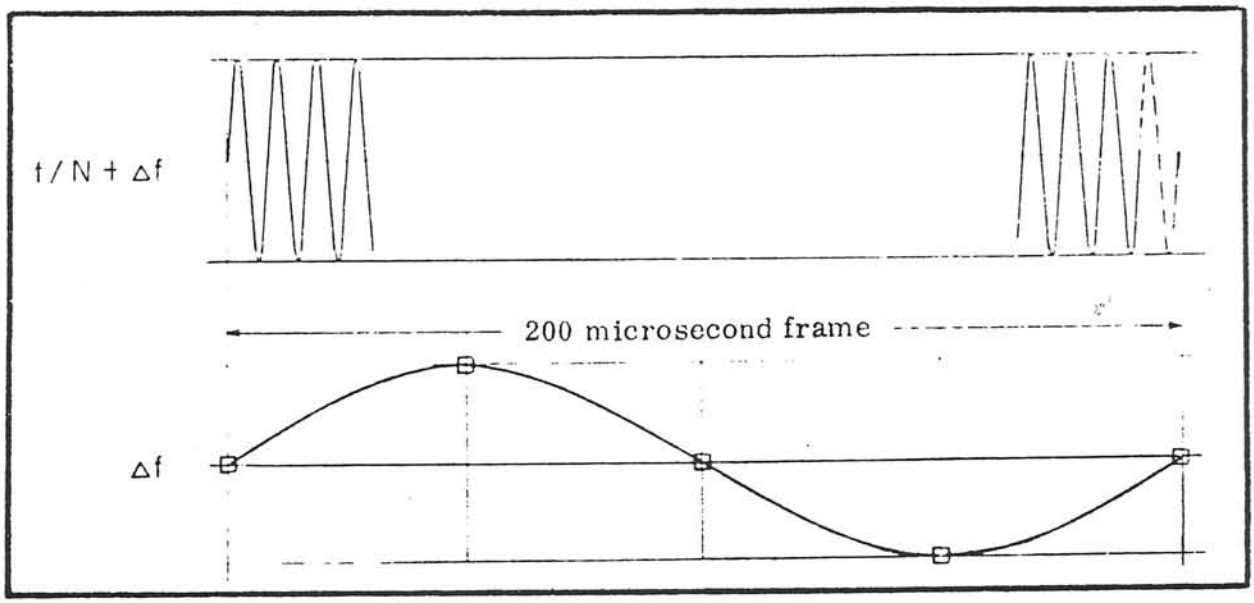


FIGURE 3-6

ADDITION OF f/N AND Δf

If f/N equals 10 megahertz, 2,000 cycles will occur in a 200 microsecond frame of one cycle of Δf. Since the vector addition of f/N and Δf adds one additional cycle of f/N, 2,001 cycles of f/N + Δf occur within the frame.

This corresponds to a time per cycle of f/N of:

$$100 \text{ nanoseconds} \left(\frac{2000}{2001}\right) \text{ or } 99.950024038 \text{ nanoseconds.}$$

The slew rate (change in time per cycle) is therefore approximately 100 nanoseconds -99.9500 nanoseconds = 0.050 nanoseconds or 50 picoseconds or exactly $50\left(\frac{2000}{2001}\right)$ picoseconds per cycle.

To obtain a solution for the value of N a hypothetical case of an input frequency (f) of 500 MHz and a countdown output (f/N) of 10 MHz with a 5 kHz slewing frequency (Δf) and corresponding slew time of 50 picoseconds will be employed as an example.

The period of a 500 megahertz signal is 2 nanoseconds. In a 200 microsecond frame, 100,000 cycles of f will occur. Similarily, 2,000 cycles of f/N will occur and, since we add precisely one cycle of f/N with Δf, 2,001 cycles of f/N + Δf will occur. Since f/N +

Δf performs the strobing of the input, 2001 sampling strobes will be performed. The sampling slewing rate is 50 picoseconds per cycle. In order to progress entirely over and sample an entire cycle of the input frequency (f), which has a period of 2 nanoseconds (2000 picoseconds), forty strobes must be performed.

2000 picoseconds ÷ 50 picoseconds = 40 (strobes)

In other words, one low frequency replica of the input will be generated after 40 samples. In a time frame of 200 microseconds where a total of 2001 strobes occur; 2001 ÷ 40 cycles of the reproduced input will occur; or 50.025 cycles.

The solution obtained is slightly high because of the approximation of the slew time at 50 picoseconds. Since the actual slew time is $50\left(\frac{2000}{2001}\right)$ picoseconds, the solution is in error by the factor $\left(\frac{2000}{2001}\right)$ The correct solution would be $50.025\left(\frac{2000}{2001}\right)$ or 50.000 cycles.

The sampler's output is the cycles (harmonic multiple) of N per cycle of Δf. The counter derives the value of N from the expression N Δf by counting the sampler's output for one period of Δf.

3.4 BLOCK DIAGRAM ANALYSIS

This section explains the theory of operation from a functional block diagram. All circuits and their respective functions are covered to present an overall understanding of the basic instrument and to complement the detailed circuit description outlined in Section 3.5.

3.4.1 Input Power Divider

The input signal is cabled directly from the INPUT connector to the input power divider where it is split into two equal signals and consequently cabled to both the countdown and input sampler circuits. A small portion of the input signal energy is tapped and routed directly to the 120 MHz DCU for low band (1 kHz - 120 MHz) applications.

3.4.2 Countdown Circuit

The countdown circuit accepts the high frequency output from the input power divider and, in turn, generates a low frequency sub-multiple (f/N) of the applied input frequency (f). The generation of the sub-multiple is accomplished by one of two astable tunnel diode multivibrators incorporated into the countdown circuitry. For mid band (110 - 600 MHz) applications, a multivibrator with a natural frequency between 8.75 and 9.75 MHz is enabled while for high band (550 - 3000 MHz) applications, a multivibrator with a natural frequency range of 32 to 37 MHz is enabled. The resonant frequency of the multivibrators is determined by the dc level output from the ramp generator. When not tuned near an integral sub-harmonic of the applied input, "error reset" signals step the ramp generator until an approximate sub-multiple is encountered.

When the frequency of the enabled multivibrator is sufficiently close to an integral sub-harmonic the influence of the applied input signal causes a "phase lock" condition that holds the multivibrator at a stable sub-harmonic.

The output from each multivibrator is routed through a low pass filter network to remove any high frequency complements, amplified and transformer matched before being coupled to both the frequency synthesizer and 120 MHz DCU. Figure 3-7 illustrates the functional block diagram for the countdown circuit.

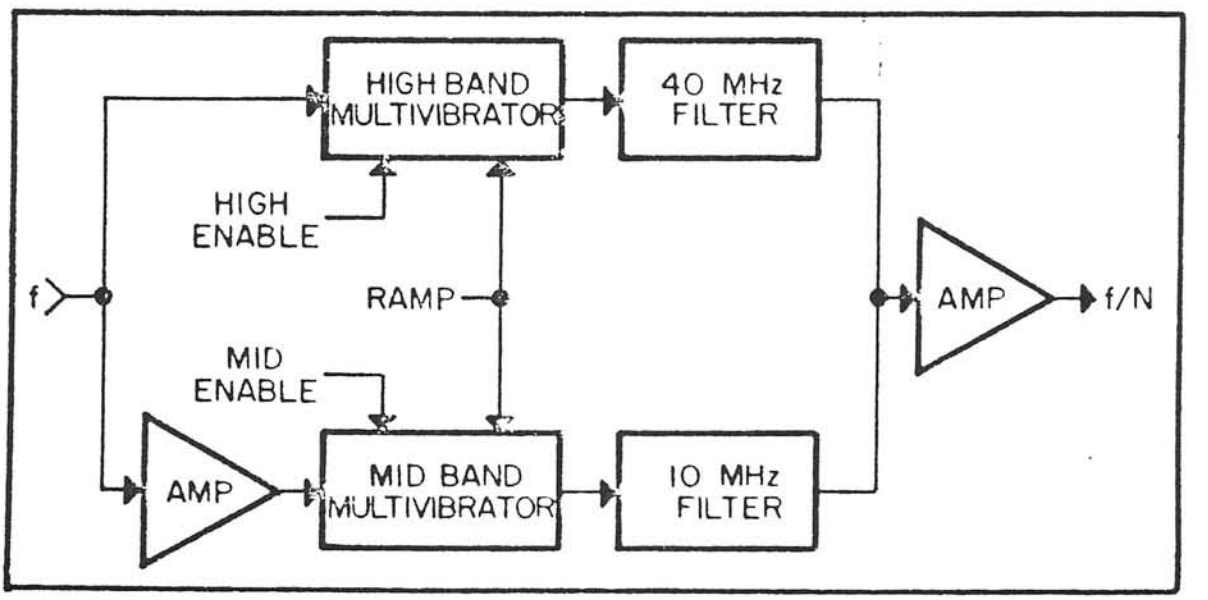


FIGURE 3-7

COUNTDOWN CIRCUIT BLOCK DIAGRAM

3.4.3 Frequency Synthesizer Circuit

The frequency synthesizer circuit provides slewing for the sampler circuit by combining the countdown circuit's output (f/N) with the 5 kHz signal (Δf) from the phase shifter. During operation employing the high band (550 - 3000 MHz), the synthesizer also provides a divide-by-four function to reduce the output frequency to within the range of the sampler circuit.

The synthesizer utilizes two RF phase shift networks, one tuned to approximately 9 MHz (mid band) and the other to approximately 36 MHz (high band), to divide the input signal (f/N) into two identical signals with a 90° phase shift.

A pair of balanced modulators accept the two phase shifted signals from the band selected phase shift network. One of the 5 kHz signals (Δf) from the phase shifter is routed to one of the balanced modulators while the other 5 kHz signal (90° out of phase) is routed to the other balanced modulator. The consequent mixing of the two signals within the modulator results in a double side band output of $f/N \pm \Delta f$ from each modulator. The combining of the two outputs, since they are out of phase, results in a single sideband output of either $f/N + \Delta f$ or $f/N - \Delta f$.

NOTE

While the sign of the slewing frequency does not alter instrument operation, the manual will refer to the slewing frequency as $f/N + \Delta f$ to maintain clarity.

In the mid band, the single sideband (SSB) output ($f/N + \Delta f$) is first filtered, amplified and then coupled to the sampler circuit by an auto transformer. In the high band, the SSB output is filtered, squared for logic level compatibility, divided-by-four by a pair of TTL flip-flops and then routed through the same filter, amplifier and auto transformer common to the mid band.

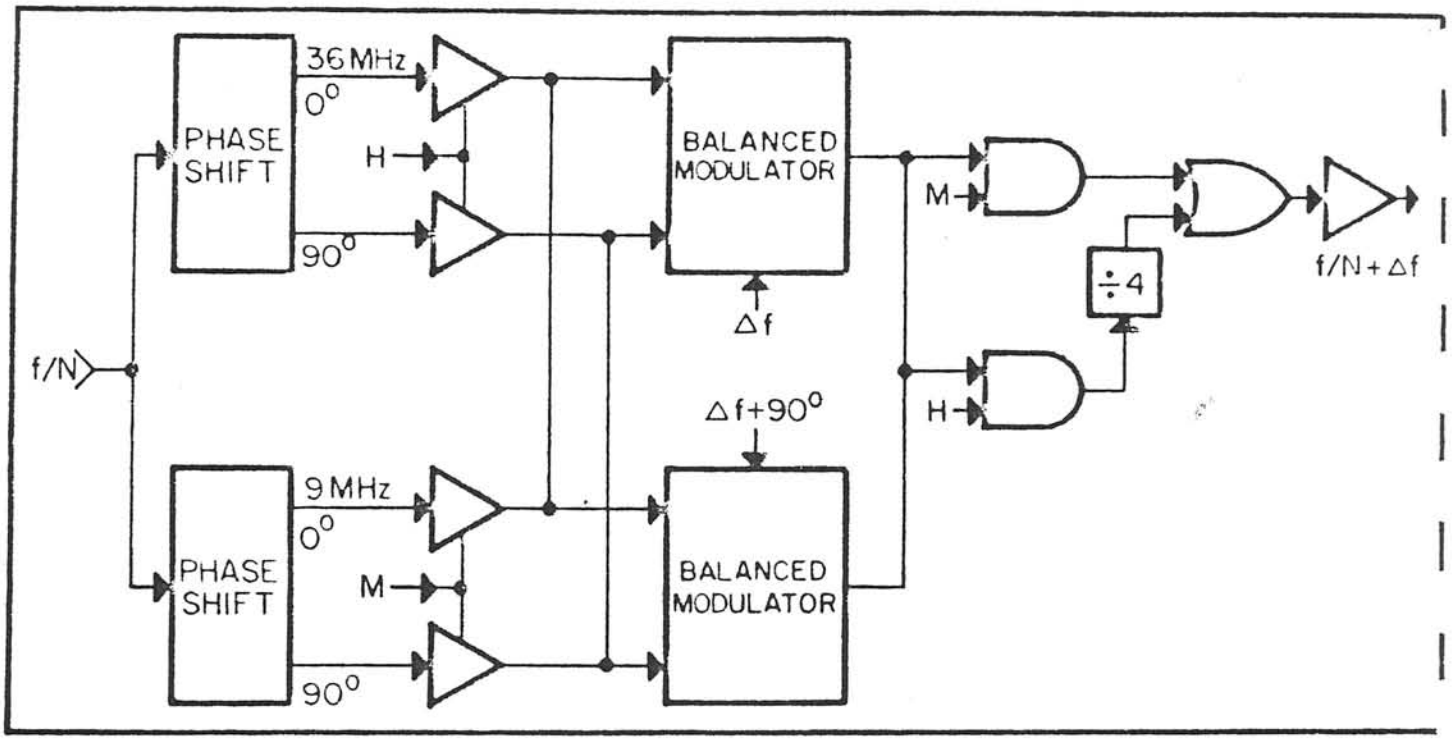


FIGURE 3-8

FREQUENCY SYNTHESIZER
BLOCK DIAGRAM

3.4.4 Sampler Circuit

The sampler circuit accepts two separate inputs; the high frequency input (f) from the power divider and the slewing input (f/N + Δf or f/4N + Δf/4) from the synthesizer circuit.

The high frequency input is coupled to a diode sampling gate while the slewing input from the synthesizer is amplified and shaped into a string of extremely fast pulses (typically 200 picoseconds). These pulses are used to open (strobe) the sampling gate thereby coupling a fraction of a cycle of the input signal to the gate of a FET source follower.

The FET output is filtered to remove the carrier (8-10 MHz). The resultant series of positive and negative pulses (rough sinewave) with a normal frequency between 40 and 500 kHz is amplified, clipped, squared and coupled to the parity circuit as the NΔf signal.

The amplitude of the NΔf sinewave decreases sharply as the input frequency increases. At the lower frequencies, the sampling pulse (approximately 200 picoseconds in duration) is considerably shorter than the period of the input signal and, is generally, totally positive or negative for the full duration of the pulse. However, at the higher frequencies, the sampling pulse width approaches the input period exhibiting a nulling effect resulting in a reduced output amplitude. A compensation network is incorporated into the amplifier stage to offset this high frequency inefficiency.

In the mid band (110 - 600 MHz), the amplifier gain is increased which, conversely, decreases the signal-to-noise ratio. This aids in the prevention of "locking on" to a false harmonic due to the higher amplitude signals characteristic of the lower frequencies.

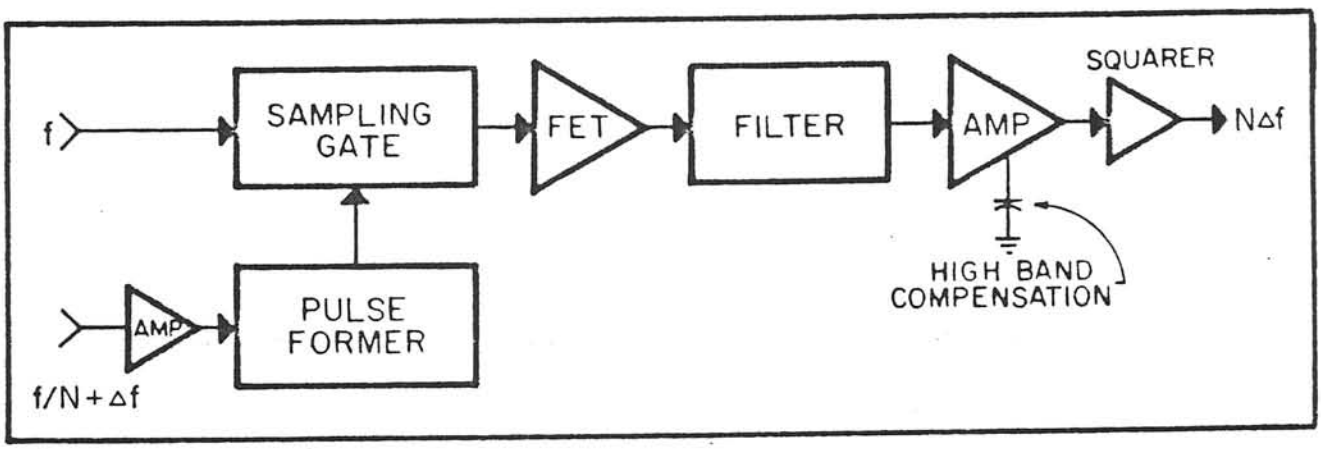


FIGURE 3-9

SAMPLER BLOCK DIAGRAM

3.4.5 Phase Shifter Circuit

The phase shifter circuit accepts the 5 kHz square wave from the time base circuitry and generates two 5 kHz sinewaves (separated by 90° phase shift) to the balanced modulators of the frequency synthesizer circuit.

The 5 kHz square wave (time base) is converted into a rough sinewave by RC circuits and coupled directly into the input of an operational amplifier. The feedback components form a highly selective "twin T notch filter" which attenuates all higher and lower

frequency components resulting in a 5 kHz sinewave of extremely low harmonic distortion. This output is the 0° phase or "sine" output. A voltage divider taps a portion of this output which is applied to a second operational amplifier, the output of which is shifted in phase by 90° (cosine output).

3.4.6 Error Counter Circuit

The error counter circuit is a six bit binary counter, the contents of which are increased by one for each "error reset" signal generated by the parity circuitry. No provision for resetting the binary is included and, on overflow, its contents simply return to zero. The initial state of the error counter is of no consequence as successive error reset signals will advance the counter to its appropriate state corresponding to the applied input and harmonic multiple.

3.4.7 Ramp Generator Circuit

The ramp generator circuit is an electronically switched voltage divider which generates an analog voltage output proportional to the contents of the error counter. Two flip-flops and a divide-by-sixteen circuit provide 64 voltage "steps" which determine the resonnant frequency of the countdown circuit's multivibrators.

3.4.8 Parity Circuit

When enabled by the time base circuitry, the parity circuit counts the $N\Delta f$ signal from the sampler for a period of Δf. The resultant tentative value of N is stored into the N counter circuitry and compared with successive values of N. If a deviation in the ensuing value of N is detected, an error reset signal is generated. This signal, in turn, resets the control logic and count chain circuitry as well as advancing the error counter which steps the ramp generator.

If the parity circuit completes four successive N consistency checks without encountering an error, the count gate is enabled and a frequency measurement is initiated. While the instrument is attempting a measurement, a fine parity circuit monitors the countdown frequency for instability. The fine parity circuit ignores the first error but will interrupt the measurement interval and generate an error reset signal upon receipt of the second fine parity error indication.

The main parity circuit performs the following tests for the value N:

1. The quantity 2N must be even. This check eliminates the possibility of a ± one count error in the N counter.
2. The value N must be equal to or greater than eight as a harmonic multiple of less than eight is possible only outside of the specified frequency bands.
3. The least significant digit of four successive values of N must be equal. This check greatly reduces the possibility of "locking on" to a false sub-harmonic.

The NΔf signal from the sampler circuit is coupled to the input of the flip-flop designated "2N" (refer to Figure 3-10). A 200 microsecond signal from the time base is coupled to the input of the "2N Gate" flip-flop. The output from the 2N Gate (divided-by-two) is used to enable the "2N" flip-flop for 400 microseconds of each 1 millisecond frame. Since 400 microseconds is equal to two periods of Δf, 2 times N pulses appear at the input. The output from the 2N flip-flop is one half the input (divided-by-two) or N with a possible one count gating error.

If the output from the 2N flip-flop is in the "1" state at the conclusion of the 400 microsecond count interval, the quantity 2 times N is considered odd. This output is coupled to the main parity gate (three-input OR gate) where it will effect an error reset.

The output of the 2N flip-flop (quantity N) is loaded into both the N counter (Section 3.4.10) and the parity counter. The parity counter is a one-decade BCD register which only counts the least significant digit of the value N. Immediately after the quantity N is loaded into the N counter, a flip-flop referred to an "N Lockout" is set by the time base. This disables the N count line denying subsequent values of N to the N counter circuitry.

The value of the least significant decade of the N counter and the contents of the parity counter are compared by a set of "exclusive OR" gates (XOR). The first comparison is obviously true as both the N counter and parity counter are loaded by the same quantity N output from the 2N flip-flop.

The second "burst of N" from the 2N flip-flop, is denyed from the N counter by the N lockout flip-flop and is therefore only counted by the parity counter. The exclusive OR gates (XOR) compare the contents of the N counter with the updated parity counter. Any discrepancy between the two counters will cause the eventual generation of an error reset signal by the action of the main parity gate.

The third input to the main parity gate is the "N must be greater than 8" function. The "over 8" flip-flop is cleared by the N Counter when the value of N exceeds the integral 8. After each "burst of N" (at the conclusion of each 1 millisecond time frame) the main parity gate is interrogated by the time base. If any of the three parity errors are present ($N \neq N_1$, $N < 8$ or $2N$ is odd), an error reset signal is generated advancing the error counter and ramp generator and initiating a new measurement. A subsequent value of N is counted by both the N and parity counters and the parity function is repeated.

If four successive N parity checks are valid (four 1 millisecond time frames), the parity circuit, after 800 microseconds, releases the time base hold off flip-flop. This represents a total time of 9.8 milliseconds as the time base was present to 5 milliseconds. The release of the TB holdoff flip-flop allows the time base to advance, in turn, enabling the control logic initiating a measurement.

During the measurement interval, fine parity circuitry checks the stability of the sampler output. The fine parity counter counts the least significant digit of the $N\Delta f$ signal for 8 milliseconds (forty times the period of Δf). If the value of N is an integral, 40N will be divisible by ten and the count decade should be clear at the end of the 8 millisecond interval. Since the binary "1" bit is not employed, a one count error is tolerable.

At the end of each 8 millisecond period, the contents of the fine parity counter are interrogated. A "2", "4" or "8" bit will set the fine parity error 1 flip-flop. A second error will clear the fine parity error 1 flip-flop and, in turn, set the fine parity error 2 flip-flop producing an error reset signal, initiating a new measurement.

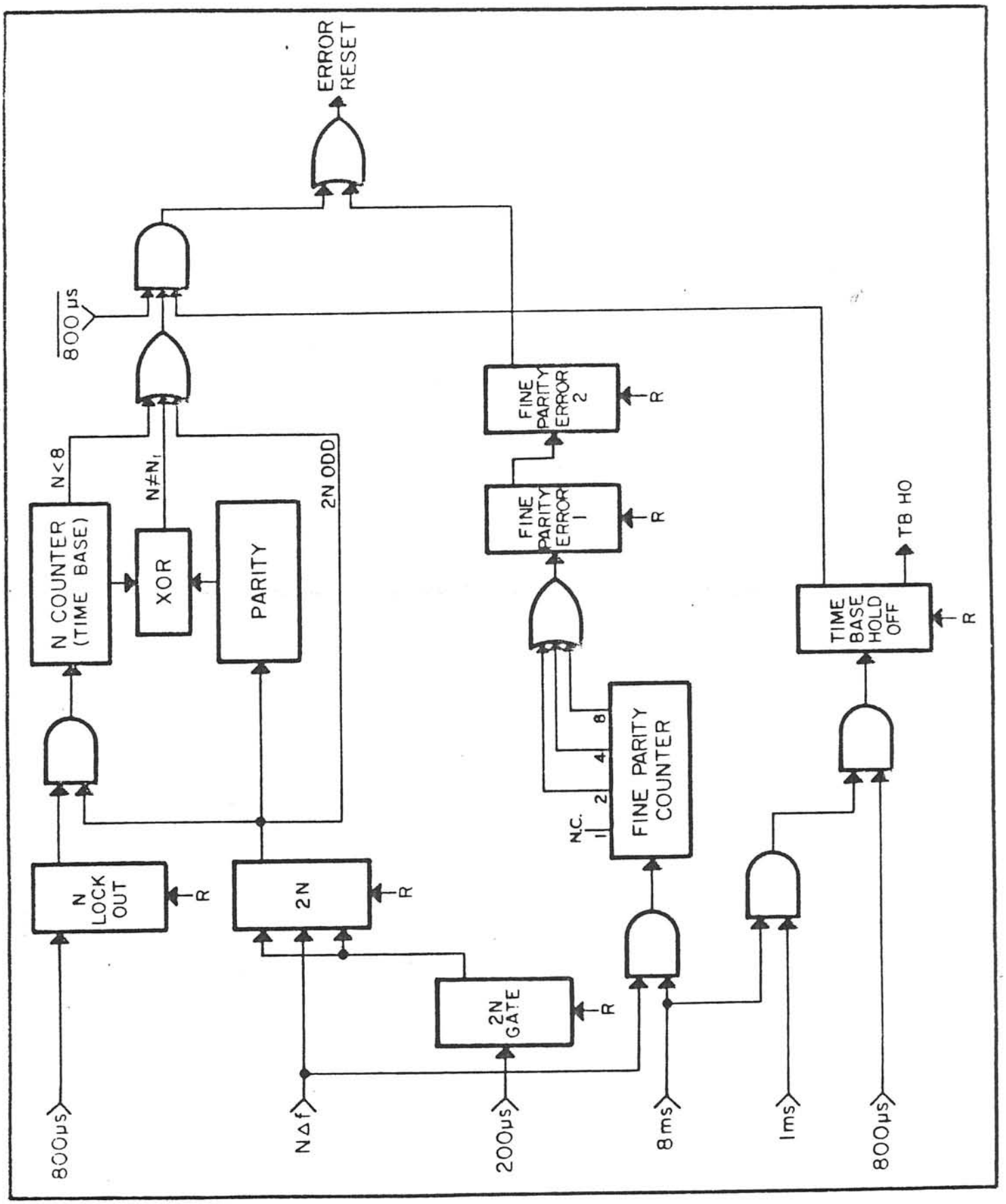


FIGURE 3-10
PARITY BLOCK DIAGRAM

3.4.9 Time Base Circuit

The time base circuit is referenced to an internal 1 MHz crystal oscillator. From this 1 MHz signal, the time base derives the timing signals required by both the parity and control circuitry. Basically, the time base circuit consists of a string of decade dividers with their corresponding reset and preset circuits and a series of gates to enable and disable the control logic (refer to the Time Base Block Diagram, Figure 3-11).

A string of four decade dividers provide the parity circuit timing signals. The squared 1 MHz output signal from the oscillator is used to load the time base multiplier from the N counter in the mid and high frequency bands. The 100 kHz output from the first decade is used to clear the TB output flip-flop immediately after it is set by the selected time base pulse. The third decade provides the 5 kHz square wave (Δf) employed by the phase shifter circuit, the 200 and 800 microsecond signals used by the parity circuit and the 1 ms timing signal to the preset-offset logic.

The fourth decade, initially set to 5 ms by the preset pulse, provides the 1 and 8 ms timing signals employed by the parity circuit and a 2 ms timing signal to the preset-offset circuit used exclusively with bands 10 and 11.

The timing signal from the preset-offset circuit, either 1 ms or 2 ms, drives a chain of four decade dividers when the TB holdoff flip-flop is cleared by the parity circuit. This chain provides the 1 ms, 10 ms, 100 ms and 1 s periods which are individually enabled by the channel switch logic, determining the corresponding channel resolution. The 10 second output from the fourth decade is not employed. Operation utilizing the mid and high bands does not require the 1 second gate time rendering both the 1 and 10 second decades available to serve as the time base multiplier. When enabled by the control circuitry, via the N flip-flop gate, the 1 MHz signal drives the N counter and the 1 second decade simultaneously. Since the N counter has been previously loaded with the value N, the 1 MHz signal adds to the value of N until the counter overflows (99 counts) disabling the 1 MHz signal. The 1 and 10 second decades, cleared by the first time base pulse, now contain 100 - N counts or the complement of N.

The time base pulse sets the TB output flip-flop. This flip-flop is cleared by the 100 kHz timing signal within the time base. The clearing of the flip-flop, not its setting, triggers the control logic.

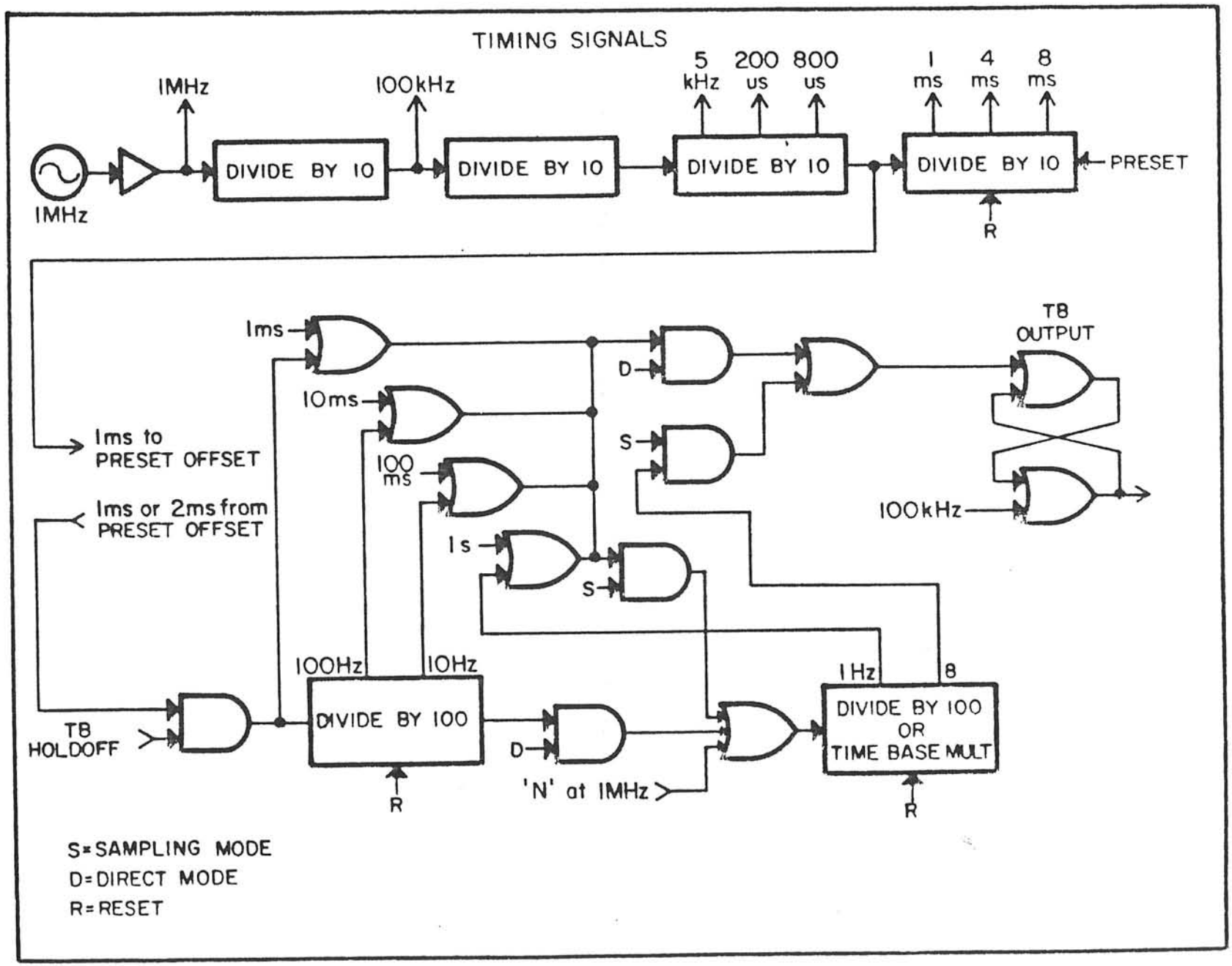


FIGURE 3-11 TIME BASE BLOCK DIAGRAM

3.4.10 N Counter

The N counter is a two-decade BCD counter that stores the value of N before transferring it to the time base multiplier.

The N counter is loaded with a tentative value of N by the parity circuit. If parity accepts the value, it releases the time base holdoff flip-flop, enabling the time base circuitry. This enables the control logic, which, in turn, sets the start-stop flip-flop and enables the N flip-flop gate. When enabled, the N flip-flop gate passes the 1 MHz time base signal to the N counter and time base multiplier as described in the previous section.

3.4.11 Control Logic

The control logic circuitry controls the count gate and generates the reset and preset signals on command from the time base or parity circuitry.

The transition of the TB output flip-flop to its zero state sets the start-stop flip-flop, opening the count gate (120 MHz DCU) and illuminating the front panel GATE lamp. The ensuing transition of the TB output flip-flop clears the start-stop flip-flop, closing the count gate thereby stopping the count, and setting the display flip-flop. The display flip-flop, in turn, enables the storage, reset and preset circuitry.

The output of the display flip-flop triggers a "one-shot" multivibrator which generates the storage-transfer pulse. This pulse transfers the accumulated count from the storage registers into the decoder circuits enabling the numerical indicator tubes. The setting of the display flip-flop also initiates the display interval by enabling the timing capacitors to charge to the conduction level of a unijunction transistor. The "firing" of the unijunction sets a flip-flop which inturn generates the reset and MECL reset pulses. These pulses clear the count chain, time base, reset and control and parity circuits. The trailing edge of the reset pulse generates the preset pulse which loads a selected preset value (determined by the preset-offset logic) in the count chain and presets the time base to 5 ms.

The generation of an error reset signal from the parity circuit will simultaneously enable both the reset and storage-transfer circuits. This action causes the display to indicate all zeros thereby avoiding an erroneous reading.

3.4.12 120 MHz DCU

The 120 MHz DCU (decimal counting unit) is, in truth, the least significant digit of the count chain. Since it is geographically distant from the remainder of the count chain, employs an exclusive family of logic and includes an important control function, the 120 MHz DCU will be discussed separately.

The 120 MHz DCU includes an input amplifier, the count gate, a decade of MECL high-speed logic and the bandswitching logic. It accepts input signals from the direct input amplifier in the low band and from the countdown circuit in the mid and high bands. The bandswitching logic enables either the output from the input amplifier or the countdown circuit output to the count gate, the instrument's primary control gate. The time base circuit enables the count gate for a fixed time interval, allowing the DCU to operate. The output from the DCU is buffered and routed directly to the succeeding DCU in the count chain.

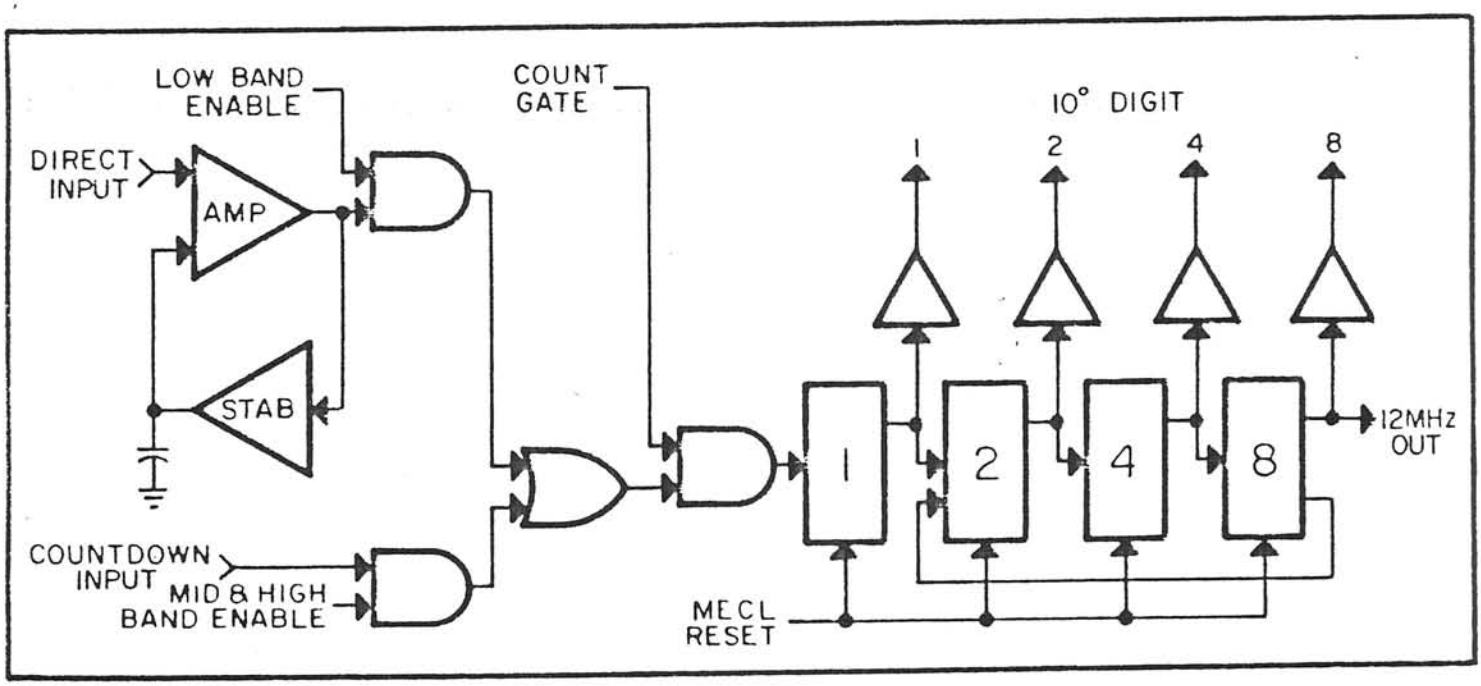


FIGURE 3-12

120 MHz DCU BLOCK DIAGRAM

3.4.13 Count Chain

The count chain consists of the remaining DCUs with their corresponding decimal indicator tubes. Each DCU is comprised of a decade counter, storage register and decimal decoder circuit. Each decade counter provides a 1-2-4-8 BCD count to its corresponding storage register and a divide-by-ten output to the succeeding decade counter. The 1-2-4-8 BCD output and the "12 MHz" carry signal from the 120 MHz DCU are directly coupled to the 12 MHz DCU. The storage register and decimal decoder circuits associated with the 120 MHz DCU are incorporated into the 12 MHz DCU card's circuitry.

The count chain consists of the 12 MHz DCU, two dual DCUs and one DCU resulting in a display of seven full digits. The four most significant digits are automatically preset when any of the offset channels are selected.

The count chain will be advanced by either the direct or countdown input until the count gate is disabled by the reset and control circuitry. The ensuing storage transfer pulse transfers the accumulated count from the storage registers to the decimal decoders which, in turn, enable the individual digits within the display indicator tubes. Since the storage transfer pulse occurs after the count gate is disabled, the display will read only the correct solution or all zeros (parity error indication).

3.4.14 Preset Offset Circuit

The preset offset circuit operates in conjunction with the CHANNEL SELECT switches or, when the REMote position is selected, from a remote device. Selecting one of the channel switch positions (either directly or remotely) enables a unique combination of time base, band, decimal point, annunciator and appropriate offset automatically. Fifteen distinct channels are incorporated into the instrument including the non-preset channels 1A, 1B and 1C (low, mid and high band respectively).

3.4.15 DAC Output

The DAC and DAC logic circuitry functions as a receiver control circuit generating an analog voltage output for a subsequent measurement variation. This voltage can be employed to control an input oscillator by establishing a "closed loop" condition maintaining the initial oscillator frequency.

When the front panel SET/LOCK switch is placed in the LOCK position, the DAC logic circuitry memorizes the BCD count of the least significant nine bits (the two least significant digits and the "1" bit from the third digit). A subsequent measurement indicating a change from the set frequency will result in an analog voltage output at pin R of the rear panel REMOTE connector. Since the DAC and DAC logic cards are supplied by an independent subcontractor, the circuit description for these circuits is not incorporated into this manual.

3.4.16 Power Supplies

The instrument derives its regulated and unregulated dc levels from either a 115 or 230 volt ac, 50-60 Hz source. Table 3-1 lists the various levels and their circuit applications.

TABLE 3-1

POWER LEVELS

VOLTAGE	APPLICATION
+230Vdc (unregulated)	Numerical indicator tube plate voltage.
+12Vdc (regulated)	High level logic.
-12Vdc (regulated)	High level logic.
+3.6Vdc (regulated)	RTL logic.
+4.5Vdc (regulated)	DTL and TTL logic.
-5.2Vdc (regulated)	MECL logic.

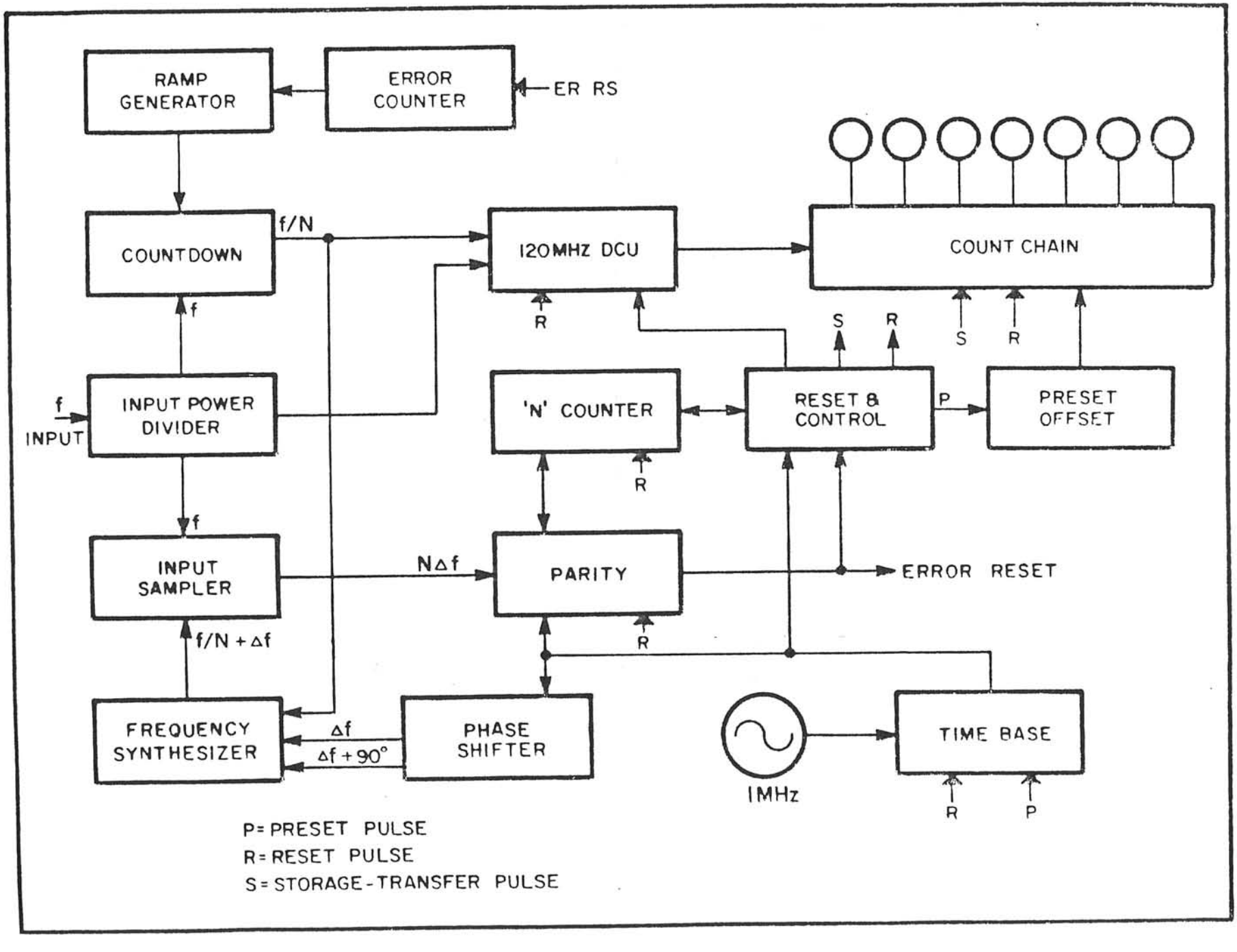


FIGURE 3-13 SIMPLIFIED BLOCK DIAGRAM

3.5 DETAILED THEORY OF OPERATION

This section approaches the theory of operation from a detailed circuit description. Subsection numbering is consistant with the block diagram analysis of section 3.4. The drawing number included in the subsection title block refers to individual schematic diagrams included at the rear of this manual.

3.5.1 Input Power Divider

The applied input signal is cabled directly from the INPUT connector to J2, the input power divider input. Two 56Ω resistors (R1 and R2) split the input signal into two equal signals which are routed to the countdown and input sampler circuits from connectors J1 and J3. Resistors R4 and R5 couple a small fraction of the input power to J4, the direct input connector to the 120 MHz DCU.

3.5.2 Countdown Circuit (D-11-06549)

The countdown circuit consists of a mid band input amplifier, two tunnel-diode multivibrators, two low pass filters and an output amplifier.

The divided input signal from the input power divider is cabled directly to the countdown and ramp pc card. Capacitor C5 couples the input signal to the emitter of Q9, the mid band input amplifier. The output, at the collector of Q9, is coupled through resistor R33 and RF choke L3 to CR9, the mid band multivibrator tunnel diode. CR11, the high band tunnel diode is driven directly from the divider comprised of R46 and R49 through capacitor C6.

The mid or high band multivibrators are enabled when +12 volts is applied to either the $\overline{M}$ lead (mid band enabled) or the $\overline{H}$ lead (high band enabled) from the reset and control circuit as determined by the CHANNEL SELECT switches and the preset offset card logic. In the low band, both multivibrators are disabled while in the sampling bands (mid and high) the selected multivibrator is permitted to free run.

Since both multivibrators are basically alike, the discussion will focus on the high band multivibrator. The corresponding components common to the mid band circuitry will be called out in brackets.

Initially, zener diode CR13 (CR8) applies 6.8 volts to the resistor string comprised of R55, 56 and 57 (R41, 42 and 43). The idling voltage and therefore the tunnel diode bias current at R55 (R41) is adjustable by potentiometer R57 (R43). Current flows through inductors L9 and L10 (L4 and L5) until the tunnel diode reaches its high-voltage state. This voltage step decreases the current through the coils and the tunnel diode returns to its low state and the cycle is repeated. The output of the ramp generator (the analog output of the error counter) is coupled to the multivibrator through R50 and CR12 (R34 and CR7). An increase in the analog voltage will increase the dc bias current through the tunnel diode increasing the frequency of the multivibrator. The high band multivibrator exhibits a frequency range of approximately 32 to 37 MHz (determined by the dc level of the ramp) while the frequency range of the mid band multivibrator is approximately 8 to 10 MHz.

A small portion of the input signal energy is coupled to the tunnel diode through C6 (C10). If the natural frequency of the multivibrator is sufficiently close to an integral subharmonic of the applied input frequency, the input signal will cause the tunnel diode to synchronize to the exact submultiple. If the multivibrator is not tuned near a submultiple, the error counter will increase the ramp voltage until synchronization occurs.

The output from the multivibrator is buffered by emitter follower Q11 (Q10) and passed through a 40 MHz (10 MHz) low-pass filter to eliminate any high frequency components from the input signal. It is amplified by Q14 (Q12) and Q13 and coupled via transformer T1 to the frequency synthesizer circuit. Voltage divider R68 and R69 reduces the signal level to approximately 1V p-p before it is coupled to the 120 MHz DCU. Capacitor C26 filters any remaining high frequency noise.

3.5.3 Frequency Synthesizer (D-11-06547)

The frequency synthesizer includes two RF phase shift networks, two balanced modulators, two low-pass filters, a divide-by-four circuit and an output amplifier.

The output from the countdown board (8-10 MHz mid band, 32-37 MHz high band) is coupled directly to input transformers T1 and T5. A pair of RC phase shift networks are associated with each transformer resulting in two outputs separated in phase by 90°. In the mid band, the networks C2, R5 and C3, C4, R6 perform the phase separation with variable capacitor C3 providing fine adjustment. In the high band, the networks C9, R15 and C10, R14 perform the phase separation with variable capacitor C10

providing fine separation adjustment.

During operation utilizing the mid band, the $\overline{M}$ lead from the reset and control circuit is at +12 volts. This potential enables the two sets of Darlington buffers (Q1-Q2 and Q3-Q4) associated with the mid band, amplifying the two mid band phase shifted signals.

Similarly, in the high band, the $\overline{H}$ lead is a +12 volts enabling the high band Darlington buffers (Q5-Q6 and Q7-Q8) amplifying the two high band phase shifted signals. The disabled phase shifted signals are ignored while the outputs from the enabled Darlington buffers are coupled to transformers T2 and T6.

Transformers T2 and T3 and the diode bridge (CR1-4) form a balanced modulator. Its inputs are the two phase shifted signals from the enabled Darlington buffers (f/N and f/N + 90°) and the 5 kHz "SIN" signal (Δf) from the phase shifter circuit via resistor R22.

Transformers T6 and T7 and the diode bridge (CR10-13) form a similar balanced modulator. Its inputs are the same two phase shifted signals from the enabled Darlington buffers (f/N and f/N + 90°) and the 5 kHz "COS" signal (Δf + 90°) from the phase shifter circuit via resistor R23. The outputs from the two balanced modulators are common. The phase separation resulting from the mixing of the two phase shifted 5 kHz signals (Δf and Δf + 90°) causes one set of side bands to cancel and the other set to reinforce, resulting in an output of either f/N - Δf or f/N + Δf at the junction of CR5 and CR14.

During operation in the mid band, the +12 volt potential ($\overline{M}$) applied to R24 enables diode gate CR5-CR6, passing the 8-10 MHz + 5 kHz slewed countdown signal to the 10 MHz low-pass filter (L3-6, C20-24). The low-pass filter eliminates any harmonics or noise that may have been generated by the modulators and shapes the signal into a rough sine wave. The signal is amplified by Q9 and Q10 and coupled to the sampler circuit through toroidal autotransformer T4.

During high band operation, diode gate CR5-CR6 is disabled while the +12 volt potential ($\overline{H}$) forward biases diode CR14 via R28. The 32-37 MHz + 5 kHz slewed countdown signal is coupled through the 40 MHz low-pass filter (L7-9, C33-36) to eliminate any unwanted harmonics or noise and squared by Q11, 12 and 13 for TTL logic compatibility.

Flip-flops MC1A and MC1B divide the signal by four. The resultant output (f/4N + 1.25 kHz) is attenuated by R25 and R26, coupled to the 10 MHz filter via enabled diode gate CR7-CR8 and amplified by Q9 and Q10 before being coupled to the sampler circuit by toroidal transformer T4. *

3.5.4 Input Sampler (D-11-06548)

The input sampler accepts the input signal from the input power divider and the slewed countdown output from the frequency synthesizer to produce an output of NΔf to the parity circuit.

The high frequency input from the input power divider is cabled directly to the input sampler, loaded to 50Ω by resistor network R1-R4 and coupled to the diode sampling gate (CR1-CR4) which is normally back biased through R24 and R9. The slewed countdown output from the frequency synthesizer is directly coupled to the input sampler at pin B. Transistors Q3, Q4 and Q5 amplify and shape the signal resulting in a series of positive and negative pulses at the emitter of Q5. Balancing transformer T1 and the transmission line consisting of C7, L3 and L4 couple the pulses to step recovery diode CR5. Inductors L3 and L4 are not actual components but the traces themselves leading to capacitor C7. CR5, the snap recovery diode increases the rise time of the pulses resulting in a positive pulse of approximately 200 picoseconds duration. These pulses are capacitively coupled to the sampling bridge through capacitors C3 and C6. The positive pulses forward bias the bridge permitting FET Q1 to observe a fraction of a cycle of the input period. The sampled signal is source and emitter followed by Q1 and Q2 respectively. The 8-10 MHz "carrier" frequency is filtered out by C4, L1 and C13 resulting in a low frequency sinewave output between 40 and 500 kHz, the NΔf signal.

The amplitude of the NΔf sinewave decreases sharply as the frequency increases. At the lower sampling frequencies, the 200 picosecond sampling pulse is considerably shorter in duration than the period of the input waveform and is likely to be totally positive or negative for the full duration of the pulse. At the higher frequencies, since the pulse width approaches the input period, the sampling pulse observes both the positive and negative characteristics of the input waveform. The corresponding output amplitude decreases due to the averaging of the two potentials.

The NΔf signal from the filter is amplified by transistors Q6, Q7 and Q8. Capacitor C16 increases the gain of Q6 for frequencies in excess of 100 kHz. C19 and C24 increase the gain of Q7 and Q8 at frequencies in excess of 200 and 400 kHz respectively. The output (collector of Q8) is clipped by diodes CR9, 10 and 11 and capacitively coupled to output amplifier MC1A. MC1B and MC1C square the signal for logic level compatibility while MC1D and MC1E buffer the NΔf signal before it is coupled to the parity circuit.

During mid band operation, diode CR12 is enabled by the positive potential on the $\overline{M}$ lead through R49. This action effectively bypasses the emitter of Q8 to ground through C27, increasing the gain of the stage and thereby decreasing the signal-to-noise ratio of the amplifier. Allowing the relative noise level to increase combats a tendency of the countdown circuit to lock on to the higher amplitude false harmonics characteristic of the mid band.

3.5.5 Phase Shifter (D-11-06546)

The phase shifter accepts the 5 kHz square wave from the time base circuit and generates the two phase shifted 5 kHz sinewaves (Δf and Δf + 90°) to the frequency synthesizer.

The 5 kHz signal from the time base is coupled to the base of Q4. The buffered output (collector) is shaped by the two RC networks R30, C10 and R31, C11, and coupled to the input of operational amplifier MC13B. The resistor-capacitor network consisting of R39-41 and C17-19 in the feedback loop is a highly selective "twin T notch filter". The filter exhibits a very high impedance at its center frequency (5 kHz) and a low impedance to all other frequencies. The input to the operational amplifier is a distorted sinewave, rich in higher-order harmonics. The twin T notch filter feedback loop converts the operational amplifier into a selective amplifier, effectively filtering all non-5 kHz components of the input resulting in pure sinewave output of extremely low harmonic distortion.

The "SIN" output (zero phase) is taken from the junction of voltage divider R42, R43 A portion of the output signal is coupled, via R37, to the input of a second operational amplifier. MC13A is, in essence, a voltage-time integrator, the time constant of which is determined by the RC network R37 and C20. The output, a 5 kHz sinewave shifted in phase by 90° (COS), is taken at the junction of voltage divider R44, R45.

Both operational amplifiers (MC13B and MC13A) include high frequency roll off networks (R34, C12, C13, C14 and R35, C15, C16) to prevent the possibility of being driven into oscillation.

The two outputs (SIN and COS) are coupled to the frequency synthesizer circuit as the Δf and $\Delta f + 90^{\circ}$ slewing frequencies.

3.5.6 Error Counter (D-11-06549)

The error counter is a six-bit binary register which advances each time an error reset signal is generated by the parity circuit. Its outputs are employed to "step" the ramp generator with each error reset pulse. There is no reset function associated with the counter and its contents do not reflect the number of error reset pulses that have occurred.

The error reset signal is coupled directly to the toggle input of MC1A, the first of two J-K flip-flops providing a divide-by-four function. The S and C lines associated with each flip-flop are permanently enabled (low state). The Q output from MC1B is directly coupled to MC2 a divide-by-sixteen counter. The overall circuit configuration results in a 64 count register with the six bits associated with the counter coupled directly to the ramp generator's voltage divider network.

3.5.7 Ramp Generator (D-11-06549)

The ramp generator translates the contents of the error counter into an analog voltage which is used to control the output frequency of the countdown circuit's multivibrators.

The bases of switching transistors Q1 through Q6 are placed at approximately +1 volt by voltage divider R12 and R15. The emitter of each transistor is connected to the -12 volt supply through a 10kΩ resistor (R18, 20, 22, 24, 26 or 28) and to the corresponding flip-flop from the error counter via diodes CR1 through CR6. A transistor is enabled when and ONLY when its associated flip-flop is in its zero state.

The precision resistor ladder consisting of resistors R1 through R11 forms a voltage divider in conjunction with R14. The equivalent resistance of the ladder network is proportional to the weighted sum of the disabled transistors. "Weighted" in this connotation is defined as "given importance according to its binary weight".

Transistor Q2, when disabled, will exhibit a greater effect on the voltage divider than if Q1 were disabled and accordingly, Q3 will exhibit more effect than Q2.

The junction of the voltage divider is coupled directly to the base of Q7. Q7 and Q8 form a Darlington emitter follower which is used to isolate the load. A portion of the output energy at the emitter of Q8 is coupled back to the emitters of the switching transistors which changes the response of the ramp from a linear function to an inverse exponential function.

The exponential function permits a greater number of voltage steps in the more critical region of the countdown multivibrator's voltage response, increasing the reliability and decreasing the search time in the high band.

3.5.8 Parity Circuit (D-11-06546)

The parity circuit is negative in nature. That is, it detects errors rather than corrects readings. If an error occurs, the parity circuit will stop the measurement, reset the instrument and advance the ramp generator for the ensuing measurement. When satisfied that the measurement is correct, the parity circuit merely refrains from generating an error reset signal.

The NΔf signal from the sampler, a square wave between 40 and 500 kHz, is coupled directly to the toggle input of 2N flip-flop, MC1B. The S and C inputs of MC1B are, in turn, controlled by the $\overline{Q}$ output from MC1A, the 2N Gate flip-flop. The 200 μs signal from the time base is inverted by MC2A and coupled to the toggle input of MC1A. The 2N flip-flop (MC1B) will therefore be enabled for 400 μs of each 1 ms frame. Since 400 μs is equal to two periods of Δf, the 2N flip-flop will count N two times. The Q output, divided-by-two, is therefore equal to N, the harmonic multiple.

The output from 2N flip-flop MC1B is directly coupled to quadruple NOR gate MC5A, the main parity gate, as the "2N odd" parity verification. Since the 2N flip-flop (MC1B) was originally in its low state and was toggled 2N times, a high state output would imply that 2N is an odd number and that N therefore could not be an integer.

The N Lockout flip-flop, MC2C and MC2D is set by the trailing edge of the 800 μs pulse from the time base through capacitor C3. This pulse occurs after one complete "burst" of N pulses has been acknowledged by the 2N flip-flop. The N count is

capacitively coupled to inverter MC2B and counted by MC3, the parity counter. The parity counter is a decade of CμL logic which counts only the least significant digit of the N count. NOR gate MC8C is enabled only when the N Lockout flip-flop is in its zero state allowing only the first burst of N to be counted by the N counter circuit before the N Lockout flip-flop changes state.

MC4, a quadruple exclusive OR gate (XOR) compares each bit from the parity counter with the corresponding bit from the least significant decade of the N counter. Each of the four XOR gate outputs will be in its high state if and only if the bits are not identical. The outputs are, in turn, coupled to NOR gate MC5B. MC6C inverts the signal from MC5B before it is coupled to MC5A, the main parity gate, as the $N \neq N_1$ parity verification.

Since the first burst of N will be loaded into the parity counter and the N counter simultaneously, the XOR gates will not detect an error and their corresponding outputs will all be in a low state. After 800 μs, the N Lockout flip-flop changes state, disabling the count from the N counter at NOR gate MC8C. The 800 μs pulse also clears the 2N flip-flop (MC1B) and the parity counter (MC3) by back biasing Q1 through C2. The next burst of N will be counted only by the parity counter. Any discrepancy between the initial count in the N counter and the current count within the parity counter will be detected by the XOR gates resulting in a high state at pin 2 of MC5A, the main parity gate.

The third main parity verification is "N must be greater than 8". MC6A and MC6B form the N>8 flip-flop which is set initially by the reset pulse. If the N counter does not reach a count of 8 to clear the flip-flop, its high state will effect the generation of an error reset signal when the contents of the main parity gate are examined.

The main parity gate is interrogated at the conclusion of each 800 μs interval of each 1 ms frame. The 800 μs signal from the time base (pin 3) is inverted by transistor Q2 and capacitively coupled to MC6D through C7. The trailing edge of the $\overline{800\ \mu s}$ pulse momentarily enables the contents of the main parity gate to MC9A the error reset gate. If any of the previously mentioned parity errors are present, the output of MC9A will assume a low state, advancing the error counter, clearing the control logic and initiating the entire parity cycle again.

If the time base is able to reach a count of 9.8 ms without the main parity circuit detecting an error, the TB holdoff flip-flop (MC12A and MC12D) will be set, enabling the time base circuit and the start-stop flip-flop in the reset and control circuit.

The TB holdoff flip-flop is set by a combination of three of the time base signals present within the parity circuit. The 8 ms and 1 ms timing pulses, at pins T and U respectively, are directly coupled to NOR gate MC8D. The high state output, after 9 ms, is inverted by MC11C and directly coupled to one of the inputs of NOR gate MC11D. The inverted 800 μs time base pulse from the collector of Q2, is coupled through R18, to the remaining input of NOR gate MC11D. The high state output, after 9.8 ms, will be coupled through capacitor C4, setting the TB holdoff flip-flop.

Recalling that the time base was initially preset to 5 ms by the preset pulse, it is evident that the TB holdoff flip-flop will be set after 4.8 ms of actual time has elapsed. The parity circuit must therefore complete four consecutive N value verifications, void of the three main parity errors, before an actual measurement can begin.

Even after the TB holdoff flip-flop is set, a fine parity circuit monitors the NΔf signal from the sampler circuit for instability. MC10, the fine parity decade counter, is permitted to count the NΔf signal for 8 ms by NOR gate MC8A. Since 8 ms is equal to forty periods of Δf, 40N must be divisible by ten and the corresponding decade outputs would be in their high state. A one count error is permissible as the binary 1 bit is not connected. If either the 2, 4 or 8 binary bit were to be in its low state at the conclusion of the 8 ms period (an indication that N is not integral), a fine parity error would be tallied in the Fine Parity Error 1 flip-flop. The setting of the TB holdoff flip-flop enables the contents of the fine parity decade at NOR gate MC12B. If one or more of the decade outputs were in their low state, the output of MC12B would assume a high state which would, in turn, be inverted by MC12C. The 9 ms interrogation pulse coupled across C5 enables the output of inverter MC12C to the fine parity error 1 flip-flop, MC7B. The output from MC7B is directly coupled to the toggle input of MC7A, the fine parity error 2 flip-flop. The second fine parity error will clear MC7B and set MC7A. The $\overline{Q}$ output at pin 14 will be in its low state upon receipt of the second fine parity error. The following $\overline{800\ \mu s}$ pulse, coupled across C8, enables NOR gate MC9C resulting in the generation of an error reset signal, resetting the count chain and advancing the error counter.

3.4.9 Time Base (D-11-06627)

The time base circuit is responsible for the generation of the various timing signals employed by the parity circuit and for the establishment of the measurement interval for which the count gate is enabled. The circuit is referenced to a 1 MHz crystal oscillator and incorporates a string of decades and related logic to perform its various functions. The time base circuitry also includes the N counter and the time base multiplier circuits.

The 1 MHz input signal from the crystal oscillator (pin 7) is squared by inverters MC6C and MC6D and coupled directly to the input of decade counter MC7. The output of MC7 (100 kHz) is coupled to the input of decade counter MC8 and to inverter MC6B. The inverted 100 kHz signal from MC6B is used to clear the TB output flip-flop, MC2A and MC2B. Decade counter MC8 provides a divide-by-ten function resulting in a 10 kHz signal at the input of MC13.

Decade MC13 provides the 200 μs and 800 μs timing signals used by the parity circuit, the 5 kHz signal (Δf) used by the phase shifter circuit and the 1 kHz signal which is coupled to the succeeding decade (MC14) and to the preset-offset circuitry. Decade MC14, another divide-by-ten circuit, provides the 2 ms signal (pin X) to the preset-offset circuit used with channels 10 and 11 to divide the time base by two and the 1 ms and 8 ms timing signals used by the parity circuit. Initially, decade MC14 is preset to 5 ms (1 ms and 4 ms) by the preset pulse from the reset and control circuit.

The time base signal from the preset-offset circuit, either 1 ms or 2 ms (channels 10 and 11) is coupled to the collector of Q9 at pin S. The clearing of the TB holdoff flip-flop (parity circuit) after 9.8 ms, enables the time base to the remaining decade dividers. MC17, the 10 ms decade, is preset to 8 as long as the TB holdoff flip-flop is set. The remaining three decades (MC18, MC15 and MC16) are each preset to 9 when the TB holdoff flip-flop is set. The presetting of these four decades, via MC19 and MC20, enables the frequency measurement to start approximately 1 ms after parity accepts a tentative value of N (mid and high bands). Decades MC18 and MC15 providing timing periods of 100 ms and 1 s respectively. The 10 second decade (MC16) is not used with the timing functions while the 1 s time base is restricted to the low band only. The selected time base is determined by the CHANNEL SELECT switch position through the corresponding preset-offset circuit's logic resulting in a low state on one of the emitter leads of transistors Q1 through Q5. A low state will

enable one of the NOR gates associated with the selected time base (MC1A, MC3A, MC3C or MC3D). Recalling that the 10 ms decade (MC17) was preset to 8 and that the remaining decades were preset to 9, when the TB holdoff flip-flop is cleared (after 9.8 ms), the 1 ms (or 2 ms) time base pulse, at the collector of Q9, will be counted by MC17. The next pulse will overflow decades MC17, MC18, MC15 and MC16. The 8 bit of each decade is coupled to its corresponding NOR gate (MC1A, MC3A, MC3C or MC3D). During operation employing the low band, the low band enable signal at pin 16 will be in its low state which will hold the parity gate (MC10D) high disabling the error reset function on the reset and control circuit and disabling the 1 MHz signal at transistor Q10. The high state output from MC10D enables NOR gate MC10A while disabling the 5 kHz Δf signal at NOR gate MC4A and the time base multiplier function at NOR gate MC1C.

The negative transition of the selected time base pulse will be inverted by its corresponding NOR gate (MC1A, MC3A, MC3C or MC4D) and inverted again through either MC9B or MC1B to the input of enabled NOR gate MC10C. The low state output from MC10C is directly coupled to enabled NOR gate MC10A producing a high state output which, coupled through capacitor C5, will set the TB output flip-flop comprised of MC2A and MC2B. The TB output flip-flop will be cleared almost immediately by the inverted 100 kHz timing signal from decade MC7. The clearing of the TB output flip-flop will set the start-stop flip-flop on the reset and control circuit enabling the count gate. The next negative transition of the time base pulse will again set the TB output flip-flop which will, in turn, be cleared by the 100 kHz time base signal. The start-stop flip-flop will be toggled to its low state disabling the count gate and stopping the count.

During mid or high band operation, the low band enable signal at pin 16 is in its high state causing the parity gate (MC10D) output to be low. The low state output enables the error reset function from the parity circuit on the logic and control board, the 5 kHz Δf signal to the synthesizer at NOR gate MC4A, the 1 MHz time base signal to transistor Q10 through MC4B and NOR gate MC1C.

The negative transition of the selected time base (1 ms, 10 ms or 100 ms) will be inverted by its corresponding NOR gate (MC3A, MC3C or MC4D) inverted again through either MC9B or MC1B to enabled NOR gate MC1C. The high state output from MC1C is coupled to the input of 4 input NOR gate MC9A adding 1 count to decade MC15. Decades MC15 and MC16, originally preset to 99 by the initial setting of the

TB hold-off flip-flop, both overflow causing the 8 bit output of MC16 to assume a high state.

The high state output is coupled directly to enabled NOR gate MC10B. The low state output from MC10B is, in turn, inverted by enabled NOR gate MC10A, setting the TB output flip-flop through C5. The clearing of the TB output flip-flop by the 100 kHz time base signal sets the start-stop flip-flop on the reset and control circuit enabling the count gate.

The setting of the start-stop flip-flop produces a low state on the N F/F gate lead at pin 2. The low state from the TEST/NORMAL switch (NORMAL position) produces a high state output from MC5D which, coupled across capacitor C1, clears the flip-flop comprised of MC5B and MC5C enabling the 1 MHz signal at NOR gate MC6A. Recalling that the N counter (decades MC11 and MC12) was previously loaded with N counts from the parity circuit, the enabled 1 MHz signal will be added to the existing count until the decade overflows, resetting the flip-flop (MC5B and MC5C). The 1 MHz signal, while being added to the N counter, is simultaneously enabled to decade MC15 through 4-input NOR gate MC9A. Since these decades were cleared by the first time base pulse, they will contain the complement of N or 100-N counts when the 1 MHz signal is disabled.

The filling of the time base multiplier (decades MC15 and MC16) will be completed prior to the receipt of the negative transition of the next time base pulse since counting is accomplished at a 1 MHz rate.

The ensuing time base pulses will be counted by the "time base multiplier" until N counts are obtained and the decades overflow. On overflow, the 8 bit from MC16 assumes a high state output which, as previously described, sets the TB output flip-flop through C5. The clearing of the TB output flip-flop by the 100 kHz time base signal toggles the start-stop flip-flop to its low state disabling the count gate.

3.5.10 N Counter (D-11-06627)

The N counter is a two decade counter comprised of MC11 and MC12, incorporated into the time base circuitry. As described, the N counter is loaded with the first tentative value of N by the parity circuit. The 1, 2, 4 and 8 bits of the least significant digit (MC11) are coupled to the exclusive OR (XOR) gates within the parity

circuit where subsequent values of N are compared. The N count from the parity circuit is coupled to NOR gate MC5A at pin 6. Since, at this time, the flip-flop comprised of MC5B and MC5C is set, the N count will be enabled through NOR gate MC5A to the input of the first count decade. The N > 8 parity function is associated with the N counter. The 8 bit of the least significant decade is coupled to the base of transistor Q6. Since the 8 bit will be in its high state until the count of 8, transistor Q6 will be forward biased holding the N > 8 lead (pin 4) to the N > 8 flip-flop low, maintaining its initial set position. On the count of 8, the 8 bit assumes a low state which will reverse bias transistor Q6, enabling the positive potential at its collector which, in turn, will clear the N > 8 flip-flop.

After parity releases the TB holdoff flip-flop and the start-stop flip-flop is set by the time base, the 1 MHz signal will be added to the N count until decade MC12 overflows resetting the flip-flop (MC5B and MC5C), disabling the 1 MHz signal to the N counter and time base multiplier.

3.5.11 Reset and Control (D-11-06678)

The reset and control circuitry opens and closes the count gate on command from the time base circuit and is responsible for the generation of the storage-transfer, reset, MECL reset and preset pulses employed throughout the instrument.

The setting of the TB holdoff flip-flop at reset clears start-stop flip-flop MC1A and display flip-flop MC1B through inverter MC2A. These flip-flops are enabled when parity releases the TB holdoff after 9.8 ms. The clearing of the TB output flip-flop by the 100 kHz timing signal after its initial setting by the selected time base pulse will toggle the Q output of MC1A to its low state and the $\overline{Q}$ output to its high state. The low state Q output enables the N F/F gate on the time base circuit (mid and high band operation) while the high state $\overline{Q}$ output back biases Q2 enabling the count gate on the 120 MHz DCU. Holding Q2 off forward biases Q3 which, in turn, forward biases Q4 illuminating the front panel GATE lamp indicating a measurement in progress.

The next cycle of the TB output flip-flop will toggle the start-stop flip-flop's Q output to its high state disabling the N F/F gate, and its $\overline{Q}$ output to its low state disabling the countgate, extinguishing the GATE lamp and toggling the display flip-flop, MC1B. The Q output from MC1B will be low disabling the J and K inputs of MC1A. The high state $\overline{Q}$ output from the display flip-flop (MC1B) performs three

separate functions. It disables the fine parity circuit, triggers the storage-transfer one-shot and initiates the display interval.

The Q output is coupled directly to the C input of the fine parity error 2 flip-flop disabling fine parity gate, MC9C on the parity P.C. board.

At 3-input NOR gate MC3C, the high state Q output from the display flip-flop produces a low state output which is coupled across C7 to inverter MC2D. Inverter MC2E provides yet another inversion driving the high level storage-transfer line to its low state, creating the storage-transfer pulse. The duration of the pulse is determined by the RC time constant of C7 and R21 (typically 15 μs).

At transistor Q1, the high state Q output forward biases the transistor resulting in a positive potential at its collector. This positive potential charges capacitor C3 when the FAST/NORM switch is placed in the FAST position or both capacitors C2 and C3 when in the NORM position. Q5, the unijunction transistor, will "fire" when the charge across the capacitor(s) reaches its conduction level. In the NORM position, the typical charge (display) time is approximately 100 ms while in the FAST position, the firing level is reached in approximately 1 ms. When the unijunction conducts, a positive transition is coupled across capacitor C5, driving the output of MC3B to its low state. The low state output is capacitively coupled to the input of inverter MC4A producing a positive going pulse at its output. This pulse clears the flip-flop comprised of MC4B and MC4C. The clearing of the flip-flop enables NOR gate MC4D. The next negative transition of the $\overline{800\ \mu s}$ pulse from the time base will set the flip-flop, coupling a positive going pulse across capacitor C13. The positive pulse is inverted by MC3A resulting in a low state output. Since the output of MC3A was previously held at a high level by its three low state inputs, capacitor C16 couples a negative transient to the base of Q11. This momentarily forward biases the transistor pulling the negative MECL reset line up towards ground generating the MECL reset pulse.

The low state output from MC3A is coupled across capacitor C15 producing a positive pulse at the output of MC5A. This pulse forward biases transistor Q13 generating the positive going reset pulse. The RC time constant determined by resistor R36 and capacitor C15 fixes the reset pulse duration at approximately 40 μs.

Capacitor C17 couples a negative pulse to the input of inverter MC5B when inverter MC5A returns to its normal low state. The positive going pulse at the output of MC5B, typically 40 μs in duration, is employed as the preset pulse, loading the count chain and presetting the time base to 5 ms.

During operation in either of the sampling bands, the parity gate at MC5D will be enabled by the time base circuit. The generation of an error reset signal by the parity circuitry will produce a high level output at MC5D. A positive pulse will be coupled across C12 to 3-input NOR gate, MC3A, generating the reset and MECL reset pulses previously described. However, before inverter MC5A returns to its low state generating the preset pulse, the high state output from MC5D will trigger the storage-transfer one-shot through capacitor C8. The RC time delay (R12 and C8) permits the storage-transfer pulse to occur after reset and MECL reset but prior to the generation of the preset pulse. This timing sequence results in a read-out display of all zeros whenever parity detects on error.

3.5.10 120 MHz DCU (D-11-06838

The 120 MHz DCU (decade counting unit) is, in essence, the least significant digit of the count chain. As it must be capable of counting frequencies to 120 MHz, the divide-by-ten function is accomplished by a series of MECL high speed logic J-K flip-flops.

The 120 MHz DCU circuitry includes a high gain amplifier, the count gate, a decade of high speed MECL logic and bandswitching logic to enable either the direct input (low band) or the countdown input (mid and high bands).

During low band (direct) operation, the input signal at connector J4 of the input power divider is cabled directly to J1, the input connector on the 120 MHz DCU card. The voltage divider comprised of R6, CR1 and R7 maintains a zero reference level to the input while zener diode CR1 forward biases emitter follower Q1. Common base transistor Q2 is forward biased by voltage divider R11 and R12, coupling the input signal to the base of amplifier Q3.

Transistors Q3, Q4, Q5 and Q7 amplify the input signal. The bypass capacitors associated with the emitter of each transistor counteract a tendency to oscillate due to the high gain of the stage. The high amplitude signal at the collector of Q7 is limited

to approximately 1.5 volts by diodes CR4-CR5 and CR6-CR7. Transistors Q8 and Q6 feed a portion of the output energy back to the emitter of Q3, decreasing the overall gain of the stage. Capacitors C7, C8 and C10 filter the signal to a dc level which, coupled through diodes CR2 and CR3, decreases the dc bias of Q3.

Transistors Q9 and Q10 form a Schmitt trigger, squaring the signal and providing the required MECL logic levels. The output, at the collector of Q10, is coupled directly to the input of MC7A. In low band, the CH. A Enable line at pin 16 will be at a high state while the Test-Override line, at pin 13, will be in its low state. The high state is inverted by MC9D and coupled to NOR gate MC9A. The low level Test-Override line is coupled directly to the remaining input of MC9A producing a high level output. The junction of voltage divider R52-R51 will therefore be positive, back biasing Q13, enabling the -5.2 volt supply through R50 to the input of MC7A. Since three of the inputs of MC7A will be at a low level, the direct input from the Schmitt trigger will be enabled to MC7B, the count gate.

With the Test-Override line in its low state, transistor Q15 will be forward biased by voltage divider R59-R60, grounding (high state) one of the inputs of MC8B. This disables the 1 MHz test signal and results in a low state output to MC7B, the count gate. The high state CH. A Enable line will be inverted by MC9C, forward biasing transistor Q14. The collector of Q14 will assume a high (ground) state disabling the countdown input at MC8A. The resulting low state output from MC8A is also coupled to MC7B. The count gate is enabled when the start-stop flip-flop reverse biases transistor Q2 on the reset and control circuitry, opening the count gate lead to the 120 MHz DCU. The voltage divider of R46-R47 produces a low state input to MC7B, enabling the direct input signal from MC7A to MC6, the first of four high speed MECL J-K flip-flops.

During mid or high band operation, the CH. A Enable line will be held in its low state by the preset-offset logic. The high state output from inverter MC9D results in a low state output from MC9A, forward biasing transistor Q13 through voltage divider R52-R51. The collector of Q13 will be at ground (high state) disabling the direct input at MC7A. Since both inputs to MC9C are in their low state, the output will assume a high level. The junction of voltage divider R56-R57 will therefore by positive in respect to ground, reverse biasing transistor Q14. With Q14 held off, the collector will be at -5.2 volts through R53, enabling the countdown frequency at MC8A.

Three of the inputs to the count gate (MC7B) will be in their low state thereby enabling the countdown frequency from MC8A.

The four MECL J-K flip-flops (MC6, 5, 4 and 3) are arranged to provide a 1-2-4-8 BCD output and a divided-by-ten function. The BCD outputs and the divide-by-ten output are buffered by MC1 and MC2 respectively for RTL logic compatibility prior to being coupled to the 12 MHz DCU.

3.5.13 Count Chain

The count chain includes the 12 MHz DCU (Schematic Drawing D-11-06542), two dual DCUs (Schematic Drawing D-11-06541) and a single DCU (Schematic Drawing C-11-06540) with their corresponding decimal indicator tubes. Each DCU includes a decade counter, storage register and decimal decoder circuit. The decade counters each provide a 1-2-4-8 BCD count to their respective storage registers and a divided-by-ten "carry" to the succeeding decade. The decades count either the direct or countdown input for the duration that the count gate is enabled. The storage-transfer pulse, which is generated at the conclusion of the measurement interval, transfers the accumulated count in the storage registers to the decimal decoders, which, in turn, enable the appropriate digit within the individual decimal indicator tubes.

The four most significant digits of the count chain are automatically preset by the preset pulse during operation employing channels 2 through 13.

3.5.14 Preset Offset Circuit (D-11-06626)

The preset offset circuit operates in conjunction with the CHANNEL SELECT switches or, during remote operation, from a remote device through the rear panel REMOTE connector. The desired channel is selected when the corresponding channel line to the preset offset circuitry is grounded. Channels 1A, 1B and 1C (low, mid and high bands respectively) are not preset while, when selecting channels 2 through 13, a unique offset is preset into the four most significant digits of the count chain. Table 3-2 lists the functions associated with each channel.

TABLE 3-2

CHANNEL FUNCTIONS

CHANNEL	BAND	TIME BASE	DECIMAL	LEGEND	PRESET VALUE
1A	low	10 ms	000.0000	MHz	none
1B	mid	10 ms	000.0000	MHz	none
1C	high	1 ms	0000.000	MHz	none
2	low	1 s	0.00000(0)	MHz	9545
3	low	100 ms	00.0000(0)	MHz	9570
4	low	100 ms	00.0000(0)	MHz	0420
5	low	100 ms	00.0000(0)	MHz	7860
6	mid	10 ms	000.000(0)	MHz	9786
7	mid	10 ms	000.000(0)	MHz	9400
8	high	10 ms	000.000(0)	MHz	9400
9	low	100 ms	00.0000(0)	MHz	3500
10	high	1 ms X2	0000.00(0)	MHz	9890 9840 +160
11	high	1 ms X2	0000.00(0)	MHz	0160 +160
12	low	1 s	(0)000.000	kHz	-700
13	high	1 ms	0000.00(0)	MHz	2100

During operation employing channels 2 through 11 and 13, the right most (least significant digit) display indicator tube is disabled (blanked) while in channel 12, the left most display indicator tube is disabled.

To simplify the circuit function of the preset offset circuit's logic, assume the selection of Channel 6 for the purpose of explanation. The selection of Channel 6 (left CHANNEL SELECT switch in the 2-12 position and the right CHANNEL SELECT switch in the 6 position) grounds (low state) the preset 6 line to the preset offset circuit at pin 19 while leaving the remaining channel select lines open circuited. The low state input is coupled directly to NOR gate MC21B enabling the 10^3 "2" bit and to inverter MC11F. The high state output from MC11F is coupled to six NOR gates. At MC20D, the high level input produces a low level output, enabling MC20A, the 10^5 "2" bit. The high level input at MC15C results in a low level output to MC17A. Since the two remaining inputs to MC17A are low, the

output to MC17C will be in its high state and consequently effect a low state output enabling MC21C, the 10^5 "1" bit. At MC19C and MC20C the high level inputs result in low level outputs enabling MC19B and MC20B, the 10^4 "8" and the 10^3 "4" bits respectively.

The mid band select NOR gate (MC5C) and the 10 ms select NOR gate (MC5A) will be similarly enabled by the high state output from inverter MC11F. The low level mid band output is coupled to the reset and control circuit where it is inverted and routed to the countdown, frequency synthesizer and input sampler circuits as the $\overline{M}$ signal, enabling the mid band functions. The low level 10 ms output is coupled directly to the time base circuit, enabling the 10 ms time base and its associated decimal point (dec 5).

Recalling that the remaining channel select lines will all be open circuited, the resultant outputs from their corresponding inverters will all assume a low state. The low state output from MC11E (channel 11) enables MC16C, the 10^6 "1" bit. The combined outputs from MC3E and MC3F (channels 5 and 13 respectively) produce a high level output from MC4D. Inverter MC11B effects a low level output which is coupled to NOR gate MC14C. The low level output from inverter MC11C (channel 9) combined with the low level output from MC11B produces a high level out from MC14C which is, in turn, inverted by MC14D. The low level output from MC14D is coupled to both 3-input NOR gates MC12A and MC12B. Again, since channel 10, 11 and 12 are not selected, the remaining inputs to MC12A and MC12B will also be in their low state, causing both outputs to assume a high state. The outputs from NOR gates MC14A and MC14B will, correspondingly, be low, enabling MC16B and MC16A, the 10^6 "8" and 10^5 "4" bits respectively.

The low level outputs from MC2D (Band 1A), MC2A (Band 1B) and MC2B (Band 1C) result in a high level output from 3-input NOR gate MC5B. Inverter MC11A produces a low level output to MC21D, enabling the preset pulse through inverter MC3C. Upon receipt of the preset pulse from the reset and control circuit, the high level output from MC21D forward biases transistor Q7, enabling the preset NOR gates.

The preset bits which were previously enabled through the channel select logic, will, at this time, all assume a high level output presetting the count chain, in this instance, to 9786.

The low level outputs from the channel 10 and 11 inverters at NOR gate MC8A result in a high level output. This disables the 2 ms time base signal at MC8B while enabling the 1 ms time base signal through inverter MC4A to the time base circuitry. The low level output from inverter MC3B (channel 12) is inverted by MC7D, forward biasing transistor Q4 which, in turn, grounds the MHz line to the annunciator block, illuminating the MHz units indicator.

The low level output from inverter MC11A combined with the low level output from MC3B (channel 12) produce a high level output at NOR gate MC7A, forward biasing transistor Q5. Transistor Q5 shunts the plate voltage of the right most indicator tube to ground through neon lamp DS1, "blanking" the least significant digit.

3.5.15 DAC Output

Circuit information and schematic drawings, common to the DAC and DAC logic circuitry incorporated into this instrument, are not available.

3.5.16 Power Supply (C-11-06675 and D-11-06625 Sheet 1)

All working voltages required by the instrument are derived from an ac primary power source. Each individual supply is regulated against source variations with the exception of the +230 volt dc unregulated plate supply. The rear panel ac power receptacle accepts the source voltage while providing the chassis ground termination. An RFI (Radio Frequency Interference) filter prevents any undesireable feedback from reaching the primary power source.

Power to the primary circuit of the power transformer is controlled by the front panel POWER switch S1 and protected by fuse F1 (1 Amp. MDL for 115 volt operation). The power transformer has two separate 115 volt primary windings. The windings are either placed in series (230 volt operation) or parallel (115 volt operation) by the rear panel 115/230 volt line switch.

The rear panel mounted fan is designed to operate ONLY from 115 volts and is connected across one of the primary windings. During 230 volt operation, the two primary windings act as an autotransformer, providing the required 115 volts to the fan.

The power transformer incorporates four separate secondary windings to derive to various dc power levels. The unregulated +230 volt dc indicator tube plate supply is referenced to the single secondary. Capacitor C1 filters the rectified high voltage signal from CR1 to the required +230 volt dc level. The remaining dc supplies are referenced to the regulated -12 volt supply.

Full wave bridge rectifier CR4 and CR5 and filter capacitors C4 and C5 reduce the 28.5V rms center tapped secondary voltage to approximately ±18 volts dc. Zener diode CR7, transistor Q8 and resistor R5 form a constant current source for the -12 volt supply. Zener diode CR10 maintains the base of transistor Q10 at -6.2 volts. The voltage divider comprised of resistors R12, R13 and R14 forward biases Q10, holding the junction between the collectors of Q8 and Q10 at approximately -12.6 volts. Transistor Q3 is the series regulator for the -12 volt supply. Since the base is held at -12.6 volts, the resultant base-emitter voltage drop places the emitter at -12 volts. Variable resistor R12 is the adjustment for the -12 volt supply. A change in the output voltage level will alter the base drive to Q10 through the voltage divider. Since the emitter is held constant, the drive to series regulator Q3 will be in opposition to the level change. Resistor R6 and transistor Q9 provide current limiting. If the voltage drop across R6 reaches the conduction level of the base-emitter junction of transistor Q9, the transistor will conduct, reducing the base drive to series regulator Q3.

The +12 volt supply is derived from the +18 volt dc potential and is referenced to the -12 volt supply. Transistors Q11 and Q14 are a differential pair. Q11 is referenced to ground while Q14 is referenced to the voltage divider (R27-R28) between the -12 volt supply and the +12 volt supply output. A change at the base of Q14 will be reflected by the collector current through Q11 varying the base drive to transistor Q12. Q12, in turn, controls the base drive to series regulator Q2, offsetting any level change. Transistor Q13 and resistor R26 are the current limiting components.

The +3.6 volt supply is current regulated. Zener diode CR8 establishes the base drive to transistor Q7 which, in turn, controls the base drive to transistor Q1, the series regulator. If the output voltage level were to increase, the base drive to Q7 would decrease. This, in turn, would decrease the base drive to Q1, decreasing the current to the load and, therefore, the output voltage level. Transistors Q5,

Q6 and resistor R3 are the current limiting components for the +3.6 volt supply.

The +4.5 volt supply is referenced to the +3.6 volt supply. Zener diode CR12 forward biases constant current source Q18. The collector is maintained at +4.5 volts by diode CR11.

The -5.2 volt supply is also current regulated and is referenced to the +12 volt supply. The voltage divider of R7 and R8 determines the base drive to transistor Q17 which in turn controls the base drive to series regulator Q4. A change in the output level will cause a subsequent change in the base drive to Q17 and, in turn, to Q4, maintaining the voltage at -5.2 volts by varying the current. Transistors Q15, Q16 and resistor R11 are the current limiting components.

SECTION 4

MAINTENANCE - CALIBRATION

4.1 INTRODUCTION

Section 4 presents pertinent information to aid in maintaining the factory-new performance of the FRO-212-1 Frequency Counter. Routine maintenance, calibration and repair procedures are included with part location drawings, schematic diagrams and integrated circuit equivalents complementing the various procedures. Table 4-1 offers a list of suggested test equipment required for instrument calibration and repair (equivalent equipment acceptable).

TABLE 4-1

RECOMMENDED TEST EQUIPMENT

INSTRUMENT DESCRIPTION	MANUFACTURER AND MODEL	MINIMUM REQUIREMENTS
Digital Volt Meter	Eldorado Model 1810	0.1% accuracy
Oscilloscope	Textronix Series 580	80 MHz bandwidth
LF Signal Generator	HP202C	Combined range from 1 kHz to 3 GHz
HF Signal Generator	HP606A	
VHF Signal Generator	HP608C	
UHF Signal Generator	HP612A	
UHF Signal Generator	HP614A	
UHF Signal Generator	HP616B	
Frequency Standard	Any	10 times internal oscillator accuracy.

4.2 PERIODIC MAINTENANCE

Periodic maintenance for the FRO-212-1 Frequency Counter is limited to only routine cleaning of the instrument and air filter. Under normal operating conditions, 90 day maintenance intervals are suggested. Table 4-2 outlines the periodic maintenance procedure.

TABLE 4-2

PERIODIC MAINTENANCE

STEP	ACTION
1	Place the POWER switch to the OFF position and remove the power cord.
2	Remove the two phillips head screws securing the filter bracket to the rear panel.
3	Cleanse the mesh filter element in a mild household detergent solution, rinse thoroughly and dry. Spray the filter element with a commercial type filter coating (RP filter coat or equivalent).
4	Remove the top and bottom cover panels by extracting the 30 #4 phillips head screws securing each panel to the chassis.
5	Clean the interior of the instrument if necessary, with CLEAN, DRY compressed air. Prior to replacing the cover panels, check the physical integrity of the plug-in P.C. boards and coaxial connectors. Replace ALL cover panel screws as they are necessary to maintain the effectiveness of the RFI shielding.
6	Replace the filter element and bracket. The exterior of the instrument may be cleaned with an equal part solution of denatured alcohol and water - stronger solvents may damage the finish or polaroid lens.

4.3 CALIBRATION

Periodic adjustment of the internal oscillator is the only normal calibration requirement for the FRO-212-1. The remaining internal adjustments, originally set at the factory, are not subject to periodic calibration.

The output frequency of the oscillator may be adjusted relative to a 1 MHz frequency standard by observing the rotation rate of a Lissajous pattern as depicted by the test

configuration in Figure 4-1. For optimum counter operation, the oscillator should be calibrated after 30 days of operation and at 90 day intervals thereafter. As oscillator aging is greatest when it is first placed in operation, instrument power should be maintained whenever possible. Table 4-3 outlines the calibration procedure for the internal oscillator.

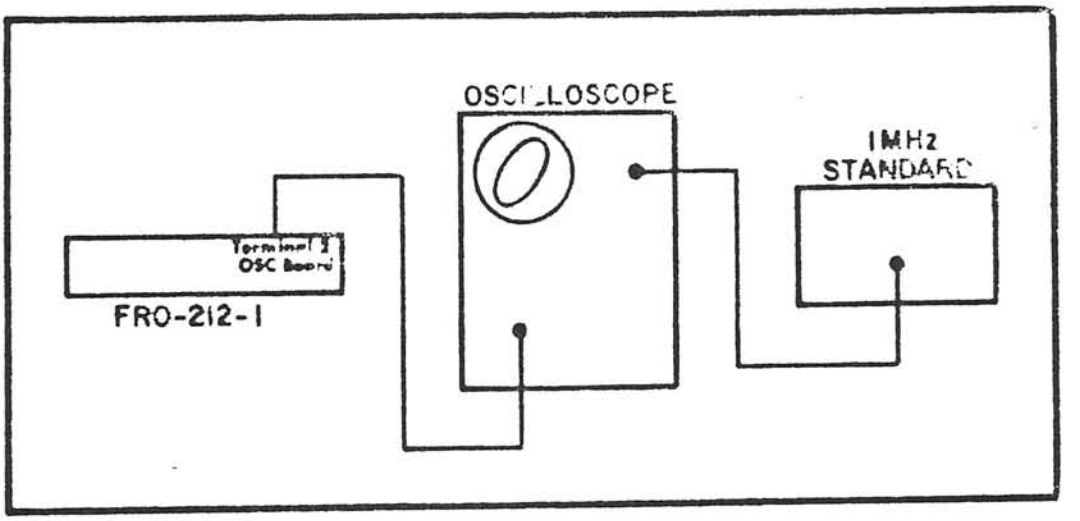


FIGURE 4-1

OSCILLATOR TEST CONFIGURATION

TABLE 4-3

OSCILLATOR CALIBRATION

STEP	ACTION
1	Remove the top cover panel by extracting the 30 #4 phillips head screws securing the cover to the chassis.
2	Apply instrument power and allow a minimum of 30 minutes continuous operation for oscillator stabilization.
3	Connect the oscilloscope's vertical input to terminal 2 on the Oscillator P.C. board (refer to Figures 4-2 and 4-3).
4	Connect the 1 MHz frequency standard to the oscilloscope's horizontal input and set the horizontal input switch to external.

TABLE 4-3 (Continued)

STEP	ACTION
5	Adjust the oscilloscope for a Lissajous pattern of convenient amplitude.
6	While observing the oscilloscope, adjust variable capacitor C1 on the Oscillator P.C. board for minimum rotation.
7	Without removing the oscilloscope's probe, replace the top cover panel and secure it in place with two or three screws. Avoid any undue pressure on the probe.
8	Observe the pattern for five minutes noting Lissajous rotation rate. If the rotation rate increases, remove the top cover panel and readjust capacitor C1 for minimum rotation. Again replace the cover panel and observe the rotation rate for five minutes. Continue to monitor and adjust the oscillator until minimum rotation is realized. The cover panel must be in place as it affects both capacitance and internal temperature.
9	Remove the cover panel and probe, then replace the cover panel using all 30 screws. Note the date for the next required calibration.

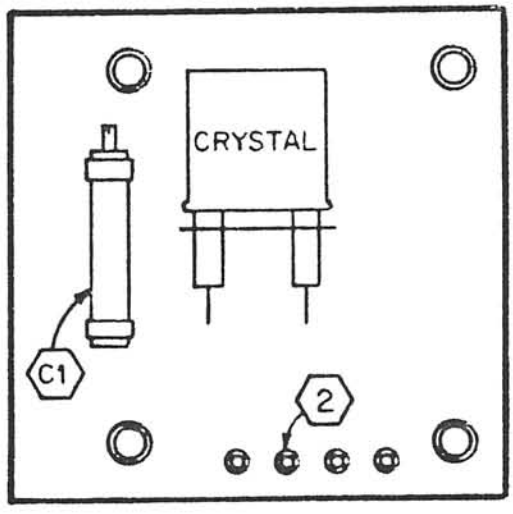
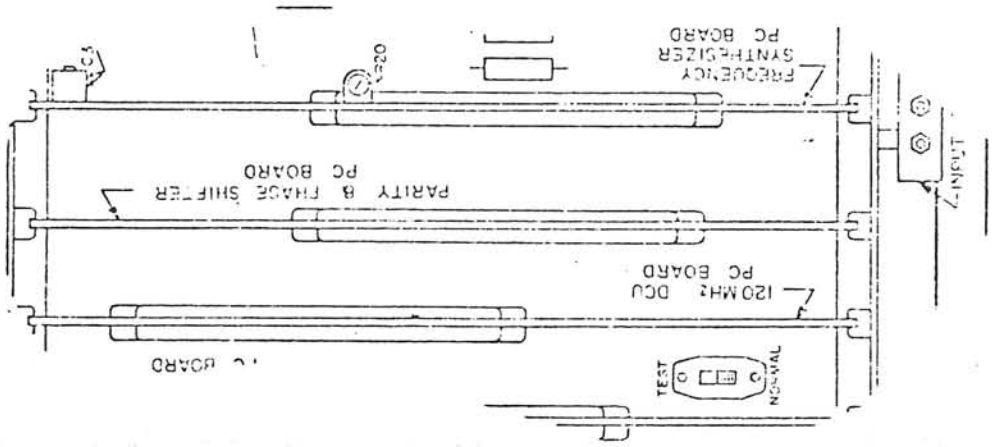


FIGURE 4-2

OSCILLATOR COMPONENT LOCATION

ADDENDUM
(FRC-212-1)

Figure 4-3, P.C. BOARD LOCATION on page 4-5 is in error. Parity and Phase Shift P.C. Board, and 120 MHz DCU PC Board are shown in reversed mounting order. Make "pen & ink" change indicating proper position.



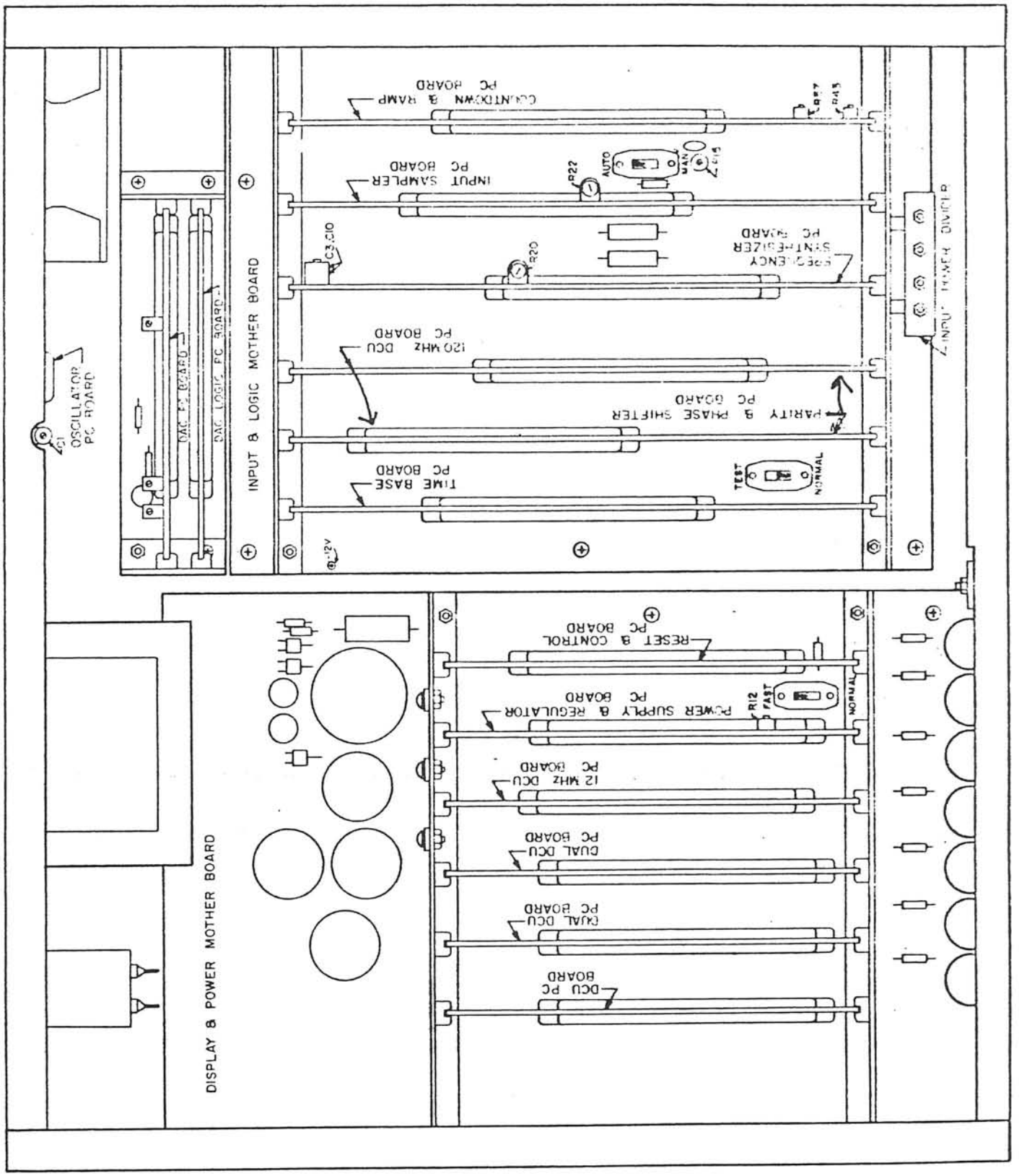


FIGURE 4-3

P.C. BOARD LOCATION

4.4 INTERNAL ADJUSTMENTS

With the exception of the oscillator, the internal calibration adjustments require no periodic compensation. Calibration of these "semi-fixed" adjustments is necessitated only if a component is replaced or if a decrease in performance specifications is apparent.

4.4.1 Power Supply Adjustment

The -12 volt dc supply is the reference for the remaining regulated supplies and incorporates the only power supply adjustment. Table 4-4 outlines the power supply calibration procedure.

TABLE 4-4

POWER SUPPLY CALIBRATION

STEP	ACTION
1	Place the POWER switch to the OFF position and remove the top cover panel by extracting the thirty 44 phillips head screws.
2	Remove the Power Supply and Regulator P.C. board (refer to Figure 4-3). Insert the extender board into the vacant connector and insert the Power Supply and Regulator P.C. board into the extender board's connector.
3	Place the POWER switch to the ON position and note that the indicator tubes illuminate.
4	Connect the DVM to chassis ground and to the -12 volt supply at terminal 3 on the Input and Logic Mother board (refer to Figure 4-3).
5	Adjust variable resistor R12 on the Power Supply and Regulator P.C. board for -12 volts ±100 mV (refer to Figure 4-4).
6	Place the POWER switch to the OFF position and remove the Power Supply and Regulator P.C. board taking care as to not disturb the calibration setting.

TABLE 4-4 (Continued)

STEP	ACTION
7	Remove the extender board and replace the Power Supply and Regulator P.C. board into its connector.

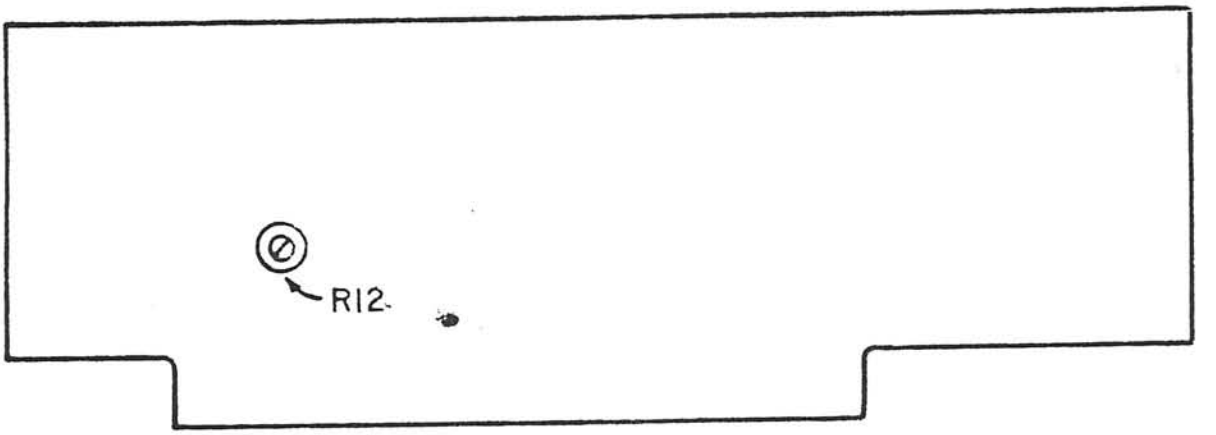


FIGURE 4-4

POWER SUPPLY ADJUSTMENT

4.4.2 Countdown Bias Adjustment

The bias current to the mid and high band tunnel diode multivibrators determines their overall range of operation. Variable resistors R43 and R57 are set for ranges of 8.75 to 9.75 MHz (mid band) and 32 to 36 MHz (high band) respectively. Table 4-5 outlines the procedure for adjusting the countdown bias current.

TABLE 4-5

COUNTDOWN BIAS ADJUSTMENT

STEP	ACTION
1	Place the POWER switch to the OFF position.
2	Remove the Countdown and Ramp P.C. board and install the extender board in the vacant connector. Insert the Countdown and Ramp P.C. board into the extender board's connector.

TABLE 4-5 (Continued)

STEP	ACTION
3	Place the TEST/NORMAL switch to the TEST position and the AUTO/MAN switch to the MAN position (refer to Figure 4-3).
4	Place the POWER switch to the ON position and place the left hand CHANNEL SELECT switch to Channel 1B (mid band).
5	The numerical indicator tubes will display the mid band multivibrator's frequency (disreguard the decimal point location).
6	Rotate variable resistor R15 on the Input and Logic Mother board (Figure 4-3) to the extreme counterclockwise position. The display should exceed 9.75 MHz. If it does not, adjust variable resistor R43 (Refer to Figure 4-5) until a reading of 9.75 MHz is reached. Rotate variable resistor R15 to the extreme clockwise position and check for a reading of approximately 8.75 MHz. Readjust variable resistor R43 as necessary to provide an overall range of 8.75 to 9.75 MHz.
7	Place the CHANNEL SELECT switch to the 1C position (high band).
8	Again rotate variable resistor R15 to the extreme counterclockwise position. The reading should exceed 36 MHz. If unattainable, adjust variable resistor R57 (refer to Figure 4-5) until a reading of 36 MHz is reached. Rotate variable resistor R15 fully clockwise. The reading should be less than 33 MHz. Readjust variable resistor R57 as necessary to provide an overall range of 32 to 36 MHz.
9	Place the POWER switch to the OFF position and remove the extender board.
10	Replace the Countdown P.C. board and place the TEST/NORMAL switch to the NORMAL position and the AUTO/MAN switch to the AUTO position.

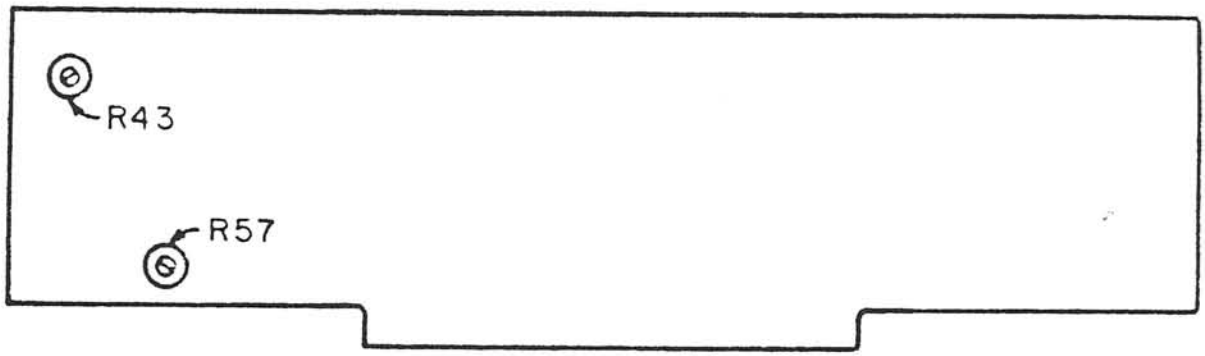


FIGURE 4-5

COUNTDOWN BIAS ADJUSTMENTS

4.4.3 Frequency Synthesizer Balance Adjustment

The 90° phase shifter networks for the frequency synthesizer's balanced modulators incorporate two trimmer capacitors to attain the required fine phase separation. Table 4-6 outlines the adjustment procedure.

TABLE 4-6

FREQUENCY SYNTHESIZER BALANCE ADJUSTMENTS

STEP	ACTION
1	Place the POWER switch to the OFF position and remove the Frequency Synthesizer P.C. board.
2	Install the extender board and mount the Frequency Synthesizer P.C. board on the extender board. Do not remove the shield assembly.
3	Place the POWER switch to the ON position.
4	Place the AUTO/MAN switch to the MAN position and rotate variable resistor R15 fully counterclockwise (Refer to Figure 4-3).

TABLE 4-6 (Continued)

STEP	ACTION
5	Trigger the oscilloscope with the 5 kHz (Δf) square wave at the test point terminal on the circuit side of the Parity and Phase Shifter P.C. board (refer to Figure 4-6). Set the oscilloscope's time base to 50 μs and amplitude to 0.05V/cm.
6	Place the left hand CHANNEL SELECT switch to the 1C position (high band).
7	Connect the oscilloscope's vertical input to the base of transistor Q12 (refer to Figure 4-7). Use a times ten probe.
8	The signal displayed will be a high frequency sinewave with some degree of modulation with the 5 kHz Δf signal.
9	Alternately adjust variable capacitor C10 and variable resistor R20 for minimum modulation. Figures 4-8A and 4-8B depict improper and ideal waveforms respectively. Use a non-metallic alignment tool taking care to remove both tool and hand from the immediate vicinity of the adjustments when observing the output waveform.
10	Place the left hand CHANNEL SELECT switch to 1B (mid band). Remove the probe from the base of transistor Q12 and connect it to the base of transistor Q10.
11	Adjust variable capacitor C10 for minimum modulation as described in step 9. Do not readjust the setting of variable resistor R20.
12	Place the POWER switch to the OFF position. Remove the extender board and replace the Frequency Synthesizer P.C. board into its connector and return the AUTO/MAN switch to the AUTO position.

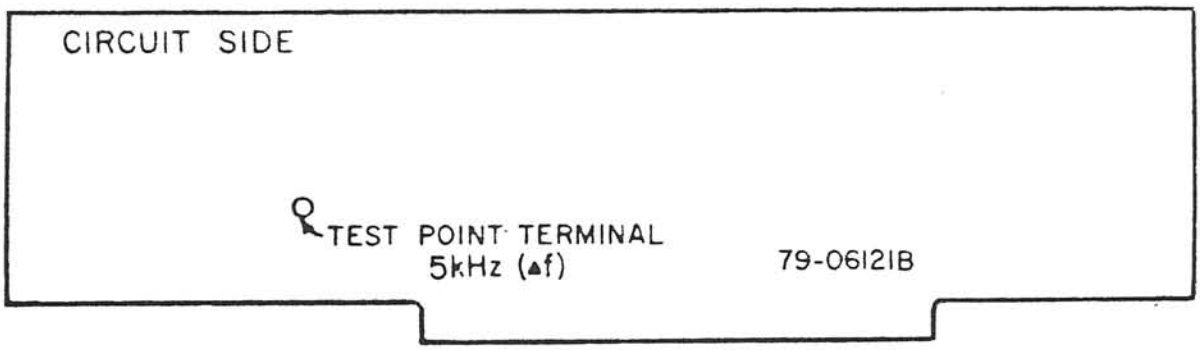


FIGURE 4-6
PARITY TEST POINT LOCATION

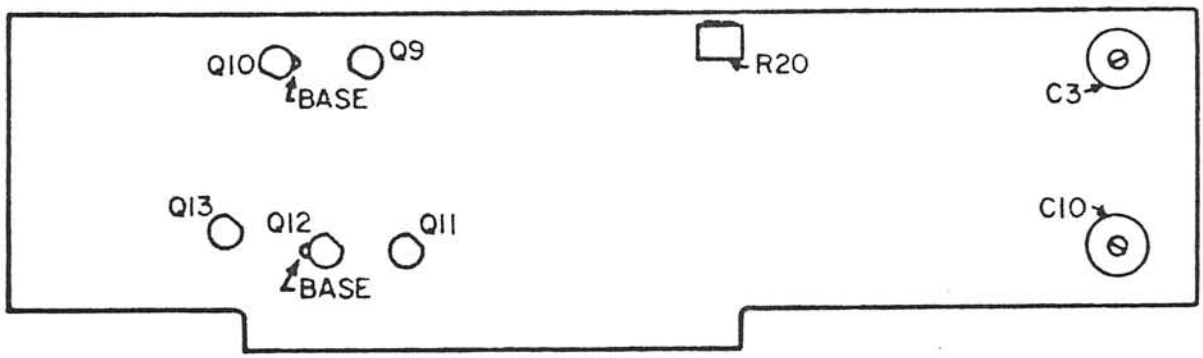


FIGURE 4-7
FREQUENCY SYNTHESIZER ADJUSTMENT LOCATION

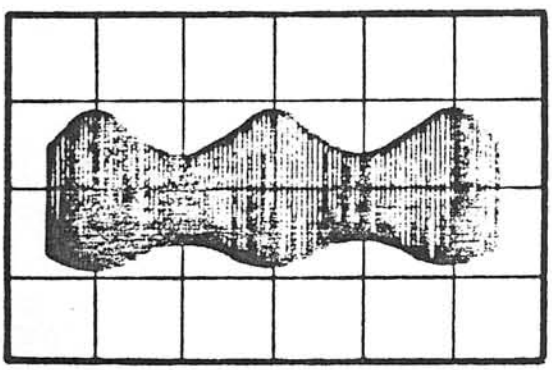


FIGURE 4-8A
IMPROPER WAVEFORM

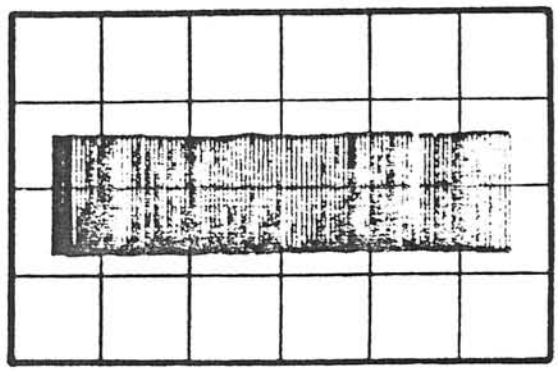


FIGURE 4-8B
IDEAL WAVEFORM

4.4.4 Sampler Bias Adjustment

The sampler bias adjustment determines the shape of the sampling pulse. This pulse, however, is not observable directly. The procedure outlined in Table 4-7 explains how the sampler is adjusted for best performance.

TABLE 4-7
INPUT SAMPLER BIAS ADJUSTMENT

STEP	ACTION
1	Place the POWER switch to the ON position.
2	Apply an input signal of approximately 3 GHz to the INPUT connector.
3	Set the input amplitude to provide a consistant reading.
4	Gradually decrease the input amplitude. Adjust variable resistor R22 for maximum sensitivity (refer to Figure 4-9).
5	Continue to decrease the input amplitude while adjusting R22 until maximum sensitivity is realized.
6	This completes the internal adjustments, place the POWER switch to the OFF position and replace the top cover panel using all thirty phillips head screws.

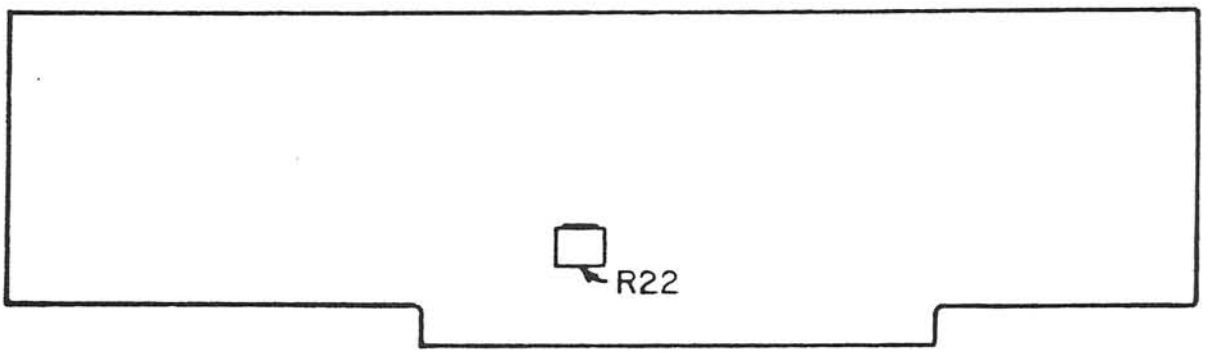


FIGURE 4-9
INPUT SAMPLER ADJUSTMENT LOCATION

4.5 TROUBLESHOOTING

This section furnishes basic information necessary to determine the nature and location of an instrument failure.

Troubleshooting of the instrument is accomplished at three increasingly detailed levels. The first level in servicing an instrument that has failed is to "sectionalize" the fault to a sub-assembly. Once traced to a particular sub-assembly, the second level or "localization" of the failure is undertaken to confine the fault to an individual stage or circuit within the sub-assembly. The third level or "isolation" involves the actual location of the defective component within the stage or circuit that has failed.

In the event of a suspected failure and before any troubleshooting or repairs are attempted:

1. Insure that the applied input is of sufficient amplitude and within the specified frequency range.

2. Verify proper positioning of all operating controls.

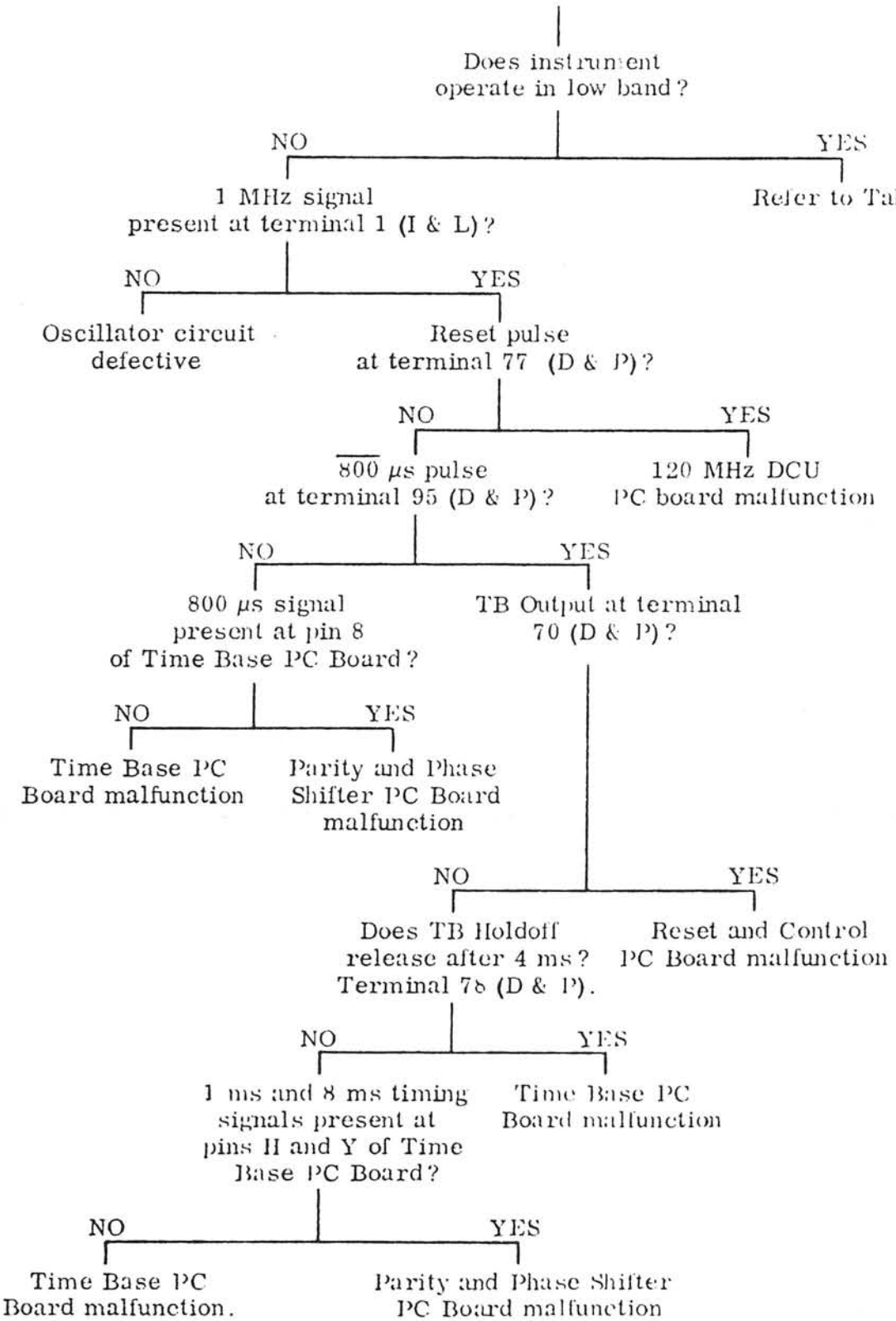
If a valid malfunction is encountered, first insure that all dc power levels are present and correct before attempting to sectionalize the malfunction.

4.5.1 Sectionalization

Sectionalization is based on performance checks and waveforms. Tables 4-8, 4-9 and 4-10 outline procedures for sectionalizing faults to the individual PC boards. The tables are sequenced and should be followed in their logical order. Figure 4-10 depicts the normal waveforms encountered during low band (CHANNEL 1A) operating while Figure 4-11 presents waveforms common to the mid and high bands (CHANNEL 1B and 1C).

TABLE 4-8

LOW BAND SECTIONALIZATION



I & L = Input and Logic Mother Board terminal location.
D & P = Display and Power Supply Mother Board terminal location.

TABLE 4-9

MID BAND SECTIONALIZATION

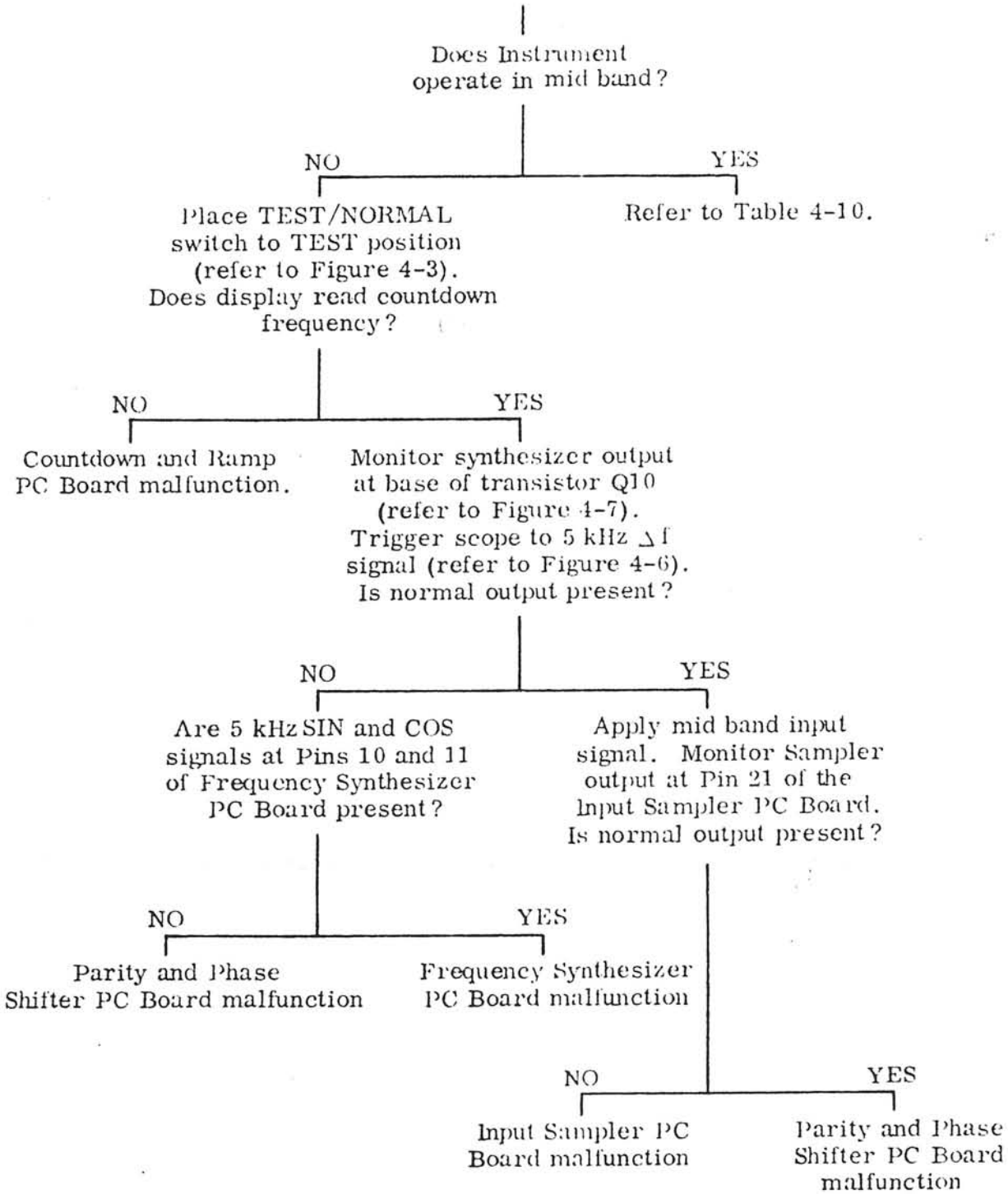
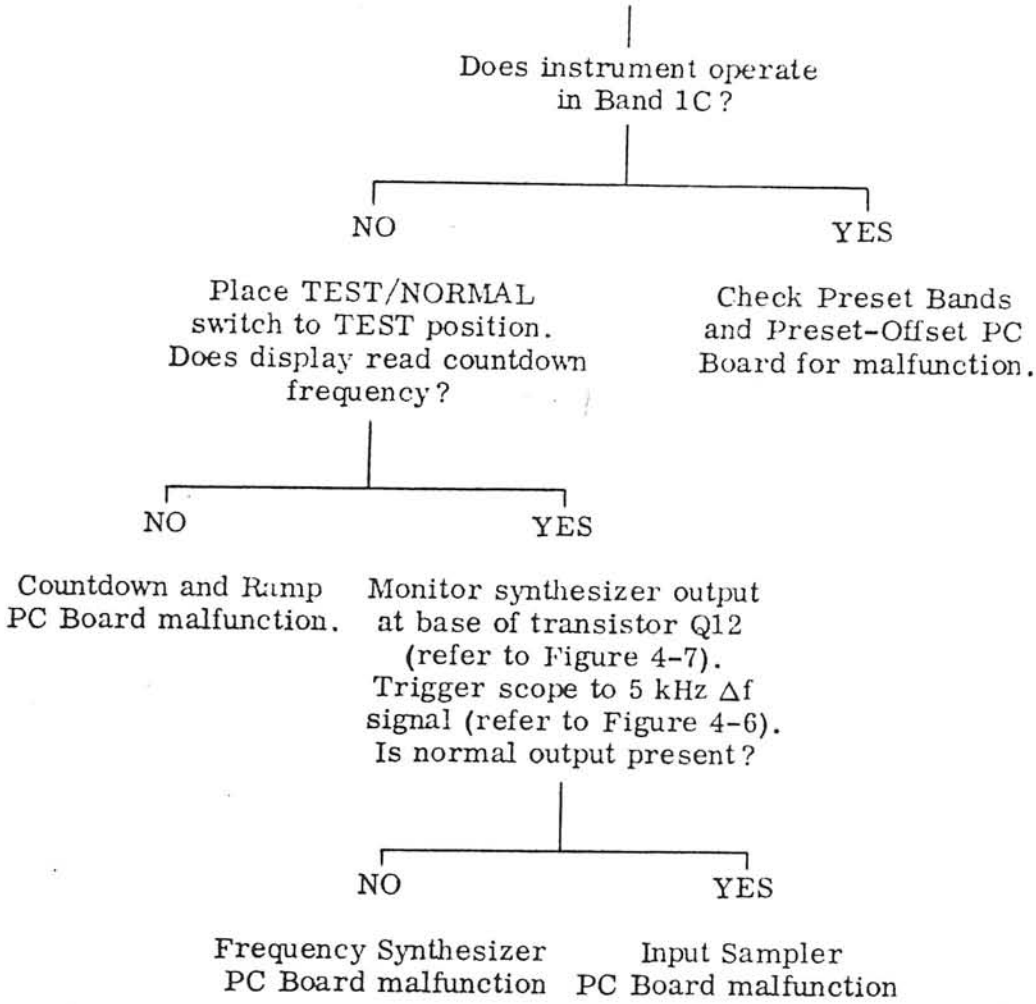


TABLE 4-10

HIGH BAND SECTIONALIZATION



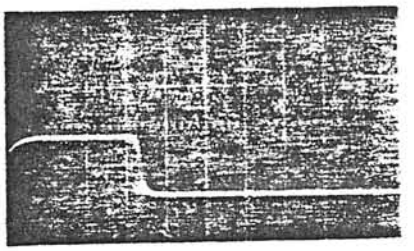


FIGURE 4-10A
RESET
(terminal 77)
10 μs/cm - 1V/cm

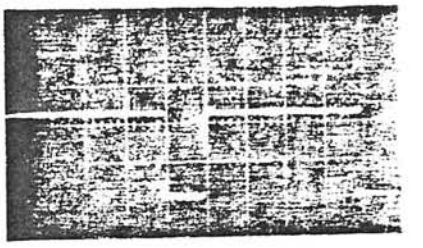


FIGURE 4-10B
800 μs
(terminal 95)
0.2 ms/cm - 1V/cm

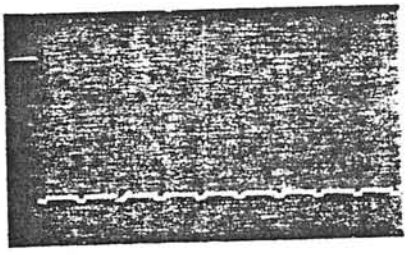


FIGURE 4-10C
TIME BASE OUTPUT
(terminal 70)
10 μs/cm - 0.5V/cm

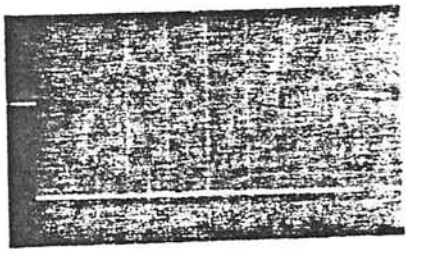


FIGURE 4-10D
TIME BASE HOLDOFF
(terminal 78)
5 ms/cm - 0.5V/cm

FIGURE 4-10

LOW BAND WAVEFORMS

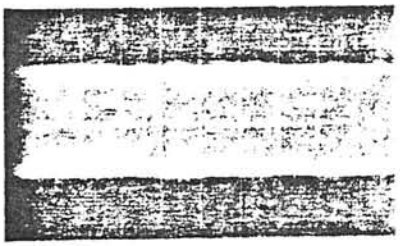


FIGURE 4-11A
NORMAL SYNTHESIZER OUTPUT
(Base of Q12, Band 1C)
50 μs/cm - 0.5 V/cm

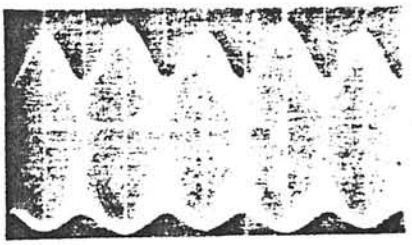


FIGURE 4-11B
MISALIGNED SYNTHESIZER OUTPUT
(Base of Q10, Band 1B)
50 μs/cm - 0.5 V/cm

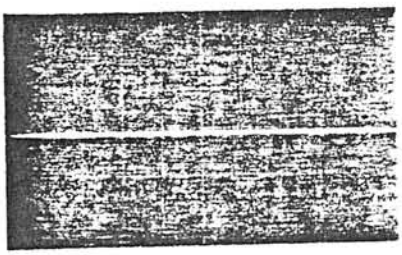


FIGURE 4-11C
SAMPLER OUTPUT
(Pin 21, Input Sampler PC Board)
20 μs/cm - 1V/cm
Input: Band 1B, 200 MHz, -15 dBm

FIGURE 4-11D
RAMP
(Pin C, Countdown and Ramp PC Board)
10 ms/cm - 1 V/cm

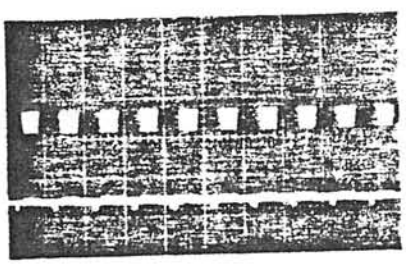


FIGURE 4-11E
SUCCESSIVE BURSTS OF N
(MC1, Pin 9 of Parity and Phase Shifter PC Board)
1 ms/cm - 0.5 V/cm
Input: Band 1B, 200 MHz, -15 dBm

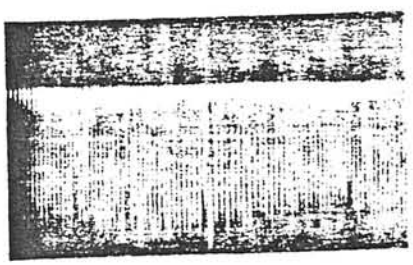


FIGURE 4-11F
SAMPLER
(Collector, Q7, Input Sampler) PC Board)
20 μs/cm - 1 V/cm
Input: 3 GHz, -7 dBm

FIGURE 4-11
SAMPLING WAVEFORMS

4.5.2 Localization

Localization of a malfunction can be accomplished by checking various signals and levels throughout the defective P.C. assembly. For increased accessibility, the assembly in question should be mounted on an extender board whenever possible. A thorough comprehension of the theory of operation (Section 3) combined with the individual schematics normally provides sufficient information to confine the malfunction to individual circuits within the assemblies.

4.5.3 Isolation

Isolation of the malfunction can normally be accomplished with routine voltage and resistance measurements. Integrated circuit equivalents are included within this section to facilitate their testing. Whenever a component or P.C. assembly is replaced, instrument calibration should be checked and recalibrated as necessary (refer to Sections 4-3 and 4-4).

4.6 REPAIR TECHNIQUES

Repair of the instrument should be undertaken only by qualified personnel adept in solid state repair techniques. When a component failure is encountered, observe these general instructions:

1. Never remove or replace a component or P.C. board while instrument power is enabled.

2. Use only a grounded, transformer-coupled, thermostatically controlled soldering iron.

3. Avoid any application of acid-core type solder.

4.6.1 Cover Removal

As most of the components are mounted on removable P.C. boards, it is normally only necessary to remove the top cover panel for immediate access. This involves extracting the thirty #4 phillips head screws which secure the cover panel to the frame. Access to the Preset-Offset P.C. board necessitates the removal of the bottom cover panel which is similarly secured in place with thirty #4 phillips head screws. When installing either of the cover panels, all thirty screws must be in place to maintain the effectiveness of the RFI shielding.

4.6.2 Preset-Offset P.C. Board Removal

Access to the circuit side of the Preset-Offset P.C. Board or to the portion of the Display and Power Supply Mother Board beneath the Preset-Offset P.C. Board entails the removal of the four phillips head screws securing the assembly to the chassis and the single phillips head screw at the center of the Preset-Offset assembly. Once the screws have been removed, the P.C. assembly can be pivoted along the center axis eliminating any need for jumper removal.

4.6.3 Power Transistor Replacement

In the event that any of the plastic power transistors fail, proceed as follows:

1. With the aid of a pneumatic solder extractor, carefully remove the solder from each lead of the defective transistor. Failure of transistor Q2, Q3 or Q4 will necessitate the removal of the Preset-Offset P.C. Board as outlined in Section 4.6.2.

2. Remove the hardware securing the transistor to its mounting. If transistor Q3 has failed, it will be necessary to first remove capacitor C2 from the Display and Power Supply Mother Board. Observe proper polarity when replacing the capacitor.

3. Coat both sides of the mica insulating washer with a heat conductive grease (Dow Corning compound 107 or equivalent).

4. Align the mica washer with the hole in the transistor mounting plate and install the replacement transistor with the exposed metallic portion towards the mica washer. Secure the transistor in place with the existing hardware.

5. Solder the transistor in place and trim the leads as warranted.

4.6.4 Integrated Circuit Replacement

The following instructions outline the proper method for the removal and replacement of a defective integrated circuit.

1. Verify that the integrated circuit in question is, in deed, defective (refer to the integrated circuit equivalent diagrams contained in Section 4.7).

2. At the component side of the P.C. board, carefully clip each lead of the defective integrated circuit at the point where the lead enters the plastic case.

3. Carefully remove each individual lead from the component side of the P.C. board with the aid of a soldering iron and long nose pliers.

4. Remove all excess solder with a pneumatic solder extractor.

5. Install the replacement integrated circuit noting correct orientation as depicted by the respective component location illustration.

6. Solder each lead on the circuit side and all top traces on the component side of the P.C. Board.

4.7 INTEGRATED CIRCUIT EQUIVALENTS

Circuit equivalents for each type of integrated circuit are described in numerical sequence within this section. If further information is required, refer to the manufacturer's description.

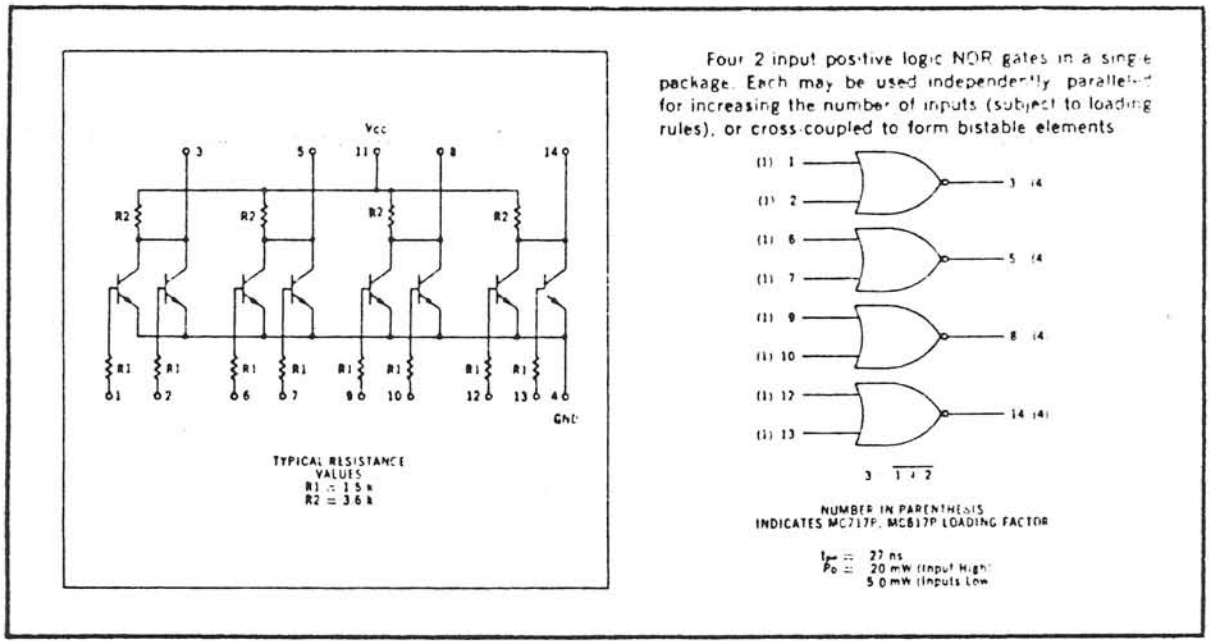


FIGURE 4-12

MC817P EQUIVALENT

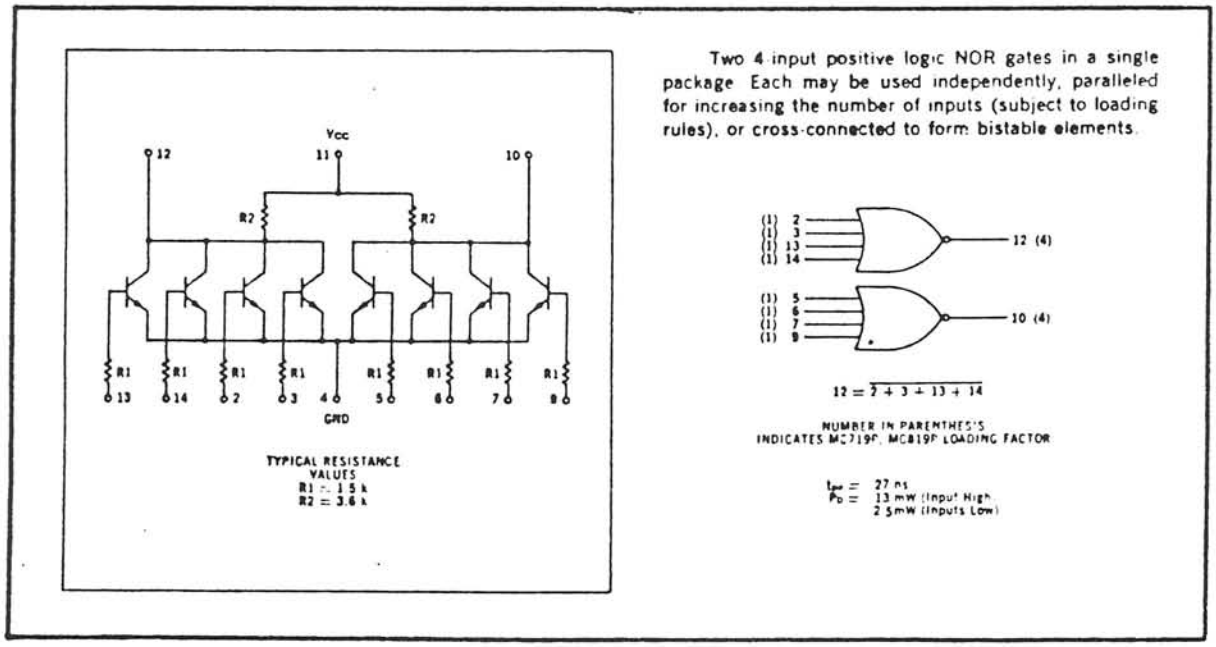


FIGURE 4-13

MC819P EQUIVALENT

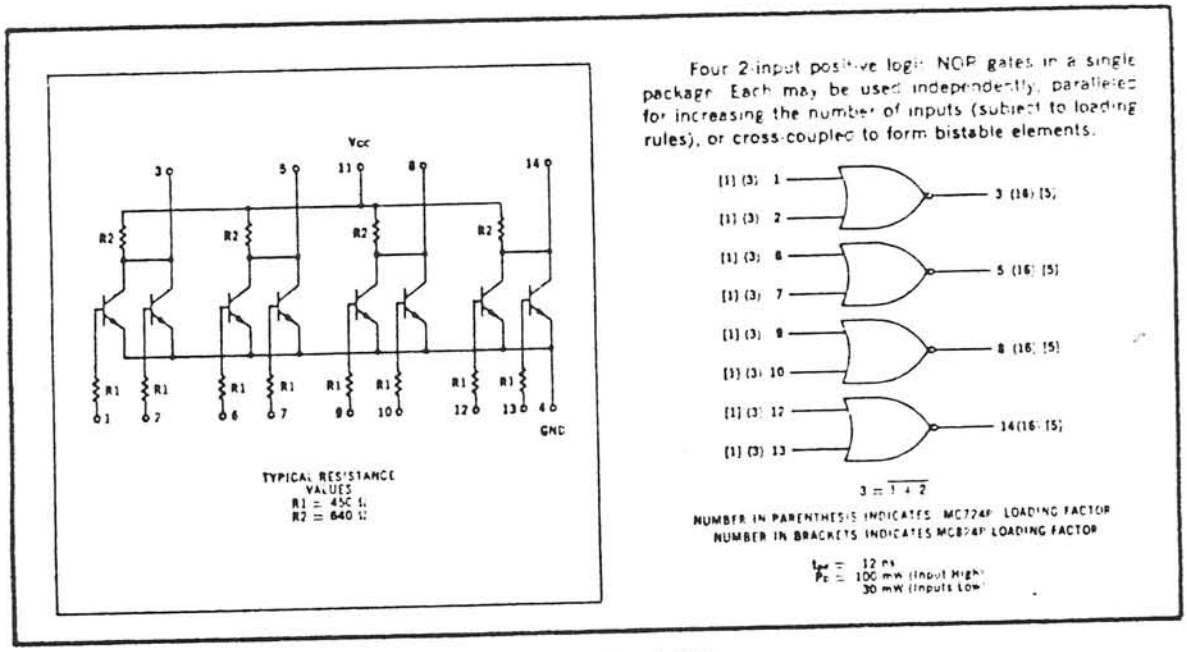


FIGURE 4-14

MC824P EQUIVALENT

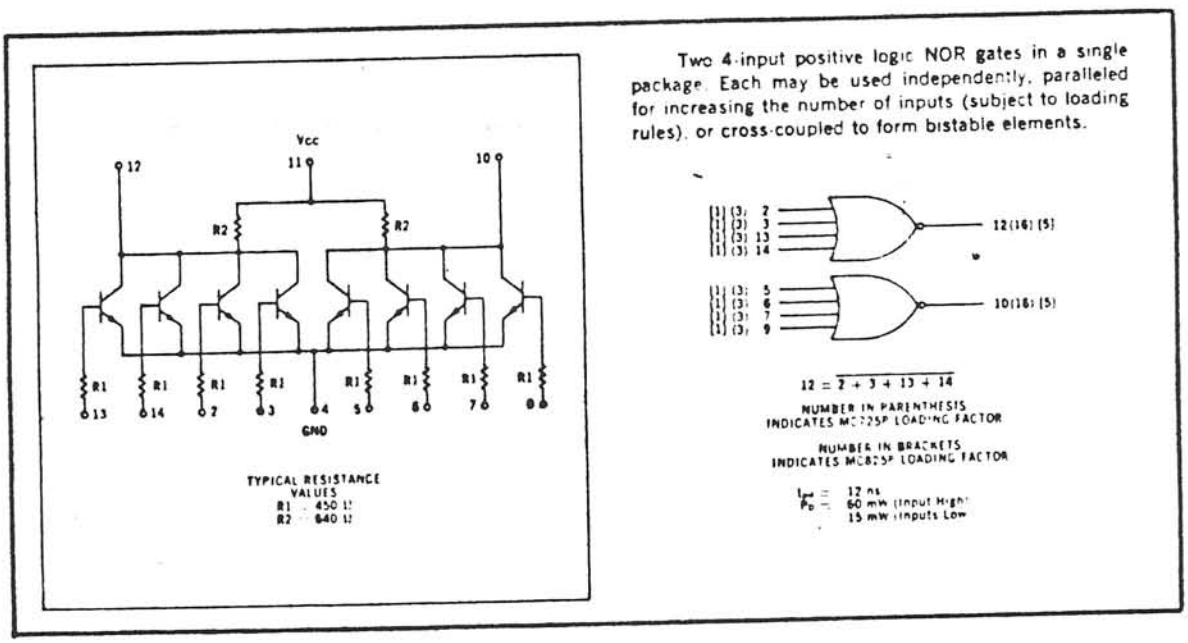


FIGURE 4-15

MC825P EQUIVALENT

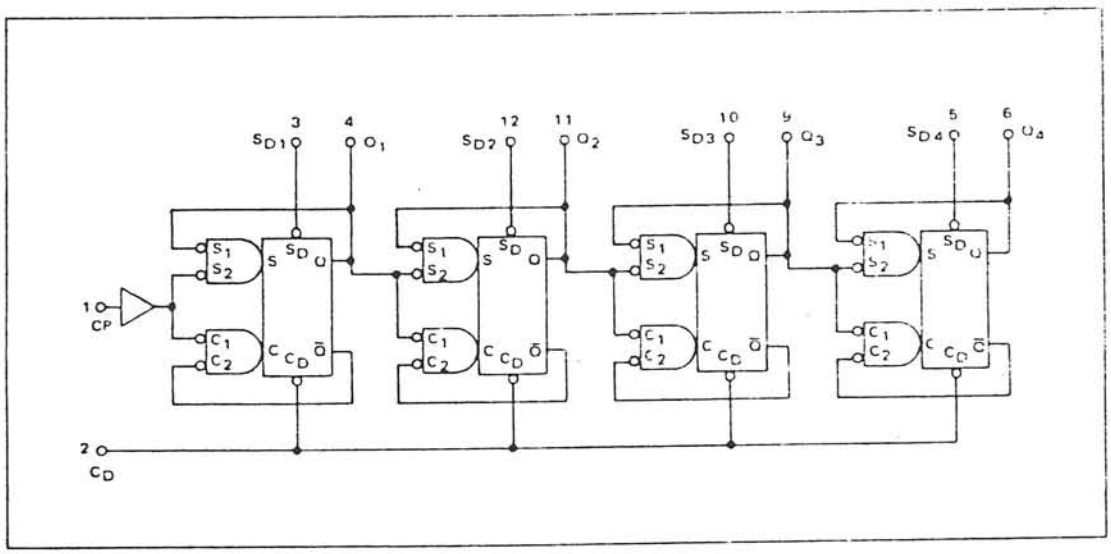
This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 binary code with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin is 1.0 volt.

Input Loading Factor
S_D 1.5
C_D 5
CP 1

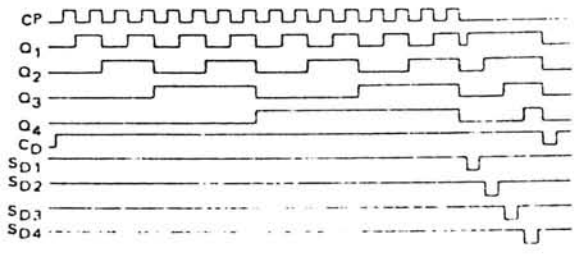
Output Loading Factor 8

Total Power Dissipation 150 mW typ pkg

Maximum Count ng Frequency 30 MHz typ



COUNTER SEQUENCE



DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
3	Q_1	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
5	Q_1	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
6	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
7	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
8	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
9	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
10	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	Q_4
11	Q_1	Q_2	$\bar{Q}_3$	Q_4
12	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	Q_4
13	Q_1	$\bar{Q}_2$	Q_3	Q_4
14	$\bar{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

FIGURE 4-16

MC839P EQUIVALENT

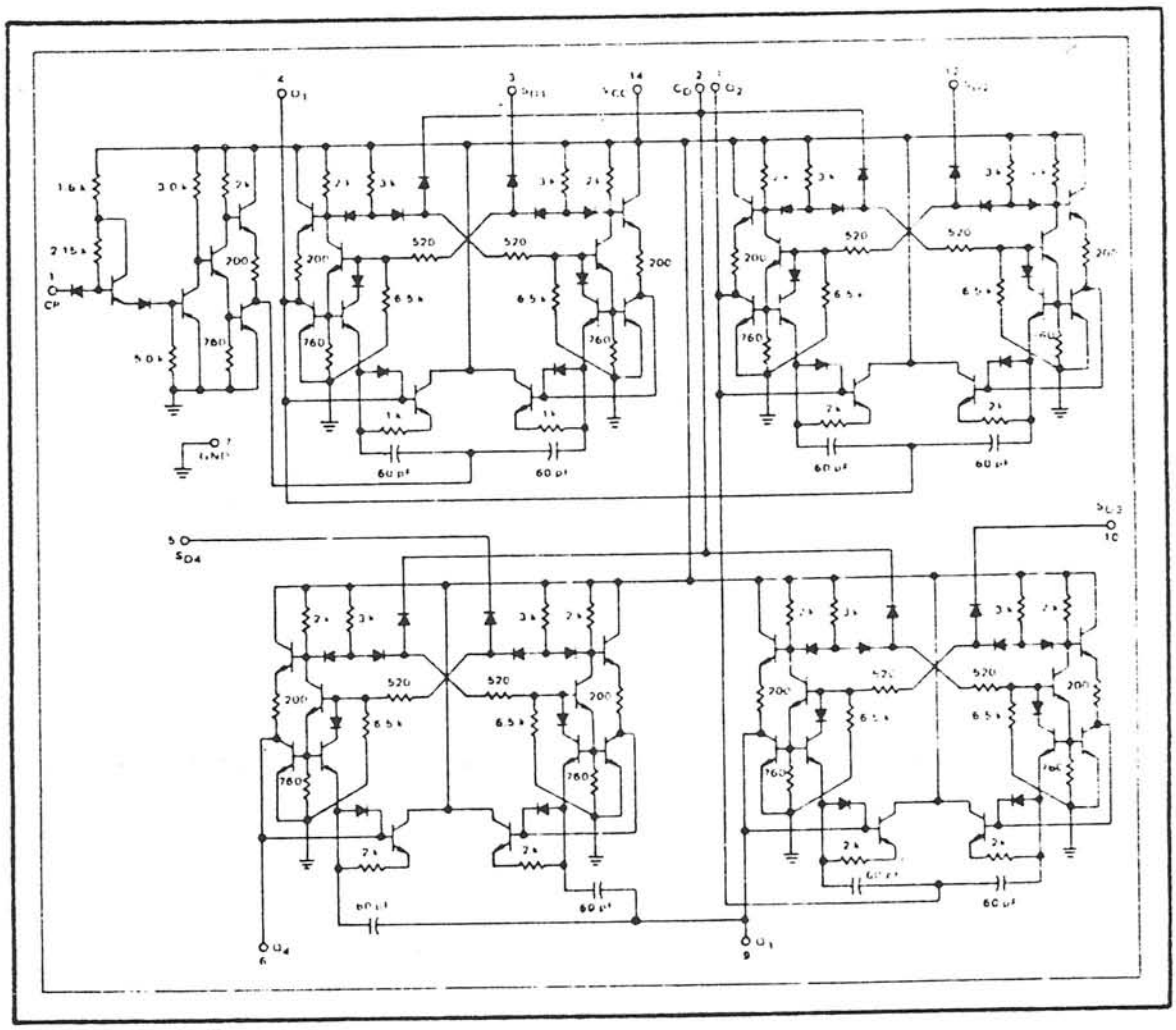
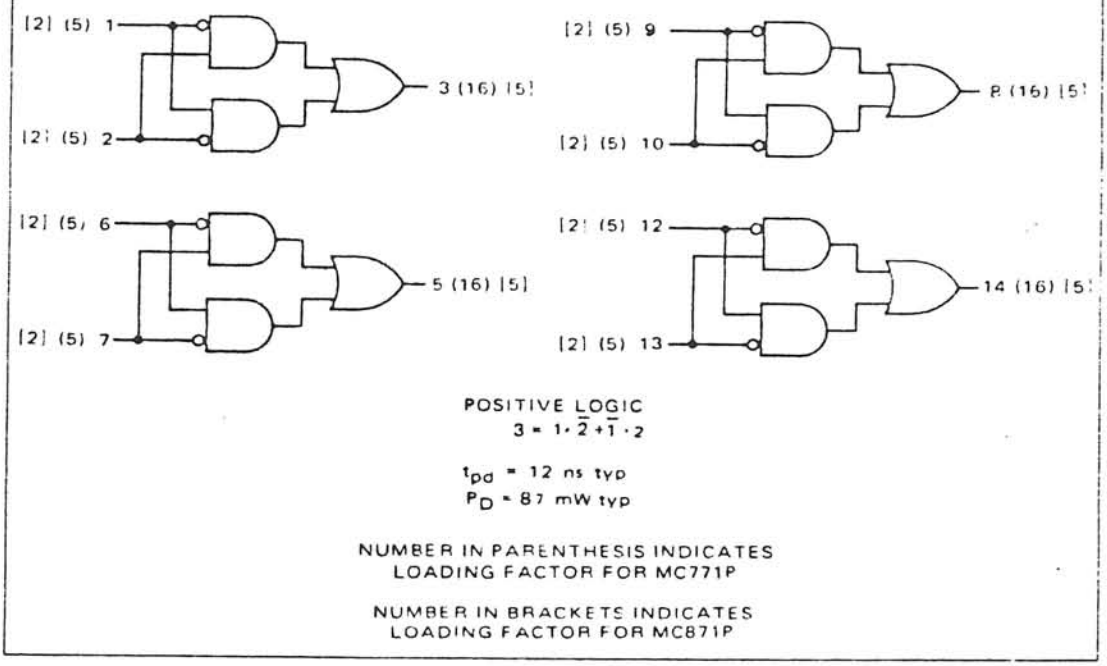


FIGURE 4-17

MC839P SCHEMATIC

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.

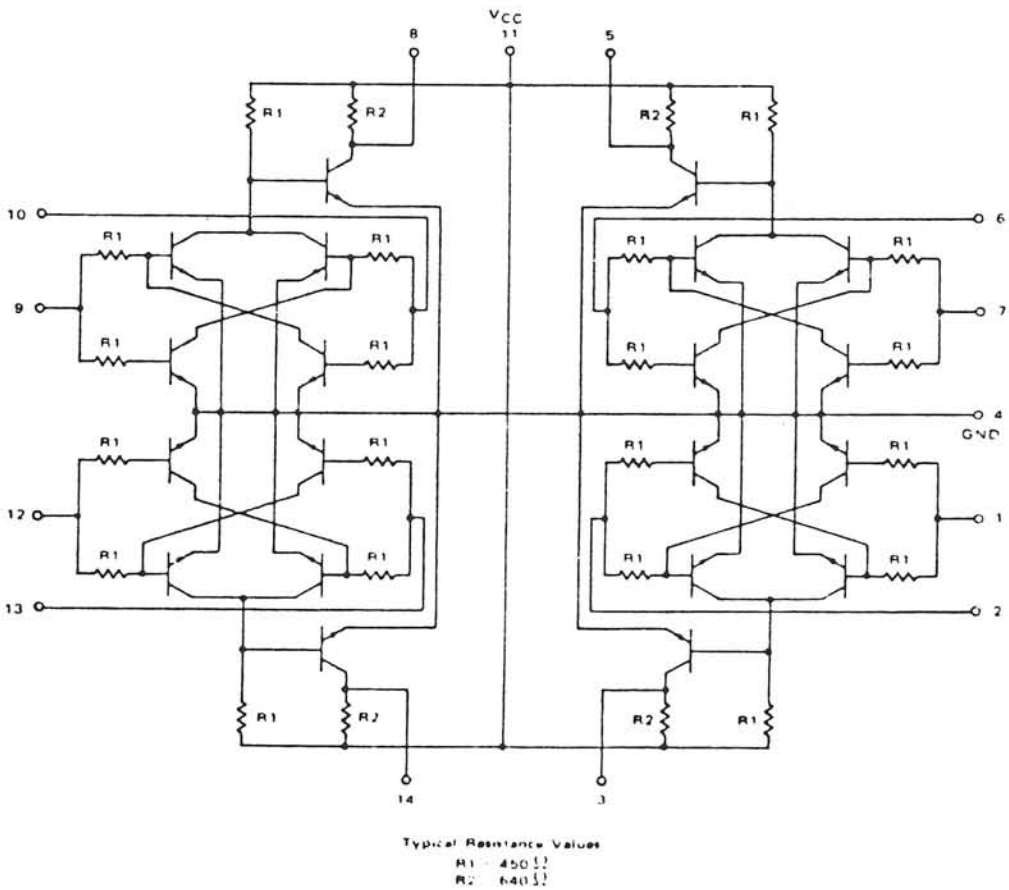


POSITIVE LOGIC
$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns typ
P_D = 87 mW typ

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC771P

NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC871P



Typical Resistance Values
R1 = 450 Ω
R2 = 640 Ω

FIGURE 4-18

MC871P EQUIVALENT

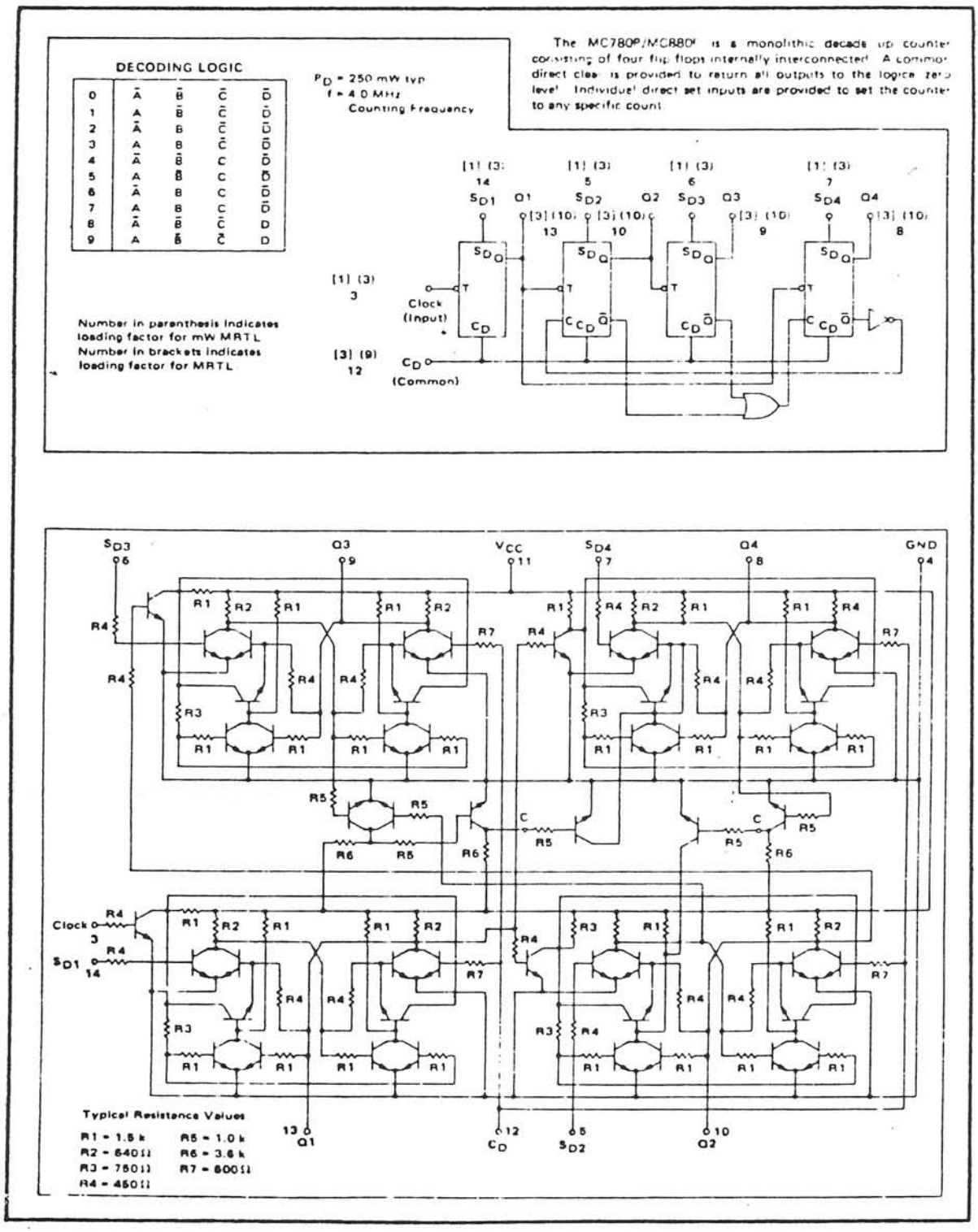
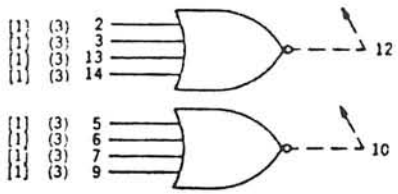


FIGURE 4-19

MC880P EQUIVALENT

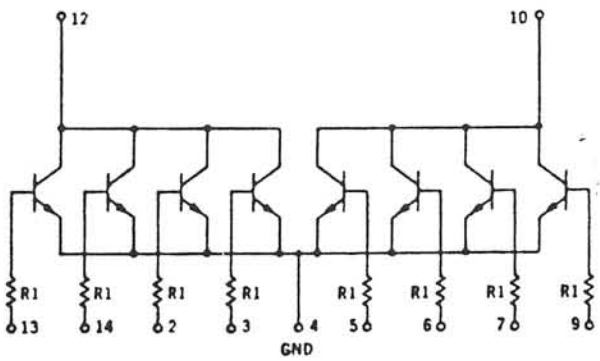
Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.



$12 = \overline{2 + 3 + 13 + 14}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC786P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC886P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES



V_{CC} CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

FIGURE 4-20

MC886P EQUIVALENT

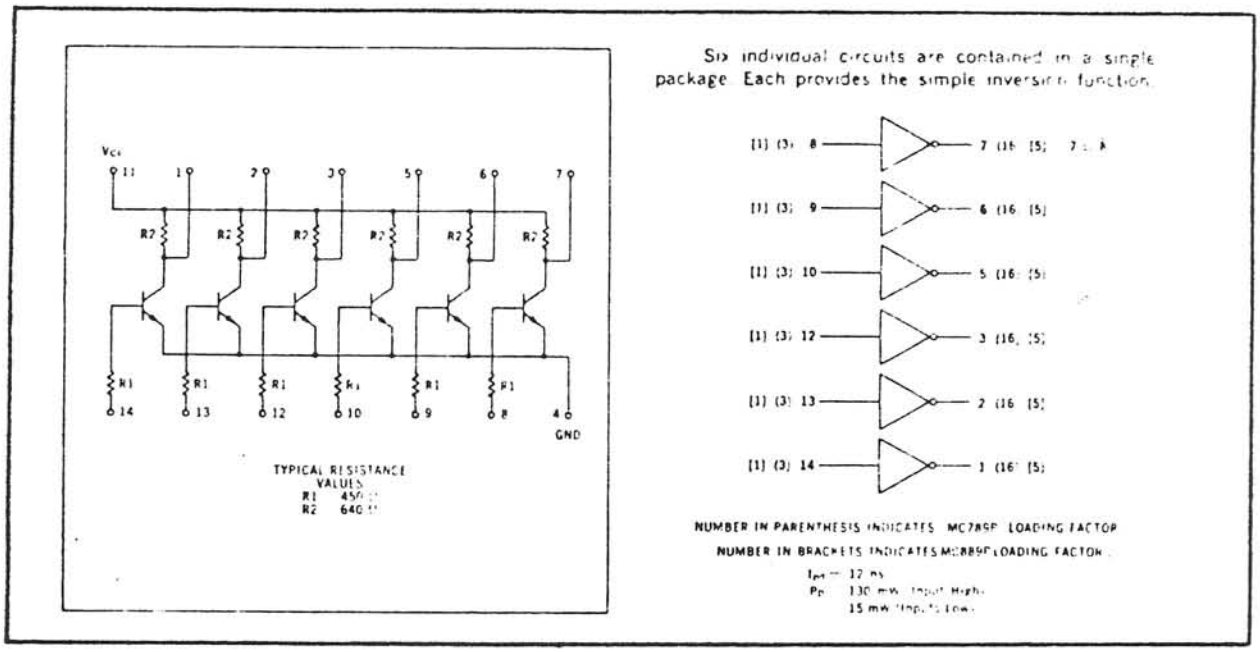


FIGURE 4-21

MC889P (MC779P) EQUIVALENT

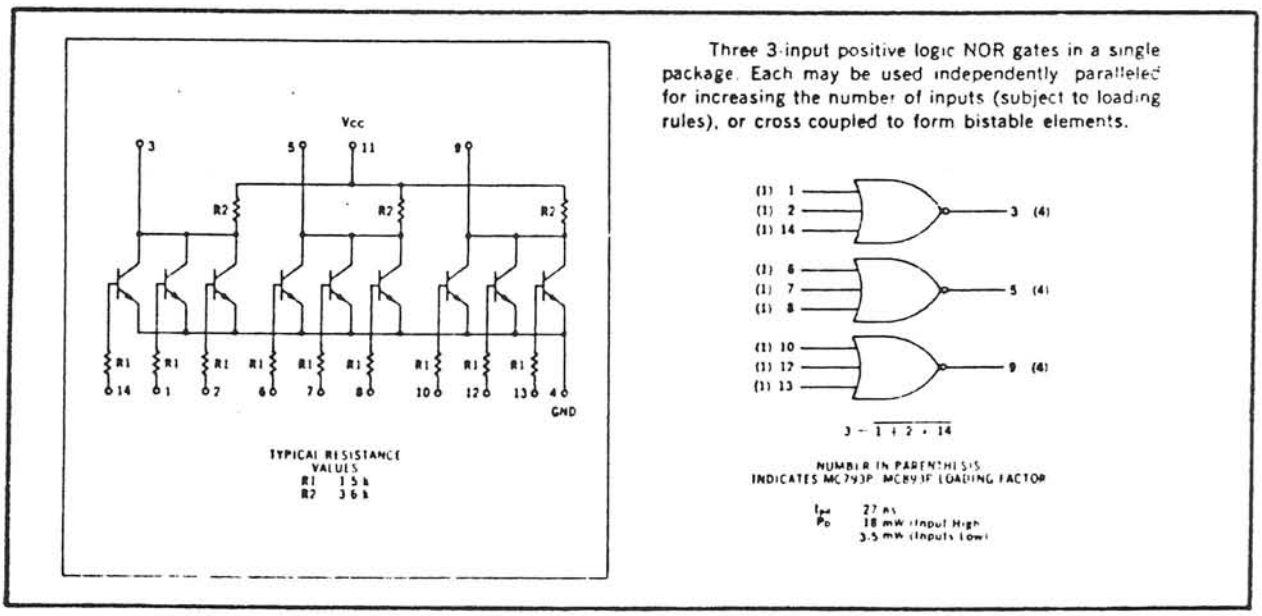
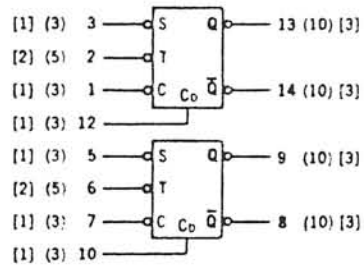


FIGURE 4-22

MC893P EQUIVALENT

Two J-K flip-flops in a single package Each flip-flop has a direct clear input in addition to the clocked inputs.



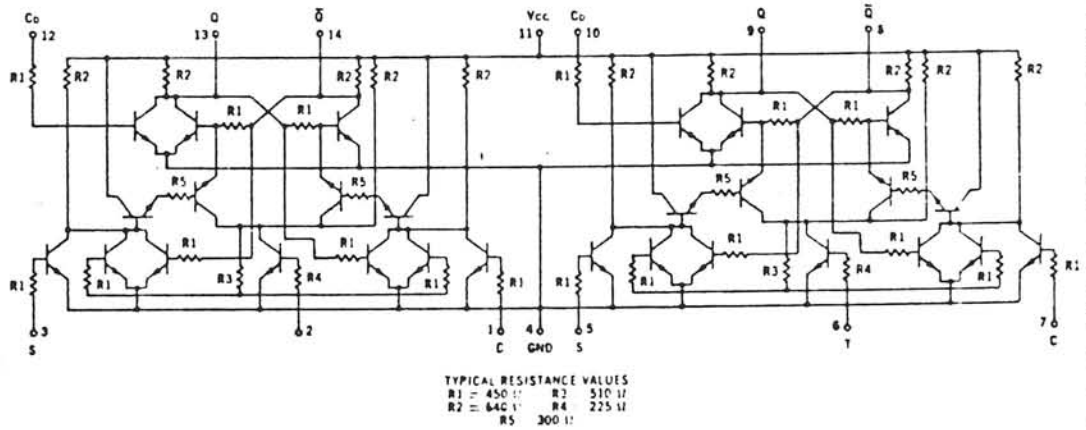
f_{toggle} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC790P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC890P

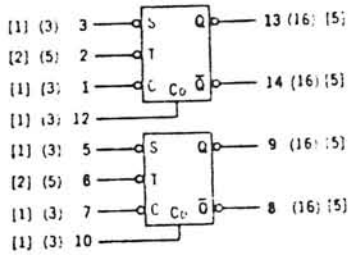


TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 510 Ω
R2 = 640 Ω R4 225 Ω
R5 300 Ω

FIGURE 4-23

MC890P EQUIVALENT

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



$f_{toggle} = 4$ MHz
$t_{pd} = 40$ ns typ

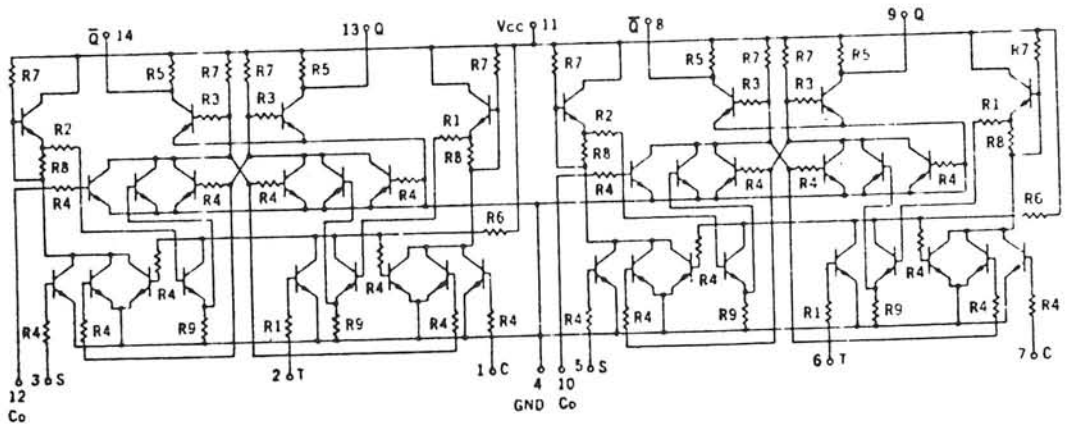
$P_D = 190$ mW typ (Only Clock Input High)
160 mW typ (Inputs Low)

CLOCKED INPUT OPERATION

t_n		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n

1. Direct input (Co) must be low
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}
3. Q_n is the state of the Q output in the time period t_n

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC791P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC891P



TYPICAL RESISTANCE VALUES
R1 = 300 Ω R4 = 600 Ω R7 = 900 Ω
R2 = 500 Ω R5 = 640 Ω R8 = 2.0 kΩ
R3 = 550 Ω R6 = 700 Ω R9 = 3.0 kΩ

FIGURE 4-24

MC891P EQUIVALENT

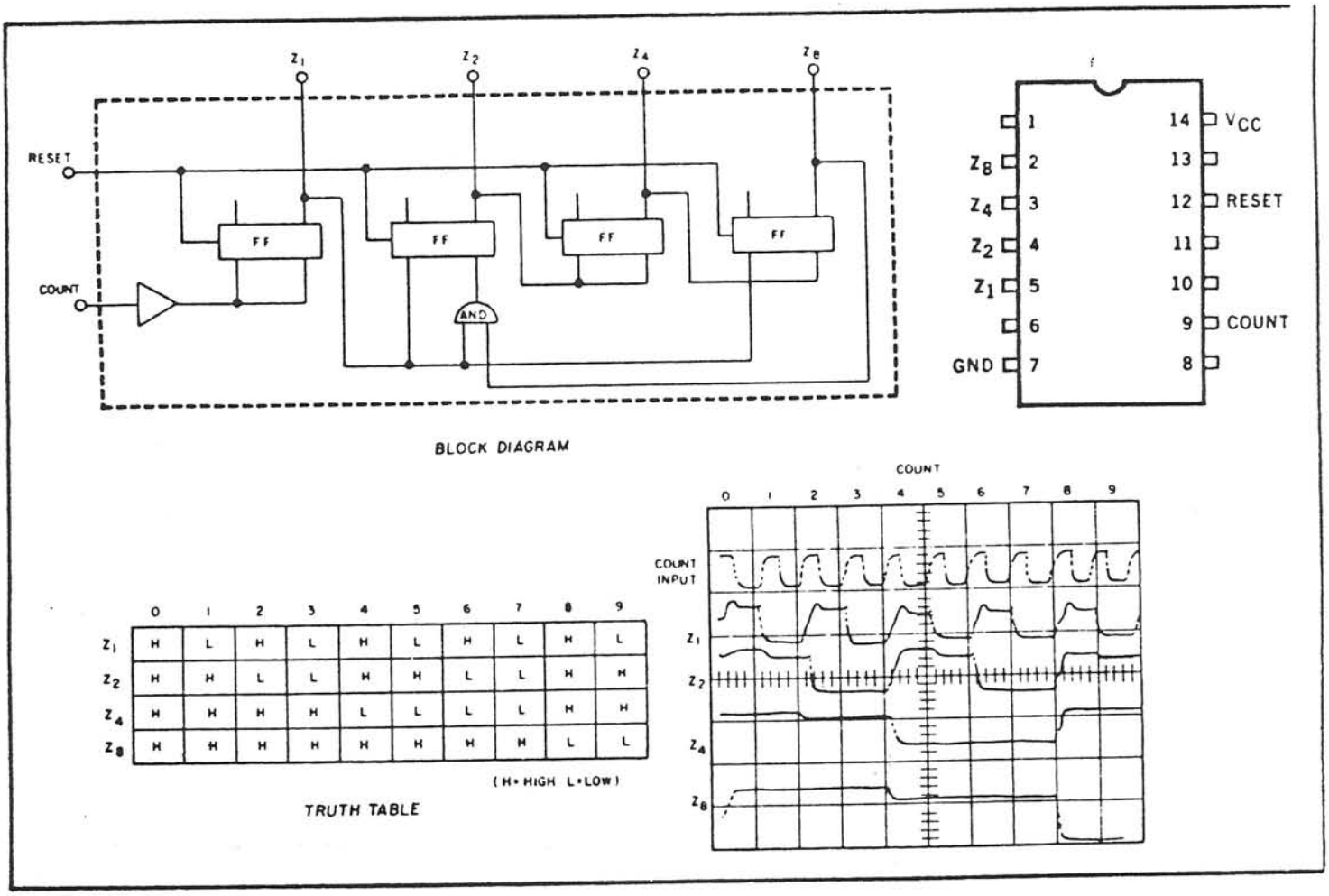
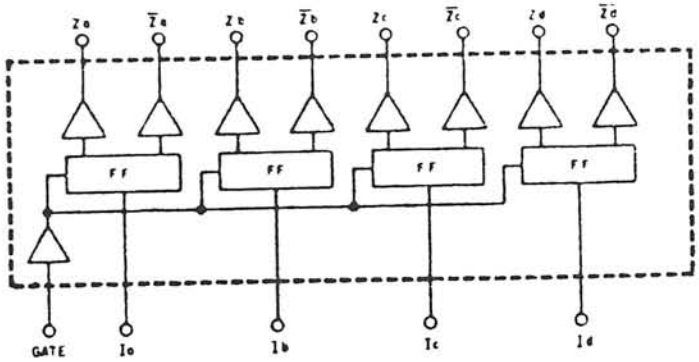
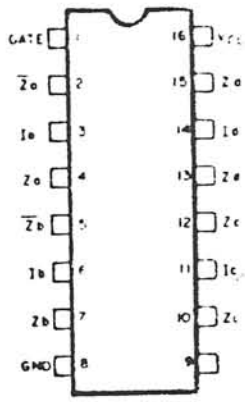


FIGURE 4-25

CμL 9958 EQUIVALENT



BLOCK DIAGRAM



BASE CONNECTIONS

GATE	I	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\overline{Q}$

H = HIGH
L = LOW
Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED

TRUTH TABLE

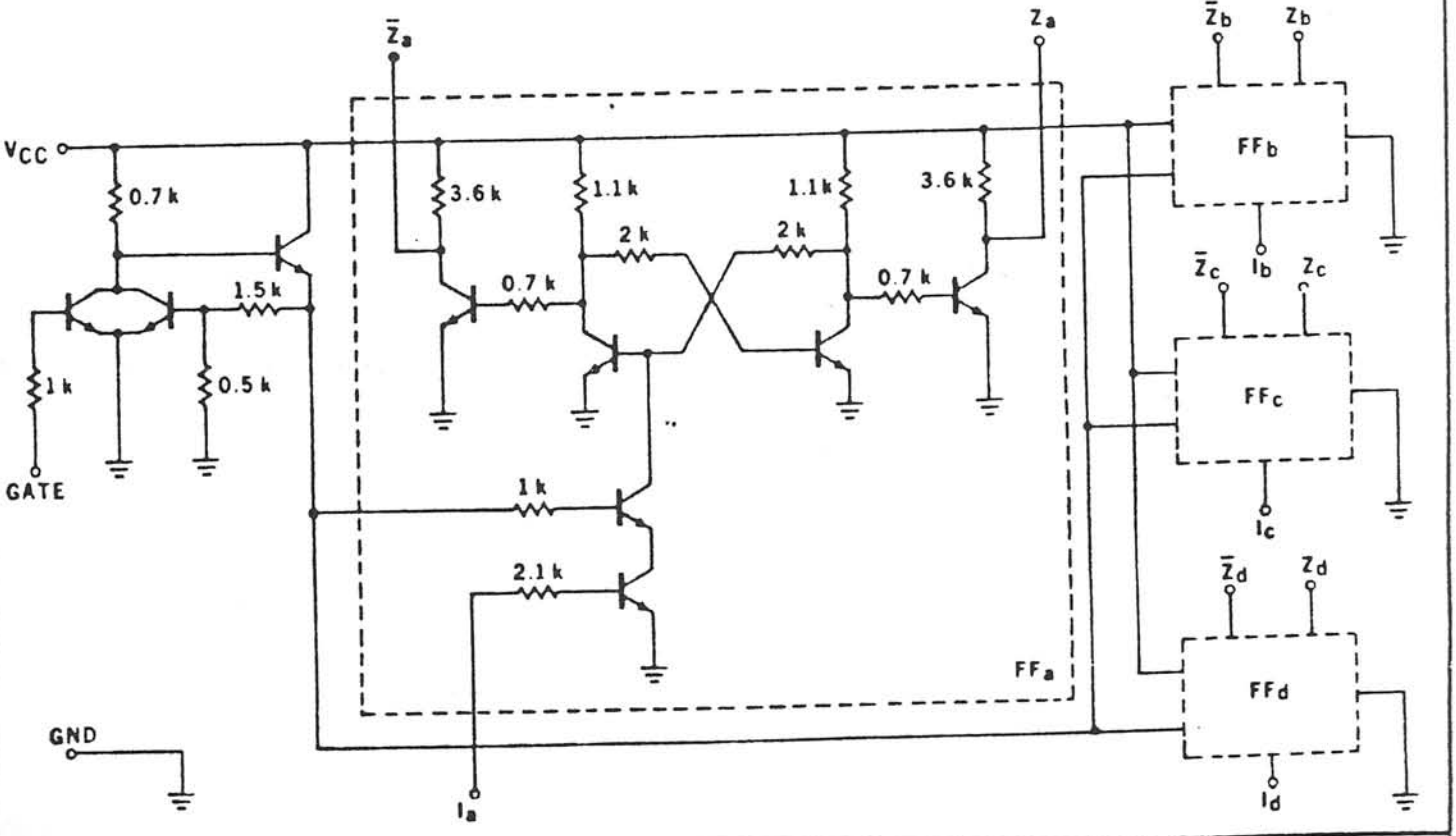


FIGURE 4-26

CμL 9959 EQUIVALENT

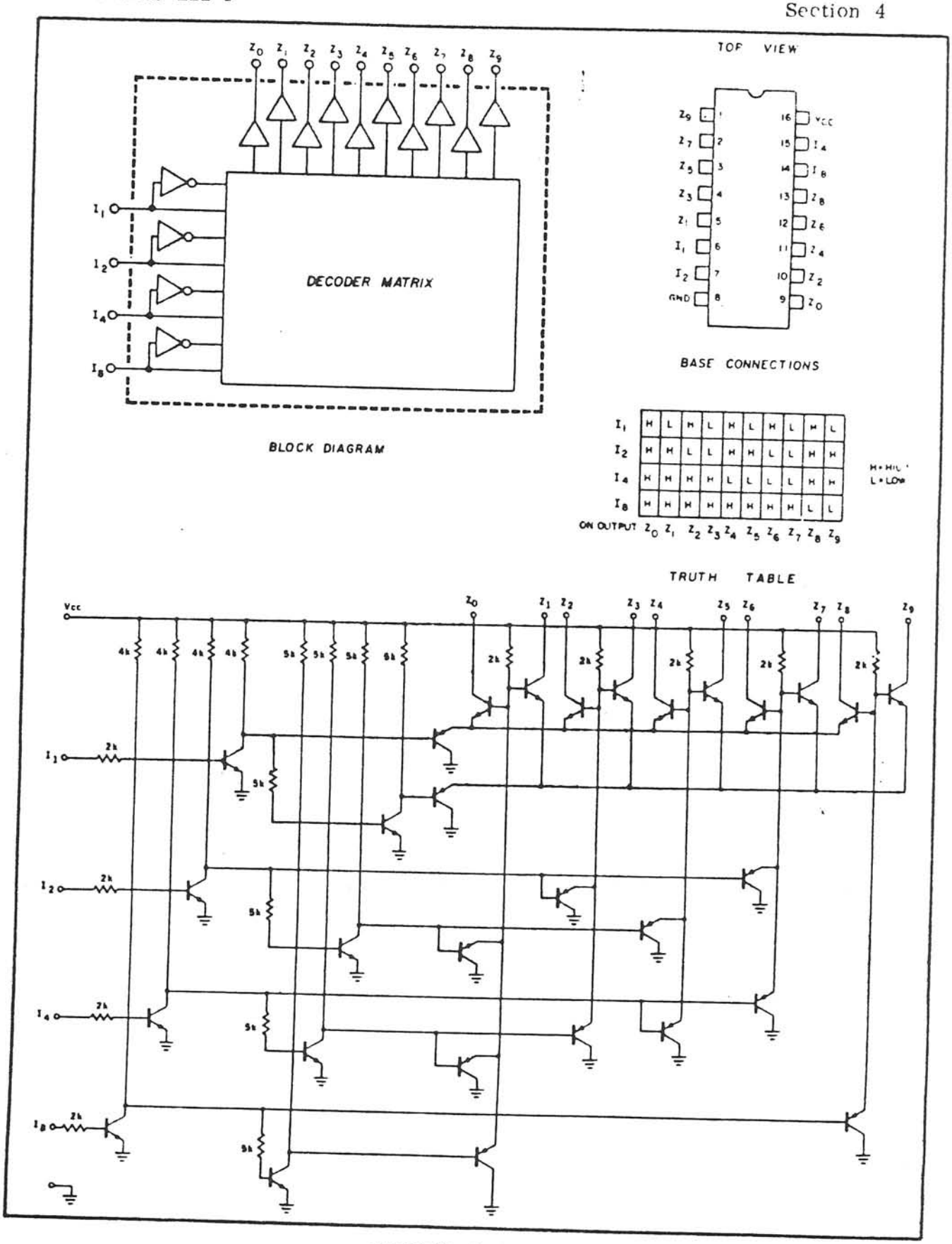
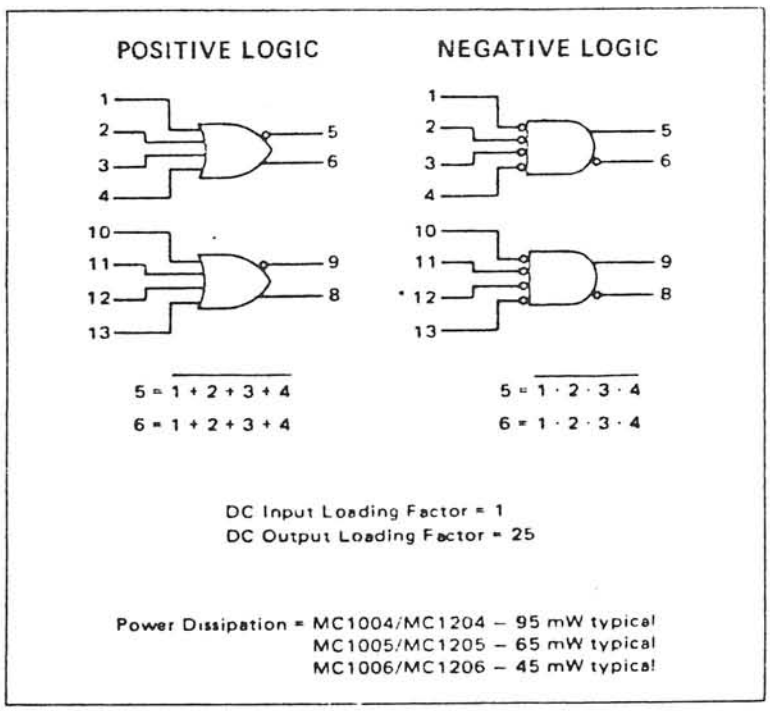


FIGURE 4-27

CμL 9960 EQUIVALENT

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



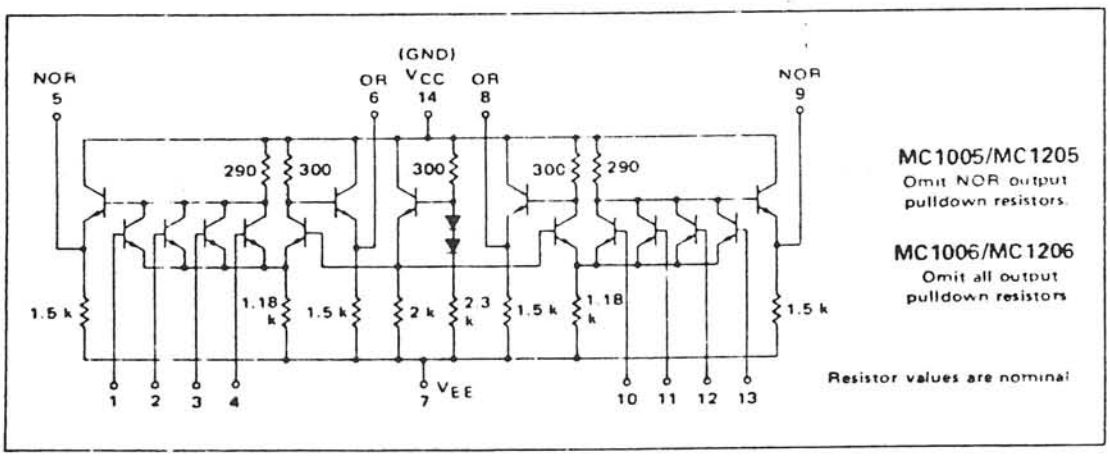
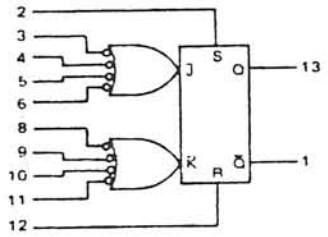


FIGURE 4-28

MC1004P(L) EQUIVALENT

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

*Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
**$\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} 0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D

All $\bar{J}$ $\bar{K}$ Inputs Are Static

$\bar{J}_D$ $\bar{K}_D$ TRUTH TABLE

Pin No.	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All Other $\bar{J}$-$\bar{K}$ Inputs And The R S Inputs Are At a "0" Level

CLOCKED $\bar{J}$ $\bar{K}$ TRUTH TABLE

Pin No.	$\bar{J}$	$\bar{K}$	$\bar{C}_D$	Q^n
	*	*	**	13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\bar{J}$-$\bar{K}$ Inputs And The R S Inputs Are At a "0" Level

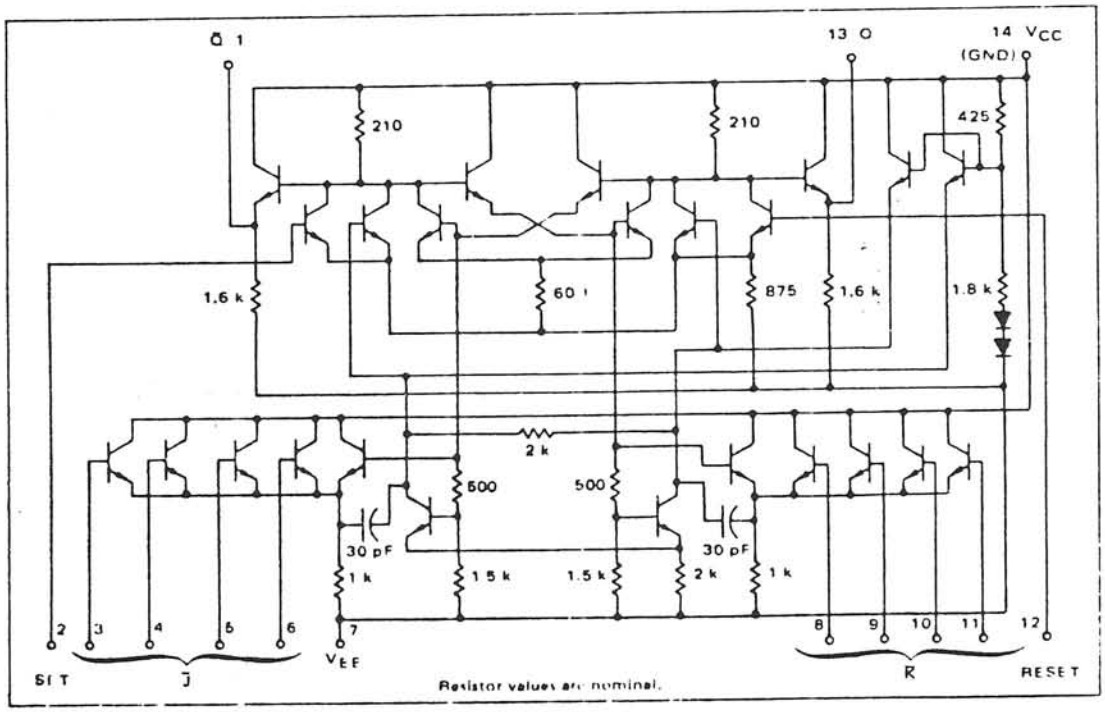
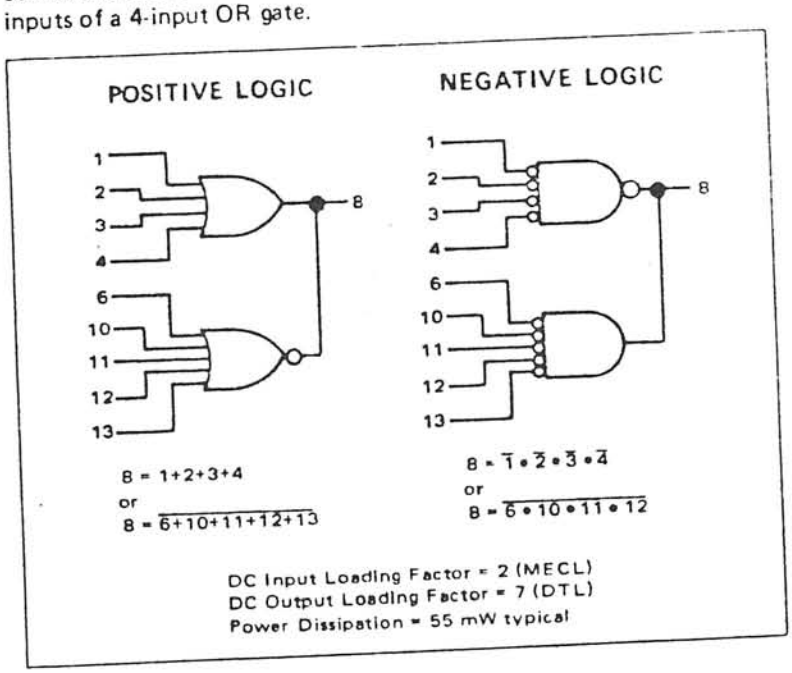


FIGURE 4-29

MC1013P(L) EQUIVALENT

Level translator intended for converting MECL signal levels to saturated logic levels. The translator will provide the positive logic OR or logic NOR function by connecting the internal bias driver output to the corresponding inputs of the differential amplifier, i.e., when pin 4 is connected to the reference bias, pin 5, pins 6, 10, 11 12, and 13 become the inputs of a 5-input NOR gate. When pin 6 is connected to the reference bias, pin 5, pins 1, 2, 3, and 4 become the inputs of a 4-input OR gate.



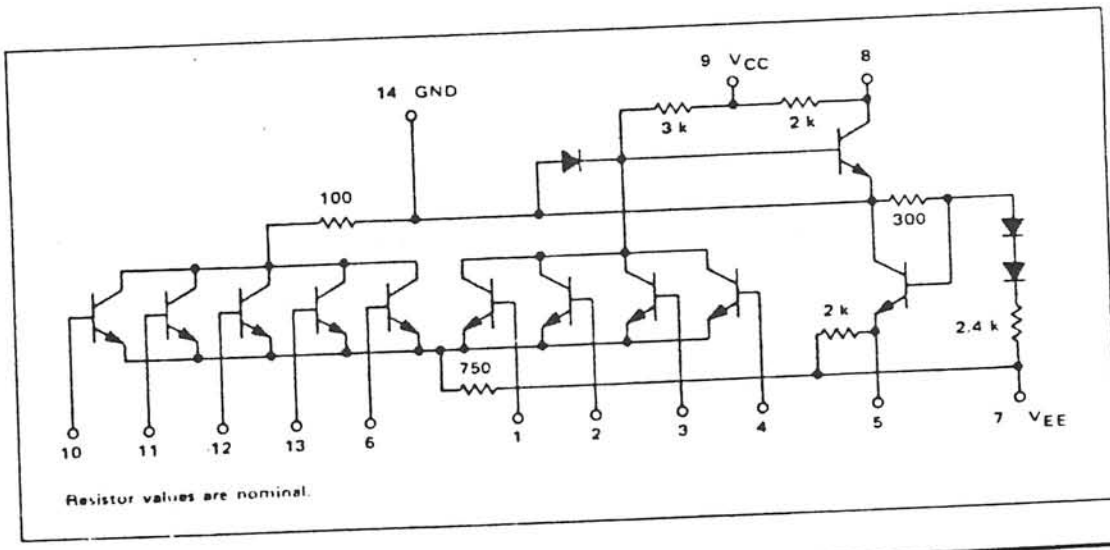
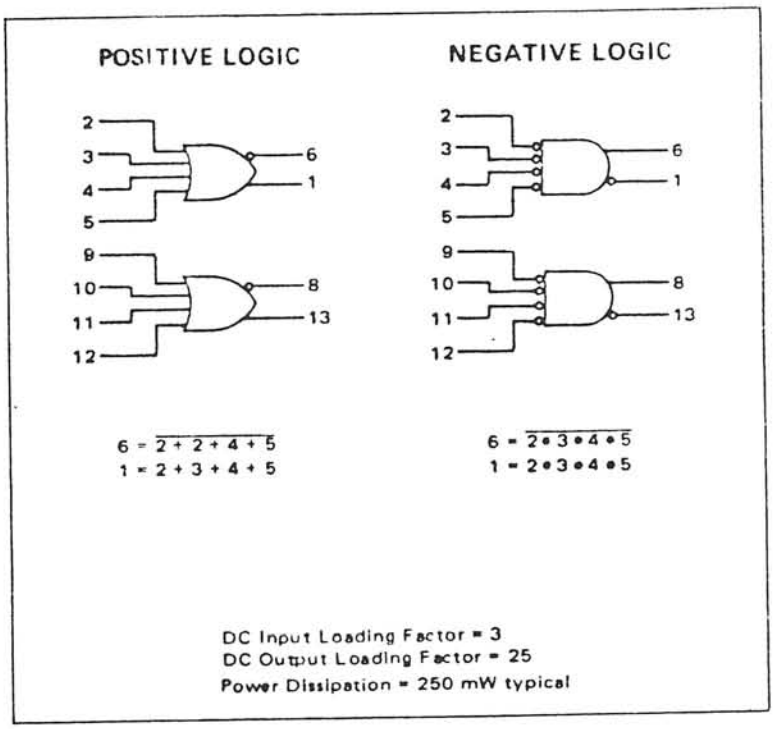


FIGURE 4-30

MC1018P(L) EQUIVALENT

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.



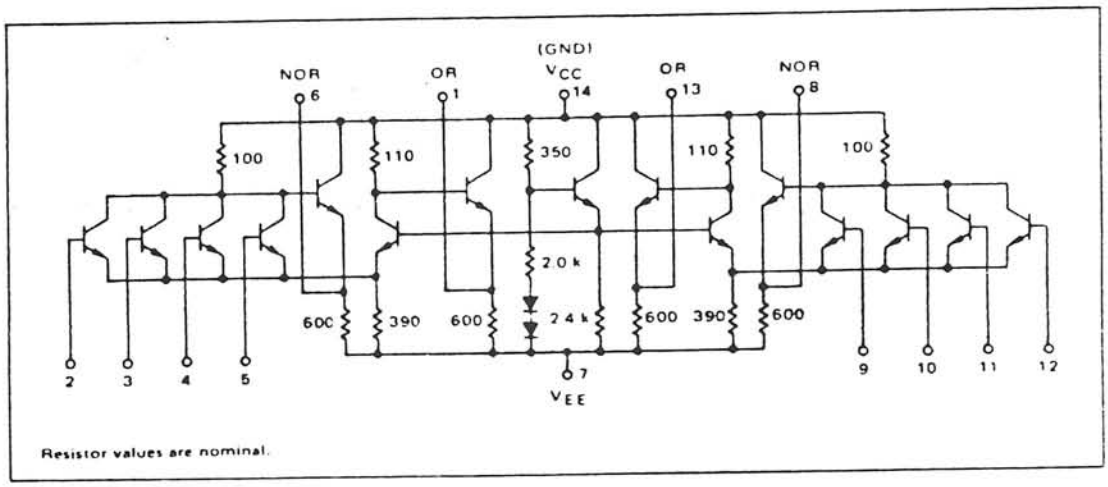
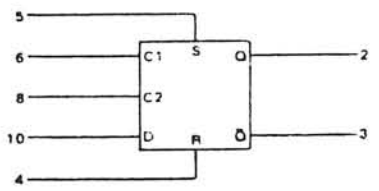


FIGURE 4-31

MC1023P(L) EQUIVALENT

Designed for clocked storage operation based on the "master slave" principle. Operation depends only on voltage levels, therefore the shape of the clock waveform becomes unimportant in determining the state of the flip flop and simplifies system application. When the clock is low, the input data is stored in the "master" and is subsequently transferred to the "slave" when the clock is high, making the data available at the outputs. In this operation the "master" is disabled before the slave is enabled, due to the design of the internal threshold skew. Along with a data input and two Clock inputs, the unit has a SET and a RESET input that are independent of the Clock

POSITIVE LOGIC



DC Input Loading Factor
C = 1, D = 2, R and S = 6
DC Output Loading Factor = 25
Power Dissipation = 185 mW typical using external 600 ohm pull down resistors
240 mW typical using internal pull down resistors

R-S TRUTH TABLE

Pin No	R 4	S 5	Q^{n+1} 2	$\bar{Q}^{n+1}$ 3
	0	0	Q^n	$\bar{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N D	N D

N D = Not Defined

CLOCKED TRUTH TABLE

Pin No	D 10	C 6 or 8	Q^{n+1} 2	$\bar{Q}^{n+1}$ 3
	0	0	Q^n	$\bar{Q}^n$
	1	0	Q^n	$\bar{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip flop at a change in level from a low state to a high state of the clock

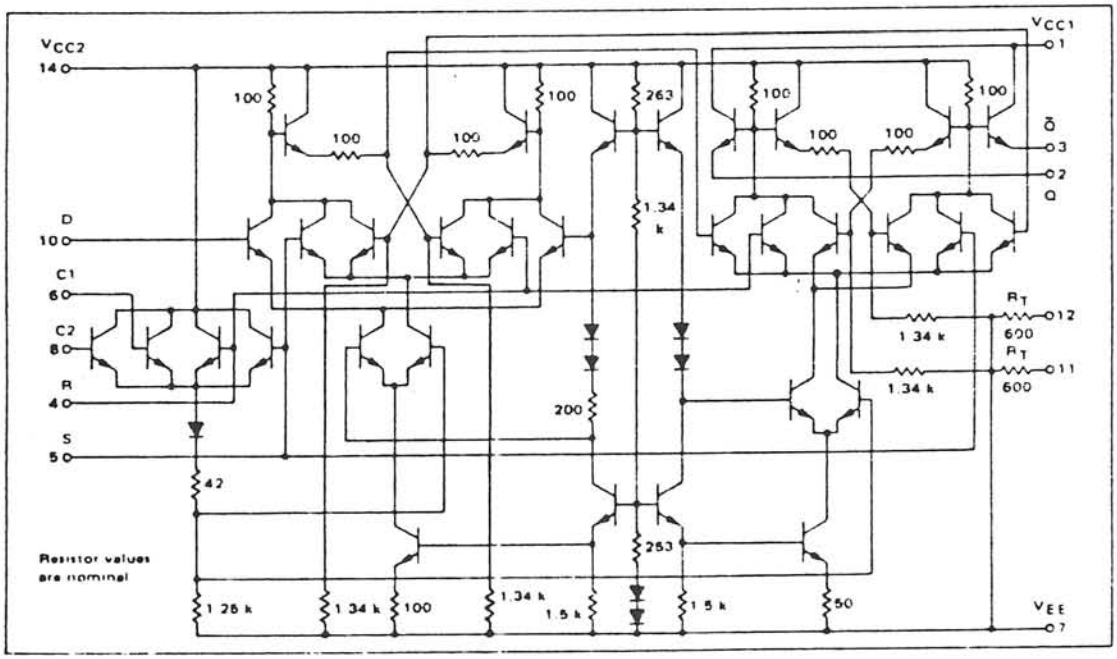


FIGURE 4-32

MC1034P(L) EQUIVALENT

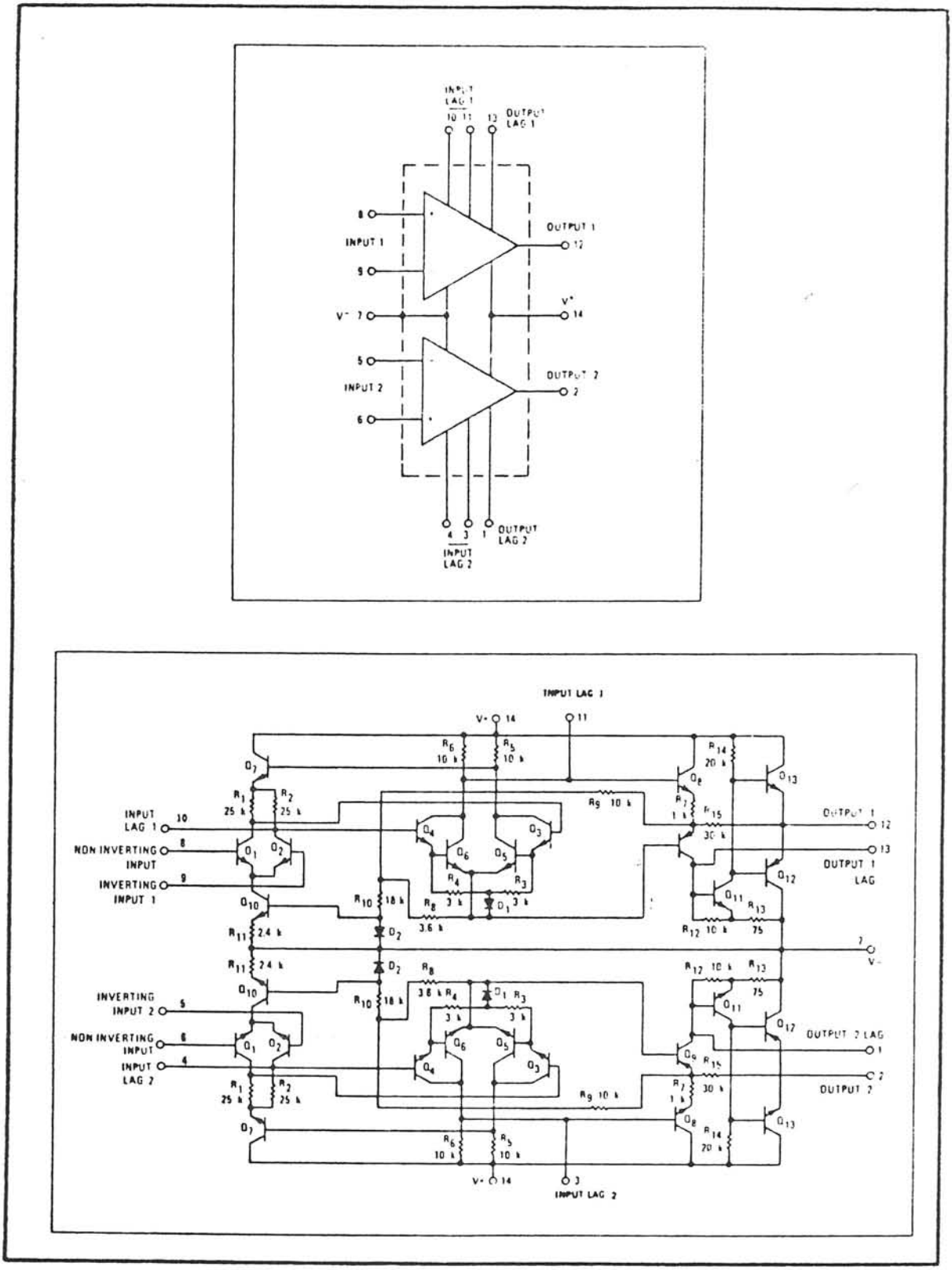


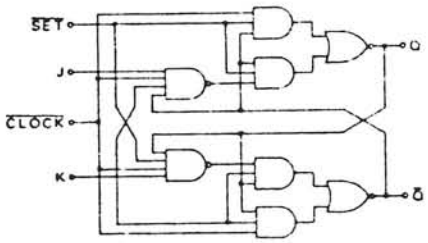
FIGURE 4-33

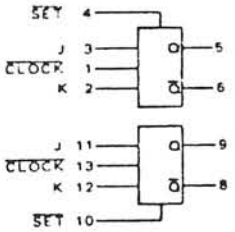
MC1437L EQUIVALENT

The MC3062 dual JK flip flop triggers on the negative edge of the clock. Each flip flop is provided with a separate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the Set up and Hold times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip flop when the clock falls. Each flip flop may be set at any time without regard to the clock state by applying a low level to the $\overline{SET}$ input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN





Input Loading Factors
$\overline{CLOCK}$, $\overline{SET}$ = 1.6
J, K = 0.6

Output Loading Factor = 10

J-K TRUTH TABLE

Typical Characteristics
(V_{CC} = 5.0 V T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd} "1" = 12 ns
t_{pd} "0" = 12 ns

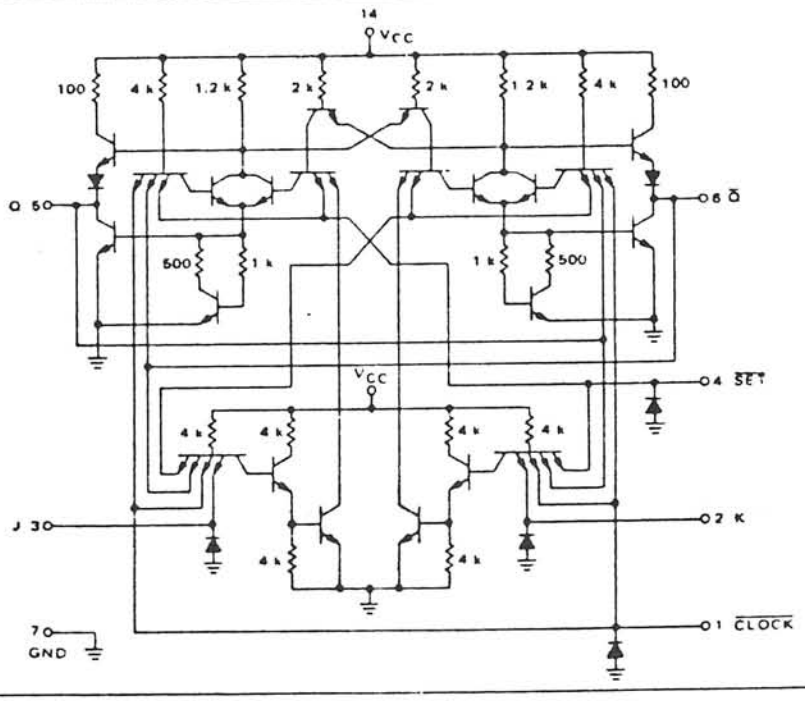
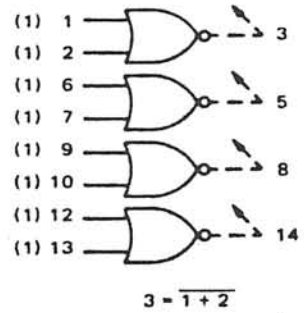


FIGURE 4-34

MC3062P(L) EQUIVALENT

Four 2-input expanders housed in a single package increase the input capability of mW MRTL gates.



$3 = \overline{1 + 2}$

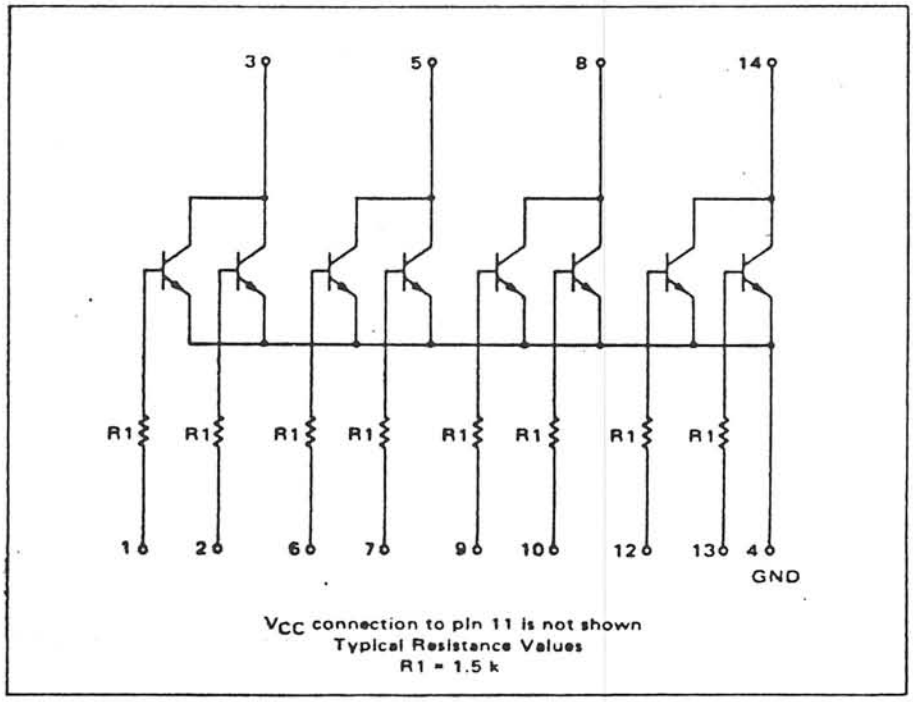
t_{pd} = 27 ns

P_D = 20 mW typ (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC9721P, MC9821P LOADING FACTOR

NOTES ON THE USE OF THE MC9721/MC9821

1. The input loading factor of the expanded gate is 1.33.
2. Pin 11 of the expander must be connected to V_{CC}.
3. The output loading factor of the expanded gate is decreased 0.5 load for every added node.



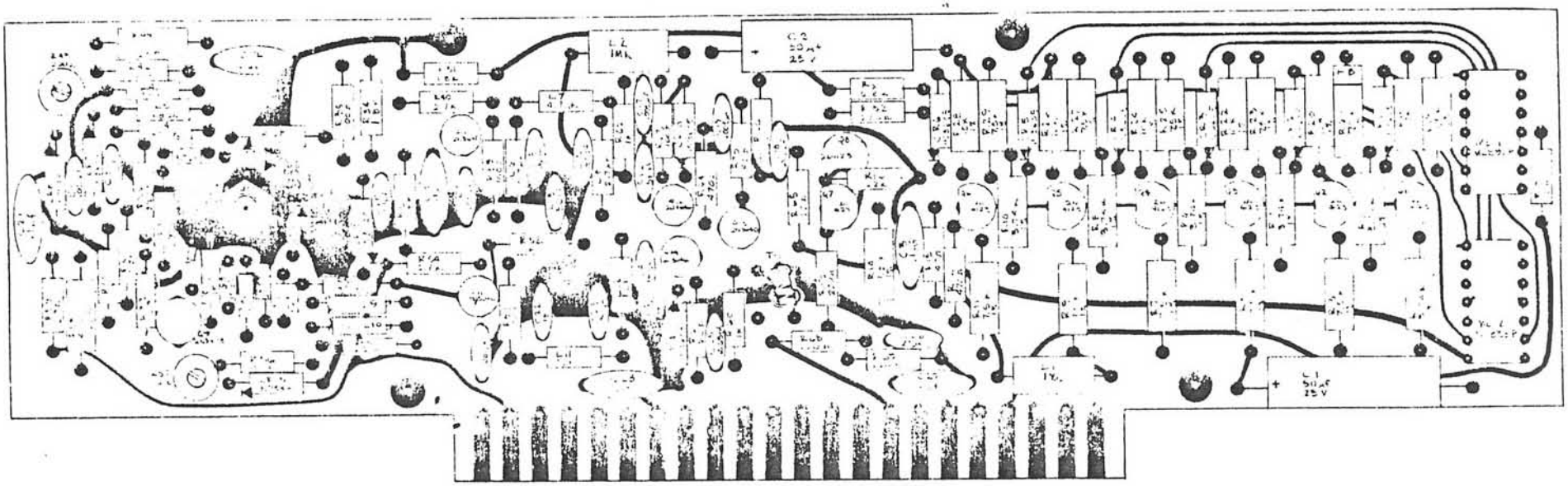
V_{CC} connection to pin 11 is not shown
Typical Resistance Values
R1 = 1.5 k

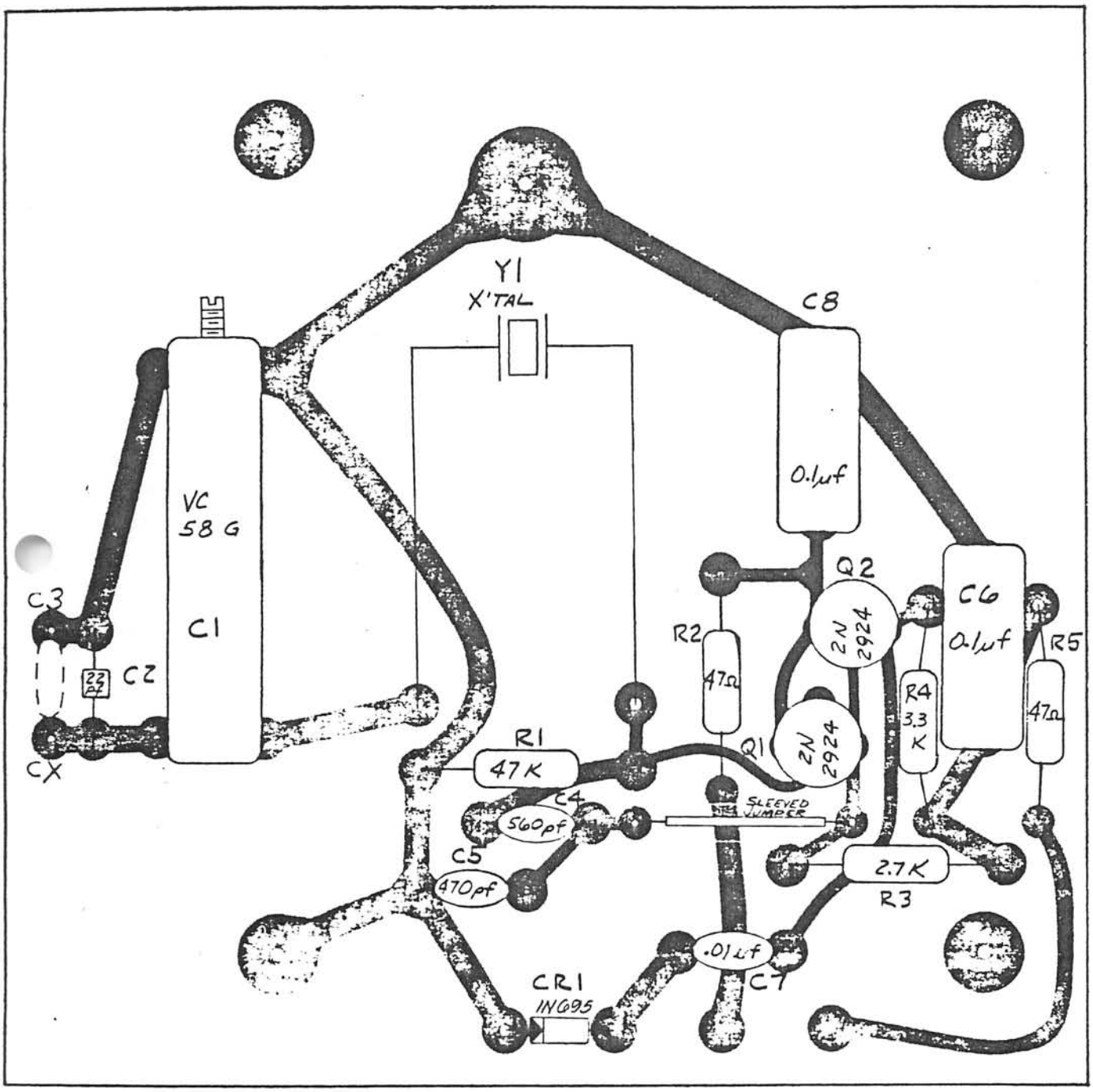
FIGURE 4-35

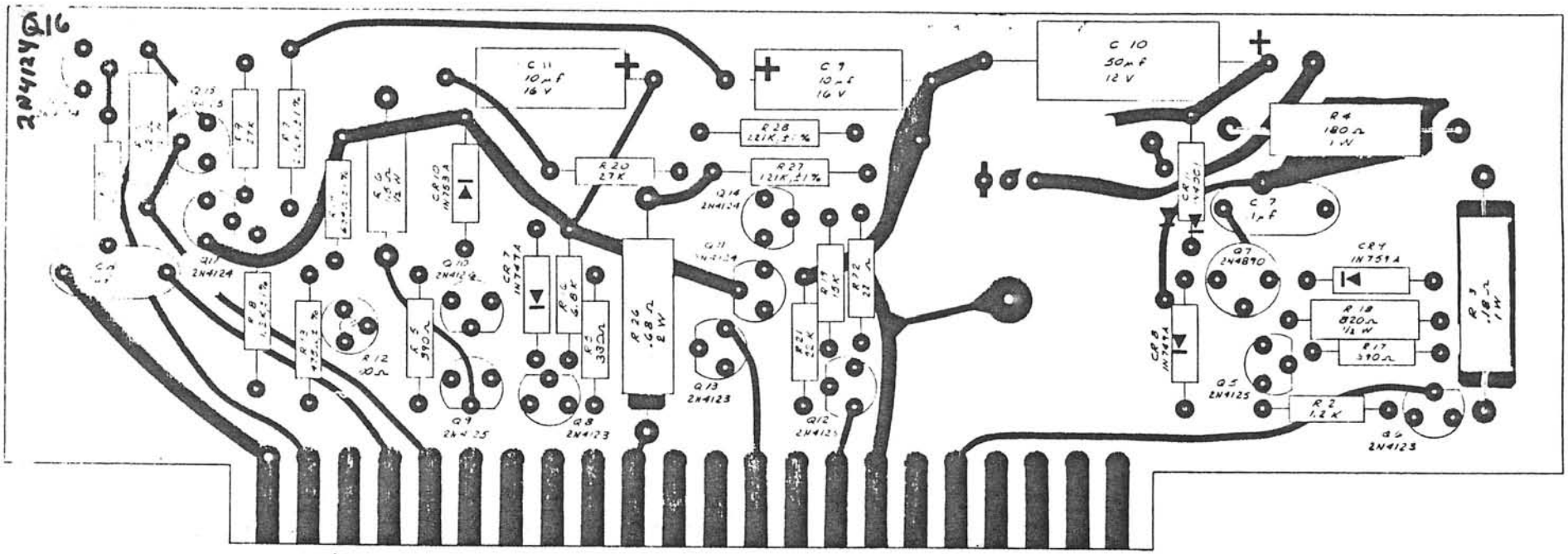
MC9721P EQUIVALENT

4.8 SCHEMATICS AND RELATED DRAWINGS

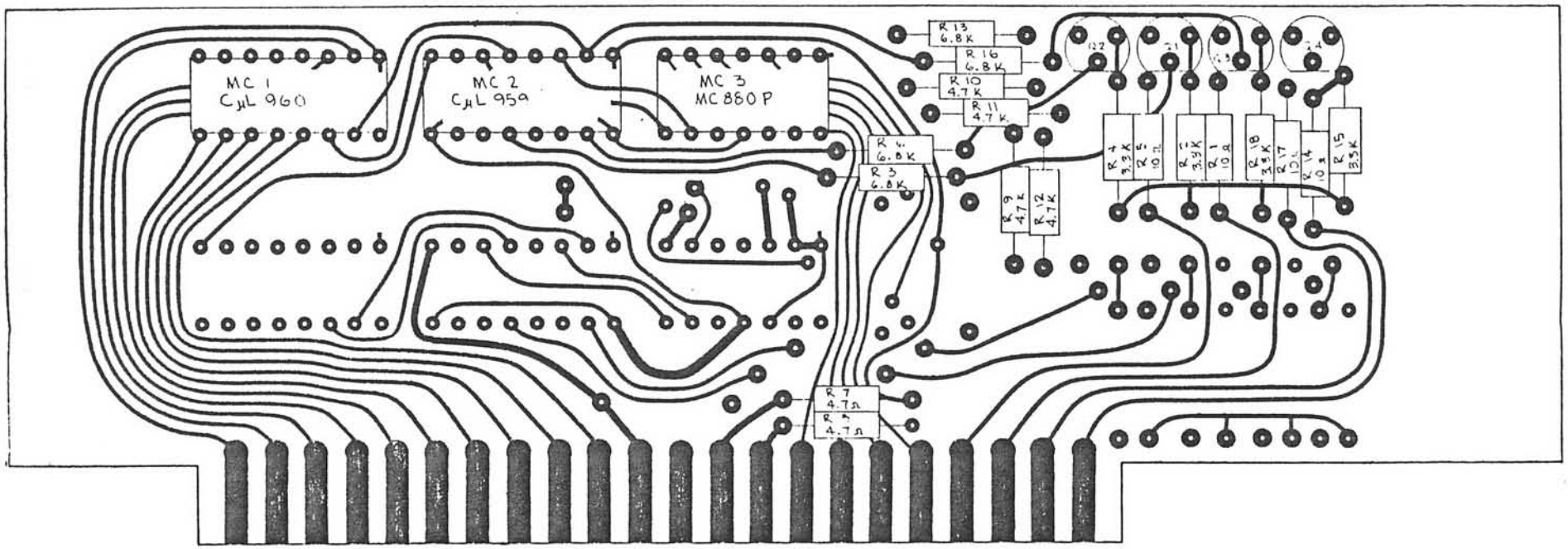
This section contains the schematics and component location illustrations for the Model FRO-212-1. The schematic appears on the fold-out sheet while the corresponding component location illustration appears on the left hand page opposite the schematic. If further component information is required, consult the individual board parts list contained in Section 5 of this manual.

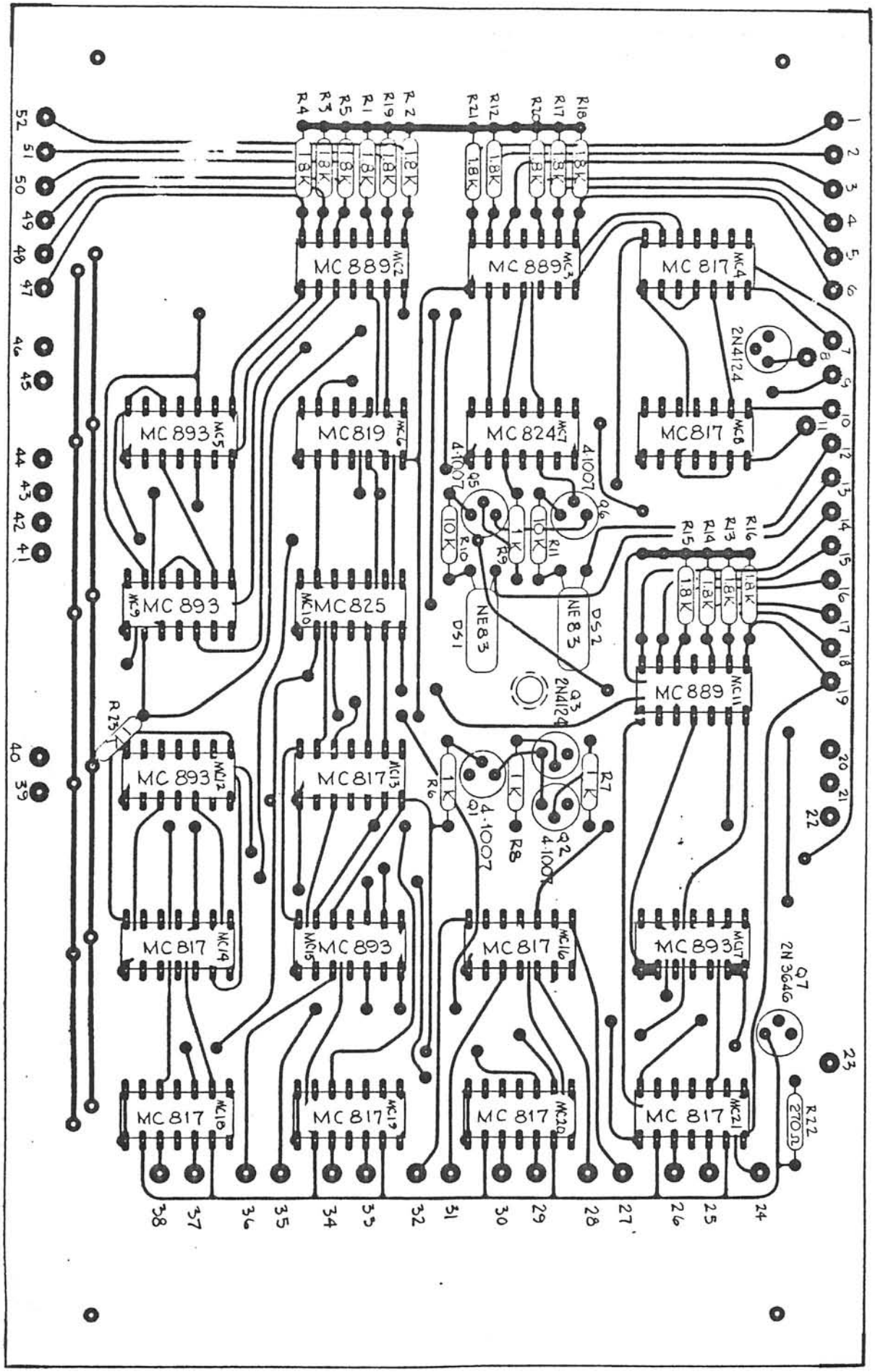


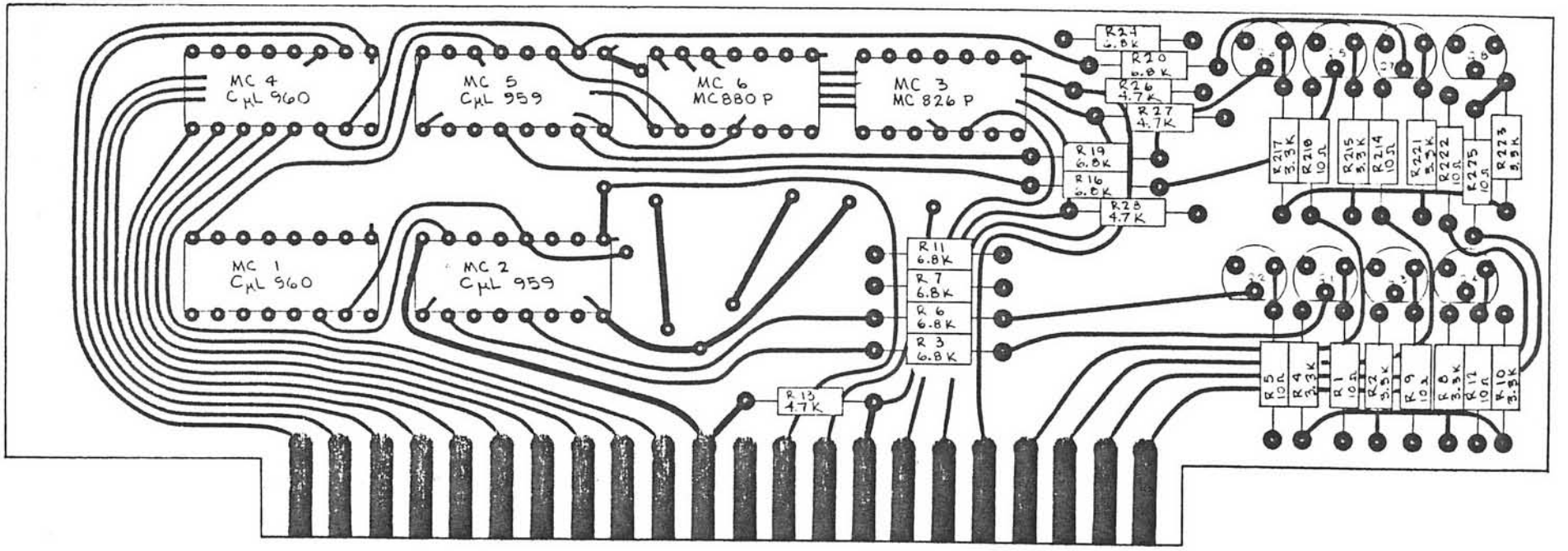


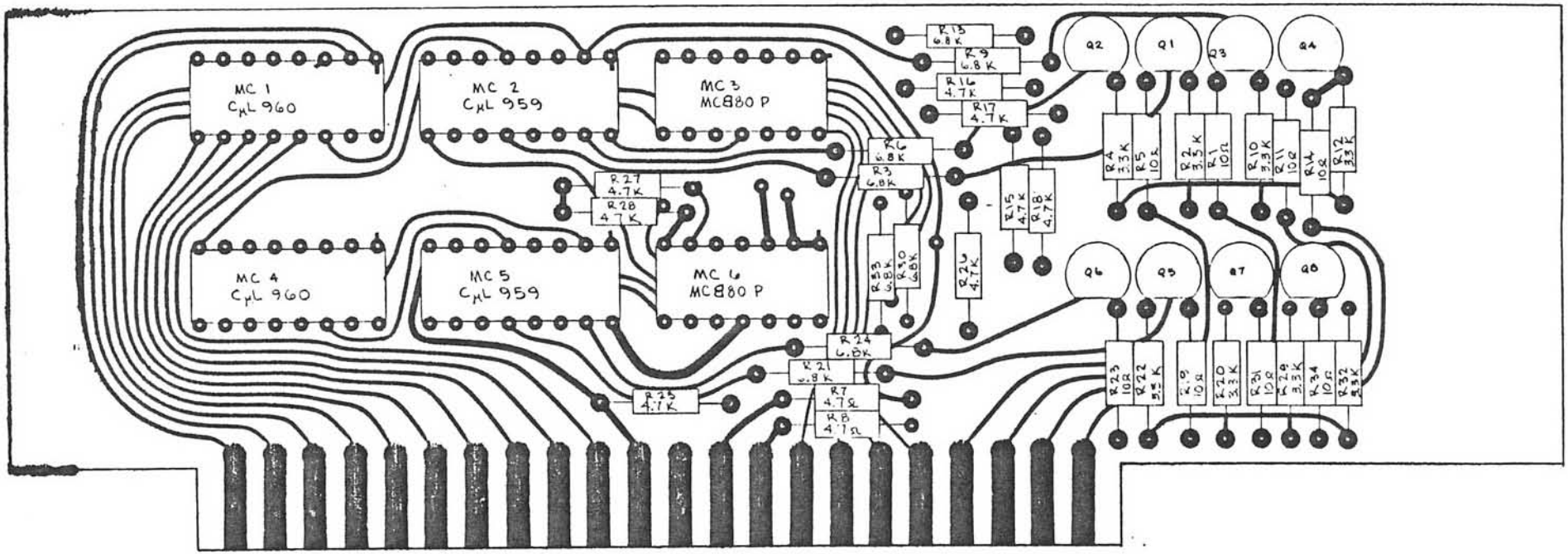


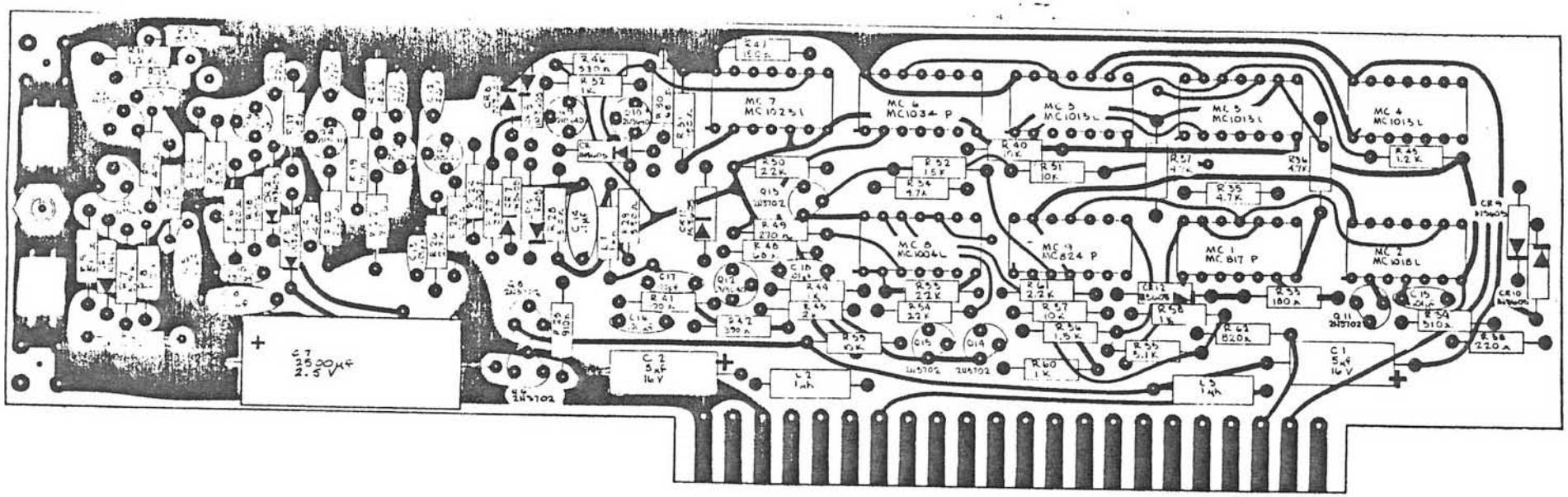
REGULATOR BOARD



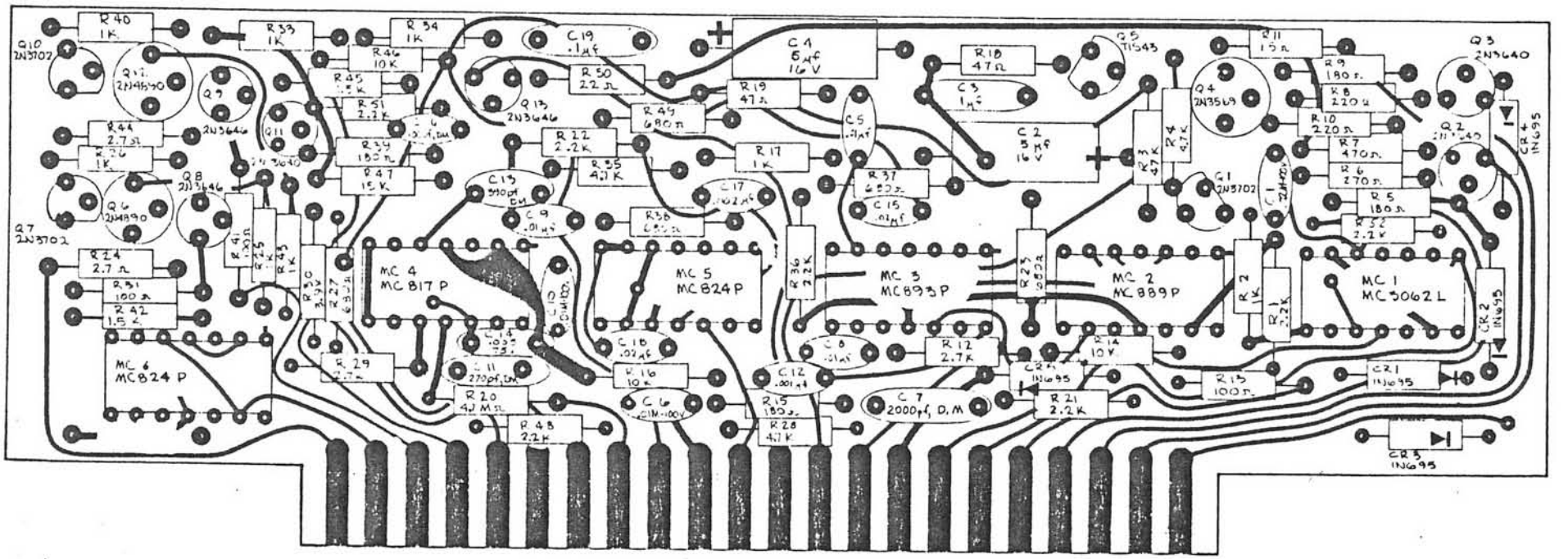




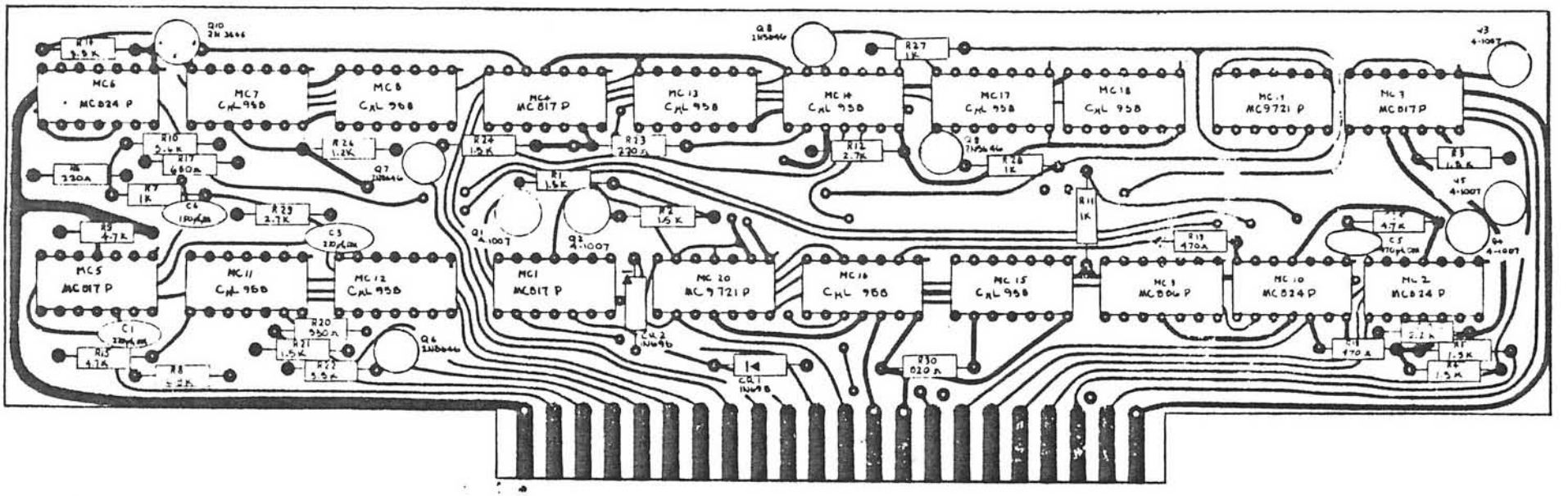


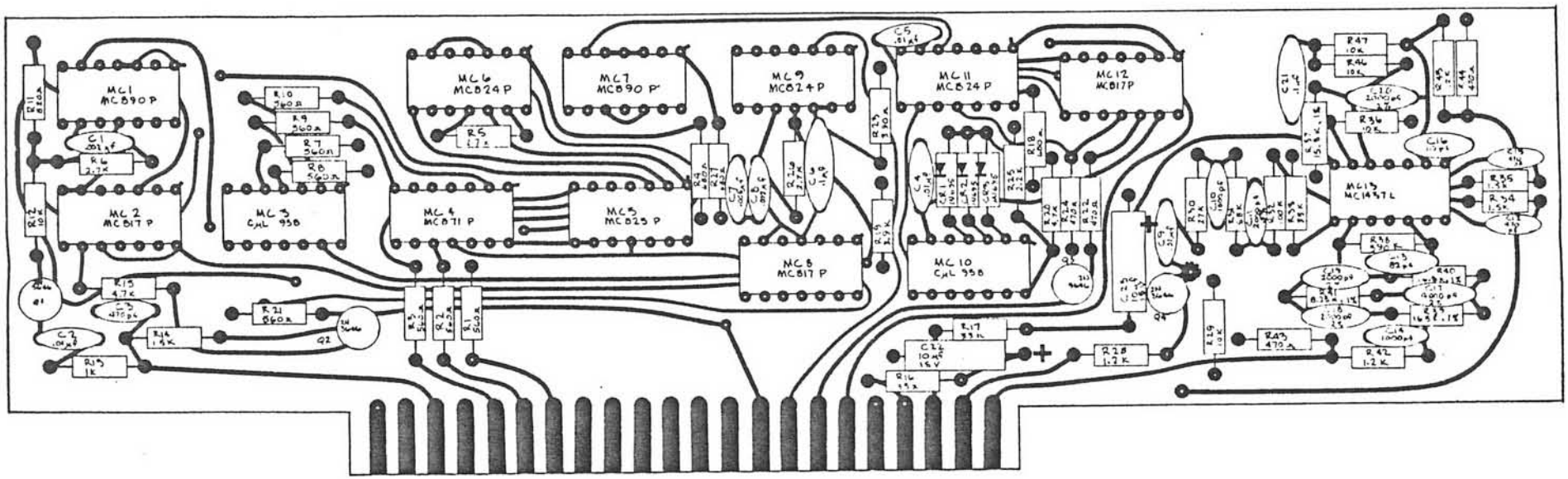


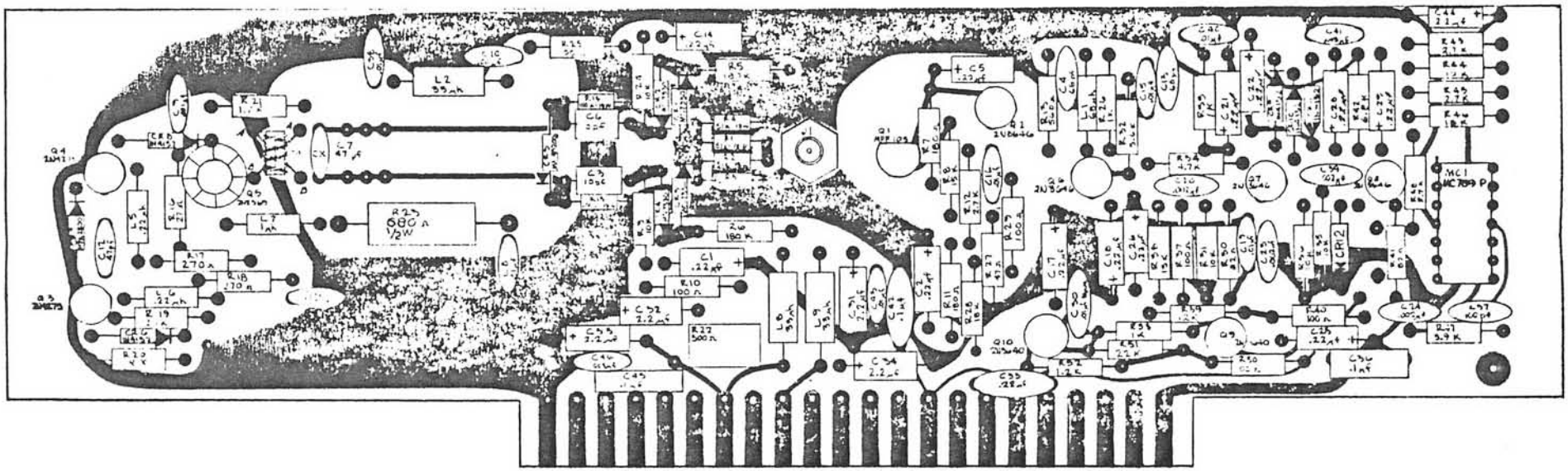
120 MHz DCU



RESET & CONTROL







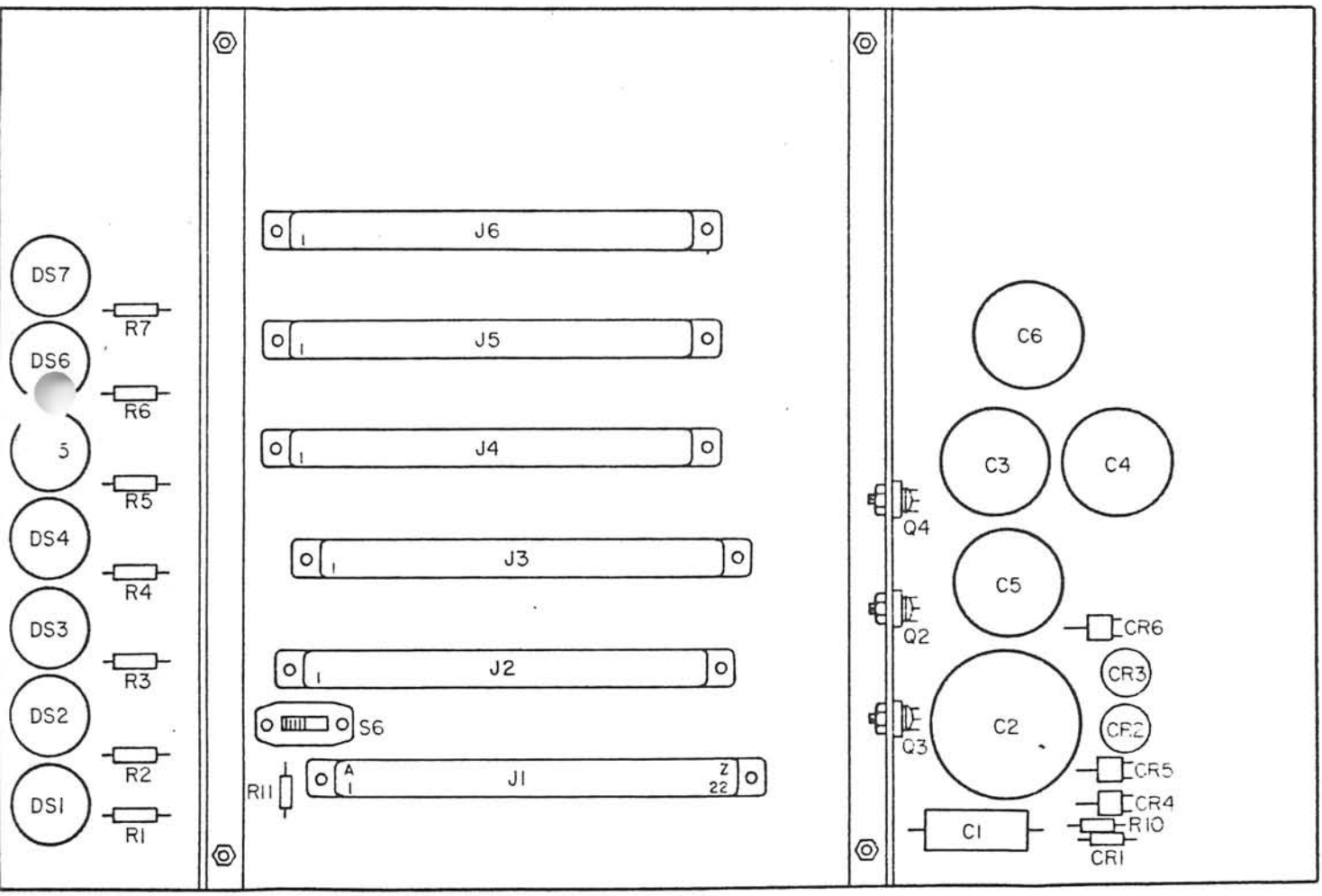


FIGURE 4-51
DISPLAY AND POWER SUPPLY P.C. B
COMPONENT LOCATION

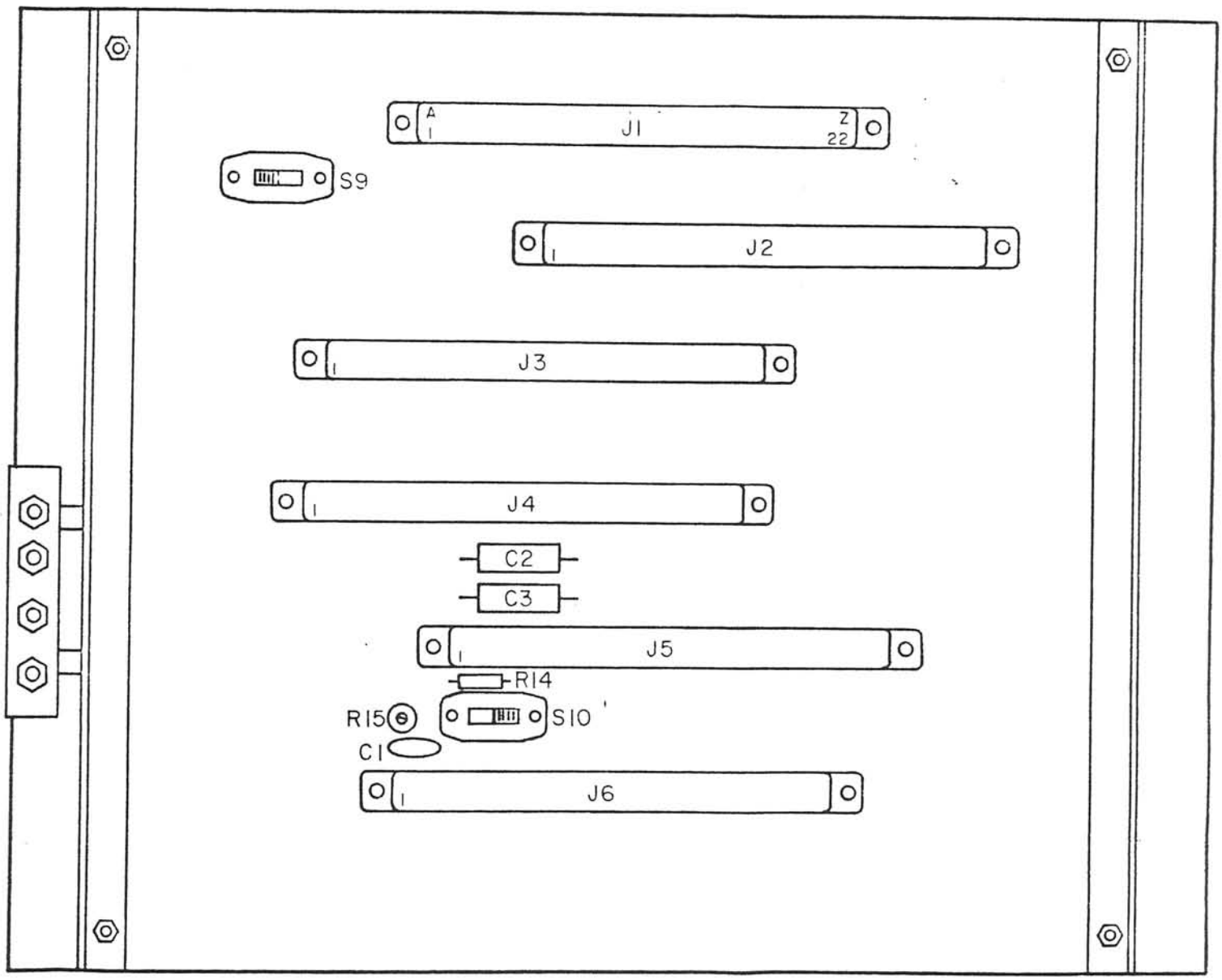


FIGURE 4-52
INPUT AND LOGIC P.C. BOARD
COMPONENT LOCATION

SECTION 5

PARTS LISTS

5.1 INTRODUCTION

This section contains the necessary information for the procurement of replacement parts from either Eldorado Electrodata or directly from commercial sources.

5.2 ORDERING INFORMATION

When it is necessary to order replacement parts directly from Eldorado Electrodata, address all orders or inquiries to:

CUSTOMER SERVICE PARTS DEPARTMENT
ELDORADO ELECTRODATA CORP.
601 Chalomar Road
Concord, California 94520
Telephone: 415-686-4200
TWX: 910-481-9476

When ordering replacement parts be certain to specify instrument model and serial number and complete part description including reference, description, manufacturer, manufacturer's part number and the six digit Eldorado part number.

PARTS LIST

COUNTDOWN AND RAMP P.C. ASSEMBLY

Reference	Description		Mfr.	Mfr. No.	EI No.	Qty.
Assembly	Countdown and Ramp		EE	D-32-06386	046386	1
C1, 2	Capacitor, Electrolytic 50 μF, 16 wvdc		Sprague	TE1160	000256	2
C3, 4, 12, 21, 27, 28	Capacitor, Mylar 0.1 μF, 200 wvdc	or	Amperex IMB	C280AE/P100K XP2C104	000211 003018	6
C5	Capacitor, Ceramic 15 pF, 300 wvdc		JFD	UY02150J	002006	1
C6	Capacitor, Fixed Mica 2.2 pF, 500 wvdc		Stackpole	GA Series	003489	1
C7	Capacitor, Chip .001 μF, 50 wvdc		Aerovox	ULA105B102M	003010	1
C8, 9, 20, 29	Capacitor, Ceramic Disc .001 μF, 1000 wvdc		Sprague	5GA-D10	000115	4
C10	Capacitor, Fixed Mica 4.7 pF, 500 wvdc		Stackpole	GA Series	003004	1
C11	Capacitor, Ceramic Disc .002 μF, 500 wvdc		Erie	X5FP-202K	003011	1
C13, 16	Capacitor, Dipped Mica 56 pF, 500 wvdc		Sangamo	D155F560JO	000069	2
C14, 15	Capacitor, Dipped Mica 180 pF, 500 wvdc		Sangamo	D155F181JO	000087	2
C17, 18, 19, 25	Capacitor, Ceramic Disc .005 μF, 50 wvdc		Sprague	TG-D50	000150	4
C22, 24	Capacitor, Dipped Mica 18 pF, 500 wvdc		Sangamo	D155C180JO	000042	2
C23	Capacitor, Dipped Mica 39 pF, 500 wvdc		Sangamo	D155E390JO	000060	1
C26	Capacitor, Dipped Mica 27 pF, 500 wvdc		Sangamo	D155E270JO	000056	1
CR1-7, 10, 12, 14	Diode, 1N3605		ITT	1N3605	000550	10
CR8, 13	Diode, Zener, 1N754A		Motorola	1N754A	000532	2
CR9	Diode, Tunnel, TD253A		GE	TD253A	000509	1
CR11	Diode, Tunnel, TD254A		GE	TD254A	000512	1
J1	Connector		Sealectro	51-051-000	003432	1
L1, 2	Inductor, 1 mH		Delevan	2500-25	003076	2
L3	Coil Assembly, 20 nH		EE	A-45-06531	046531	1
L4, 5	Inductor, .68 μH		Delevan	1025-16	000655	2

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
L6, 8	Inductor, 2.7 μH	Delevan	1025-30	000662	2
L7	Inductor, 4.7 μH	Delevan	1025-36	000665	1
L9, 10	Coil Assembly, 75 nH	EE	A-45-06532	046532	2
L11, 12	Inductor, 1 μH	Delevan	1025-20	000657	2
MC1	Micromodule, MC891P Dual J-K Flip-flop	Motorola	MC891P	003430	1
MC2	Micromodule, MC839P Divide-By-Sixteen	Motorola	MC839P	003098	1
Q1-8	Transistor, 2N4123	Motorola	2N4123	003266	8
Q9	Transistor, 2N3478	RCA	2N3478	003261	1
Q10, 11, 13	Transistor, 2N3640	Fairchild	2N3640	001728	3
Q12, 14	Transistor, 2N3646	Fairchild	2N3646	001731	2
R1, 2, 4, 6, 8, 10	Resistor, Metallic Film 3.74kΩ, 1/4W, 1%	IRC	RN60 B3741F	003212	6
R3, 5, 7, 9, 11, 14, 19, 21, 23, 25, 27, 29	Resistor, Metallic Film 7.5 kΩ, 1/4W, 1%	IRC	RN60 B7501F	001114	12
R12, 37, 51, 64	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001092	4
R13, 32, 66, 68, 69	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	Allen Bradley	CB2215	001086	5
R15	Resistor, Carbon Comp. 47Ω, 1/4W, 5%	Allen Bradley	CB4705	001075	1
R16	Resistor, Carbon Comp. 22 kΩ, 1/4W, 5%	Allen Bradley	CB2235	001120	1
R17, 41	Resistor, Carbon Comp. 10Ω, 1/4W, 5%	Allen Bradley	CB1005	001067	2
R18, 20, 22, 24, 26, 28	Resistor, Metallic Film 10 kΩ, 1/4W, 1%	IRC	RN60 B1002F	001116	6
R30	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5% (nom.)	Allen Bradley	CB6825	001113	1
R31, 34, 50	Resistor, Carbon Comp. 1.8 kΩ, 1/4W, 5%	Allen Bradley	CB1825	001101	3
R33, 36	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	Allen Bradley	CB3315	001090	2
R35, 39, 46, 53, 56, 63	Resistor, Carbon Comp. 100Ω, 1/4W, 5%	Allen Bradley	CB1015	001081	6
R38, 45	Resistor, Carbon Comp. 2.2 kΩ, 1/4W, 5%	Allen Bradley	CB2225	001103	2
R40, 54	Resistor, Carbon Comp. 2.7 kΩ 1/4W, 5%	Allen Bradley	CB2725	001105	2

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R42	Resistor, Carbon Comp. 120Ω, 1/4W, 5%	Allen Bradley	CB1215	001082	1
R43	Potentiometer, 200Ω	Beckman	62PR200	000934	1
R44	Resistor, Carbon Comp. 100Ω, 1/2W, 5%	Allen Bradley	EB1015	001172	1
R47, 48, 52, 60, 62	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	5
R49	Resistor, Carbon Comp. 27Ω, 1/4W, 5% (nom.)	Allen Bradley	CB2705	001072	1
R55	Resistor, Carbon Comp. 6.2Ω, 1/4W, 5%	Allen Bradley	CB62G5	003168	1
R57	Potentiometer, 100Ω	Beckman	62PR100	000927	1
R58	Resistor, Carbon Comp. 47Ω, 1/2W, 5%	Allen Bradley	EB4705	001166	1
R59	Resistor, Carbon Comp. 2.7Ω, 1/4W, 5%	Allen Bradley	CB27G5	003451	1
R61, 65	Resistor, Carbon Comp. 22Ω, 1/4W, 5%	Allen Bradley	CB2205	001071	2
R67	Not Used				
R70	Resistor, Carbon Comp. 82Ω, 1/4W, 5%	Allen Bradley	CB8205	001080	1
T1	Transformer	EE	A-45-06530	046530	1

PARTS LIST

FREQUENCY SYNTHESIZER P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Frequency Synthesizer	EE	D-32-06382	046382	1
C1, 5, 6, 8, 15, 17, 25, 26, 29, 31, 37	Capacitor, Ceramic Disc. .005 μF, 100 wvdc	Sprague	TG-D50	000150	11
C2, 21, 23	Capacitor, Dipped Mica 150 pF, 500 wvdc	Sangamo	D155F151JO	000084	3
C3	Capacitor, Variable 7-25 pF	Erie	7-25B	000350	1
C4	Capacitor, Dipped Mica 10 pF, 500 wvdc	Sangamo	D155C100JO	000034	1
C7, 16, 27, 38	Capacitor, Ceramic Disc .01 μF, 100 wvdc	Sprague	TG-S10	000158	4
C9	Capacitor, Dipped Mica 22 pF, 500 wvdc	Sangamo	D155E220JO	000050	1
C10	Capacitor, Variable 3-15 pF	Erie	3-15D	003039	1
C11, 13	Capacitor, Mylar .1 μF, 200 wvdc	IMB	XP2C104	003018	2
C12, 14	Capacitor, Electrolytic 10 μF, 16 wvdc	Sprague	TE1155	000267	2
C18, 19	Capacitor, Dipped Mica 270 pF, 500 wvdc	Sangamo	D155F271JO	000091	2
C20, 24	Capacitor, Dipped Mica 33 pF, 500 wvdc	Sangamo	D155E330JO	000059	2
C22	Capacitor, Dipped Mica 180 pF, 500 wvdc	Sangamo	D155F181JO	000087	1
C28	Capacitor, Dipped Mica 100 pF, 500 wvdc	Sangamo	D155F101JO	000079	1
C30	Capacitor, Electrolytic .22 μF, 20 wvdc	Sprague	150D224X0020A2	000225	1
C32	Capacitor, Electrolytic 27 μF, 10 wvdc	Sprague	150D276X9010B2	003486	1
C33, 36	Capacitor, Dipped Mica 12 pF, 500 wvdc	Sangamo	D155C120JO	000035	2
C34, 35	Capacitor, Dipped Mica 47 pF, 500 wvdc	Sangamo	D155E470JO	000065	2
C39	Capacitor, Dipped Mica 82 pF, 500 wvdc	Sangamo	D155F820JO	000074	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
CR1-4, 10-13	Diode, HPA2800	HP	HPA2800	003067	8
CR5-8, 14	Diode, 1N4152	ITT	1N4152	000564	5
CR9, 15	Diode, Zener, 1N751A	Motorola	1N751A	000529	2
L1, 2	Inductor, 100 μH	Delevan	1025-68	000682	2
L3, 6	Inductor, 2.2 μH	Delevan	1025-28	000661	2
L4, 5	Inductor, 4.7 μH	Delevan	1025-36	000665	2
L7, 9	Inductor, 0.82 μH	Delevan	1025-18	000656	2
L8	Inductor, 1.2 μH	Delevan	1025-22	000658	1
MC1	Micromodule, MC3062P Dual J-K Flip-flop	Motorola	MC3062P	003116	1
Q1-8, 10, 12	Transistor, 2N3640	Fairchild	2N3640	001728	10
Q9, 11, 13	Transistor, 2N3646	Fairchild	2N3646	001731	3
R1, 7, 13, 17	Resistor, Carbon Comp. 3.9k, 1/4W, 5%	Allen Bradley	CB3925	001108	4
R2, 8	Resistor, Carbon Comp. 56Ω, 1/4W, 5%	Allen Bradley	CB5605	001077	2
R3, 9, 39, 43	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001092	4
R4, 10, 11, 16, 29, 33	Resistor, Carbon Comp. 820Ω, 1/4W, 5%	Allen Bradley	CB8215	001097	6
R5, 6	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	Allen Bradley	CB3315	001090	2
R12, 18	Resistor, Carbon Comp. 68Ω, 1/4W, 5%	Allen Bradley	CB6805	001079	2
R14, 25	Resistor, Carbon Comp. 180Ω, 1/4W, 5%	Allen Bradley	CB1815	001084	2
R15	Resistor, Carbon Comp. 390Ω, 1/4W, 5%	Allen Bradley	CB3915	001091	1
R19, 21, 22, 23	Resistor, Carbon Comp. 51Ω, 1/4W, 5%	Allen Bradley	CB5105	001076	4
R20	Potentiometer, 500Ω	Bourns	3305W-1-501	003487	1
R24, 27, 35, 41, 42	Resistor, Carbon Comp. 1kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	5
R26, 44	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen	CB3325	001107	2
R28, 34	Resistor, Carbon Comp. 2.2 kΩ, 1/4W, 5%	Allen Bradley	CB2225	001103	2
R30	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	Allen Bradley	CB2215	001086	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
R31	Resistor, Carbon Comp. 15Ω, 1/4W, 5%	Allen Bradley	CB1505	001069	1
R32	Resistor, Carbon Comp. 82Ω, 1/4W, 5%	Allen Bradley	CB8205	001080	1
R36	Resistor, Carbon Comp. 27Ω, 1/4W, 5%	Allen Bradley	CB2705	001072	1
R37	Resistor, Carbon Comp. 680Ω, 1/4W, 5%	Allen Bradley	CB6815	001096	1
R38	Resistor, Carbon Comp. 220Ω, 1/2W, 5%	Allen Bradley	EB2215	001178	1
R40	Resistor, Carbon Comp. 22Ω, 1/4W, 5%	Allen Bradley	CB2205	001071	1
T1, 2, 3, 5, 6, 7	Transformer	Pac. Inst	T1398	003251	6
T4	Transformer	EE	A-45-06527	046527	1

PARTS LIST

INPUT SAMPLER P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Input Sampler	EE	D-32-06384	046384	1
C1, 2, 5, 14, 17, 18, 21, 22, 25, 26, 28, 29	Capacitor, Electrolytic .22 μF, 20 wvdc	Sprague	150D224X0020A2	000225	12
C3, 6	Capacitor, Fixed Mica 10 pF, 500 wvdc	Stackpole	GA Series	003005	2
C4, 13	Capacitor, Dipped Mica 68 pF, 500 wvdc	Sangamo	D155F680JO	000070	2
C7, 12	Capacitor, Dipped Mica 47 pF, 500 wvdc	Sangamo	D155E470JO	000065	2
C8, 15, 16, 19, 38, 40, 43	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	7
C9, 10	Capacitor, Ceramic Disc. .001 μF, 1000 wvdc	Centralab	DD-102	000117	2
C11, 41, 46	Capacitor, Ceramic Disc. .005 μF, 100 wvdc	Sprague	TG-D50	000150	3
C20, 23, 24, 27, 39	Capacitor, Ceramic Disc. .002 μF, 500 wvdc	Erie	X5F0-202K	003011	5
C30	Capacitor, Mylar .01 μF, 200 wvdc	ECI	215B1C103M2	000161	1
C31, 32, 33, 34, 44	Capacitor, Electrolytic 2.2 μF, 20 wvdc	Sprague	150D225X9020A2	000257	5
C35	Capacitor, Ceramic .22 μF, 50 wvdc	Sprague	5C023224X0500B3	000221	1
C36, 42, 45	Capacitor, Mylar .1 μF, 200 wvdc	IMB	XP2C104	003018	3
C37	Capacitor, Dipped Mica 100 pF, 500 wvdc	Sangamo	D155F101JO	000079	1
CR1-4	Diode, Matched Set	EE	A-61-06529	046529	4
CR5	Diode, Snap	Micro Assoc.	MA-4B200	003052	1
CR6, 8, 9-12	Diode, 1N4152	ITT	1N4152	000564	6
CR7	Diode, HPA2800	HP	HPA2800	003067	1
J1	Connector	Sealectro	51-051-0000	003432	1
L1	Inductor, 68 μH	Delevan	1025-64	000680	1
L2, 8, 9	Inductor, 33 μH	Delevan	1537-52	000711	3

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
L5, 6	Inductor, .22 μH	Delevan	1025-04	000649	2
L7	Inductor, 1 μH	Delevan	1025-20	000657	1
MC1	Micromodule, MC789P Hex Inverter	Motorola	MC789P	000862	1
Q1	Transistor, MPF105	Motorola	MPF105	003275	1
Q2, 6, 7, 8	Transistor, 2N3646	Fairchild	2N3646	001731	4
Q3, 4	Transistor, 2N4275	Fairchild	2N4275	003269	2
Q5	Transistor, 2N2369	Fairchild	2N2369	001710	1
Q9, 10	Transistor, 2N3640	Fairchild	2N3640	001728	2
R1-4	Resistor, Carbon Comp. 51 Ω, 1/8W, 5%	Allen Bradley	BB5105	001042	4
R5, 6	Resistor, Carbon Comp. 180 kΩ, 1/4W, 5%	Allen Bradley	CB1845	001134	2
R7, 11	Resistor, Carbon Comp. 180 Ω, 1/4W, 5%	Allen Bradley	CB1815	001084	2
R8, 38	Resistor, Carbon Comp. 15 kΩ, 1/4W, 5%	Allen Bradley	CB1535	001118	2
R9, 24, 31, 35, 44	Resistor, Carbon Comp. 10 kΩ, 1/4W, 5%	Allen Bradley	CB1035	001116	5
R10, 25, 29, 37, 40, 50	Resistor, Carbon Comp. 100Ω, 1/4W, 5%	Allen Bradley	CB1015	001081	6
R12, 19, 43, 45, 48	Resistor, Carbon Comp. 2.7 kΩ, 1/4W, 5%	Allen Bradley	CB2725	001105	5
R13	Resistor, Carbon Comp. 560Ω, 1/4W, 5%	Allen Bradley	CB5615	001094	1
R14, 15	Resistor, Carbon Comp. 100Ω, 1/8W, 5%	Allen Bradley	BB1015	001044	2
R16	Resistor, Carbon Comp. 27Ω, 1/4W, 5%	Allen Bradley	CB2705	001072	1
R17, 18	Resistor, Carbon Comp. 270Ω, 1/4W, 5%	Allen Bradley	CB2715	001088	2
R20	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001092	1
R21, 52	Resistor, Carbon Comp. 1.2 kΩ, 1/4W, 5%	Allen Bradley	CB1225	001099	2
R22	Potentiometer, 500Ω	Bourns	3305W-1-501	003487	1
R23	Resistor, Carbon Comp. 270Ω, 1W, 5%	Allen Bradley	GB2715	001280	1
R26, 33, 53	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	3
R27	Resistor, Carbon Comp. 47Ω, 1/4W, 5%	Allen Bradley	CB4705	001075	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
R28, 46	Resistor, Carbon Comp. 18 kΩ, 1/4W, 5%	Allen Bradley	CB1835	001119	2
R30, 41	Resistor, Carbon Comp. 82Ω, 1/4W, 5%	Allen Bradley	CB8205	001080	2
R32	Resistor, Carbon Comp. 5.6 kΩ, 1/4W, 5%	Allen Bradley	CB5625	001111	1
R34	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	1
R36	Resistor, Carbon Comp. 10Ω, 1/4W, 5%	Allen Bradley	CB1005	001067	1
R39	Resistor, Carbon Comp. 12 kΩ, 1/4W, 5%	Allen Bradley	CB1235	001117	1
R42	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	1
R47	Resistor, Carbon Comp. 3.9 kΩ, 1/4W, 5%	Allen Bradley	CB3925	001108	1
R49	Resistor, Carbon Comp. 1.8 kΩ, 1/4W, 5%	Allen Bradley	CB1825	001101	1
R51	Resistor, Carbon Comp. 22 kΩ, 1/4W, 5%	Allen Bradley	CB2235	001120	1
T1	Transformer	EE	A-45-06528	046528	1

PARTS LIST

PARITY AND PHASE SHIFTER P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Parity and Phase Shifter	EE	D-32-06380	046380	1
C1, 8	Capacitor, Ceramic Disc. .002 μF, 1000 wvdc	Centralab	DD-202	000127	2
C2, 4, 5, 9	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	4
C3, 12, 15	Capacitor, Dipped Mica 470 pF, 500 wvdc	Sangamo	D155F471JO	000102	3
C6, 21	Capacitor, Mylar .1 μF, 200 wvdc	Amperex	C280AE/P100K	000211	2
C7	Capacitor, Ceramic Disc. .005 μF, 100 wvdc	Sprague	TG-D50	000150	1
C10, 14	Capacitor, Dipped Mica 1000 pF, 500 wvdc	Sangamo	D155F102JO	000110	2
C11	Capacitor, Dipped Mica 2000 pF, 500 wvdc	Sangamo	D195F202JO	003342	1
C13	Capacitor, Dipped Mica 82 pF, 500 wvdc	Sangamo	D155F820JO	000074	1
C16	Capacitor, Dipped Mica 10 pF, 500 wvdc	Sangamo	D155C100JO	000034	1
C17	Capacitor, Dipped Mica 4000 pF, 2%, 500 wvdc	Sangamo	D195F402GO	003012	1
C18, 19, 20	Capacitor, Dipped Mica 2000 pF, 2%, 500 wvdc	Sangamo	D195F202GO	000128	3
C22, 23	Capacitor, Electrolytic 10 μF, 16 wvdc	Sprague	TE1155	000267	2
CR1-3	Diode, 1N695	Sylvania	1N695	000523	3
MC1, 7	Micromodule, MC890P Dual J-K Flip-flop	Motorola	MC890P	000875	2
MC2, 8, 12	Micromodule, MC817P Quad 2-Input Gate	Motorola	MC817P	000868	3
MC3, 10	Micromodule, CμL 9958 Decade Counter	Fairchild	CμL 9958	003101	2
MC4	Micromodule, MC871P Quad Exclusive OR Gate	Motorola	MC871P	003456	1
MC5	Micromodule, MC825P Dual 4-Input Gate	Motorola	MC825P	003452	1
MC6, 9	Micromodule, MC824P Quad 2-Input Gate	Motorola	MC824P	000871	3

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
MC13	Micromodule, MC1437L Dual Operational Amplifier	Motorola	MC1437L	003115	1
Q1-4	Transistor, 2N3646	Fairchild	2N3646	001731	4
R1, 2, 3, 7-10, 21	Resistor, Carbon Comp. 560Ω, 1/4W, 5%	Allen Bradley	CB5615	001094	8
R4, 18, 27	Resistor, Carbon Comp. 680Ω, 1/4W, 5%	Allen Bradley	CB6815	001096	3
R5, 6, 26	Resistor, Carbon Comp. 2.7 kΩ, 1/4W, 5%	Allen Bradley	CB2725	001105	3
R11	Resistor, Carbon Comp. 820Ω, 1/4W, 5%	Allen Bradley	CB8215	001097	1
R12, 29, 36, 46, 47	Resistor, Carbon Comp. 10 kΩ, 1/4W, 5%	Allen Bradley	CB1035	001116	5
R13	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	1
R14, 34, 35	Resistor, Carbon Comp. 1.5 kΩ, 1/4W, 5%	Allen Bradley	CB1525	001100	3
R15, 20	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	2
R16, 17	Resistor, Carbon Comp. 33Ω, 1/4W, 5%	Allen Bradley	CB3305	001073	2
R19	Resistor, Carbon Comp. 3.9 kΩ, 1/4W, 5%	Allen Bradley	CB3925	001108	1
R22, 24, 43, 44	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001092	4
R23	Resistor, Carbon Comp. 390Ω, 1/4W, 5%	Allen Bradley	CB3915	001091	1
R25	Resistor, Carbon Comp. 2.2 kΩ, 1/4W, 5%	Allen Bradley	CB2225	001103	1
R28, 42, 45	Resistor, Carbon Comp. 1.2 kΩ, 1/4W, 5%	Allen Bradley	CB1225	001099	3
R30	Resistor, Carbon Comp. 27 kΩ, 1/4W, 5%	Allen Bradley	CB2735	001121	1
R31	Resistor, Carbon Comp. 68 kΩ, 1/4W, 5%	Allen Bradley	CB6835	001127	1
R32	Resistor, Carbon Comp. 100 kΩ, 1/4W, 5%	Allen Bradley	CB1045	001131	1
R33	Resistor, Carbon Comp. 33 kΩ, 1/4W, 5%	Allen Bradley	CB3335	001122	1
R37	Resistor, Metallic Film 15.8 kΩ, 1/4W, 1%	IRC	RN60B1582F	003458	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
R38	Resistor, Carbon Comp. 390 kΩ, 1/4W, 5%	Allen Bradley	CB3945	001140	1
R39,40	Resistor, Metallic Film 16.5 kΩ, 1/4W, 1%	IRC	RN60B1652F	003459	2
R41	Resistor, Metallic Film 8.25 kΩ, 1/4W, 1%	IRC	RN60B8251F	003457	1

PARTS LIST

TIME BASE P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Time Base	EE	D-32-06618	046618	1
C1, 3	Capacitor, Dipped Mica 270 pF, 500 wvdc	Sangamo	D155F271JO	000091	2
C2, 4	Not used				
C5	Capacitor, Dipped Mica 470 pF, 500 wvdc	Sangamo	D155F471JO	000102	1
C6	Capacitor, Dipped Mica 150 pF, 500 wvdc	Sangamo	D155F151JO	000084	1
CR1, 2	Diode, 1N695	Sylvania	1N695	000523	2
MC1, 3, 4, 5	Micromodule, MC817P Quad 2-Input Gate	Motorola	MC817P	000868	4
MC2, 6, 10	Micromodule, MC824P Quad 2-Input Gate	Motorola	MC824P	000871	3
MC7, 8, 11-18	Micromodule, CμL 9958 Decade Counter	Fairchild	CμL 9958	003101	10
MC9	Micromodule, MC886P Dual 4-Input Expander	Motorola	MC886P	003100	1
MC19-20	Micromodule, MC9721P Quad 2-Input Expander	Motorola	MC9721P	003114	2
Q1-5	Transistor, 4-1007	CDC	4-1007	001759	5
Q6-10	Transistor, 2N3646	Fairchild	2N3646	001731	5
R1-5, 21, 24	Resistor, Carbon Comp. 1.5 kΩ, 1/4W, 5%	Allen Bradley	CB1525	001100	7
R6, 23	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	Allen Bradley	CB2215	001086	2
R7, 11, 27, 28	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	4
R8	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	1
R9, 15, 25	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	3
R10	Resistor, Carbon Comp. 5.6 kΩ, 1/4W, 5%	Allen Bradley	CB5625	001111	1
R12, 29	Resistor, Carbon Comp. 2.7 kΩ, 1/4W, 5%	Allen Bradley	CB2725	001105	2
R13	Resistor, Carbon Comp. 2.2 kΩ, 1/4W, 5%	Allen Bradley	CB2225	001103	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty
R14,22	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	2
R16	Not Used				
R17	Resistor, Carbon Comp. 680Ω, 1/4W, 5%	Allen Bradley	CB6815	001096	1
R18, 19	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001090	2
R20	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	Allen Bradley	CB3315	001090	1
R26	Resistor, Carbon Comp. 1.2 kΩ, 1/4W, 5%	Allen Bradley	CB1225	001099	1
R30	Resistor, Carbon Comp. 820 Ω, 1/4W, 5%	Allen	CB8215	001097	1

PARTS LIST

RESET AND CONTROL P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Reset and Control	EE	D-32-06680	046680	1
C1, 15, 18	Capacitor, Ceramic Disc. .02 μF, 100 wvdc	Sprague	TG-S20	000176	3
C2, 4	Capacitor, Electrolytic 5 μF, 16 wvdc	Sprague	TE1152	003026	2
C3, 19	Capacitor, Mylar .1 μF, 200 wvdc	Amperex	C280AE/P100K	000211	2
C5, 6, 8, 9, 10	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	5
C7	Capacitor, Dipped Mica 2000 pF, 500 wvdc	Sangamo	D195F202JO	003342	1
C11	Capacitor, Dipped Mica 270 pF, 500 wvdc	Sangamo	D155F271JO	000091	1
C12	Capacitor, Ceramic Disc. .001 μF, 1000 wvdc	Centralab	DD-102	000115	1
C13	Capacitor, Dipped Mica 390 pF, 500 wvdc	Sangamo	D155F391JO	000100	1
C14	Capacitor, Ceramic Disc. .005 μF, 100 wvdc	Sprague	TG-D50	000150	1
C16	Capacitor, Dipped Mica 100 pF, 500 wvdc	Sangamo	D155F101JO	000079	1
C17	Capacitor, Ceramic Disc. .002 μF, 1000 wvdc	Centralab	DD-202	000127	1
CR1-5	Diode 1N695	Sylvania	1N695	000523	5
MC1	Micromodule MC3062P Dual J-K Flip-flop	Motorola	MC3062P	003116	1
MC2	Micromodule MC889P Hex Inverter	Motorola	MC889P	000874	1
MC3	Micromodule MC893P Triple 3-Input Gate	Motorola	MC893P	000877	1
MC4	Micromodule MC817P Quad 2-Input Gate	Motorola	MC817P	000868	1
MC5, 6	Micromodule MC824P Quad 2-Input Gate	Motorola	MC824P	000871	2
Q1, 7, 10	Transistor, 2N3702	TI	2N3702	001733	3
Q2, 3, 11	Transistor, 2N3640	Fairchild	2N3640	001728	3
Q4	Transistor, 2N3569	Fairchild	2N3569	001724	1
Q5	Transistor, TIS43	TI	TIS43	001751	1

PARTS LIST

120 MHz DCU P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	120 MHz DCU	EE	D-32-06839	046839	1
C1, 2	Capacitor, Electrolytic 5 μF, 16 wvdc	Sprague	TE1152	003026	2
C3	Capacitor, Dipped Mica 470 pF, 500 wvdc	Sangamo	D155F471JO	000102	1
C4, 13, 15, 18	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	4
C5, 8, 14	Capacitor, Ceramic .1 μF, 25 wvdc	Sprague	3C023104X0250A3	000200	3
C6, 9, 11, 12	Capacitor, Dipped Mica 22 pF, 500 wvdc	Sangamo	D155E220JO	000050	4
C7	Capacitor, Electrolytic 2500 μF, 2.5 wvdc	Amperex	C437AR/A2500	003034	1
C10	Capacitor, Dipped Mica 330 pF, 500 wvdc	Sangamo	D155F331JO	000095	1
C16	Capacitor, Mylar .01 μF, 200 wvdc	ECI	215B1C103M2	000161	1
C17	Capacitor, Dipped Mica 100 pF, 500 wvdc	Sangamo	D155F101JO	000079	1
CR1	Diode, Zener, 1N746A	Motorola	1N746A	001731	1
CR2-12	Diode, 1N3605	Sylvania	1N3605	000550	11
J1	Connector	Sealectro	51-051-0000	003432	1
L1	Inductor, 1 μH	Delevan	1025-20	000657	1
L2, 3	Inductor, 1 μH	Delevan	1537-12	000690	2
MC1	Micromodule, MC817P Quad 2-Input Gate	Motorola	MC817P	000868	1
MC2	Micromodule, MC1018P MECL-to-Saturated Logic	Motorola	MC1018P	003110	1
MC3, 4, 5	Micromodule, MC1013P J-K Flip-flop	Motorola	MC1013P	003105	3
MC6	Micromodule, MC1034P Type D Flip-flop	Motorola	MC1034P	003596	1
MC7	Micromodule, MC1023P Dual 4-Input Clock Driver	Motorola	MC1023P	003111	1
MC8	Micromodule, MC1004P Dual 4-Input OR/NOR Gate	Motorola	MC1004P	003109	1
MC9	Micromodule, MC824P Quad 2-Input Gate	Motorola	MC824P	000871	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
R27	Resistor, Carbon Comp. 33Ω, 1/4W, 5%	Allen Bradley	CB3305	001073	1
R28, 39	Resistor, Carbon Comp. 510Ω, 1/4W, 5%	Allen Bradley	CB5115	001093	2
R32, 44, 58, 60	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	4
R40, 51, 57, 59	Resistor, Carbon Comp. 10 kΩ, 1/4W, 5%	Allen Bradley	CB1035	001116	4
R41	Resistor, Carbon Comp. 100Ω, 1/4W, 5%	Allen Bradley	CB1015	001081	1
R42	Resistor, Carbon Comp. 390Ω, 1/4W, 5%	Allen Bradley	CB3915	001091	1
R43	Resistor, Carbon Comp. 2 kΩ, 1/4W, 5%	Allen Bradley	CB2025	001102	1
R47	Resistor, Carbon Comp. 150Ω, 1/4W, 5%	Allen Bradley	CB1515	001083	1
R49	Resistor, Carbon Comp. 270Ω, 1/4W, 5%	Allen Bradley	CB2715	001088	1
R50, 53, 54	Resistor, Carbon Comp. 22kΩ, 1/4W, 5%	Allen Bradley	CB2235	001120	3
R52, 56	Resistor, Carbon Comp. 1.5 kΩ, 1/4W, 5%	Allen Bradley	CB1525	001100	2
R55	Resistor, Carbon Comp. 5.1 kΩ, 1/4W, 5%	Allen Bradley	CB5125	001110	1
R61	Resistor, Carbon Comp. 2.2 kΩ, 1/4W, 5%	Allen Bradley	CB2225	001103	1

PARTS LIST

12 MHz DCU P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	12 MHz DCU	EE	D-32-06368	046368	1
MC1, 4	Micromodule, CμL 9960 Decimal Decoder	Fairchild	CμL 9960	003103	2
MC2, 5	Micromodule, CμL 9959 Buffer Register	Fairchild	CμL 9959	003102	2
MC3	Micromodule, MC826P J-K Flip-flop	Motorola	MC826P	000872	1
MC6	Micromodule, MC880P Decade Counter	Motorola	MC880P	003293	1
Q1-Q8	Transistor, 2N4123	Motorola	2N4123	003266	8
R1, 5, 9, 12, 14, 18, 22, 25	Resistor, Carbon Comp. 10Ω, 1/4W, 5%	Allen Bradley	CB1005	001067	8
R2, 4, 8, 10, 15, 17, 21, 23	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	8
R3, 6, 7, 11, 16, 19, 20, 24	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	8
R13, 26, 27, 28	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	4

PARTS LIST

DUAL DCU P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Dual DCU	EE	D-32-06366	046366	1
MC1, 4	Micromodule, CμL 9960 Decimal Decoder	Fairchild	CμL 9960	003103	2
MC2, 5	Micromodule, CμL 9959 Buffer Register	Fairchild	CμL 9959	003102	2
MC3, 6	Micromodule, MC880P Decade Counter	Motorola	MC880P	003293	2
Q1-8	Transistor, 2N4123	Motorola	2N4123	003266	8
R1, 5, 11, 14, 19, 23, 31, 34	Resistor, Carbon Comp. 10Ω, 1/4W, 5%	Allen Bradley	CB1005	001067	8
R2, 4, 10, 12, 20, 22, 29, 32	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	8
R3, 6, 9, 13, 21, 24, 30, 33	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	8
R7, 8	Resistor, Carbon Comp. 4.7Ω, 1/4W, 5%	Allen Bradley	CB47G5	001066	2
R15-18, 25-28	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	8

PARTS LIST

DCU P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	DCU	EE	D-32-06364	046364	1
MC1	Micromodule, CμL 9960 Decimal Decoder	Fairchild	CμL 9960	003103	1
MC2	Micromodule, CμL 9959 Buffer Register	Fairchild	CμL 9959	003102	1
MC3	Micromodule, MC880P Decade Counter	Motorola	MC880P	003293	1
Q1-4	Transistor, 2N4123	Motorola	2N4123	003266	4
R1, 5, 14, 17	Resistor, Carbon Comp. 10Ω, 1/4W, 5%	Allen Bradley	CB1005	001067	4
R2, 4, 15, 18	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	4
R3, 6, 13, 16	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	4
R7, 8	Resistor, Carbon Comp. 4.7Ω, 1/4W, 5%	Allen Bradley	CB47G5	001066	2
R9-12	Resistor, Carbon Comp. 4.7 kΩ, 1/4W, 5%	Allen Bradley	CB4725	001109	4

PARTS LIST

PRESET OFFSET P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Preset Offset	EE	C-33-06620	046620	1
DS1, 2	Lamp, Neon	Chicago Lamp	NE83	003506	2
MC1	Not Used				
MC2, 3, 11	Micromodule, MC889P Hex Inverter	Motorola	MC889P	000874	3
MC4, 8, 13, 14, 16, 18, 19, 20, 21	Micromodule, MC817P Quad 2-Input Gate	Motorola	MC817P	000868	9
MC5, 9, 12, 15, 17	Micromodule, MC893P Triple 3-Input Gate	Motorola	MC893P	000877	5
MC6	Micromodule, MC819P Dual 4-Input Gate	Motorola	MC819P	000870	1
MC7	Micromodule, MC824P Quad 2-Input Gate	Motorola	MC824P	000871	1
MC10	Micromodule, MC825P Dual 4-Input Gate	Motorola	MC825P	003452	1
Q1, 2, 5, 6	Transistor, 4-1007	CDC	4-1007	001759	4
Q3, 4	Transistor, 2N4124	Motorola	2N4124	003294	2
Q7	Transistor, 2N3646	Fairchild	2N3646	001731	1
R1-5, 12-21	Resistor, Carbon Comp. 1.8 kΩ, 1/4W, 5%	Allen Bradley	CB1825	001101	15
R6-9, 23	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	5
R10, 11	Resistor, Carbon Comp. 10 kΩ, 1/4W, 5%	Allen Bradley	CB1035	001116	2
R22	Resistor, Carbon Comp. 270Ω, 1/4W, 5%	Allen Bradley	CB2715	001088	1

PARTS LIST

OSCILLATOR P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Oscillator	EE	C-33-05262	045262	1
C1	Capacitor, Variable 1-12 pF	JFD	VC58G	003042	1
C2	Capacitor, Ceramic 22 pF, 500 wvdc	Mucon	1U22RK	003067	1
C3	Capacitor, Dipped Mica (osc. trim as required)	Sangamo	Type D15		1
C4	Capacitor, Dipped Mica 560 pF, 500 wvdc	Sangamo	D155F561JO	000104	1
C5	Capacitor, Dipped Mica 470 pF, 500 wvdc	Sangamo	D155F471JO	000102	1
C6, 8	Capacitor, Mylar .1 μF, 200 wvdc	Amperex	C280AE/P100K	000211	2
C7	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	1
CR1	Diode, 1N695	Sylvania	1N695	000523	1
Q1, 2	Transistor, 2N2924	GE	2N2924	001716	2
R1	Resistor, Carbon Comp. 47 kΩ, 1/4W, 5%	Allen Bradley	CB4735	001124	1
R2, 5	Resistor, Carbon Comp. 47Ω, 1/4W, 5%	Allen Bradley	CB4705	001075	2
R3	Resistor, Carbon Comp. 2.7 kΩ, 1/4W, 5%	Allen Bradley	CB2725	001105	1
R4	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	1
Y1	Crystal, 1 MHz	Filtaire	CR-18/U	003049	1

PARTS LIST

REGULATOR P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Regulator	EE	D-32-06370	046370	1
C7, 8	Capacitor, Mylar .1 μF, 200 wvdc	Amperex	C280AE/P100K	000211	2
C9, 11	Capacitor, Electrolytic 10 μF, 16 wvdc	Sprague	TE1155	000267	2
C10	Capacitor, Electrolytic 50 μF, 12 wvdc	Sprague	TE1133	000295	1
CR7	Diode, Zener, 1N747A	Motorola	1N747A	000525	1
CR8	Diode, Zener, 1N749A	Motorola	1N749A	000527	1
CR9	Diode, Zener, 1N759A	Motorola	1N759A	000537	1
CR10	Diode, Zener, 1N753A	Motorola	1N753A	000531	1
CR11	Diode, 1N4001	ITT	1N4001	003062	1
Q5, 9, 12, 15	Transistor, 2N4125	Motorola	2N4125	001736	4
Q6, 8, 13	Transistor, 2N4123	Motorola	2N4123	003266	3
Q7	Transistor, 2N4890	Motorola	2N4890	003271	1
Q10	Transistor, 2N4126	Motorola	2N4126	003267	1
Q11, 14, 16, 17	Transistor, 2N4124	Motorola	2N4124	003294	4
R2	Resistor, Carbon Comp. 1.2 kΩ, 1/4W, 5%	Allen Bradley	CB1225	001099	1
R3	Resistor, Wire Wound .18Ω, 2W, 5%	IRC	Type BWH	003193	1
R4	Resistor, Carbon Comp. 180Ω, 1W, 5%	Allen Bradley	GB1815	001277	1
R5	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	Allen Bradley	CB4715	001092	1
R6	Resistor, Carbon Comp. 1.5Ω, 1/2W, 5%	Allen Bradley	EB15G5	003186	1
R7	Resistor, Metallic Film 2.32 kΩ, 1/4W, 1%	IRC	RN60D2321F	003450	1
R8, 27, 28	Resistor, Metallic Film 1.21 kΩ, 1/4W, 1%	IRC	RN60D1211F	003449	3
R9, 20	Resistor, Carbon Comp. 27 kΩ, 1/4W, 5%	Allen Bradley	CB2735	001121	2
R10	Resistor, Carbon Comp. 820Ω, 1/4W, 5%	Allen Bradley	CB8215	001097	1
R11	Resistor, Carbon Comp. 1.2Ω, 1/2W, 5%	Allen Bradley	EB12G5	003445	1

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
R12	Potentiometer, 100Ω	Beckman	62PR100	000926	1
R13	Resistor, Metallic Film 475Ω, 1/4W, 5%	IRC	RN60D4750F	003447	1
R14	Resistor, Metallic Film 634Ω, 1/4W, 5%	IRC	RN60D6340F	003448	1
R15, 17	Resistor, Carbon Comp. 390Ω, 1/4W, 5%	Allen Bradley	CB3915	001091	2
R16	Resistor, Carbon Comp. 6.8 kΩ, 1/4W, 5%	Allen Bradley	CB6825	001113	1
R18	Resistor, Carbon Comp. 820Ω, 1/2W, 5%	Allen Bradley	EB8215	001188	1
R19	Resistor, Carbon Comp. 15 kΩ, 1/4W, 5%	Allen Bradley	CB1535	001118	1
R21	Resistor, Carbon Comp. 22 kΩ, 1/4W, 5%	Allen Bradley	CB2235	001120	1
R22	Resistor, Carbon Comp. 22Ω, 1/4W, 5%	Allen Bradley	CB2205	001071	1
R25	Not Used				
R26	Resistor, Wire Wound .68Ω, 2W, 5%	IRC	Type BWH	003446	1

PARTS LIST

DISPLAY AND POWER SUPPLY P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Display and Power Supply	EE	D-33-06614	046614	1
C1	Capacitor, Electrolytic 2 μF, 350 wvdc	Mallory	TC595	003022	1
C2	Capacitor, Electrolytic 8000 μF, 12 wvdc	STM	91C12SH83	003036	1
C3, 4, 5, 6	Capacitor, Electrolytic 1000 μF, 25 wvdc	STM	23C25TS13	003032	4
CR1	Diode, 1N4005	ITT	1N4005	003063	1
CR2, 3	Diode, 1N4997	Motorola	1N4997	003324	2
CR4, 6	Rectifier, MDA-950A2	Motorola	MDA-950A2	003055	2
CR5	Rectifier, MDA-940A2	Motorola	MDA-940A2	003054	1
*CR12	Diode, Zener, 1N746A	Motorola	1N746A	000524	1
DS1-7	Tube, Indicator	National	NL-848	001772	7
J1-6	Connector, 22 pin	Cinch	252-22-30-160	003454	6
Q2	Transistor, MJE520	Motorola	MJE520	003274	1
Q3, 4, *18	Transistor, MJE370	Motorola	MJE370	003273	3
R1-7	Resistor, Carbon Comp. 47 kΩ, 1/2W, 5%	Allen Bradley	EB4735	001218	7
R8, 9	Not Used				
R10	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	Allen Bradley	CB 2215	001086	1
R11	Resistor, Carbon Comp. 1MΩ, 1/4W, 5%	Allen Bradley	CB1055	001145	1
*R23	Resistor, Wire Wound 5.6Ω, 2W, 5%	IRC	Type BWH	003663	1
*R24	Resistor, Carbon Comp. 470Ω, 1W, 5%	Allen Bradley	GB4715	001284	1
S6	Switch, DPDT	Cont. Wirt	G-126-PCT	001553	1

* Power supply components mounted on DAC adapter assembly.

PARTS LIST

INPUT AND LOGIC P.C. ASSEMBLY

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
C1	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	1
C2, 3	Capacitor, Electrolytic 10 μF, 16 wvdc	Sprague	TE1155	000267	2
J1-6	Connector, 22 pin	Cinch Jones	252-22-30-160	003454	6
R14	Resistor, Carbon Comp. 750Ω, 1/4W, 5% (nom.)	Allen Bradley	CB7515	003179	1
R15	Potentiometer, 500Ω	Beckman	62PR500	003487	1
S9, 10	Switch, DPDT	Cont. Wirt.	G-126-PCT	001553	2

PARTS LIST

INPUT POWER DIVIDER

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	Input Power Divider	EE	B-45-06686	046686	1
J1-4	Connector	Sealectro	51-051-0000	003432	4
R1, 2	Resistor, Carbon Comp. 56Ω, 1/2W, 5%	Allen Bradley	EB5605	001168	2
R3, 4	Resistor, Carbon Comp. 51Ω, 1/4W, 5%	Allen Bradley	CB5105	001076	2

PARTS LIST

DAC ADAPTER

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
Assembly	DAC Adapter	EE	B-33-06616	046616	1
J1	Connector, 22 pin	Amphenol	143-022-07	003047	1
J2	Connector, 22 pin	Cinch Jones	252-22-30-160	003505	1
Q1	Transistor, 2N3646	Fairchild	2N3646	001731	1
R1	Resistor, Carbon Comp. 1 kΩ, 1/4W, 5%	Allen Bradley	CB1025	001098	1
R2	Resistor, Carbon Comp. 3.3 kΩ, 1/4W, 5%	Allen Bradley	CB3325	001107	1

PARTS LIST

FRONT PANEL

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
DS10	Lamp, Gate	Dialco	507-3917	003089	1
DS11, 12, 13	Lamp, Annunciator	Chicago Min.	CM8-680	000806	3
J1	Connector, Type N	Sealectro	51-075-6701	003491	1
S1	Switch, Rotary, SPST	Arrow H & H	1561AS	003239	1
S3	Switch, Toggle, SPDT	C & K	7101	003242	1
S7, 8	Switch, Rotary, 12 position	CTS	T205	001579	2

PARTS LIST

REAR PANEL

Reference	Description	Mfgr.	Mfgr. No.	EE No.	Qty.
B1	Fan	Pamotor	8500	003068	1
C6	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	Sprague	TG-S10	000158	1
F1	Fuse, 1 Amp. SLO-BLO	Littel-Fuse	312001	000592	1
	Filter, RFI	Elect. Mag. Filter	P694-3	003070	1
J1	Connector, Type N	Sealectro	51-075-6701	003491	1
J2	Connector, 24 pin	Amphenol	MS3102A-24-28S	003043	1
Q1	Transistor, MJ480	Motorola	MJ480	001745	1
S2	Switch, DPDT	Switch-craft	46256LF	001588	1
T1	Transformer	Tranex	4-2297	003490	1

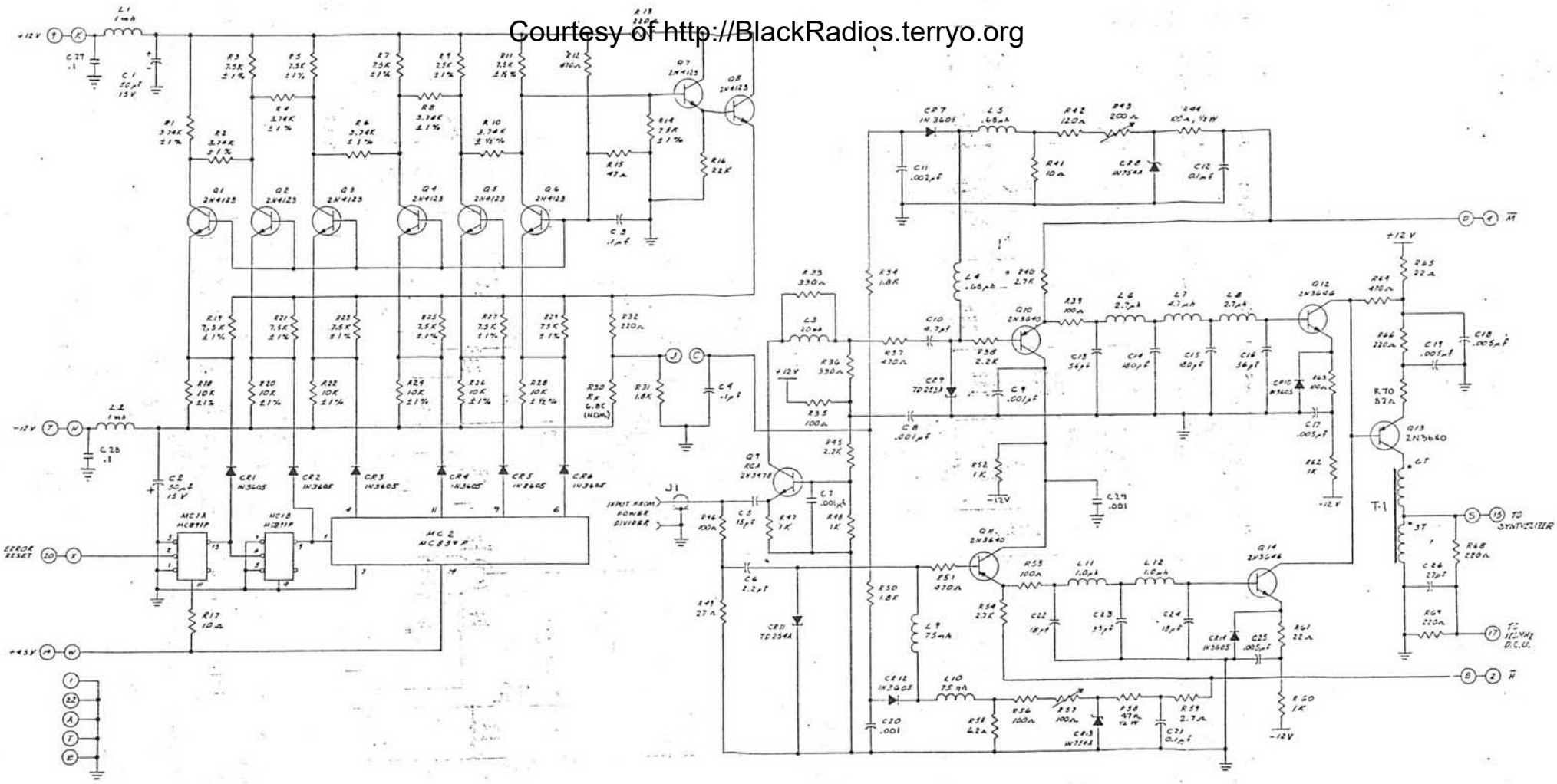


FIGURE 4-36 COUNTDOWN AND RAMP SCHEMATIC AND COMPONENT LOCATION D-11-06549

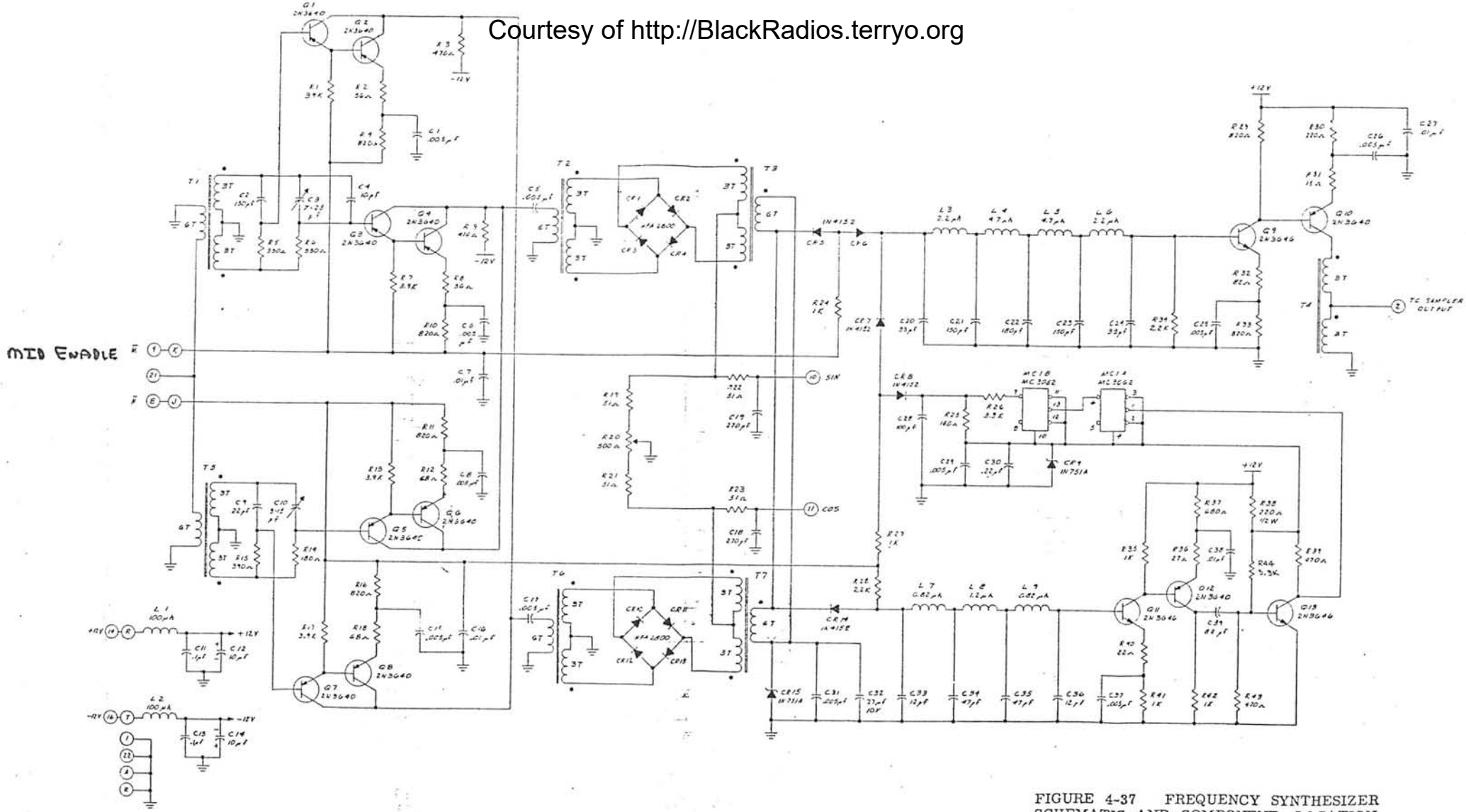
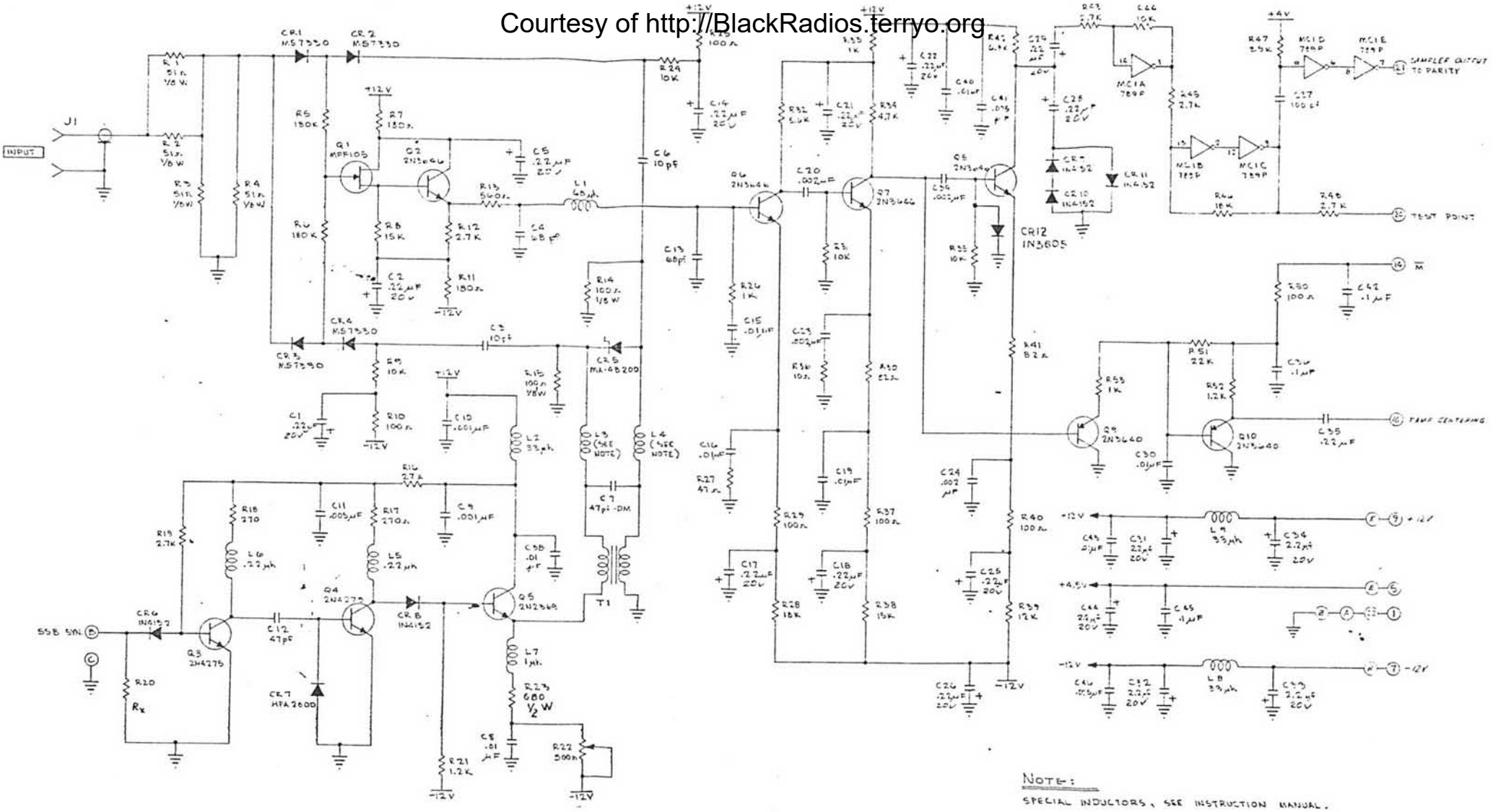


FIGURE 4-37 FREQUENCY SYNTHESIZER SCHEMATIC AND COMPONENT LOCATION D-11-06547



NOTE:
SPECIAL INDUCTORS, SEE INSTRUCTION MANUAL.

FIGURE 4-38 INPUT SAMPLER
SCHEMATIC AND COMPONENT LOCATION
D-11-06548

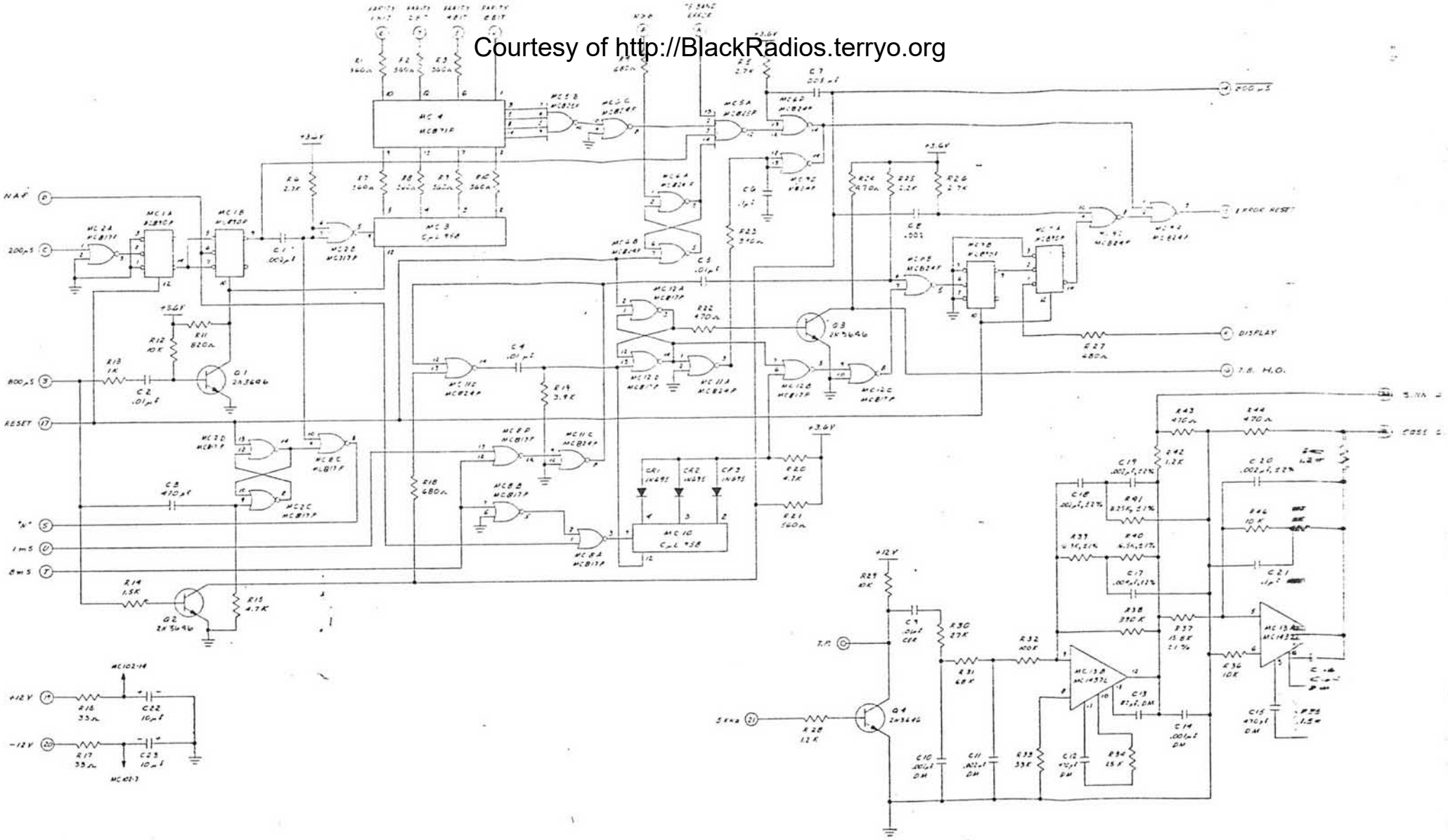


FIGURE 4-39 PARITY AND PHASE SHIFTER SCHEMATIC AND COMPONENT LOCATION D-11-06546

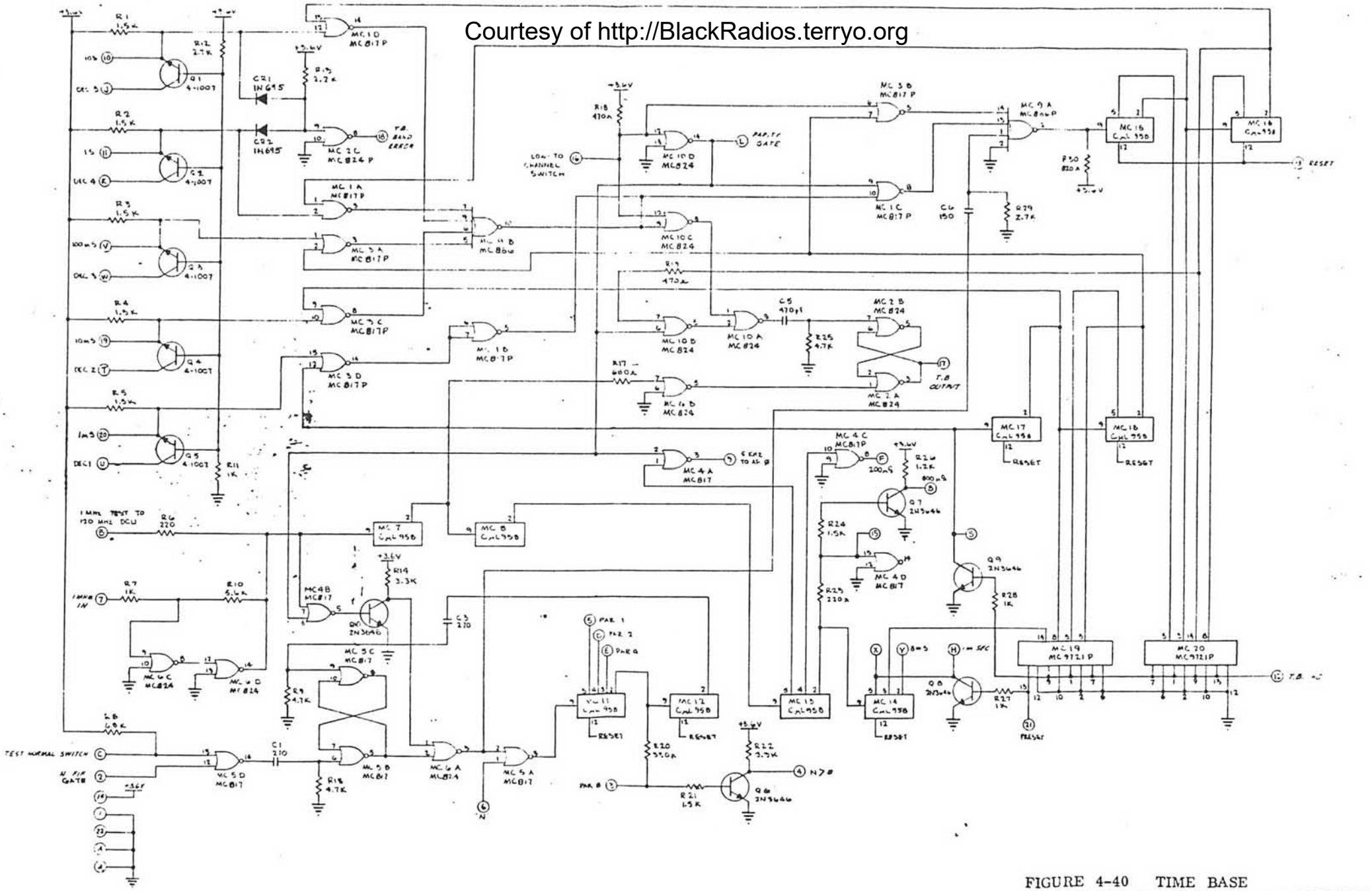


FIGURE 4-40 TIME BASE
SCHEMATIC AND COMPONENT LOCATION
D-11-06627

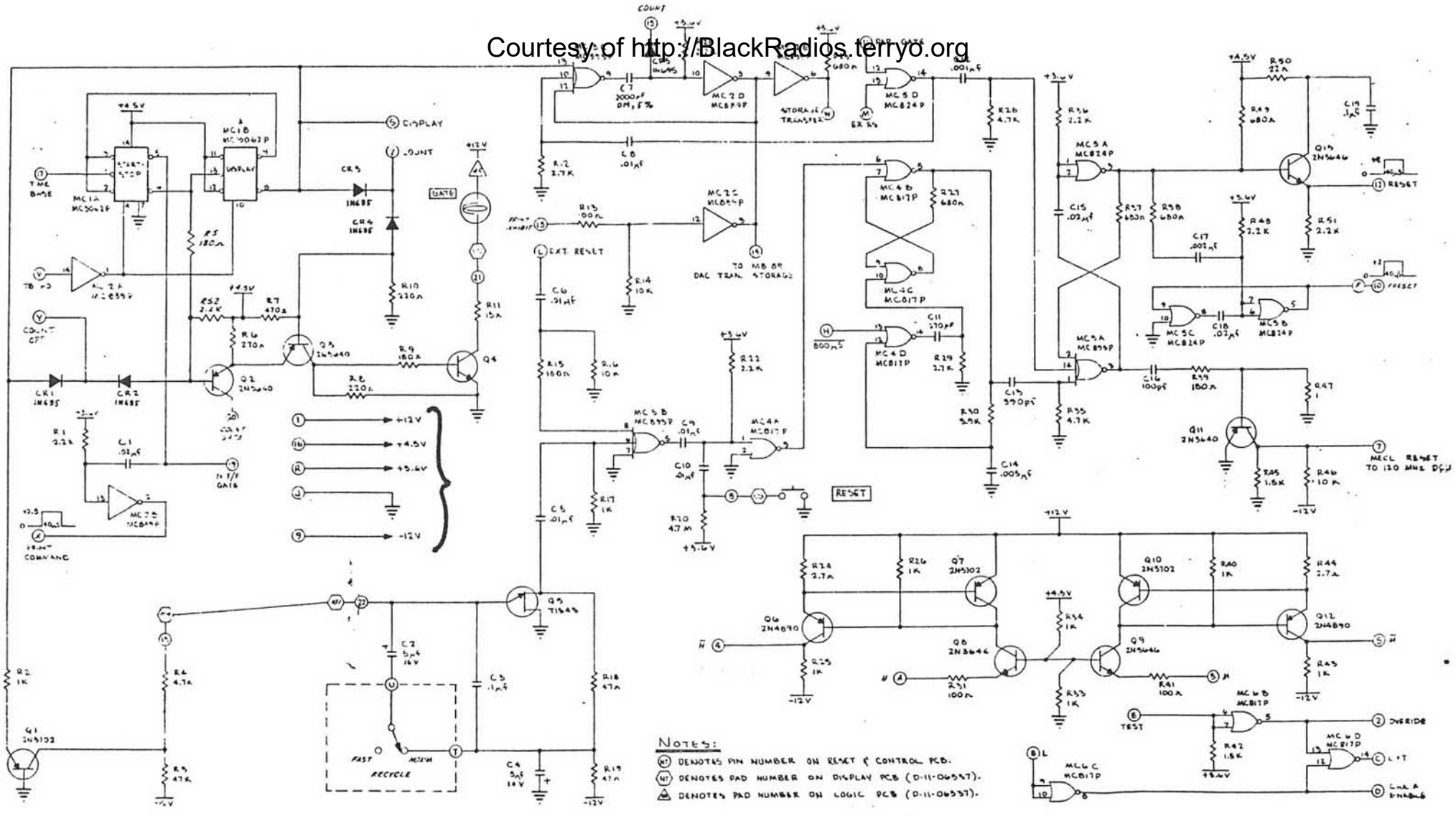


FIGURE 4-41 RESET AND CONTROL SCHEMATIC AND COMPONENT LOCATION D-11-06678

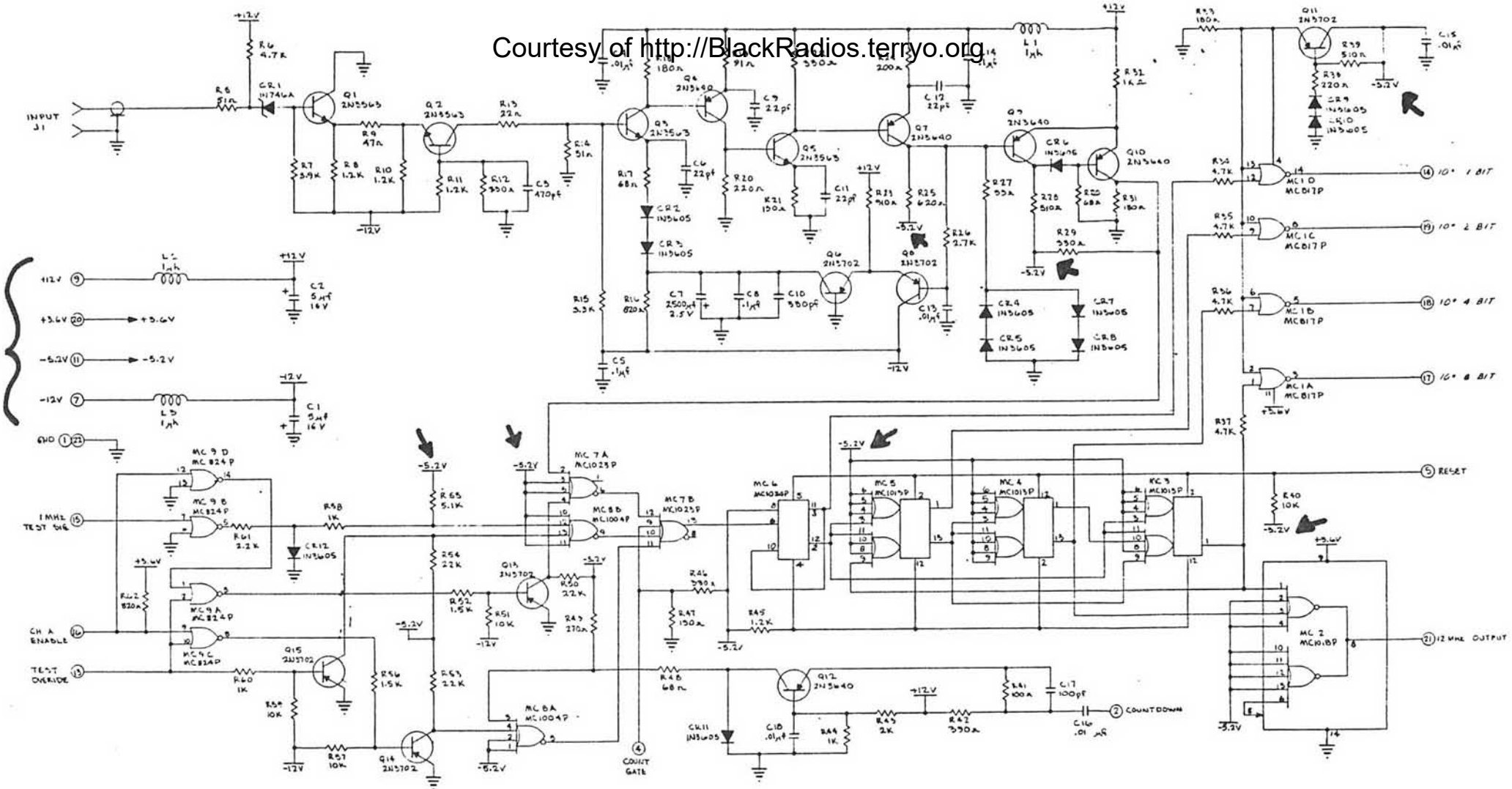


FIGURE 4-42 120 MHz DCU
SCHEMATIC AND COMPONENT LOCATION
D-11-06838

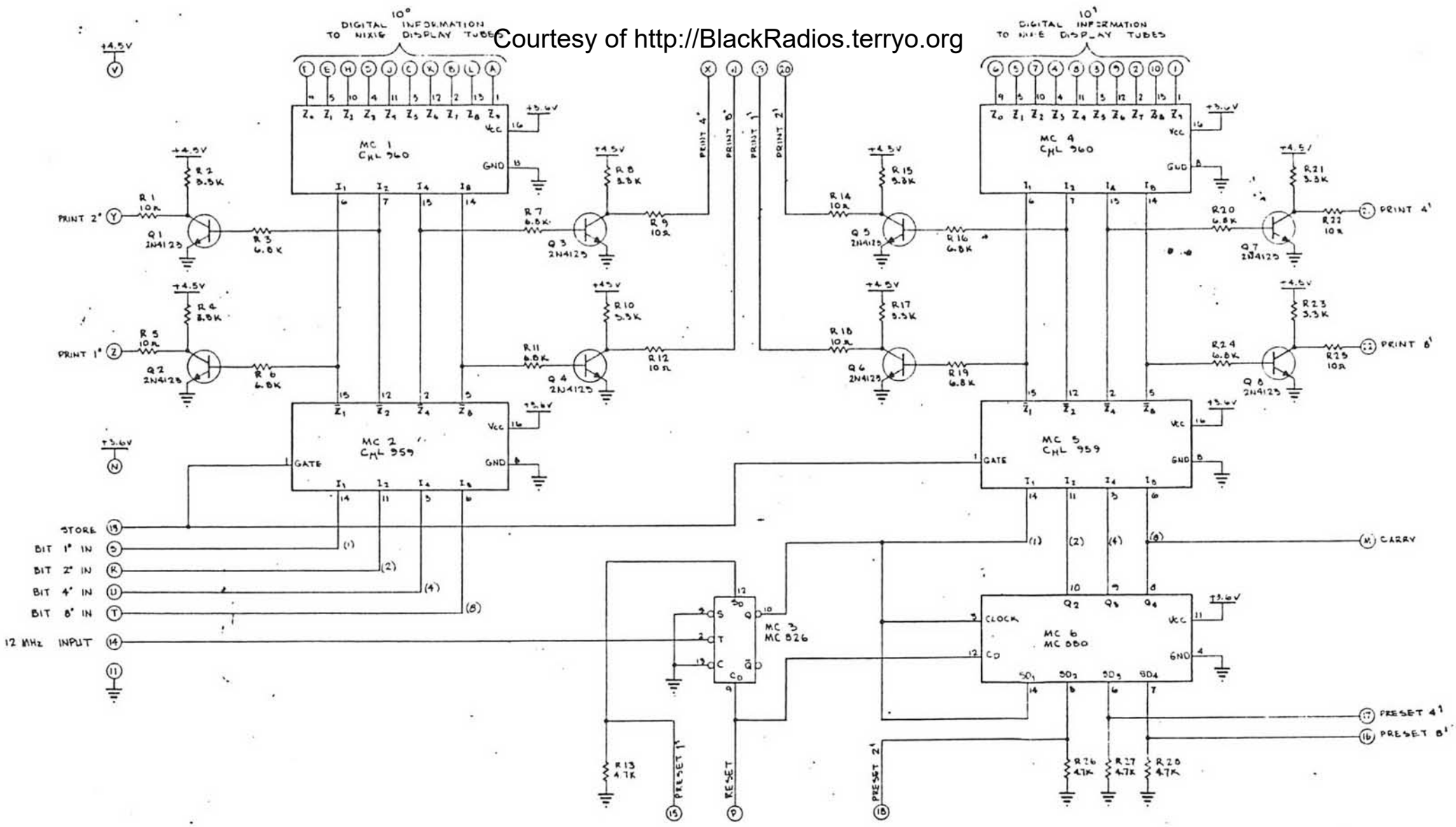


FIGURE 4-43 12 MHz DCU
SCHEMATIC AND COMPONENT LOCATION
D-11-06542

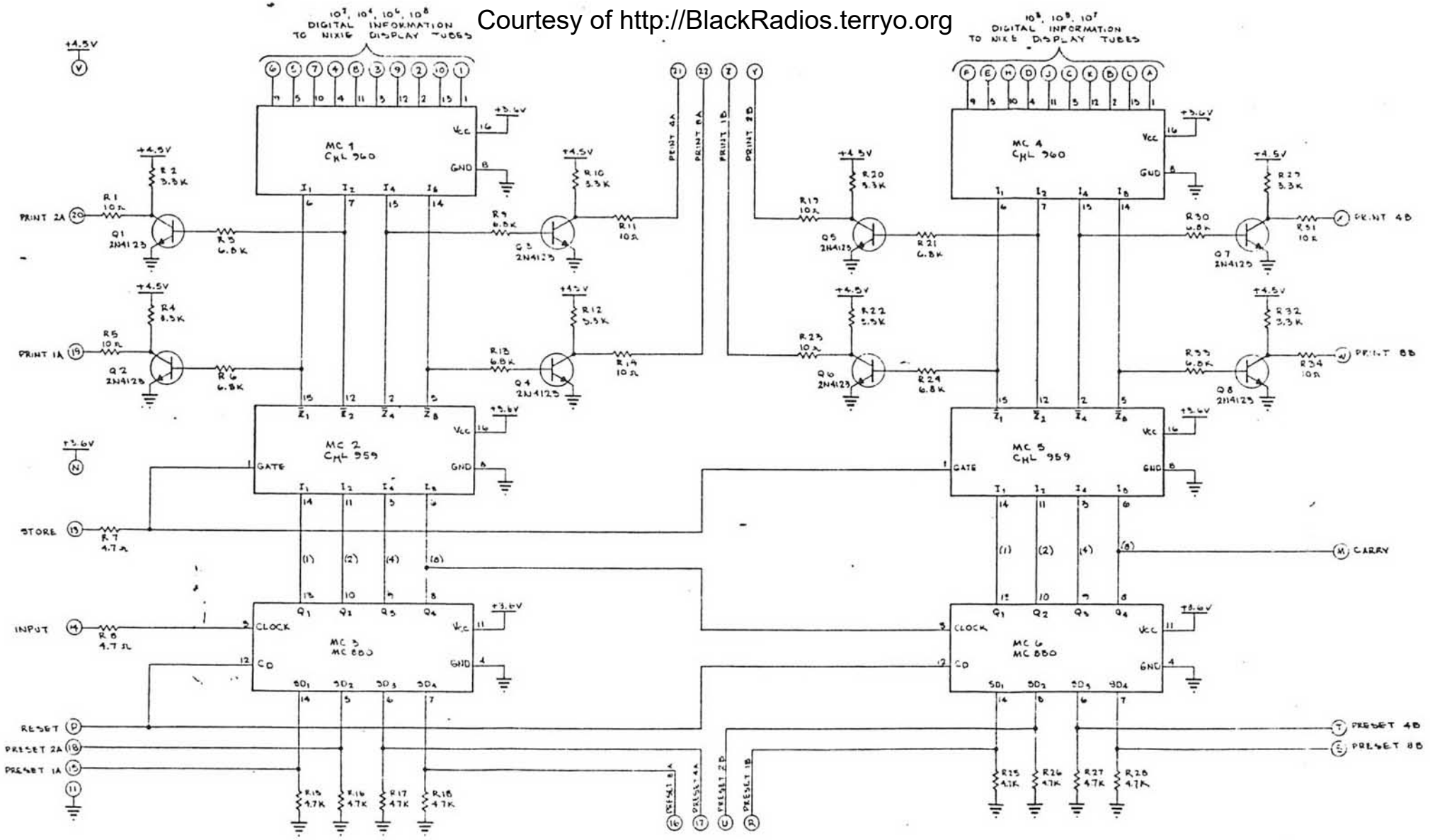


FIGURE 4-44 DUAL DCU
SCHEMATIC AND COMPONENT LOCATION
D-11-06541

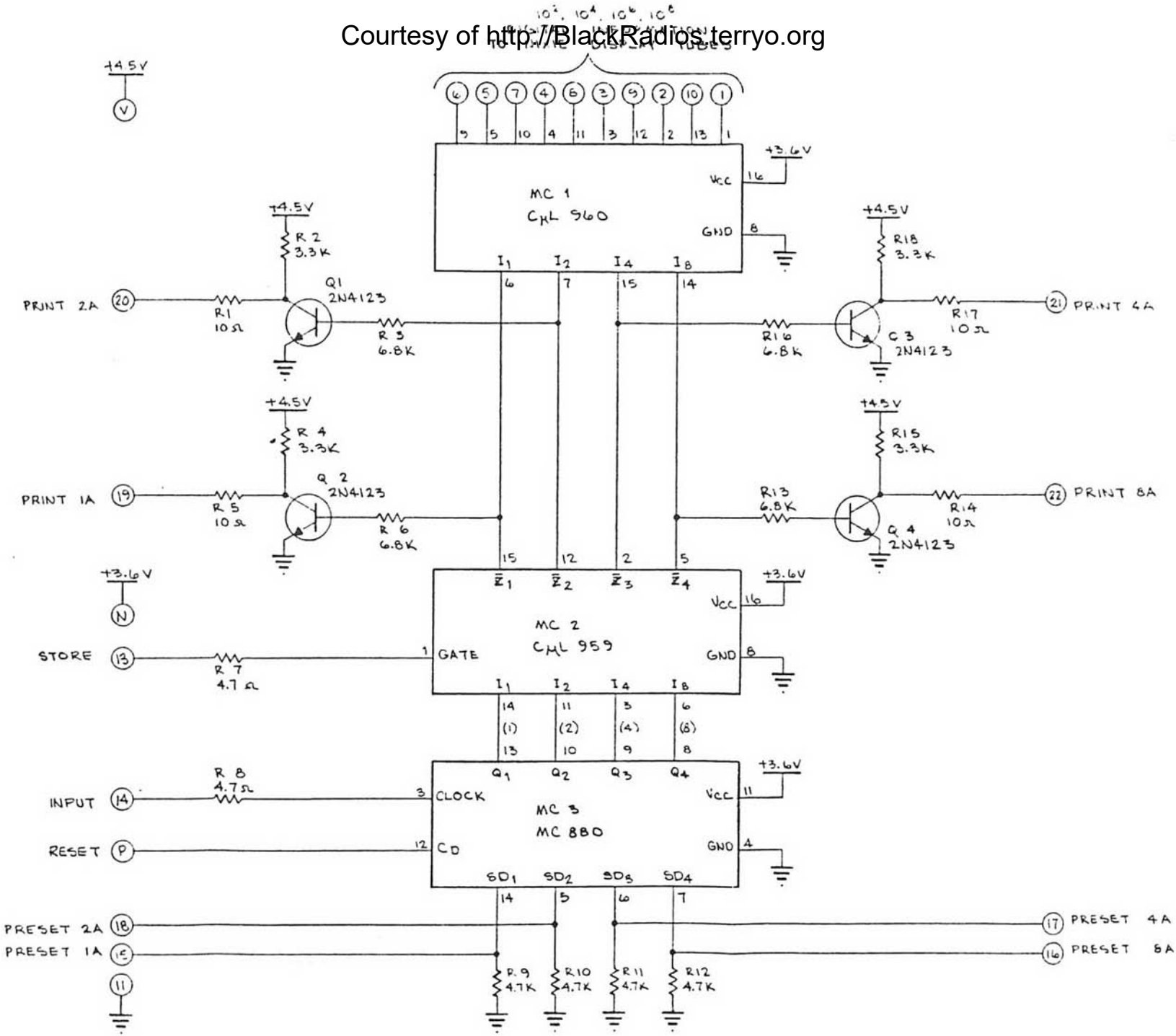


FIGURE 4-45 DCU
SCHEMATIC AND COMPONENT LOCATION
D-11-06540

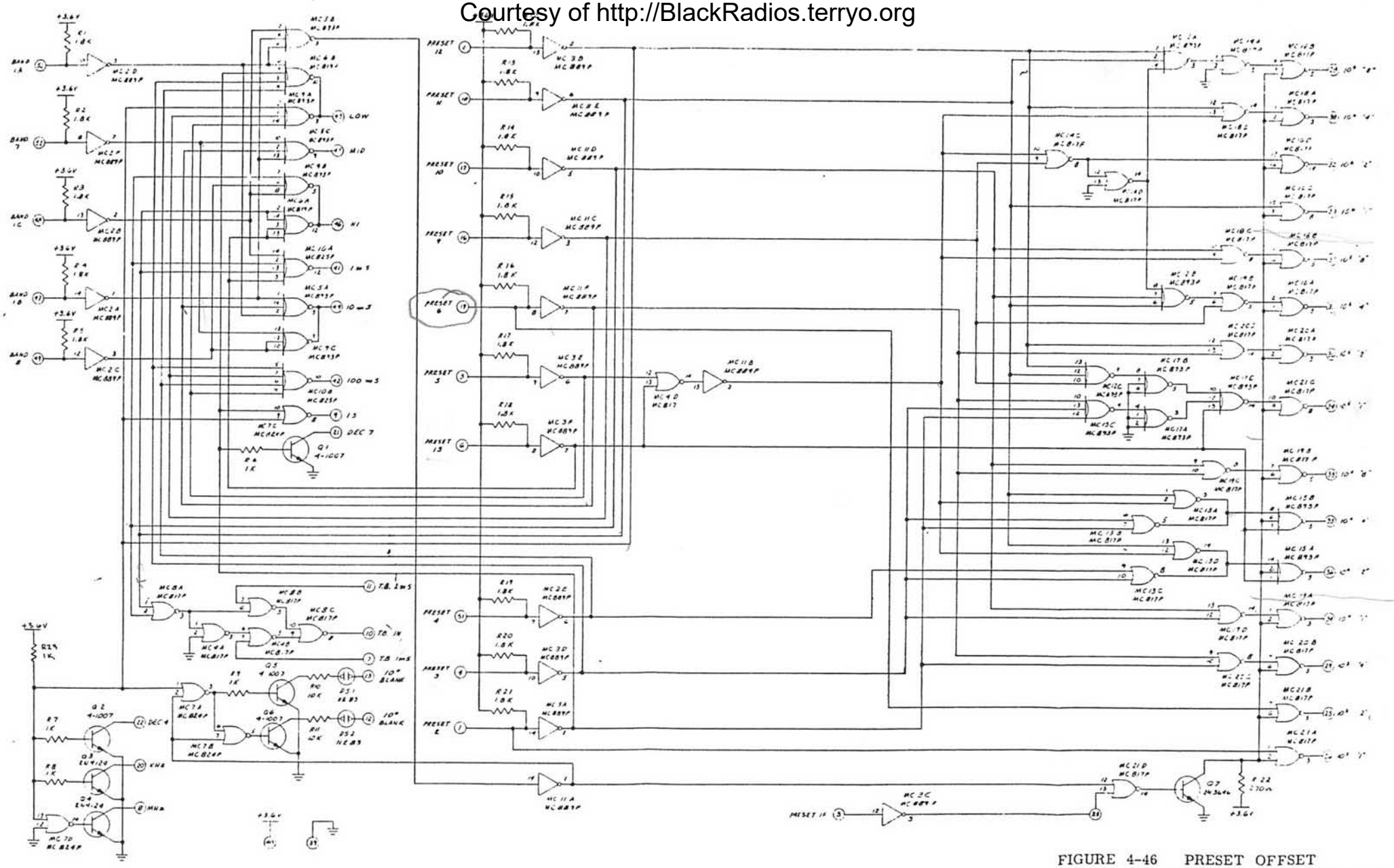


FIGURE 4-46 PRESET OFFSET
SCHEMATIC AND COMPONENT LOCATION
D-11-06626

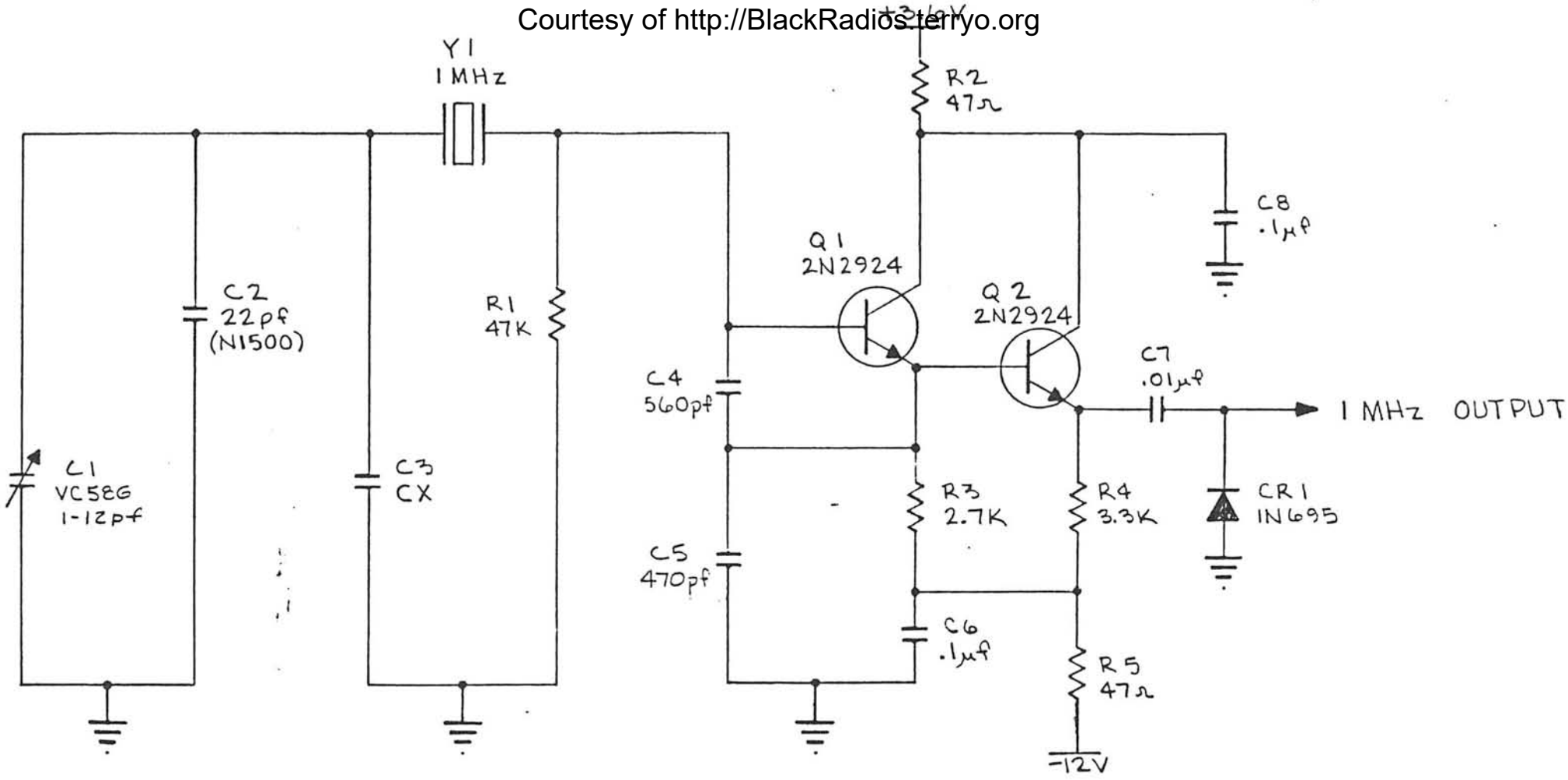


FIGURE 4-47 OSCILLATOR
SCHEMATIC AND COMPONENT LOCATION

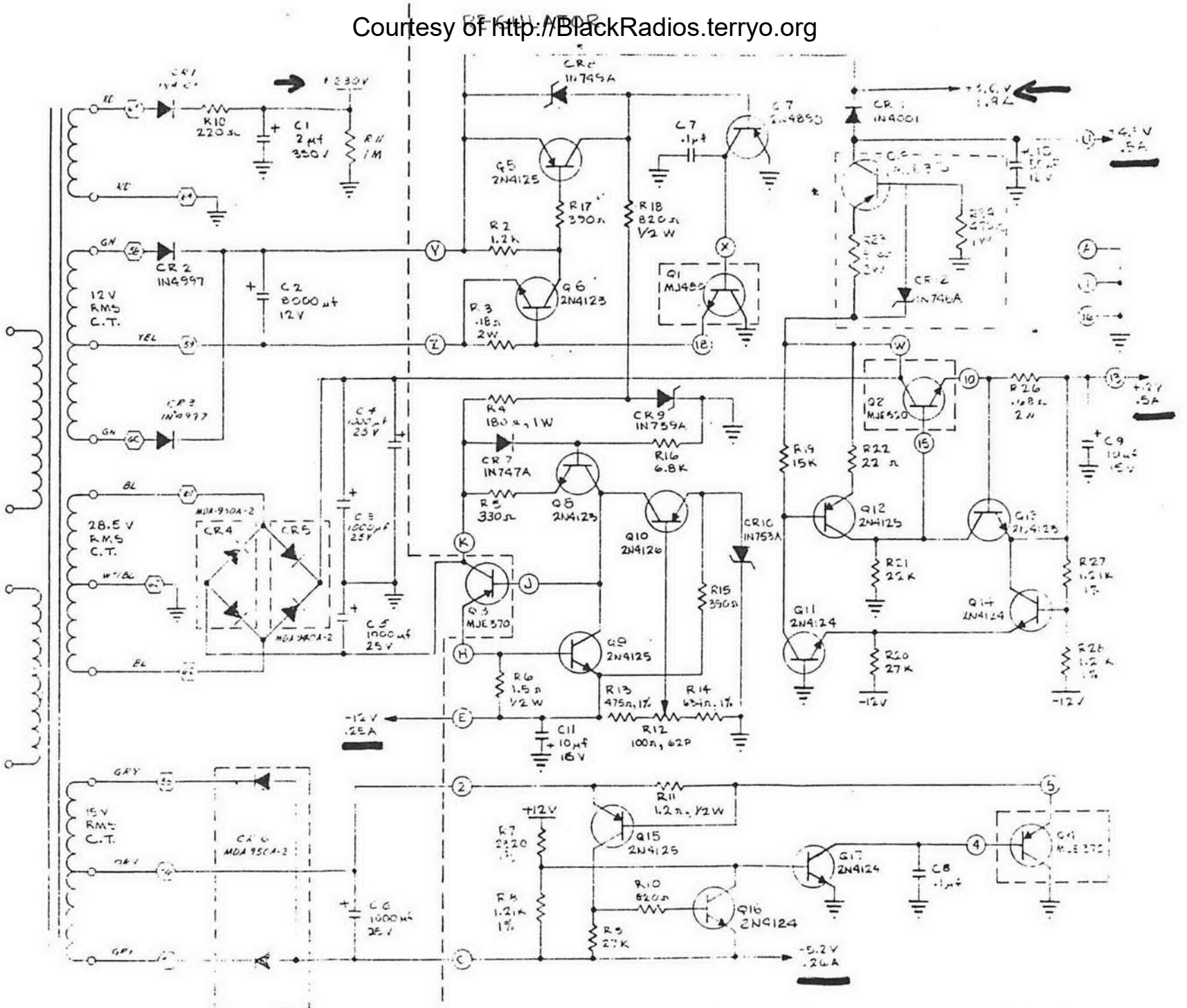


FIGURE 4-45 POWER SUPPLY AND REGULATOR SCHEMATIC AND COMPONENT LOCATION
C-11-06675

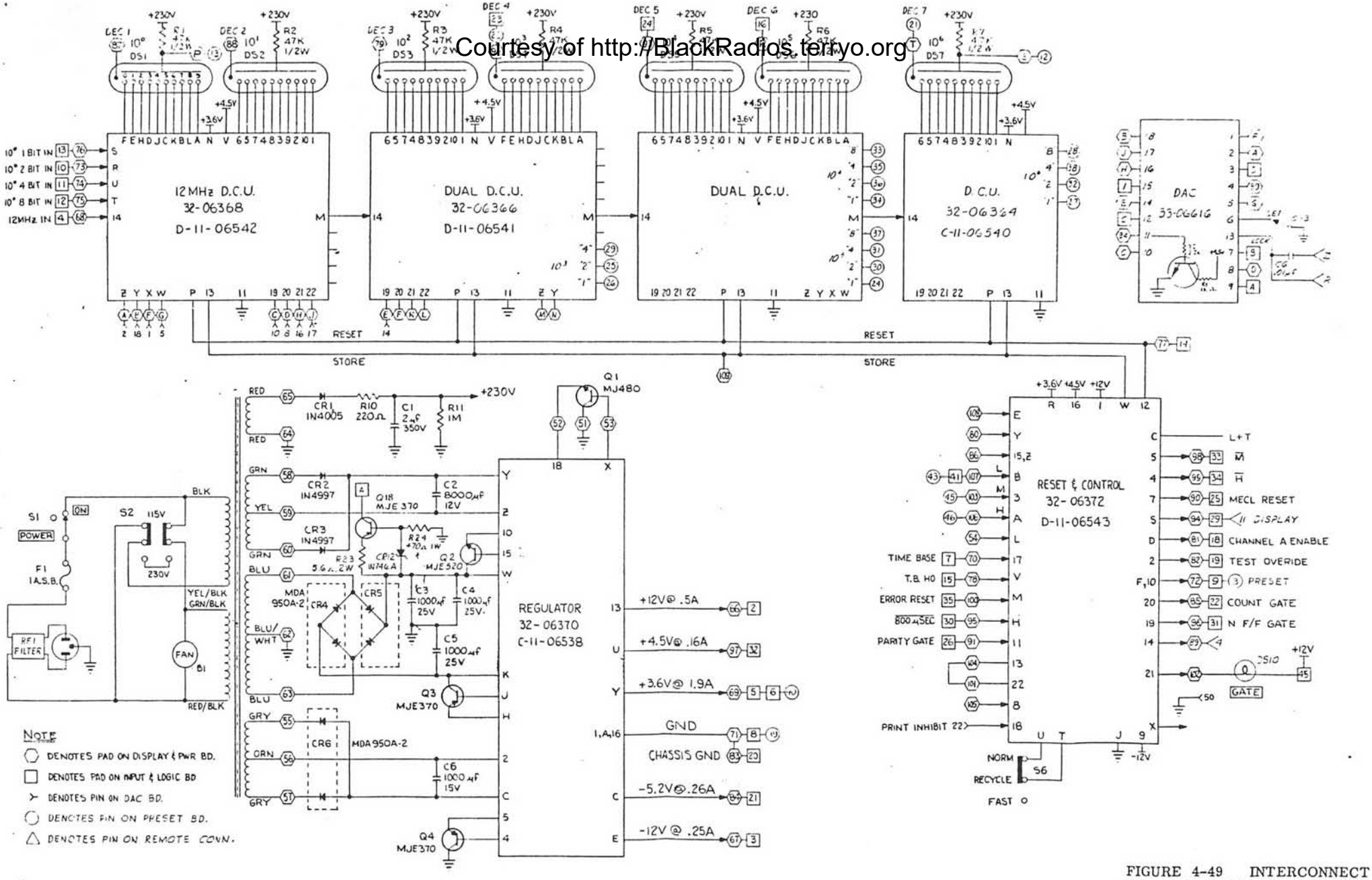


FIGURE 4-49 INTERCONNECT SCHEMATIC DIAGRAM (Sheet 1)
D-11-06625

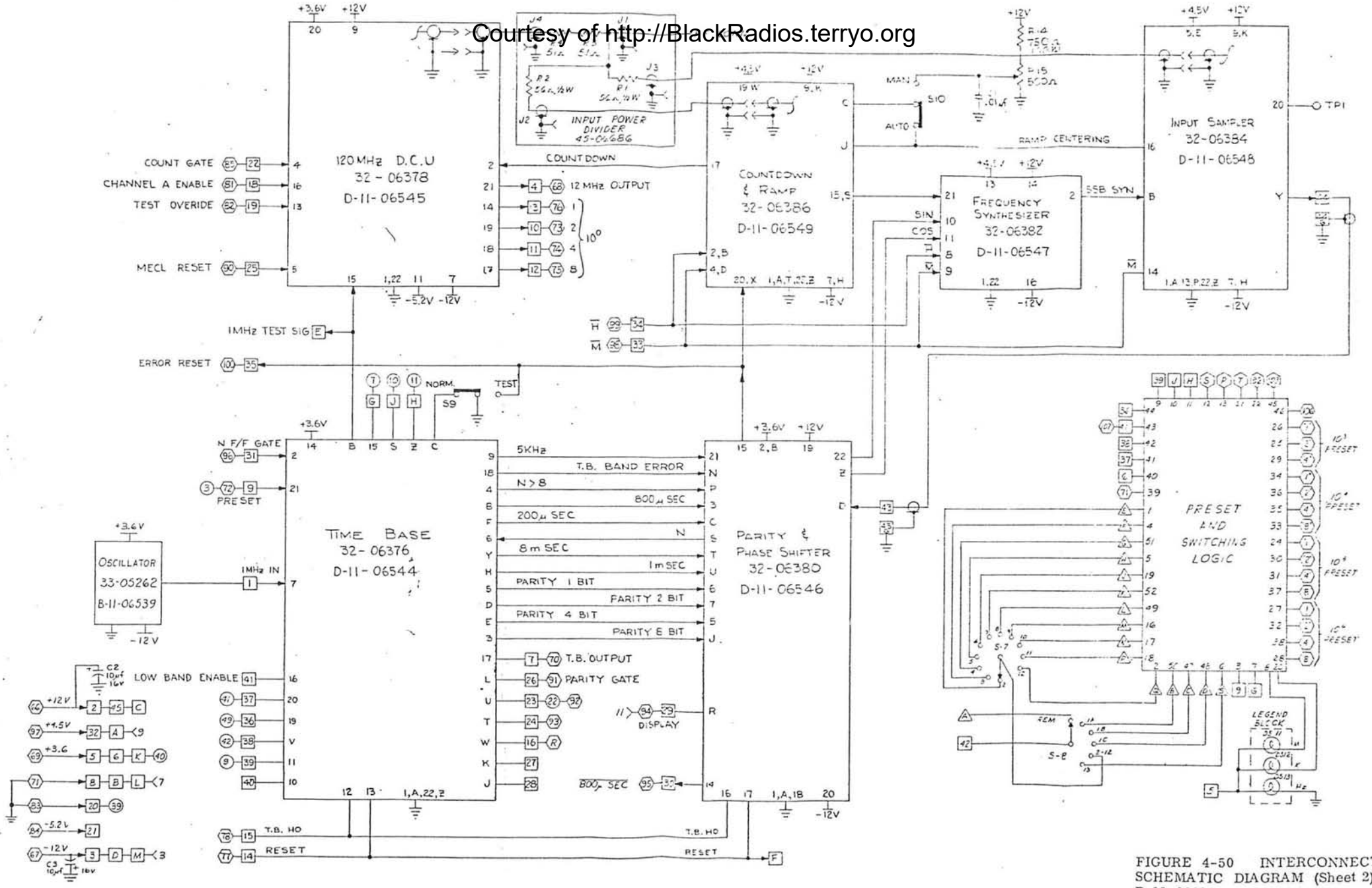


FIGURE 4-50 INTERCONNECT SCHEMATIC DIAGRAM (Sheet 2)
D-11-06625