TECHNICAL MANUAL

R-3030

RECEIVER, DUAL, VLF-HF

and

R-3080

RECEIVER, HALF-RACK, SINGLE, VLF-HF

5 kHz to 30 MHz

CUBIC COMMUNICATIONS

A member of the Cubic Corporation family of companies

305 Airport Rd., Oceanside, CA 92054

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SCOPE

This manual has been prepared to help the equipment installer and operator get the best performance from either the R-3030 dual receiver or the R-3080 half-rack single receiver. It contains information about technical specifications, optional configurations, installation requirements, and operational procedures including operator maintenance and fault isolation to the module level.

Theory of operation and detailed circuit descriptions are included in an appendix to aid in the understanding of the operation of the equipment. This material is contained as an appendix due to the many variations in configuration resulting from customer requests and to accommodate improvements in design from the original configuration.

Maintenance, including component replacement and internal adjustments, will ordinarily be performed at the designated maintenance depot. Therefore, detailed fault isolation to the component level and repair information is not included in this manual. We urge that this manual be read from cover to cover before applying power to the equipment and that it be kept available for reference.

WARNING NOTE

DO NOT APPLY POWER TO THIS EQUIPMENT UNTIL THIS MANUAL IS READ AND UNDERSTOOD.

PROPRIETARY DATA

CORRECTION NOTICE

The information contained in this document is believed to be correct as of the date of publication. Any errors noted within are requested to be directed to the factory for correction of future issues and update of existing issues.

RIGHTS RESERVED

STANDARD COMMERCIAL WARRANTY

Cubic Communications, Inc. warrants their equipment to be free from defects in material and workmanship, except for tubes and solid-state devices, under normal use and service when used for the purpose for which designed, for a period of one year from date of shipment, provided that the notice of such defect is given to Cubic Communications, Inc., or its authorized service depot, within 60 days after discovery thereof and provided that inspection by Cubic Communications, Inc., or its authorized service depot, indicates the equipment or parts are defective to Cubic Communications, Inc. reasonable satisfaction. Tubes and solid-state devices are warranted for a period of ninety days.

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No warranties other than those expressly stated herein are given or implied with respect to the equipment furnished and Cubic Communications, Inc. shall in no event be liable for consequential damages, or for loss, damage, or expense directly or indirectly arising from the use of the products, or any inability to use them either separately or in combination with other equipment or materials, or from any other cause.

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1.0 INTRODUCTION

The R-3030 and R-3080 are high performance multi-mode receivers tuning the frequency range from 5 kHz to 30 MHz and having usable performance from 50 KHz to 30 MHz. The intended use of this receiver is in manually operated or remote controlled arrays of receivers. The R-3030 in its various configurations contains two receivers in one chassis while the R-3080 is a single receiver in a chassis half the width of a standard rack chassis. Each receiver may be assigned a unique address and can be operated in groups of up to 14 receivers via an IEEE-488 remote control bus or in groups of up to 99 receivers via a serial control bus. A complete set of front panel controls and displays is also provided.

The type of remote control bus, selection of bandpass filter bandwidths, and external reference frequency (10 or 1 MHz) are option items selected at the time of order. These items may be changed in the field if required. Contact the factory for details. Filter and bus changes require software changes.

Receivers are comprised of individually shielded module assemblies. Each receiver has individual RF input and IF output connections and individual power supplies with individual power switches. One external frequency standard input connector and one frequency standard output connector with a single internal/external frequency standard selector switch is provided for each single or dual receiver assembly.

Manual operation of this receiver is by means of a 20 button keypad used for selection of frequency, mode, BFO and IF shift, manual gain, and other parameters. A manual adjustment knob is also provided for control of many of the above parameters. The display for this receiver includes frequency, mode, bandwidth, and AGC time constant as well as (when selected), BFO and IF shift, manual gain, threshold for squelch or scan stop, and other parameters. Each unit also contains a light bar type meter for indication of signal strength, audio signal level, or relative frequency of the input signal.

Operation of this receiver may also be entirely under the control of the computer system operator via the remote control bus. Choice of tuned frequency, mode, BFO offset (when the CW mode is selected), AGC time constant, and other parameters is all performed through the system console.

By proper selection of mode, bandwidth, BFO offset, gain control, AGC time constants, and other parameters, the operator is able to detect and demodulate a wide variety of signals including amplitude modulated, on/off keyed, and single sideband signals including full carrier, reduced carrier, and suppressed carrier signals. Frequency shift keyed signals can be demodulated as single sideband suppressed carrier signals or as true FM signals. All detector outputs are available as fixed level audio signals on a 600 ohm balanced line and the FM detector output is also available as a DC coupled signal on a single ended line. Headphone jacks are provided on both front and rear panels -- the signal level on these headphone jacks is controlled by a front panel volume control.

First IF output signals at 40.455 MHz and second IF output signals at 455 KHz are brought out for display or analysis by other equipment. On special order, the normal 455 kHz output may be converted to another frequency.

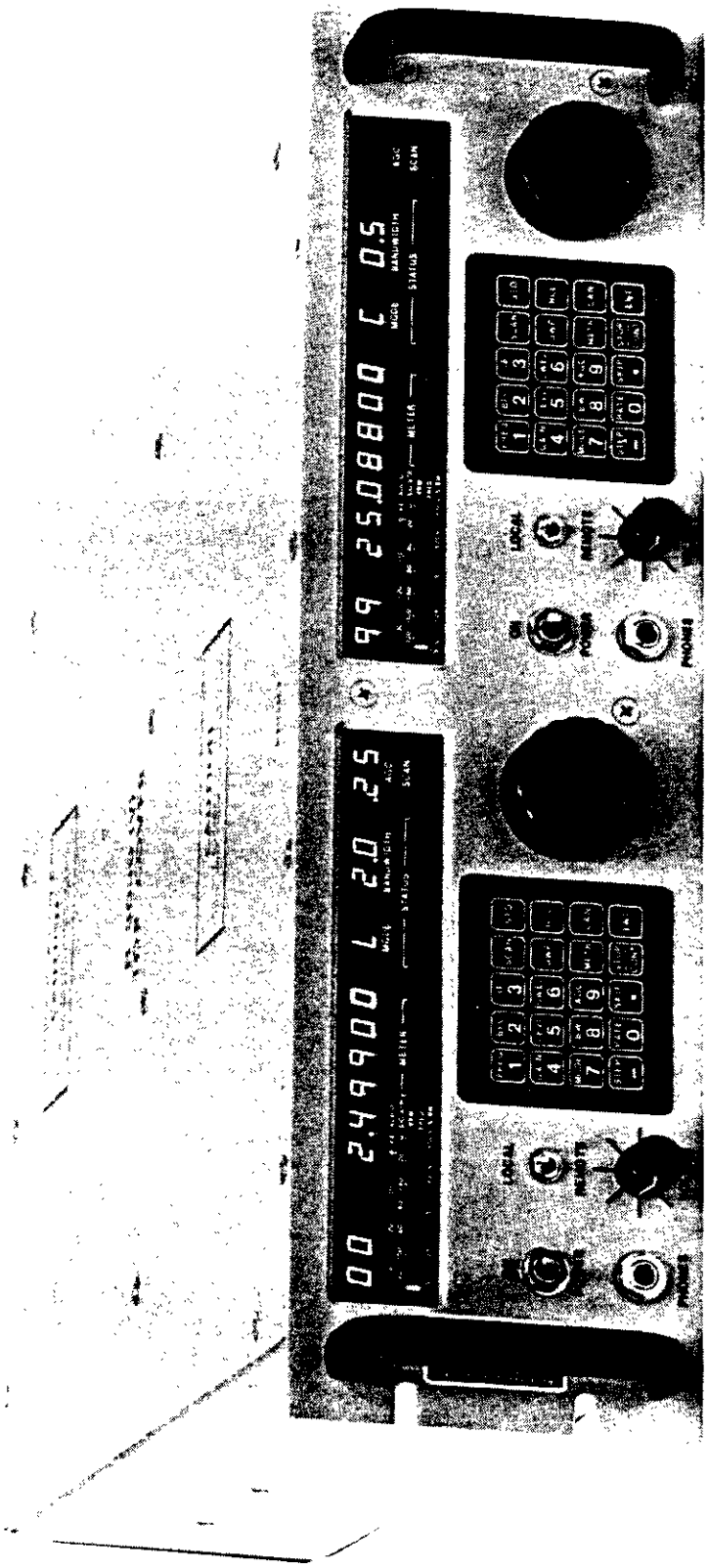


FIGURE 1-1
R-3030 PHOTOGRAPH

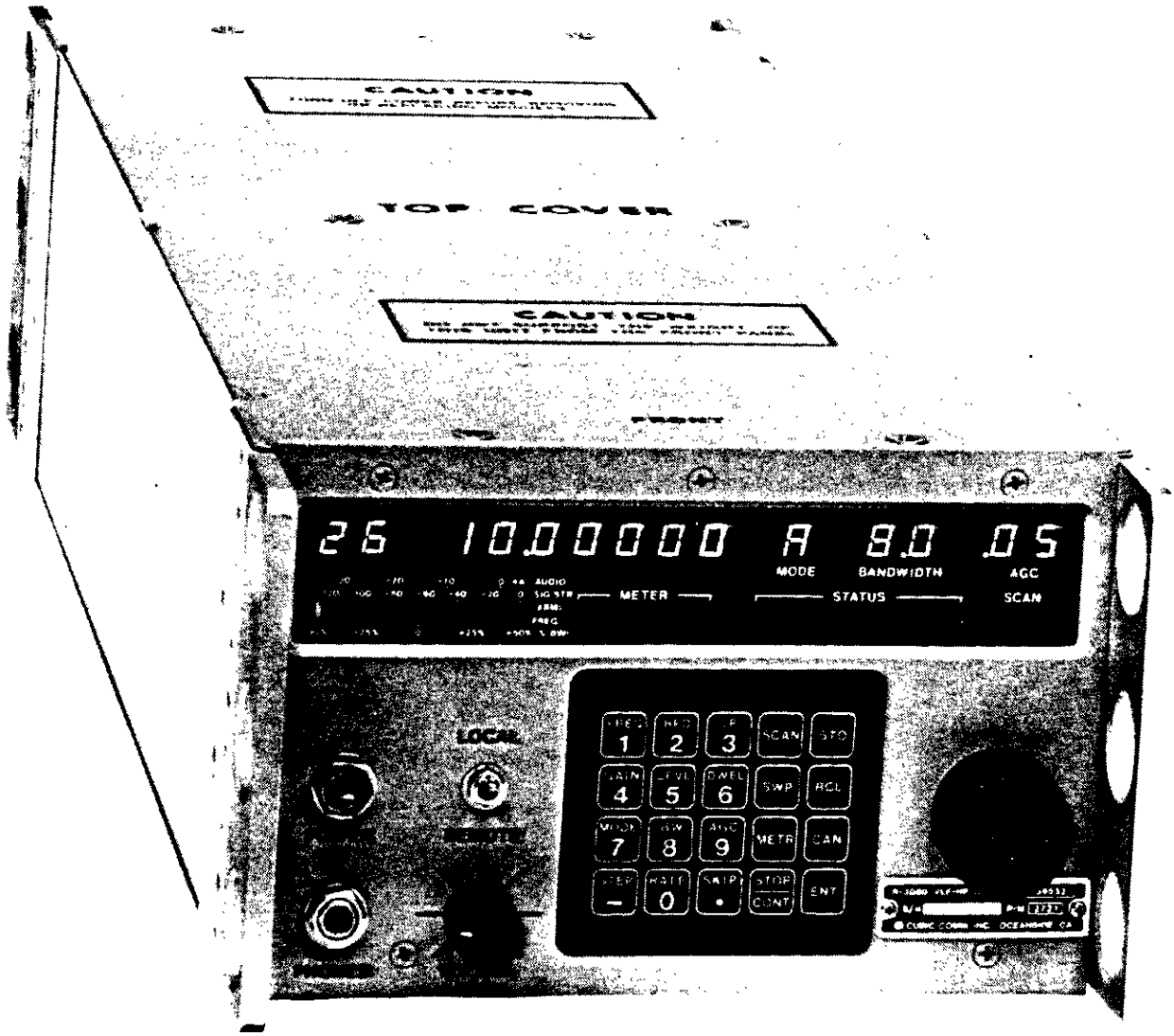


FIGURE 1-2
R-3080 PHOTOGRAPH

2.0 SPECIFICATIONS

2.1 PERFORMANCE

2.1.1 Frequency

Range	5 kHz - 30 MHz (Tunes to 0 Hz, optimum above 50 kHz)
Resolution	10 Hz steps
Accuracy	1 part per million over temperature range .01 parts per million per week aging
External Standard	Input/Output: 1 or 10 MHz (Option), 0 dBm, 50 ohms
Synthesizer Lock Time	5 ms typical, 15 ms worst case

2.1.2 Modes

Selectable	LSB, USB, AM, CW, FM
Always Active	FM Video

2.1.3 RF Section

Input	50 ohms, TNC or BNC female (Option)	
Input VSWR	less than 3:1	
Protection	Withstands application of RF power up to 100 Volts RMS from a 50 ohm source without damage.	
Noise Figure	13 dB maximum above 1600 kHz, slight degradation below	
Sensitivity for 10 dB SINAD (above 1600 kHz)	SSB (2 kHz Bandwidth)	-118 dBm
	CW (500 Hz Bandwidth)	-124 dBm
	AM (8 kHz Bandwidth, 90% modulation)	-110 dBm

2.1.4 Preselection

RF input filter in eight bands covering 1.6-30 MHz in approximate one half octave bands. Band selection automatic and switched by PIN diodes. Filter shape factor approximately 8 to 1. Filters used below 1.6 MHz relay switched for low signal distortion.

Frequency bands as follows:

Band	Frequencies (MHz)	Band	Frequencies (MHz)
1	0.000 to 0.4999	6	4.800 to 6.8999
2	0.500 to 1.5999	7	6.900 to 9.8999
3	1.600 to 2.2999	8	9.900 to 14.2999
4	2.300 to 3.2999	9	14.300 to 20.4999
5	3.300 to 4.7999	10	20.500 to 30.0000

2.1.5 IF Section

IF Frequencies	First IF: 40.455 MHz Second IF: 455 kHz
IF Bandwidth	First IF: 10 kHz or 20 kHz (Option)
	Second IF: Selectable at time of order Up to 5 of the following bandwidths
	0.3 kHz 0.5 kHz 1.0 kHz 2.0 kHz 2.7 kHz (USB or LSB) 3.2 kHz 4.0 kHz 6.0 kHz 8.0 kHz
	Optional 6th bandwidth 16 kHz

2.1.6 AGC RF derived in selected bandwidth.

a. Fast attack, selectable hold, fast release

Attack Time	15 ms maximum
Hold Time (Selectable)	
Zero	15 ms maximum
Short	50 ms nominal
Medium	250 ms nominal
Long	3 seconds nominal
Off	Remote gain control only
Release Time	200 ms maximum

b. Average type -- AM mode only using Envelope detector

Attack and release time constant 220 milliseconds nominal

AGC Range	120 dB minimum
AGC Threshold	0.5 uV (-6 dB audio reference level at 50 uV)
AGC Disable	Automatic Gain Control or Manual Gain Reduction
Manual Gain Control	0 to 127 dB gain reduction with AGC disabled

2.1.7 Interference Immunity

IF Rejection	100 dB typical
Image Rejection	90 dB typical
Spurious Responses	-130 dBm equivalent or less for -50 dBm input signals
Generated Spurious	-123 dBm input equivalent or less, 2 to 30 MHz
Cross Modulation	Unmodulated wanted signal of 100uV together with a modulated (30% at 1 kHz) unwanted signal of 250mV spaced 100 kHz apart produces less than 10% cross modulation of wanted signal.
Blocking	Attenuation of a wanted RF signal of 50 uV and caused by an unmodulated unwanted signal of 1V spaced 100 kHz away, less than 3 dB.
Inherent Oscillator Re-radiation	1 uV, worst case from antenna connector into 50 Ohms.
Intermodulation Distortion (typical)	The 3rd order I.M. products resulting from two input signals at -20 dBm each less than -120 dBm.

2.1.8 I/O Signals

Outputs:

First IF (Wideband)	40.455 MHz with 1 MHz minimum bandwidth, 50 Ohms at approximately 10 dB gain from input
Second IF (Selected)	455 kHz at selected bandwidth and nominal 0 dBm level 0 ± 3 dBm over AGC range (other IF optional)
Synthesizer Reference	0 dBm, 50 ohm output, 1 or 10 MHz (Option)
Audio	
AM. CW, LSB or USB	0 ±3 dBm, 600 ohms balanced (with AGC active)
FM	.5 V/kHz AC coupled (4 V p-p maximum)
FM Video (always present)	1 V per kHz (positive sense, DC coupled) 93 ohm single ended
Signal Strength	Digital format on bus Analog voltages on AUDIO connector (0 to + 5 VDC)

Inputs:

Synthesizer Reference	50 mV minimum, 1 or 10 MHz (Option)
Antenna	Nominal 50 ohm input impedance

2.1.9 Remote Control via IEEE-488 or Serial Bus (One only)

2.1.9.1 Receiver Functions

a. Selected Frequency (10 Hz increments)
b. Mode: LSB, USB, AM, CW, or FM
c. IF Bandwidth (fixed as optioned in LSB or USB modes)
d. BFO Frequency (± 9.99 kHz shift in 10 Hz steps)
e. IF Shift (± 9.99 kHz shift in 10 Hz steps)(fixed in LSB or USB modes)
f. Automatic or Remote Gain Control
g. AGC Hold Time (0, 50, 250, or 3000 msec) Note: AM selects average AGC
h. IF Gain (0 to -127 dB reduction in 1 dB steps with AGC disabled)
i. Setup of sweep step size and threshold offset in Sweep or Scan modes
j. Start and Stop of Sweep and Scan Functions

2.1.9.2 IEEE-488 Bus Functions

With the IEEE-488 interface module installed, the receiver implements the following IEEE-488 bus functions:

Code	Description	Comments
SH1	Source Handshake	Standard
AH1	Acceptor Handshake	Standard
T5	Talker	No Extended Capability
L3	Listener	No Extended Capability
SR1	Service Request	Rear Panel switchable SRQ enable
RL1	Remote, Local	REM and GTO, no LLO
DC1	Device Clear	Standard
DT1	Device Trigger	Standard with GET command

Interface — Driver and receiver circuits are Bus compatible. Receivers contain Bus terminating resistors and have 500 mV hysteresis. Drivers are three-state devices, capable of driving up to 15 other Bus compatible devices. Power up/down protection is included to prevent transmitting invalid data to the Bus.

Format — Sixteen lines, eight data and eight for control status message. Data transfer is byte serial using a three-wire handshake per IEEE-488 Standard.

Transfer Rates — Data transfer rates is typically 11K bytes/sec when talking and 5K bytes/sec when listening.

2.1.9.3 Serial Bus Functions

The serial bus interface module is capabile of communicating in all normal serial asychronous modes. A separate serial bus connector plate and adapter board is required for each type of bus. At the time of publication of this issue of the manual, the following buses are available:

RS-232C, single drop

RS-422A/RS-449, multiple drop

2.1.9.3 Serial Bus Functions and Description

With the serial bus interface module and appropriate bus connector board installed, the receiver may be controlled in all normal functions. A different serial bus connector board is required for each type of bus.

Depending on the type of connector board installed in the receivers, a number of different serial data buses may be accommodated. These may include the EIA RS-232, EIA RS-422, EIA RS-423, EIA RS-485, or MIL-STD-188 as required by the application. These specifications do not actually call out a bus structure but only a method of signalling on a set of wires. Unlike the IEEE-488 standard, all messages must be defined for the unit being controlled and do not follow any bus protocol except for that defined by the equipment.

RS-232

The RS-232 bus is an unbalanced bus capable of signalling over short distances and with limited data rates. This bus is ordinarily used over distances of up to 50 feet with a single controller and single controlled device. This bus uses two single wires (one for each direction of transmission) and ground and is generally found to be disturbed by noise or other common mode signals with over distances greater than a few meters.

MIL-STD-188C

The MIL-STD-188C bus is similar to the RS-232 bus except for a more limited voltage swing (+ and - 5 to 7 volts instead of + and - 5 to 15 volts) and for the fact that the mark and space conditions are defined opposite to the RS-232 standard. The same limitations on the use of the RS-232 apply to the MIL-STD-188C bus.

MIL-STD-188-114 (Unbalanced)

This bus is similar to the other unbalanced buses discussed above except that the standard requires a differential bus receiver to sense signal against the ground lead and hence allows for transmission over distances of up to 4000 feet (with a baud rate less than 1000). Transmission at rates up to 100 K Baud are recognized with cable lengths no longer than 40 feet. As with the other unbalanced buses, the signal path consists of a single wire for each direction of transmission plus a common signal ground wire. The output signal swings are limited to + and - 4 to 6 volts around signal ground. This standard allows for up to 10 receivers with a single driver.

RS-423

This bus is similar to the MIL-STD-188-144 (Unbalanced) bus except that controlled linear wave shaping allows signalling at rates of up to 9000 baud for 4000 feet of cable. Waveshaping with RC time constants limits the baud rate to 3000 for 4000 feet of cable and the maximum baud rate is limited under any condition to 100 K baud. As with all unbalanced buses, common mode noise can be a serious problem with long cable runs in the presence of other electrical noise sources and usually provides a baud rate and cable length limit much less than that listed above. This standard allows for up to 10 receivers with a single driver.

MIL-STD-188-114 (Balanced)

This is a balanced bus with signalling being performed by the differential voltage between two wires and in the presence of relatively large common mode voltages. A separate pair of wires is used for each direction of data transmission for this and for the other balanced buses. Signalling is allowed at rates of up to 100 K baud with cable length of 4000 feet with rates of up to 10 M baud with cable length of 40 feet. Exceptional rejection of common mode noise results from this bus configuration. This standard allows for up to 10 receivers with a single driver.

RS-422

This is a balanced bus essentially identical to the MIL-STD-188-114 (Balanced) bus discussed above. This standard allows for up to 10 receivers with a single driver. Some systems have been implemented with a larger number of bus receivers.

RS-485

The RS-485 bus is the only bus defined that allows for multiple bus transmitters or drivers. The standard allows for up to 32 drivers and 32 receivers on the bus. The bus receivers are high impedance under all conditions (including power off) while the bus transmitters are high impedance until commanded to transmit. This bus is otherwise similar to the RS-422 and MIL-STD-188-114 (Balanced) bus and shares similar characteristics.

A summary of the various bus characteristics is presented below:

SPEC.	EIA RS-232	EIA RS-423	MIL-STD -188C SEC. 7.2	MIL-STD -188-114 SEC. 5.2	MIL-STD -188-114 SEC. 5.1	EIA RS-422	EIA RS-485	
MODE	UNBAL	UNBAL	UNBAL	UNBAL	BALANCED	BALANCED	BALANCED	
DRIVERS	1	1	1	1	1	1	32	
RECEIVERS	1	10	1	10	10	10	32	
MAX LEN.	NO SPEC	4000	NO SPEC	4000	4000	4000	4000	feet
@ RATE	NO SPEC	3 K	NO SPEC	1 K	100 K	100 K	100 K	Baud
MAX RATE	20 K	100 K	NO SPEC	100 K	10 M	10 M	10 M	Baud
@ LENGTH	NO SPEC	100	NO SPEC	40	40	40	40	feet
MARK	-	-	+	-	-	-	-	
	DRIVER CHARACTERISTICS:							
MIN OUT	+/-5V	+/-3.6V	+/-5V	+/- 4V	+/-2V	+/-2V	+/-1.5V	
MAX OUT	+/-15V	+/-6V	+/-7V	+/-6V	+/-6V	+/-6V		
LOAD RES	3-7 K	450 min	NO SPEC	400 min	90 min	100 min	60 min	Ohms
OFF RES	300	60 K	NO SPEC	60 K	60 K	60 K	120 K	Ohms
	RECEIVER CHARACTERISTICS:							
RESIS.	3-7 K	4 K min	6 K min	4 K min	4 K min	4 K min	12 K min	Ohms
SENS.	+/- 3V	+/- .2V	+/- .6V	+/- 3V	+/- .2V	+/- .2V	+/- .2V	
COM MODE	N/A	N/A	N/A	N/A	+/- 7V	+/- 7V	+12/-7V	

2.1.10 Front Panel Keypad Control Functions

The following functions on the receiver are controlled from the front panel keypad. Some keys are single function while others share a numeric entry key.

2.1.10.1 Single Function Keys

STO Saves current frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, manual gain setting, channel lockout (skip) flag, scan threshold, sweep step size, and scan dwell time in designated channel.

RCL Puts frequency, mode, bandwidth, and AGC hold time from designated channel memory in display. Recalls also BFO offset, IF Shift, AGC hold time, and manual gain setting for use by receiver if ENTER key pressed. Recalls channel lockout (skip) flag, scan threshold, and scan dwell time for resetting if desired.

CAN Cancels current keypad operations (before ENT key press), returns unit to previous state. Disables knob control changes.

ENT Causes current displayed frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, manual gain setting, and signal threshold to be programmed into receiver. Disables knob control of numerical functions.

SCAN Starts scan of memory channels from channel recalled and entered to channel recalled just before SCAN key press at approximately 50 channels per second (20 msec per channel). Uses frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, and manual gain setting from memory. Omits any channel with skip flag set. Pauses on each frequency for a time period adjustable by main adjustment knob. Stops scan on channel with signal above programmed and stored threshold for programmed and stored dwell time.

SWP Starts sweep of frequency bands determined by parameters in memory channels. May sweep one band selected by even numbered channel recalled and entered sweeping to frequency stored in next higher odd numbered channel or all bands from odd numbered channel recalled and entered to channel recalled just before SWP key press.

Starting with first frequency in even numbered channel for sweep, uses frequency, mode, bandwidth, BFO offset, IF Shift, AGC hold time, and manual gain setting from memory. Sweep increment is set by stored step size and frequency is changes at approximately 50 frequencies per second. Pauses on each frequency for a time period adjustable by main adjustment knob. Halts sweep on frequency with signal above programmed and stored threshold for programmed and stored dwell time then continues sweep. Stops sweep at frequency stored in next odd numbered channel, then restarts sweep under control of frequency and other paramenters stored in next even numbered channel. Contines with sweep parameters set by even numbered channels and stop frequency set by frequency in odd numbered channels. Omits any sweep range designated by skip flag set in even numbered channel.

STOP/ CONT — Causes SCAN or SWEEP to stop on current channel or frequency. Allows adjustment of any receiver parameter while stopped. Causes stopped SCAN or SWEEP to be continued from current channel or frequency.

METR — Alternate press toggle the meter between signal strength, audio, and frequency.

2.1.10.2 Keys That Open the Numeric Function

FREQ (1) — Allows adjustment of frequency by adjustment knob. If numeric key pressed, allows keypad entry of frequency. Enter key terminates numeric entry. Display indicates "Fr" and frequency of RF input (7 digits plus decimal point at MHz).

BFO (2) — Allows adjustment of BFO offset by adjustment knob. If numeric key pressed, allows keypad entry of offset frequency. Enter key terminates numeric entry. Display indicates "bF" and offset frequency of BFO (3 digits plus sign plus decimal point at kHz).

IF (3) — Allows adjustment of IF shift by adjustment knob. If numeric key pressed, allows keypad entry of shift frequency. Enter key terminates numeric entry. Display indicates "IF" and shift frequency of IF (3 digits plus sign plus decimal point at kHz).

GAIN (4) — Allows adjustment of RF gain by adjustment knob. If numeric key pressed, allows keypad entry of RF gain. Enter key terminates numeric entry. Display indicates "GA" and RF gain reduction in dB (3 digits).

LEVL (5) — Allows adjustment of threshold level for scan or sweep stop by adjustment knob. If numeric key pressed, allows keypad entry of threshold level. Enter key terminates numeric entry. Display indicates "L" and threshold level in dBm (3 digits).

DWEL (6) — Allows adjustment of time for dwell during scan or sweep operations when signal is sensed to be above programmed threshold by adjustment knob. If numeric key pressed, allows keypad entry of dwell time. Enter key terminates numeric entry. Display indicates "d" and dwell time in seconds (1 digit).

STEP (-) — Allows adjustment of step size used in frequency sweep. Minus sign used for BFO offset, IF shift, and threshold offset only.

2.1.10.3 Sequential Function Keys (Numeric function not opened)

MODE (7) — Sequences mode selection between LSB, USB, AM, FM, and CW. Indicated by single letter on mode display (L, U, A, F, or C)

BW (8) — Sequences IF bandwidth between filters installed. Approximate bandwidth indicated on display.

AGC (9) — Sequences AGC hold time between zero, 0.05, 0.25, 3.0 seconds and off. (Manual gain control only in off position). Indicated by numbers indicating approximate hold time. Blank when AGC disabled (off).

RATE — Sequences tuning rate between 10 Hz, 100 Hz, and 1 kHz per step or 1 dB per step on main adjustment knob and adjustment knob lock. Rate indicated by intensifying significant digit in main display. Knob lock indicated by not intensifying digit.

SKIP (.) — Alternate presses toggle the channel skip flag used during scan of memory channels. Indicated by SKIP annunciator.

2.1.11 Front Panel Displays

The following parameters are displayed on the front panel of the receiver. All functions are for each receiver in a 2 receiver assembly.

FUNCTION DISPLAY — Two alphanumeric characters -- 00 through 99 for store or recall, F for frequency, bF for BFO offset, IF for IF shift, GA for Gain, L for threshold level, d for dwell time, SE for step size adjustment, OF for threshold offset adjustment, blank otherwise.

MAIN DISPLAY — Seven digits numeric plus decimal points and minus sign. Used for the following functions:

FREQUENCY -- 7 digits plus . at MHz -- normal display

BFO Offset -- sign (blank or -) plus 3 digits and . at kHz -- displayed during BFO offset adjustment only.

IF Shift -- sign (blank or -) plus 3 digits and . at kHz -- displayed during IF shift adjustment only.

RF GAIN -- minus sign plus 3 digits -- displayed during RF gain adjustment only

THRESHOLD -- minus sign plus 3 digits -- displayed during threshold adjustment only.

DWELL TIME -- 1 digit -- displayed during dwell time adjust only

MODE DISPLAY — Single character -- L, U, A, C, or F

BANDWIDTH — Two characters plus decimal point indicating approximate bandwidth in kHz -- set by option configuration

AGC DISPLAY — Two digits plus decimal point indicating approximate hold time in seconds (.00, .05, .25, 3.0, or blank for MGC only)

ANNUNCIATORS

AUDIO	indicates that meter reads mode selected audio level
FREQ	indicates that meter reads relative frequency
REM	indicates that control of unit is via remote control bus
FAULT	indicates an internal detected fault
KPAD	indicates keypad entry is active, display does not necessarily indicate current frequency.
SKIP	indicates channel is skipped during scan operations

METER; 20 segment light bar meter, calibrated from -120 to 0 dBm for signal strength, -35 to + 4 dBm for audio, -50% to + 50% of IF BW for frequency.

2.1.12 Other Front Panel Controls and Functions

POWER ON/OFF SWITCH -- toggle type circuit breaker

LOCAL/REMOTE SWITCH -- small toggle switch for taking positive local control or allowing remote control function (Not IEEE-488 standard).

MAIN ADJUSTMENT KNOB -- 1.75 inch diameter knob on optical shaft encoder

VOLUME -- Adjusts audio level to phones jack tip and ring contacts

PHONES JACK -- Tip and ring contacts driven independently by selected mode audio. Series resistor in each circuit to protect amplifier from short circuit due to use of single circuit phone plug.

2.1.13 Rear Panel Controls

Reference Selector -- One Internal/External switch per assembly.

Address Selector (IEEE-488 only) -- 8 individual 2-position switches for selecting individual bus addresses and talker only, listener only, and SRO enable functions. The R-3030 has 2 such groups of switches, the R-3080 only one.

2.1.14 Connectors (all on rear panel)

RF	Antenna	TNC or BNC (Option) Female
IF	First IF	TNC or BNC (Option) Female
IF	Second IF	TNC or BNC (Option) Female
REF	Reference In	TNC or BNC (Option) Female
REF	Reference Out	TNC or BNC (Option) Female

REMOTE CONTROL

IEEE-488 BUS (24 cont.) Amphenol Blue Ribbon IEEE-488 stacking connector

or

RS-232C DB-25P on chassis, mates with DB-25S

or

RS-422/RS-449 DC-37P on chassis, mates with DC-37S

AUDIO

12 contact MIL crimp MS3122A14-92P or Burndy G2B14-92PNH on chassis, mates with cable connector

or MS3126F14-92S or Burndy G6F14-92SNH

19 Contact MIL solder MS3112E-14-19S on chassis, mates with cable conn. MS3116F-14-19P

or

15 contact D DA-15S on chassis, mates with DA-15P

POWER

4 contact MIL crimp MS3122A10-4P or Burndy G2B10-4PNH on chassis, mates with cable connector MS3126F10-4S or Burndy G6F10-4SNH

or (Line on pins A and C, Ground on Pins B and D)

3 contact commercial CEE 22 Form VI (3 pin)

PHONE JACKS Rear panel 1/4 inch phone jacks connected in parallel with front panel phone jacks

2.1.15 Running Time Meter

Each receiver has a 0 to 9999 hour running time meter installed. This meter operates whenever the front panel power switch is turned on and the unit is connected to AC power. The meter is mounted on the rear panel and visible from the rear of the unit.

2.1.16 Power Requirements

100 - 130 VAC or 200 - 260 VAC (selectable)
47-420 Hz, 40 watts maximum per receiver.

2.2 ENVIRONMENTAL CONDITIONS

2.2.1 Temperature

-20°C to +60°C Operating
-40°C to +70°C Storage

Tested to MID-STD-810D, Method 501.2, Table 501.2-111 and MIL-STD-810D, Method 501.2, Table 2.2-1.

2.2.2 Relative Humidity

Humidity test per MIL-STD-810D, Method 507.2, Procedure I, Temperature 50°C, Figure 507.2-1, 5 total cycles.

2.2.3 Shock and Vibration

Shock per MIL-STD-810D, Method 516.3 Figure 516.3-4 20g 11 ms sawtooth, 30g 11 ms in one axis

High impact shock per MIL-S-910C.

Vibration per MIL-STD-810d, Method 514.3, Figure 514.3-36 W_o = .003g^2/Hz (Random)

2.2.4 Electromagnetic Emission and Susceptibility

In conformance with the applicable provisions of MIL-STD-461B, class A1a as applicable to Navy and Air Force procurements.

Filtering in conformance with MIL-STD-461B, section 4.2.1.

Requirements per MIL-STD-461B as follows:

CE01 Conducted Emissions, Power and Interconnecting Leads, Low Frequency (up to 15 kHz)
CE03 Conducted Emissions, Power and Interconnecting Leads, 0.015 to 50 MHz
CE07 Conducted Emissions, Power Leads, Spikes, Time Domain
CS01 Conducted Susceptibility, Power Leads 30 Hz to 50 kHz
CS02 Conducted Susceptibility, Power Leads 0.05 to 400 MHz
CS06 Conducted Susceptibility, Spikes, Power Leads
RE01 Radiated Emissions, Magnetic Field, 0.03 to 50 kHz
RE02 Radiated Emissions, Electric Field, 14 kHz to 10 GHz
RS01 Radiated Susceptibility, Magnetic Field, 0.03 to 50 kHz
RS02 Radiated Susceptibility, Magnetic Induction Field, Spikes and Power Frequencies
RS03 Radiated Susceptibility, Electric Field, 14 kHz to 40 GHz

2.3 PHYSICAL CHARACTERISTICS

2.3.1 Construction

All chassis and module assemblies use chem-film treated aluminum alloy and stainless steel hardware in accordance with the provisions of sections 3.4.9.13 and 3.4.11.2 (j) of MIL-E-16400. No steel or other materials subject to destructive corrosion are used.

The front panel is painted with semi-gloss light gray enamel in accordance with the requirements of MIL-E-15090, Class 2, Type II or Type III, color number 26307 of FED-STD-595, with black legends and handles. Finish of all painted surfaces is in accordance with the provisions of section 3.4.11.3 of MIL-E-16400.

2.3.2 Maintainability

Access to replaceable module assemblies is by means of 1/4 turn captive fastners. Modules are secured with 1/4 turn captive fasteners. Correct module position in assembly indicated by a diagonal stripe on the module top surfaces.

2.3.3 Size

R-3030
Modules for two complete receivers are packaged in one standard 5.25 inch high by 19 inch wide rack panel and chassis with provisions for mounting slides. Slides are furnished if specified on the purchase order. Recommended slide is Chassis-Trak model C-300-S-118, Option Revision C (single hole mounting).

R-3080
Modules for one receiver are packaged in one 5.25 inch high by 8.4 inch wide chassis designed for side-by-side mounting with similarly sized equipment to make a standard rack chassis configuration. Attaching hardware and rack angles furnished if specified on the purchase order.

Depth, including protective handles, is approximately 21.2" behind the front panel. Connectors on the rear panel are inside the handle dimensions and are protected by the handles and chassis from contact with any flat surface large enough to contact both handles simultaneously at any angle of contact. The rear handles of the R-3030 include a receptacle for a standard ATR tapered locating pin. One pair of Barry 3098-005-000 pins furnished with each 2-receiver assembly.

2.3.4 Weight

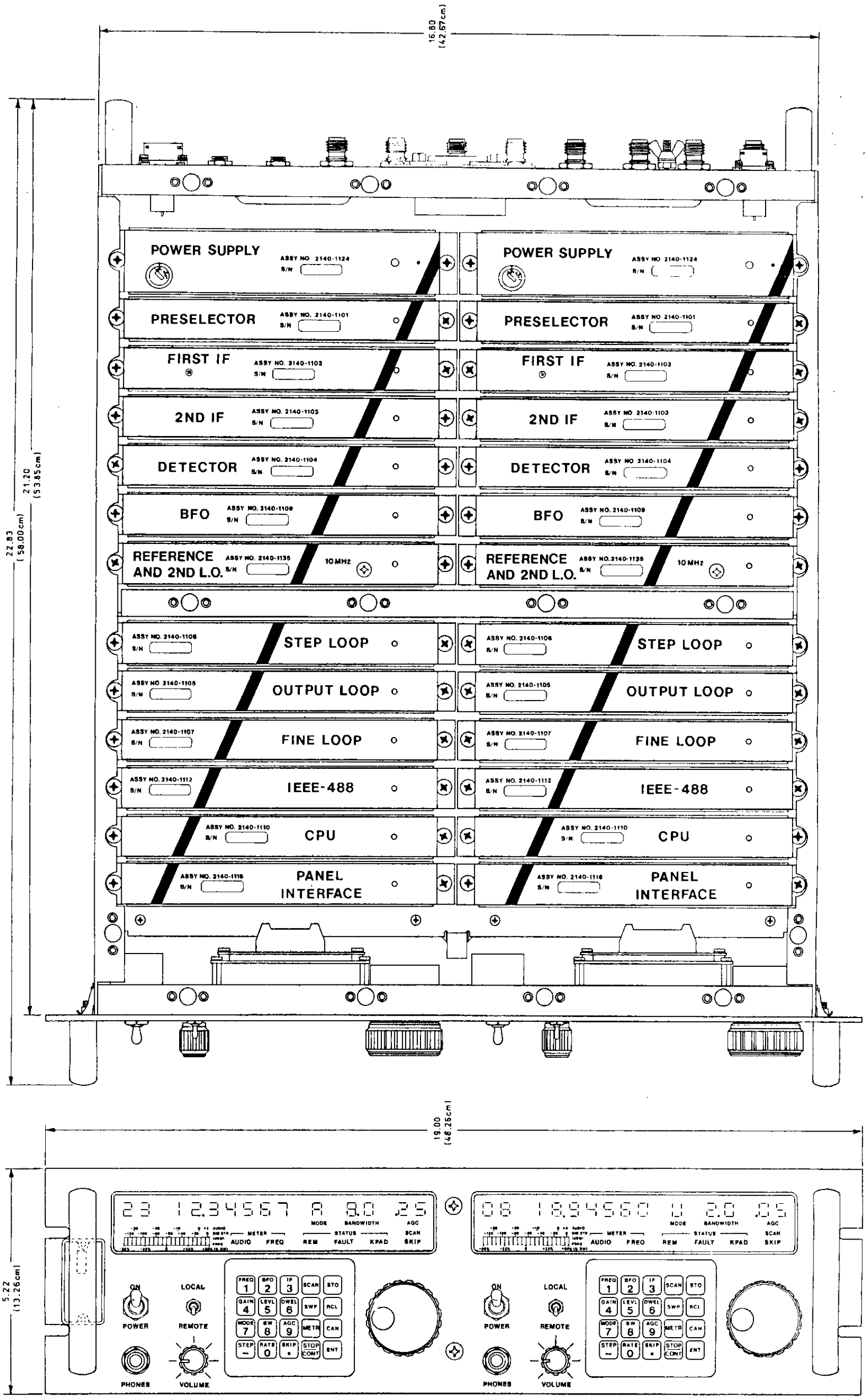
R-3030
Approximately 47 pounds for one chassis containing modules for two receivers not including mounting slides (optional items).

R-3080
Approximately 25 pounds for one chassis containing modules for one receiver.

2.3.5 Reliability

The calculated Mean Time Between Failures is approximately 5000 hours per receiver unit when calculated using the methods and failure rates of MIL-HDBK-217D with failure rates of unrated components calculated using the methods of MIL-HDBK-217D.

FIGURE 2-1
R-3030 OUTLINE AND MOUNTING



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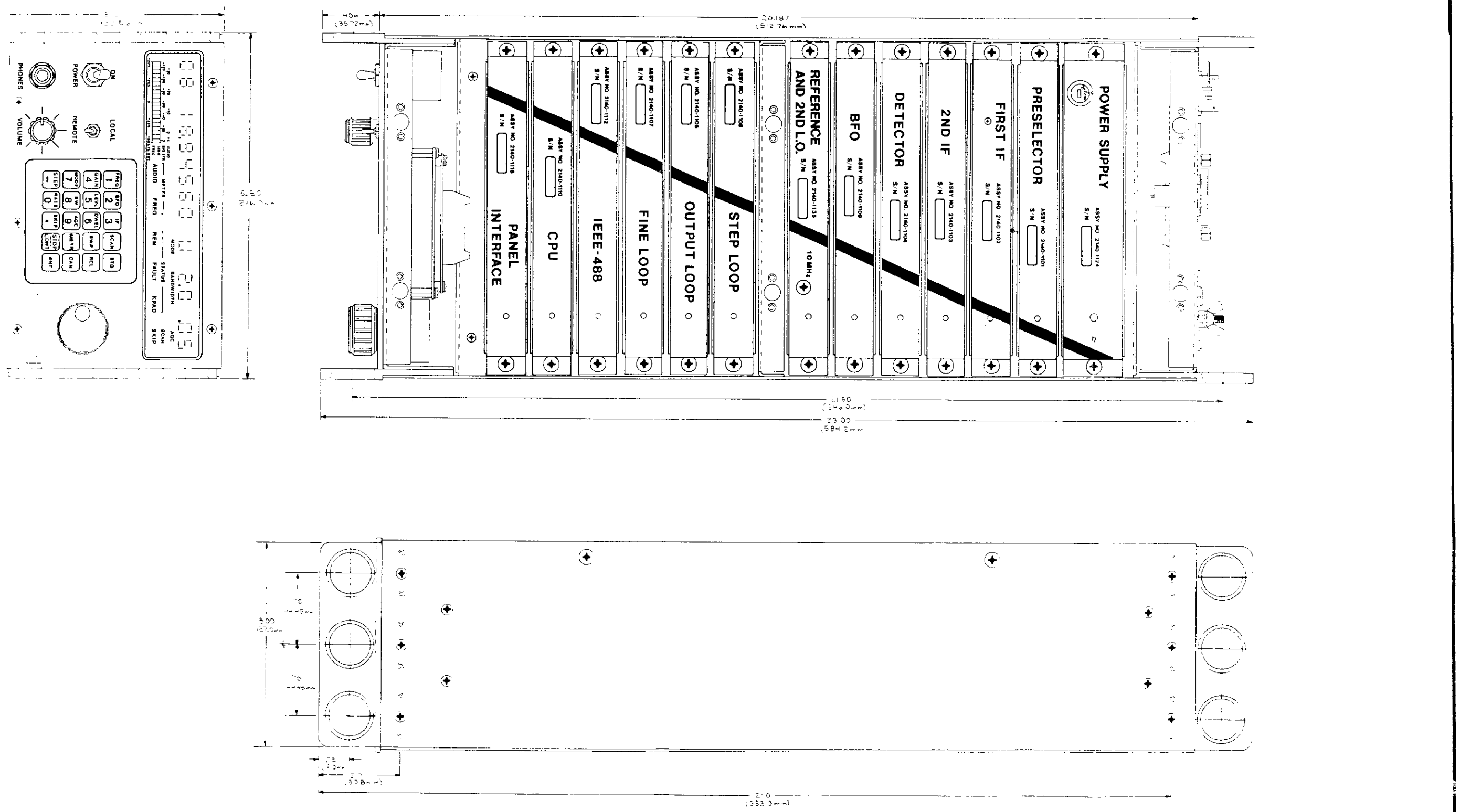


FIGURE 2-2
R-3080 OUTLINE AND MOUNTING

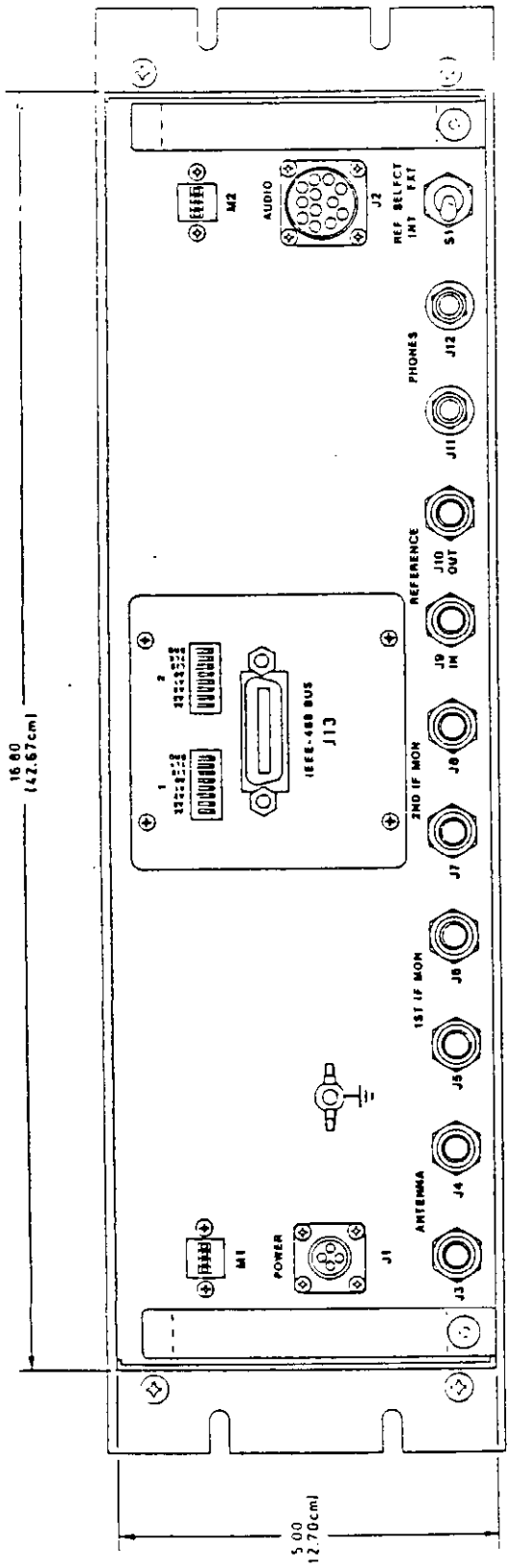


FIGURE 2-3
R-3030 REAR PANEL / MS AUDIO CONNECTOR

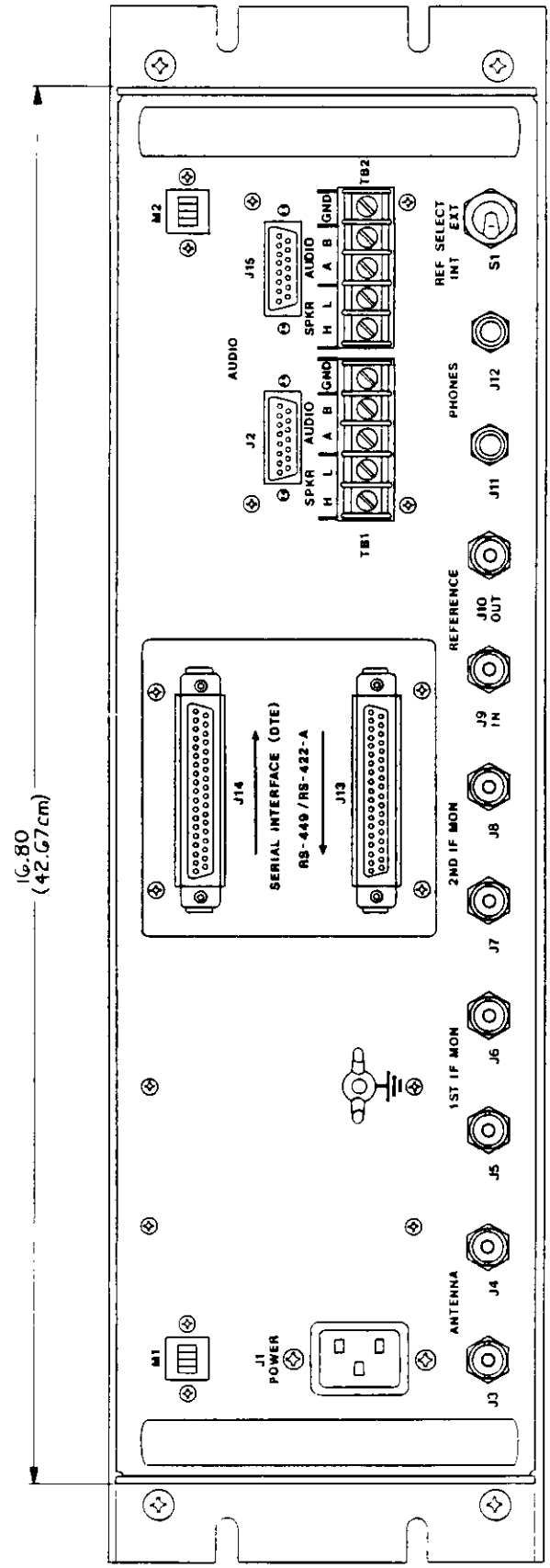


FIGURE 2-4
R-3030 REAR PANEL / D AUDIO CONNECTORS

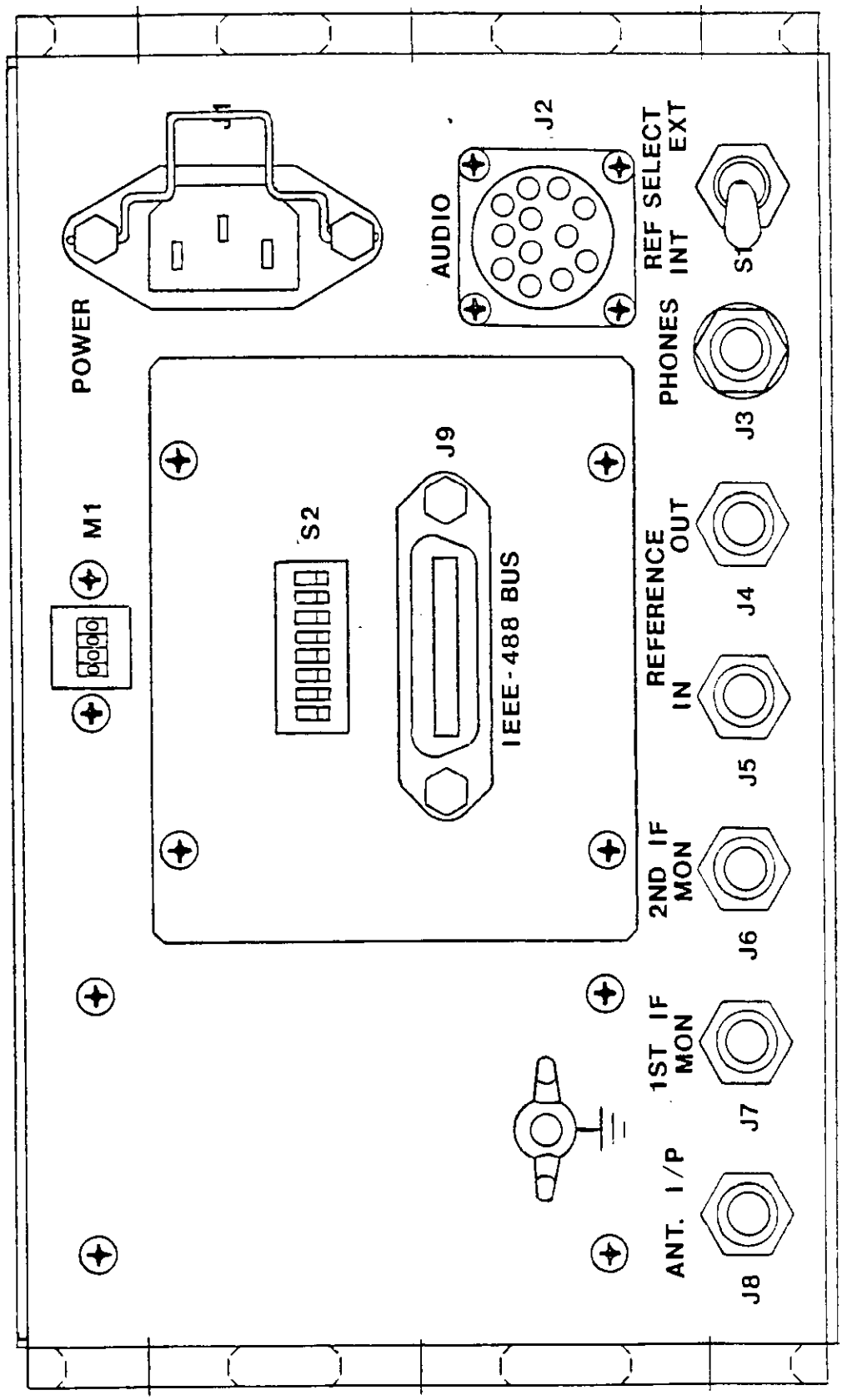


FIGURE 2-5
R-3080 REAR PANEL / MS AUDIO CONNECTOR

3.0 INSTALLATION

3.1 UNPACKING AND INSPECTION

Examine the shipping carton for damage before unpacking the unit. If the carton is damaged, open the carton in the presence of an agent of the shipping carrier if possible. If the carton is not damaged, retain the carton and packing materials for inspection if damage is found after the unit is unpacked.

Open the carton and remove the foam packing material on top of the unit. Lift the unit free of the carton. No packing materials are required or provided inside the unit. Replace the foam packing material in the carton. The carton may be saved for possible re-shipment if required.

Upon unpacking, inspect the unit for obvious external damage. Pay particular attention to dents or bent sheetmetal. If damage is evident, remove the top and bottom covers of the unit and inspect for further damage such as modules removed from their mounts or damaged circuit boards. Do not attempt to operate the unit if such damage is noted until further checks are made.

3.2 MOUNTING

The unit is designed for table top or rack panel mounting in a fixed or mobile environment in a relatively protected location. The unit is not water proof but is considered dustproof and will withstand normal interior exposure.

R-3030
If slide mounting is to be used, securely mount the outer section of the slides to the rack cabinet being sure to select the correct mounting holes for the front flanges and the rear brackets. Before tightening the mounting screws securely, slide the chassis assembly into the rack mounted portion of the slides and adjust the hardware position as required for a smooth siding fit. Securely tighten all hardware. After securing all cables to the rear of the unit, insure that the proper 10-32 screws are used to secure the panel of the receiver assembly to the rack.

R-3080
If the unit is to be installed together with other equipment in a full rack width configuration, secure the two units together using the inserts for the handle holes. Insert the threaded fasteners and tighten securely. Slides are not used in this configuration.

If the unit is not to be mounted on chassis slides, insure that a suitable shelf or angle bracket is used to support the weight of the unit and that the unit is suitably braced to prevent movement in the event of motion of the vehicle or platform in which it is installed. If it is not installed in a vehicle or other mobile platform, it may not be necessary to brace the unit against movement. The weight of the unit must, however, be adaquately supported.

CAUTION: DO NOT SUPPORT THE WEIGHT OF THE UNIT BY THE FRONT PANEL ONLY. USE CHASSIS SLIDES OR A SUITABLE SUPPORT SHELF

3.3 POWER

The unit is powered from either a source of 100 to 130 VAC or 200 to 260 VAC, 47 to 400 Hz. One power connector is used per two receiver assembly (R-3030) and each receiver has its own power control circuit breaker.

The AC power connector (J1) may be a military standard type having crimp type male contacts or a international standard commercial type depending on the option ordered. The power cable has the socket type contacts. On the military style connector, pins A and C are used for the AC line while pin B is used for ground. If the power cable used is the shielded type, pin D may be used for the shield. Both pins B and D are connected to chassis ground.

A mating cord set is provided having a U.S.A. standard 3 pin plug for 115V service. Should a different plug be required, either cut off the U.S.A. standard plug and replace it with the desired plug or replace the cord set. The U.S.A. standard cord uses the black wire for the AC line live side, the white wire for the AC line neutral, and the green wire for chassis ground. Only the green wire is connected to the chassis. International color code for these functions uses a brown wire for the AC line live side, a light blue wire for the AC line neutral, and a green wire with a yellow tracer for the chassis ground. Either type of color code may be found in the power cable.

The unit will normally be marked with the line voltage for which it was set at the factory if the factory setting was for 220 VAC operation. Unless otherwise specified, the unit will be set to be operated from a source of 110 VAC. If the line voltage available is not as marked or if there is some doubt as to how the unit is set, remove the top cover of the assembly by undoing the 1/4 turn captive fasteners. The power supply modules are in the rear of the assembly.

Determine the AC line voltage available. If it is in the range of 100 to 130V, set the rotary switch on the power supply module to the 110V position. If the available line voltage is in the 200 to 260V range, set the rotary switches to the 220V position.

CAUTION: BE SURE THAT THE VOLTAGE SELECTOR SWITCH IS SET TO THE CORRECT POSITION FOR THE LINE VOLTAGE AVAILABLE FOR <u>BOTH</u> RECEIVERS IN THE R-3030 TWO-RECEIVER ASSEMBLY.

3.4 ANTENNA

R-3030
Connect the antennas to be used to the ANTENNA receptacles on the rear panel. A separate antenna connection is made to each receiver in the assembly. As viewed from the rear of the chassis, the antenna connector on the left (J3) is connected to the receiver chassis on the left while J4 is connected to the receiver on the right. This means that the receiver connected to the antenna via J4 is controlled from the left side of the front panel and vice versa. (Front to back reverses right and left) The impedance presented to the antenna will be approximately 50 ohms with a VSWR of less than 3 to 1.

R-3080
The R-3080 has only one antenna receptacle. Connect the antenna to be used.

3.5 FREQUENCY STANDARD

The unit is designed to use either its internal frequency standard or an external frequency standard where very high accuracy is required. The internal frequency standard provides an overall frequency accuracy of approximately 1 part per million (30 Hz at the highest frequency). On special order, an internal oven stabilized crystal oscillator having an overall frequency accuracy of 0.1 parts per million may be installed in the Reference and 2nd L.O. module.

R-3030
With the rear panel REF SELECT switch set to the INT position, the rear panel REFERENCE OUT receptacle (J10) will provide an output from the internal standard in receiver number 2 (right side as viewed from the rear, left side as viewed from the front) for frequency measurement or other uses. Output frequency is optionally 1 or 10 MHz and is approximately a sine wave. Output level is approximately 0.6V peak-to-peak and the unit can deliver this voltage into a 50 ohm load.

R-3030
With the rear panel REF SELECT switch set to the EXT position, the rear panel REFERENCE IN receptacle (J9) will accept an input from an external frequency standard. The unit will require a sine or square wave at 10 MHz (optionally 1 MHz) with a level of 0.1V to 2V peak-to-peak. Input impedance is approximately 1K ohms. The signal from the external fequency standard will be repeated on the REFERENCE OUT receptacle (J10) at the same level as the internal frequency standard. NOTE: When operating from an external standard, both receivers must be turned on to insure proper operation.

R-3080
The reference input and output connections to the R-3080 are similar except, of course, only one receiver and reference oscillator is present.

Set the INT/EXT selector switch to the desired position. If required, connect coaxial cables from the frequency standard receptacles to a frequency measuring device, another receiver, or an external frequency standard as required.

3.6 WIDEBAND 1st IF MONITOR OUTPUT

A wideband 1st IF MON(itor) output from each receiver in the assembly is available on separate rear panel receptacles. This signal is centered at 40.455 MHz with a bandwidth of approximately 1 MHz. The signal level at this output is approximately 10 dB larger than the signal level into the antenna input. This output may be used for wideband reception modes or connected to a suitable spectrum analyzer. As with the ANTENNA connectors, the connector on the left (J5) is connected to the receiver on the left and vice versa for J6. The R-3080 has only one such connector.

3.7 2nd IF MONITOR OUTPUT

A narrowband 2nd IF MON(itor) output is available from both receivers in the assembly on rear panel receptacles. This signal is centered at 455 kHz with a bandwidth determined by the selected bandwidth. The signal level at this output is established by the AGC circuits to be approximately -3 to +3 dBm into a 50 ohm load over an input signal level range of -110 dBm (1 microvolt) to -10 dBm. As previously, the connector on the left (J7) is connected to the receiver on the left and vice versa for J8. The R-3080 has only one such connector.

On special order, an IF output converter board may be mounted inside the rear panel of the receiver. This board converts the normal 455 kHz IF signal to another frequency as determined by the requirements of the purchase order.

3.8 AUDIO AND ANALOG CONNECTOR

One or two of three different types of audio connectors may be found on the rear panel of the receiver. These include a 12 contact MS connector with removable crimp contacts including both twisted pair and coaxial contacts, a 19 contact MS connector with captive solder type contacts, and a single or dual 15 pin D connector with associated barrier type terminal strips.

12 CONTACT MS, REMOVABLE CRIMP

Each two-receiver assembly has a common audio and analog connector for the two receivers. This connector (J2) is a military standard type with crimp type male contacts. The cable end has socket type contacts. The connections to this connector are as follows:

MS CONNECTOR	SIGNAL OR CONTROL	REMARKS
A	RECEIVER 1 AUDIO	600 Ohm Balanced Pair
A	RECEIVER 1 AUDIO RETURN	0 dBm nominal level
B	RECEIVER 2 AUDIO	600 Ohm Balanced Pair
B	RECEIVER 2 AUDIO RETURN	0 dBm nominal level
C	SPARE	
D	SPARE	
E	RECEIVER 1 FM VIDEO	1 V/KHz coax, DC coupled
E	RECEIVER 1 FM SHIELD	
F	RECEIVER 2 FM VIDEO	1 V/KHz coax, DC coupled
F	RECEIVER 2 FM SHIELD	
G	RECEIVER 1 SIG STR ANALOG	0 to + 5V
H	RECEIVER 1 ANALOG COMMON	Ground
J	RECEIVER 2 SIG STR ANALOG	0 to + 5V
K	RECEIVER 2 ANALOG COMMON	Ground
L	SHIELD	Chassis ground
M	SPARE	

NOTE: Each balanced audio pair is connected to a single pin in the MS connector. Likewise, each FM video coaxial cable is connected to a single pin in the MS connector. In each case, both contacts are made by a single mating pin.

19 CONTACT MS, CAPTIVE SOLDER

Each two-receiver assembly has a common audio and analog connector for the two receivers. The R-3080 has connections for receiver 1 only. This connector is a military standard type with solder type female contacts. The cable end has pin type contacts. The connections to this connector are as follows:

MS CONNECTOR	SIGNAL OR CONTROL	REMARKS
M	RECEIVER 1 AUDIO	600 Ohm Balanced Pair
N	RECEIVER 1 AUDIO RETURN	0 dBm nominal level
P	RECEIVER 2 AUDIO	600 Ohm Balanced Pair
R	RECEIVER 2 AUDIO RETURN	0 dBm nominal level
G	RECEIVER 1 FM VIDEO	1 V/KHz coax, DC coupled
H	RECEIVER 1 FM SHIELD	
K	RECEIVER 2 FM VIDEO	1 V/KHz coax, DC coupled
L	RECEIVER 2 FM SHIELD	
S	RECEIVER 1 SIG STR ANALOG	0 to + 5V
T	RECEIVER 1 ANALOG COMMON	Ground
U	RECEIVER 2 SIG STR ANALOG	0 to + 5V
V	RECEIVER 2 ANALOG COMMON	Ground
A	SHIELD	Chassis ground
C,D,E,F,G	SPARES	

15 CONTACT D, TERMINAL STRIP

Each receiver has a separate audio and analog connector plus a barrier type terminal strip. The barrier strip connection data is screened on the chassis. The connections to the 15 pin D connector are as follows:

D CONNECTOR	SIGNAL OR CONTROL		REMARKS
9	RECEIVER	AUDIO	600 Ohm Balanced Pair
10	RECEIVER	AUDIO RETURN	0 dBm nominal level
13	RECEIVER	FM VIDEO	1 V/KHz coax, DC coupled
4	RECEIVER	FM SHIELD	
12	RECEIVER	SIG STR ANALOG	0 to + 5V
11	RECEIVER	ANALOG COMMON	Ground
1	SHIELD		Chassis ground
15	SPEAKER		
8	SPEAKER RETURN		

The barrier strip has only the speaker, speaker return, audio, audio return, and chassis ground connections. The speaker connections are labeled as follows:

SPKR H	Speaker high side, same as Speaker
SPKR L	Speaker low side, same as Speaker Return
AUDIO A	One side of audio balanced line, same as Receiver Audio
AUDIO B	Other side of audio balanced line, same as Receiver Audio Return
GROUND	Chassis ground, use for shield if required

It is recommended that the Speaker and Speaker Return (SPKR H and SPKR L) connections not be made common with any other signal including ground.

3.9 IEEE-488 BUS CONNECTOR

If the unit is configured for remote control via a IEEE-488 bus, connection of the unit to the bus is made via a standard IEEE-488 bus connector, which is a 24 pin ribbon type connector. It is recommended that a commercially manufactured cable be used for this connection, being sure that both the cable and connectors are completely shielded. The receiver bus connector will be found on the conector plate on the rear panel of the receiver.

Cable requirements for the IEEE-488 bus are determined by the actual system design and reference should be made to the hardware installation instructions provided with the Bus Controller. As a general guide, however, the bus cables may be connected in either a "star" or "daisy chain" fashion, or any combination of the two, and the total cable length must not exceed 20 meters (65.5 feet) or 2 meters (6.5 feet) for each bus device connected, whichever is less. The IEEE-488 bus connector on the rear panel of the receiver is of the type specified in the IEEE-488-1972 standard and uses metric studs. Be sure the locking devices are engaged on all connectors in the system.

3.10 IEEE-488 ADDRESSING AND SRQ FUNCTIONS

Each individual receiver's bus address is selectable from 0 through 30 at the rear panel address switches using 5 of the 8 switches provided. The other 3 switches are used to enable the Talker Only, Listener Only, and SRQ Enable functions. In normal operation, the talker only and listener only functions are not enabled and the receiver functions both as a talker and a listener. The SRQ Enable function may be used if desired by the system controller software.

Each separate receiver in the assembly has its own set of address and function switches. These switches will be found on the connector plate on the rear panel of the assembly.

Each receiver must be configured to a unique bus address so that the controller can send information to it independently of other devices on the bus. This is done by setting the address switches on the rear panel to the desired address between 0 and 30. The address switch has eight small switches that can be in either the up (on) position or the down (off) position. The address is set into the five left most switches in a binary code with switch number A4 as the most significant bit and switch number A0 as the least significant bit. Use the following table to determine the binary code required:

TABLE 4-1
ADDRESS SWITCHES

BUS ADDRESS	CODE 43210	BUS ADDRESS	CODE 43210	BUS ADDRESS	CODE 43210
0	00000	10	01010	20	10100
1	00001	11	01011	21	10101
2	00010	12	01100	22	10110
3	00011	13	01101	23	10111
4	00100	14	01110	24	11000
5	00101	15	01111	25	11001
6	00110	16	10000	26	11010
7	00111	17	10001	27	11011
8	01000	18	10010	28	11100
9	01001	19	10011	29	11101
				30	11110

NOTE: 0 = SWITCH DOWN, 1 = SWITCH UP

For all normal applications, set the T and L switches to the down position and the S switch to the up position.

If the switches are changed while the power is applied, the POWER switch must momentarily turned off and then back on for the unit to recognize the new address. When choosing addresses, be sure that the number selected is not in use by any other device on the bus.

3.11 SERIAL BUS CONNECTOR

If the receiver is configured for serial bus control via either an RS-232 or RS-422 connection, connections must be made through the normal connector for the selected interface. The RS-232 interface uses a 25 pin D connector while the RS-422 interface uses a 37 pin D connector. The interfaces are configured at Data Terminal Equipment (DTE) with male pins on the chassis connector.

If connected directly to a computer interface also configured as DTE, a reversal of transmit and receive date and request to send and clear to send lines may be necessary. The Request to Send and Clear to Send lines may be jumpered together on the mating connector if required by the system. These reversals or jumpers will not normally be required if the units are connected through a modem.

The connections for these interfaces are listed below.

RS-232

Signal	Pin	Function
CHASSIS	1	Safety or shield ground
TXD	2	Transmit Data, Status data from receiver
RXD	3	Receive Data, Control data to receiver
RTS	4	Request To Send (set true from receiver)
CTS	5	Clear To Send (to receiver, must be set true)
DSR	6	Data Set Ready (to receiver, not used)
GROUND	7	Logic Ground
RLSD	8	Received Line Signal Detect (to receiver, not used)
DTR	20	Data Terminal Ready (set true from receiver)

RS-422

Signal	Pin	
CHASSIS	1	Safety or shield ground
SD A	4	Send Data, Status data from receiver
SD B	22	Send Data, Status data from receiver
RD A'	6	Receive Data, Control data to receiver
RD B'	24	Receive Data, Control data to receiver
RS A	7	Request to Send (set true from receiver)
RS B	25	Request to Send (set true from receiver)
CS A'	9	Clear to Send (to receiver, must be set true)
CS B'	27	Clear to Send (to receiver, must be set true)
DM A'	11	Data Mode (to receiver, not used) (Same as DSR)
DM B'	29	Data Mode (to receiver, not used) (Same as DSR)
RR A'	13	Receiver Ready (to receiver, not used) (Same as RLSD)
RR B'	31	Receiver Ready (to receiver, not used) (Same as RLSD)
TR A	12	Terminal Ready (set true from receiver) (Same as DTR)
TR B	30	Terminal Ready (set true from receiver) (Same as DTR)

3.12 SERIAL BUS ADDRESSING AND CONFIGURATION

In order to operate the receiver under control of a serial data bus, certain functions must be set into the receiver and a bus address must be set. All of these functions are set using the front panel keypad and display with the functions retained even under power off conditions. In order to set the address and other configuration functions, switch the receiver power on, set the REMOTE/LOCAL switch to the LOCAL position, and follow the Special Function procedures. This procedure must be followed when initially installing the receiver in a serial bus control configuration.

The Special Functions including serial bus control are accessed by the key sequence "RCL SKIP" (or "RCL ·"). At this point, the channel display will show "Fn" indicating that the keypad is ready to take a function selection. The "KPAD" annunciator will be illuminated. At this point the operator may cancel by pressing the CAN key or select a function by pressing any number key from 1 through 0. Currently only the first 5 functions are implemented. Additionally, instead of pressing a number key, the operator may elect to clear all 100 memory channels to the default conditions by pressing the following key sequence "SKIP, 9, 1, 1, ENT". This process may be aborted at any stage before the ENT key is pressed by pressing CAN.

The 5 available functions are:

1 Software Version Number (Version 3.0 and up only)
2 Skip Memory Clear
3 Address Selection
4 Baud Rate Selection
5 Line Parameter Selection

Press the sequence "RCL SKIP" followed by the number of the desired special function and then follow the directions corresponding to the function pressed from the following paragraphs.

#1. Software Version Number

The Channel display will show "Sn" and the Frequency display will show the CPU software version number. This will be one or two digits, a point, and one or two more digits. Operator may press CAN or ENT which will return the front panel to normal operation. This function is useful mainly in maintenance.

#2. Skip Memory Clear

This function is used to clear the memory used to store frequencies to be skipped in sweep operation. The channel display will show "SP" and the SKIP annunciator will illuminate. The frequency display will remain blank. The operator may press CAN to cancel the operation or ENT to proceed with clearing the skip memory. In both cases the front panel will return to normal operation.

#3. Serial Bus Address Selection

This function allows user verification or modification of the Serial Interface address for the unit. The channel display will show "Ad" and the frequency display will show the current address as two decimal digits. If ENT or CAN is pressed the current address is unchanged and the panel reverts to normal operation. Alternatively, a new address may be entered by pressing two number keys. The first key press will cause the new digit to replace the left digit of the old address and a "-" to replace the right digit. The second key press will fill the right digit. At this time, pressing the ENT key will cause the old address to be replaced with the new address. Pressing the CAN key will cause the any new key entries to be ignored and the address will continue to be the old address. In both cases the front panel will revert to normal operation. If a new address is selected, it becomes effective immediately and is remembered when the power is turned off.

#4 Serial Bus Baud Rate Selection

This function allows selection of the Serial Interface baud rate from a list of options. The channel display will show "bd" and the frequency display will show the current baud rate. If ENT or CAN is pressed the current baud rate remains unchanged and the panel reverts to normal operation. If the operator presses the STEP key the frequency display will display the next selection from the list of options. Repeated pressing of the STEP key will show all options and repeat the list. At any time before pressing ENT, the operator may press CAN to retain the old baud rate and return the front panel to normal operation. Pressing ENT will cause the currently displayed baud rate to replace the old baud rate and be saved in memory. If a new baud rate is selected, it becomes effective immediately and is remembered when the power is turned off. (Available options are 110, 150, 200, 300, 600, 1200, 2400, 4800, 9600, and 19200 baud.)

#5 Serial Bus Line Parameter Selection

This function allows selection of the number of data bits, the number of stop bits and whether a parity bit is generated and if so whether parity is even or odd. The channel display will show "LP" and the frequency display will show three groups of information. From left to right these are the number of data bits ("7b" or "8b" for 7 or 8 data bits respectively), the number of stop bits ("1S" or "2S" for 1 or 2 stop bits respectively), and parity selection ("E" for even parity, "O" for odd parity, or "-" for no parity generated or checked). If ENT or CAN is pressed, the current line parameters remain unchanged and the front panel reverts to normal operation. If the operator instead presses the STEP key, the frequency display will cycle through the list of options. All 12 combinations of the three parameters are available and will appear in the display before the list repeats. At any time before pressing ENT, the operator may press CAN to retain the old line parameter selection. Pressing ENT will cause the currently displayed combination of line parameters to replace the old parameters and be saved in memory. If new line parameters are selected, they become effective immediately and are remembered when the power is turned off.

4.0 OPERATION

The receiver can be operated either by an operator using the front panel controls or remotely using a computer or bus controller. The receiver may be supplied with a remote control interface for an IEEE-488 bus, or a serial remote control interface for the bus ordered.

When operating the receiver, it is ordinarily desirable to set the receiver parameters in the following manner for signals having the indicated characteristic.

Signal	Bandwidth	Mode	AGC	BFO or IF Shift	Remarks
AM Voice	4 to 8 kHz	AM	N/A	N/A	Average AGC
SSB Voice		LSB or USB	.25		Automatic from panel
SSB Voice	2 to 4 kHz	CW	3.0	IF ± 2.3 kHz	Wideband Voice
CW Morse	.3 to .5 kHz	CW	.25	BFO .8 TO 1kHz	Operator Preference
SSB Data	.3 to 1 kHz	CW	.05	BFO 1 to 3 kHz	Narrow Band data
SSB Data	1 to 4 kHz	CW	.05	BFO 1 to 3 kHz	Wide Band data
FSK Data	.5 to 1 kHz	Frequency	.05	N/A	Narrow Band date
FSK Data	1 to 4 kHz	Frequency	.05	N/A	Wide Band data
Pulse	8 kHz	AM	Off	N/A	Manual gain reduction
Sweep	8 kHz	CW	.05	BFO 1 kHz	Search for Unknown

The LSB and USB modes select one bandwidth and IF shift automatically with no operator intervention necessary or possible. The bandwidth and shift are chosen to be optimum or as specified by the purchase order.

It is important to note that the receiver frequency set for all but LSB or USB modes is the center of the information band and does not bear any particular relationship to the carrier frequency for SSB voice or data signals while receiving in the CW mode. The IF shift function may be used to shift the apparent bandwidth with respect to the indicated frequency in the CW mode or the BFO offset may be used to vary the apparent pitch of the signal centered on the indicated frequency. Using IF shift, the apparent pitch remains the same while the position of the bandwidth varies with respect to the carrier frequency.

In all cases using the CW mode, the BFO signal is used to substitute for the carrier signal and the true carrier frequency will be equal to the indicated receiver frequency plus the BFO offset with a zero beat condition. The BFO offsets will be negative for USB signals and positive for LSB signals.

The frequency detector can be used to demodulate or determine the frequency shift of FSK data signals. A more optimum detection process will be to use the product detector in CW mode and process the resultant tones through a suitable audio modem. This technique will take advantage of narrower bandwidth filters in the audio modem and can result in data copy even in cases where selective fading has temporarily removed one of the tones.

4.1 MANUAL OPERATION

Manual operation is performed using the 20 button keypad, front panel displays, and adjustment knob. The front panel volume control is used to vary the signal level to the headphone jacks only and does not affect the level of signal supplied to the 600 Ohm balanced line. To select manual operation, set the front panel LOCAL/REMOTE switch to the LOCAL position and turn the power switch on. The receiver will power up with the frequency and other parameters last set into it before power was removed.

In order to adjust the receiver parameters, locate the parameter desired to be changed or reviewed below. Follow the instructions and indications listed and refer to the control panel pictorial in Figure 4-1.

4.1.1 Normal State -- Press CAN or ENT for the normal state

In the normal state (that is, no attempt is being made to change any of the numeric parameters), the display indicates the following information:

Function -- If the frequency and other parameters have been recalled from memory, this display indicates the 2 digit memory indication, otherwise the display is dark.

Frequency -- Display indicates the frequency in MHz -- carrier frequency in LSB or USB, center frequency in the other modes. The digit selected for tuning will be of higher intensity.

Mode -- A single letter -- L for LSB, U for USB, C for CW, A for AM, F for FM.

Bandwidth -- 2 numeric digits and a decimal point indicating the nominal bandwidth as ordered as option items.

AGC -- 2 numeric digits and a decimal point indicating the nominal AGC hold time -- 0.0, .05, .25, and 3.0. Display is dark if manual gain control has been selected.

METER -- 2 annunciators, if neither one is illuminated, the bargraph meter indicates RF signal strength; if the AUDIO annunciator is illuminated, the meter indicates audio output level; if the FREQ annunciator is illuminated, the meter indicates the relative frequency of the input signal with respect to the band center -- each bar represents 5% of the bandwidth selected.

REM -- Dark annunciator in local control

FAULT -- Dark annunciator in the absence of a fault

KPAD -- Dark annunciator

SKIP -- Annunciator used in Scan operations only.

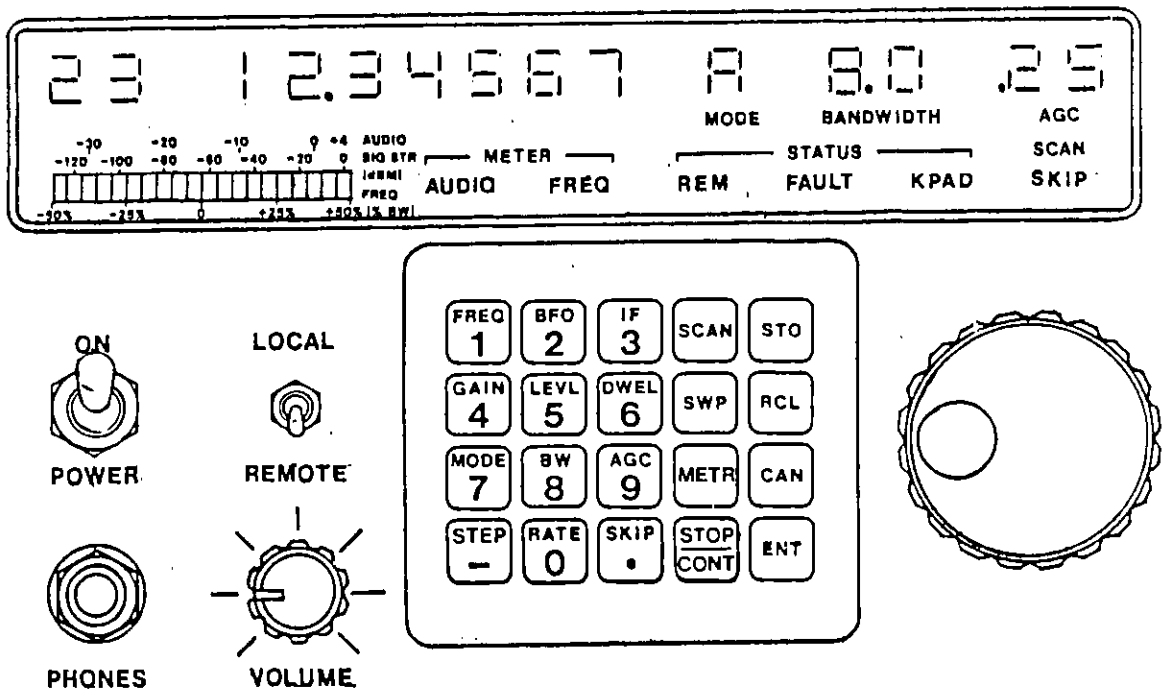


FIGURE 4-1
CONTROL PANEL PICTORIAL

4.1.2 Direct Function Changes

MODE -- Press the MODE (7) key from the normal state
Observe the MODE letter change, select the mode desired
C is CW, A is AM, L is LSB, U is USB, and F is FM

BANDWIDTH -- Press the BW (8) key from the normal state
Observe the BW value change, select the bandwidth desired
Note that bandwidth is always fixed in LSB or USB

AGC -- Press the AGC (9) key from the normal state
Observe the AGC hold time value change from off (dark), 0.0, .05, .25, and 3.0 seconds

METER -- Press the METR key
Observe the meter annunciators change from dark to AUDIO to FREQ to dark again and observe the bargraph meter indication change accordingly.

When the annunciator is dark, the meter indicates input signal strength (when AGC is enabled) from -120 to 0 dBm (into 50 Ohms). Each segment of the display represents approximately 6 dB. When AGC is disabled, the manual gain control can be used to position the indication to the middle of the meter scale.

When the annunciator indicates AUDIO, the meter indicates audio output level to the 600 Ohm line from -30 to +4 dBm (with a 600 Ohm load). Each segment of the display represents approximately 2 dB.

When the annunciator indicates FREQ, the meter indicates the approximate frequency of the signal with respect to the center of the IF bandwidth. Each segment of the display represents approximately 5% of the total IF bandwidth.
Note: when exactly on the center frequency, both segments on either side of 0 should be observed to be flashing.

RATE -- Press the RATE (0) key from the normal state.
Observe the 10 Hz, 100 Hz, and 1 kHz digit in the frequency display sucessively intensify. This function will select the digit that the adjustment knob will change when the FREQ key is later pressed.

SKIP -- Press the SKIP (.) key from the normal state.
Observe the SKIP annunciator alternately illuminate and go dark. This function is used to indicate memory channels to be skipped during a scan operation and frequencies to be skipped during a sweep operation.

4.1.3 Knob or Numeric Entry

FREQUENCY -- Press the FREQ (1) key from the normal state.
The function display should show "Fr"
The adjustment knob is enabled for the intensified digit
Digits to the right of the intensified digit will go to zero
when the adjustment knob is moved
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last frequency
Press CAN to cancel data or ENT to enter data
Receiver is now at new frequency
The KPAD annunciator should be dark

BFO OFFSET -- Press the BFO (2) key from the normal state.
The function display should show "bF"
The display should show the current BFO offset or "OFF"
The adjustment knob is enabled in CW mode only
The 10 Hz digit can then be adjusted with the 100 Hz and 1 kHz
digits changing as required
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required in CW mode only
The receiver stays at the last BFO offset
Press CAN to cancel data or ENT to enter data
Receiver is now at new BFO offset
The KPAD annunciator should be dark

IF SHIFT -- Press the IF (3) key from the normal state.
The function display should show "IF"
The display should show the current IF shift or "OFF"
The adjustment knob is enabled in CW mode only
The 10 Hz digit can then be adjusted with the 100 Hz and 1 kHz
digits changing as required
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required in CW mode only
The receiver stays at the last IF shift
Press CAN to cancel data or ENT to enter data
Receiver is now at new IF shift
The KPAD annunciator should be dark

RF GAIN -- Press the GAIN (4) key from the normal state.
The function display should show "GA"
The adjustment knob is enabled for 1 dB adjustment steps
The receiver follows the displayed value if AGC is off
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last gain reduction
Press CAN to cancel data or ENT to enter data
Receiver is now at new RF gain if AGC is off
The KPAD annunciator should be dark

LEVEL -- Press the LEVL (5) key from the normal state.
The function display should show "L"
The display should show the current level for squelch or scan stop
The adjustment knob is enabled for 1 dB adjustments steps
The receiver follows the displayed value
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press numbers and decimal point as required
The receiver stays at the last threshold
Press CAN to cancel data or ENT to enter data
Receiver is now at new level for squelch or scan stop
The KPAD annunciator should be dark
Data must be stored in a channel memory for scan or sweep stop

DWELL -- Press the DWEL (6) key from the normal state.
The function display should show "d"
The display should show the current dwell time for scan or sweep stop
The adjustment knob is enabled for one second adjustment steps
1 through 9 indicates dwell time, 0 indicates extended dwell
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes and 1 digit
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press another number as required
The receiver stays at the last dwell time
Press CAN to cancel data or ENT to enter data
Receiver is set for new dwell time for scan or sweep stop
The KPAD annunciator should be dark
Data must be stored in a channel memory to be effective

STEP -- Press the STEP key from the normal state.
The function display should show "SE"
The display should show the current step size for sweep
The adjustment knob is enabled for .1 kHz step size
Press CAN or ENT to return to normal state or;

Press any numeric key, display should clear to dashes
The adjustment knob is disabled
The KPAD annunciator should be illuminated
Press keys for the desired step size
Press CAN to cancel data or ENT to enter data
Receiver is set for new step size during sweep
The KPAD annunciator should be dark
Data must be stored in a channel memory to be effective

4.1.4 Store and Recall Functions

STORE -- Press the STO key from the normal state.
The function display should show 2 dashes.
Press 2 numeric keys in sucession (00 through 99).
All channel data is stored in the memory indicated.

RECALL -- Press the RCL key from the normal state.
The function display should show 2 dashes.
The KPAD annunciator should be illuminated.
Press 2 numeric keys in sucession (00 through 99) and/or
Use the adjustment knob to increment or decrement the channel
The display should show the recalled parameters.
The receiver remains at the last entered frequency.
Press CAN to cancel data or ENT to enter data, or;

Press the BFO (2) key to review the BFO offset recalled.
Press the IF (3) key to review the IF shift recalled.
Press the GAIN (4) key to review the RF gain recalled.
Press the LEVL (5) key to review the squelch level recalled.
Press the DWEL (6) key to review the dwell time recalled.
The adjustment knob can be used to recall data from all channels.

Press CAN to cancel recall or ENT to enter data.
The KPAD annunciator should be dark.
Receiver is on recalled frequency if ENT key pressed.
Receiver is on previous frequency if CAN key pressed.
Press skip key, SP will appear in the channel display.
Press ENT to clear skip memory at this point.

Note: Recalled memory numbers remain illuminated as long as no parameters are changed from keypad. If any parameter is changed, memory numbers are no longer displayed. New parameters must be stored to be placed back in memory.

ERASE -- To clear all memory channels of all entered data and replace data with a frequency of 10 MHz, AM mode, 8 kHz bandwidth:
Press RCL . . 9 1 1 ENT

4.1.5 Scan and Sweep Operations

All scan and sweep operations are performed from the condition where one channel has been recalled from memory and entered (using the ENT key) into the receiver. Scan is the sequential recall from memory of all channel parameters from a series of channels while sweep is the sequential entry of a series of frequencies using parameters set from one even numbered recalled channel and incrementing or decrementing the frequency as required until the frequency equals the frequency of an adjacent odd numbered channel. Multiple frequency bands can be covered in the sweep process.

Scan or sweep stop is performed when a signal is observed to be greater than the stored and recalled threshold level and the scan or sweep remains stopped for the recalled dwell time. If the recalled dwell time indicates 0, the scan or sweep will stop until the signal level falls below the threshold level. Scan or sweep rate is under the control of the adjustment knob and can also be stopped or continued under keypad control.

SCAN -- Recall and enter the desired numbered channel for scan start.
Recall, but do not enter the desired numbered channel for scan stop (may be higher or lower in number than for start).
Press the SCAN key.
The function display should show "OF".
The adjust knob will be enabled for threshold offset adjustment, and/or the keypad will be enabled for threshold offset adjustment.
The offset is + or - dB from the stored threshold level
Press ENT to start the scan
The receiver will sequentially scan from the start channel to the stop channel and continue.
The scan will stop if the signal level is above the stored level as modified by the offset adjustment.
The scan will restart at the end of the stored dwell time.
The receiver will skip all channels having the SKIP status stored.
Rotate the adjustment knob counter-clockwise to slow the scan.

Press the STOP/CONT key to stop the scan.
The adjustment knob will be enabled for frequency adjustment.
At this point, any receiver parameter may be changed under keypad and/or knob control as required.
Press the SKIP key if is desired to skip this channel on the next and successive scans.
Press the STOP/CONT key to continue the scan from stop.
Press the CAN key to leave the scan mode from stop.

Quick reference:

RCL ## ENT RCL %% SCAN * ENT**

Where *##* is the start channel, *%%* the stop channel, and *** the offset.

SWEEP -- Recall and enter the even numbered channel containing the start frequency for sweep.
Recall, but do not enter, the odd numbered channel containing the stop frequency. This may be several or many channels away from the channel selected for start.
Press the SWP key.
The function display should show "OF".
The adjust knob will be enabled for threshold offset adjustment, and/or the keypad will be enabled for threshold offset adjustment.
The offset is + or - dB from the stored threshold level
Press ENT to start the sweep.
The receiver will use the parameters in the even numbered channel recalled and entered.
The receiver will increment or decrement the frequency by the entered step size as required until the frequency equals the frequency in the next highest odd numbered channel.
The sweep will stop if the signal level is above the stored level as modified by the offset adjustment.
The sweep will restart at the end of the stored dwell time.
The receiver will skip all frequencies having the SKIP status stored in the even numbered channel at the start of each sweep.
The sweep will continue from the next even numbered channel.
The sweep will continue until the odd numbered channel recalled just before the press of the SWP key is reached.
The sweep will restart from the even numbered channel recalled and entered.
Rotate the adjustment knob counter-clockwise to slow the sweep.

Press the STOP/CONT key to stop the sweep at any time.
The adjustment knob will be enabled for frequency adjustment.
At this point, any receiver parameter may be changed under keypad and/or knob control as required.
Press the SKIP key if it is desired to skip this frequency on the next and successive sweeps.
Press the STOP/CONT key to continue the sweep from stop
Press the CAN key to leave the sweep mode from stop

Quick reference:

RCL ## ENT RCL %% SWP * ENT**

Where ## is the start channel, %% the stop channel, and *** the offset.

CLEAR SKIP -- When in normal state, the keypad sequence: RCL, SKIP, ENT clears all frequencies from the skip memory in early units. For receivers ordered and delivered after February of 1986 using version 3 software (serial bus control and other new configurations), the keypad sequence: RCL, SKIP, 2, ENT clears all frequencies from the skip memory. If the letters Fn appear in the status display after RCL SKIP, the unit has version 3 software. In these units, a press of the 2 key will cause the letters SP to appear prior to clearing of the skipped frequencies.

4.2 REMOTE OPERATION VIA IEEE-488 BUS

If the optional IEEE-488 bus module, bus connector board and appropriate CPU software is installed, the receiver may be operated under remote control using the IEEE-488 bus and a suitable bus controller. To operate in this manner, set the front panel LOCAL/REMOTE switch to the REMOTE position. If the controller takes control, the REM annunciator on the display panel will be lighted. Note that the front panel LOCAL/REMOTE switch has positive control over the remote control function. This is slightly different from the IEEE-488 standard in which the remote control device has positive control.

4.2.1 IEEE-488 Bus Description

The IEEE-488 Bus transfers data and commands between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel to the signal lines.

Eight of the lines (DIO1-DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, NDAC). The other five lines are for control of Bus activity.

Devices connected to the Bus may be talkers, listeners, or controllers. The controller dictates the role of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO1-DIO8). Addresses are set into each device at the time of system configuration either by switches built into the device or by jumpers on a PC board. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers will be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of the five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using the ASCII code. When ATN is false, any data code of 8 bits or less, understood by both talker and listener(s) may be used.

The other control lines are IFC, REN, SRQ, and EOI.

IFC (interface clear) places the interface system in a known quiescent state.

REN (remote enable) is used with other coded messages to select either local or remote control of each device.

Any device on the IEEE-488 Bus can set the SRQ (service request) line true. This indicates to the controller that some device on the Bus wants attention, e.g., a receiver has detected a signal above the programmed threshold and wants to transmit the reading to the controller.

The receiver is designed to act as a listener and talker but may be designated to operate as a talker only or as a listener only by activation of rear panel switches. In addition, the SRQ function may be activated or de-activated by means of a rear panel switch. The normal mode of operation will be for the receiver to operate as both a listener and a talker with SRQ activated.

4.2.2 Listen Data Sequence

When the receiver is addressed to listen, it accepts data in the following format:

Frequency: F1234567
Where digits 1 through 7 represent the 7 digits of the receiver operating frequency with 1 representing the most significant (10 MHz digit) and 7 representing the least significant (10 Hz).

BFO Offset: B-123
Where - represent the sign (+ or -) and 1, 2, and 3 represent the significant figures of the BFO offset with 1 representing the kHz, 2 the 100 Hz, and 3 the 10 Hz increments. Valid in CW mode only.

IF Shift: I-123
Where - represents the sign (+ or -) and 1, 2, and 3 represent the significant figures of the IF offset with 1 representing the kHz, 2 the 100 Hz, and 3 the 10 Hz increments. Valid in CW mode only.

Gain: G123
Where digits 1 through 3 represent the significant figures of the IF gain reduction with 1 representing the 100 dB, 2 the 10 dB, and 3 the 1 dB gain reduction increments. Valid with AGC off only.

Level: L123
Where digits 1 through 3 represent the significant figures of the signal level for scan or sweep stop or for squelch opening with 1 representing the 100 dB, 2 the 10 dB, and 3 the 1 dB representation of the threshold in dB below one milliwatt.

IF Bandwidth: W#
Where # represents a one character number to select the IF bandwidth ranging from 0 for the narrowest bandwidth up to 5 for the widest bandwidth.

AGC Hold Time: A#
Where # represents a one character number to select the AGC hold time ranging from 0 for the shortest hold time up to 3 for the longest hold time and 4 for no AGC. (Manual or Remote gain control only in state 4).

Mode: M*
Where * represents a one character mode code chosen from the following set: L for LSB, U for USB, A for AM, C for CW, F for FM

Dwell time : D#
Where # represents a one character number to select the dwell time after signal detection during scan or sweep operations.

Skip: SK or NSK
NSK removes the skip flag for scan operations while SK sets the skip flag. Command must be followed by a store operation to be effective in a later scan.

Step: SE##
Where ## represents the step size to be used in computing the next frequency in sweep in units of 100 Hz (e.g. SE33 represents a 3.3 kHz step size).

Offset: O-###
Where - respresents the sign (+ or -) and ### represents the number of dB above or below the stored threshold level to be used for scan or swep stop or for squelch opening.

Clear: CL
Clears all channel memory locations to 10 MHz, AM mode

Store: ST##
Where ## represents the two digits of the memory channel to store the current parameters of the receiver.

Recall: RC##
Where ## represents the two digits of the memory channel from which to recall the stored parameters of the receiver. Recalled data is entered immediately. This recalled channel data may also be used as the starting channel for scan or sweep operations. If sweep operations are required, the recalled channel number must be an even number. See SC and SW below for further information.

Cancel: K; current command is immediately cancelled

Start Scan of Memory Channels: SC##
Where ## represents the two digits of the highest memory channel to be scanned. The scan starts at the memory channel most recently recalled. See RC above and the scan description in section 4.1.5 for further information.

Start Sweep of Frequency Bands: SW##
Where ## represents the two digits of the highest odd numbered memory channel from which to take the sweep stop frequency. The sweep starts at the frequency of the memory channel most recently recalled. See RC above and the sweep description in section 4.1.5 for further information

Stop Scan or Sweep Operations: SP

Continue Scan or Sweep Operations: C

Return Unit to Local Control: T (With front panel switch in REMOTE position)

Place Unit under Remote Control: X (With switch in REMOTE position)

All characters are sent using the ASCII code representation for that character. The command sequence must be terminated by the carriage return and line feed characters. Only 1 command can be sent in any 1 message.

4.2.3 Talk Data Sequence

When the controller addresses the unit to talk and obtain a status reading on any parameter, the command shall be *? where * represents the one letter command header for any of the commands (F, M, W, A, B, I, G, L, D, S, and O) The response from the unit then contains the command header and the data characters corresponding to the listed data commands as detailed in section 4.2.2.

In addition, the following commands are recognized:

Signal Strength: SS?
The response is SS123 where the digits 1, 2, and 3 represent the equivalent signal strength in dB below one milliwatt (-103 dBm for example).

Complete Status Report: R?
The response from the unit is as follows:

F1234567B1231-123G123L123W#A$M*D#S12SS123

where the headers for each segment of the message are as defined above for commanded parameters and signal strength with the exception of step size (S).

A status byte is available by executing a serial poll. The byte returned is configured as follows:

Bit 7	6	5	4	3	2	1	0
FAULT	SRQ		SQUELCH	BUSY	ERROR	REMOTE SWITCH	

Where:

FAULT - radio fault status; updated when radio is given another command.
SRQ - IEEE SRQ status.
SQUELCH - this bit is high when the radio has open squelch.
BUSY - alerts the user the IEEE controller is busy and should not be sent another command.
ERROR - an error occurring in the receiver due to command timing.
REMOTE SWITCH - status of remote switch; 1 = switch in remote postion.

For the case where the unit is configured as a listener and a talker on the IEEE-488 bus and the SRQ function is enabled, the unit will set the SRQ line true any time that the programmed signal threshold is exceeded. This will hold true if the unit is stopped on a particular frequency or channel or if the programmed threshold level is exceeded during scan or sweep operations. If SRQ is set and the unit is addressed to talk, the signal strength message will be sent. If the unit is addressed to listen, either the signal strength or the complete status message may be requested by the bus controller. The scan or sweep operation will be halted until the SRQ is acknowledged and the status message sent.

4.2.4 Talk Only Data Sequence.

When the unit is set up to be a talker only by means of the rear panel, selector switch, the unit will send a complete status report as defined above once any time that the programmed threshold is exceeded while in a scan or sweep operation and the scan or sweep is stopped or while fixed on a particular frequency or channel. Note that this function can only be set by one receiver in the chassis assembly and that no other talker only units can be connected to the bus. This function would be useful in the case where an unaddressed printer is attached to the unit and is used for logging of frequencies where activity is sensed.

4.3 OPERATION USING SERIAL BUS

If the optional serial bus interface module, serial bus connector board and appropriate CPU software is installed, the receiver may be operated under remote control using the serial bus and a suitable bus controller. To operate in this manner, set the front panel LOCAL/REMOTE switch to the REMOTE position. If the controller takes control, the REM annunciator on the display panel will be lighted. Note that the front panel LOCAL/REMOTE switch has positive control over the remote control function. However, as with the IEEE-488 bus, the bus controller may allow local control or prevent local control when the switch is in the REMOTE position.

Insure that the communications parameters are set in accordance with the system requirements and that the unit address, if required, is set appropriately. Refer to section 3.12 for the correct installation procedures. As indicated, the baud rate, number of data bits, type of parity used, and number of stop bits must match the requirements of the system controller.

Remote operation using the serial bus is similar to operation using the IEEE-488 bus. All messages on the bus start with the ASCII character STX (start of text). Certain systems require that 3 successive STX characters be sent to initiate a valid message. This must be indicated on the purchase order. All messages are terminated by the CR character (carriage return).

Information will be passed as characters in an asynchronous serial format. Each character will consist of a start bit, 7 or 8 data bits with the least significant bit sent first, an optional parity bit which may provide odd or even parity, and one or two stop bits. The serial baud rate will be one the following standard baud rates: 110, 150, 200, 300, 600, 1200, 2400, 4800, 9600, or 19200. Number of data bits, number of stop bits, parity options and baud rate are all selectable from the front panel of the receiver through the keypad and are stored in non-volatile memory. All characters transmitted will be interpreted as conforming to the ASCII character code.

4.3.1 Message Format

All messages, whether from the controller to a receiver unit or from a receiver unit to the controller, will conform to the following format.

The first character of a message will always be STX (start of text). Optionally, 3 STX characters may be specified for a start of message indication on special order.

The next two characters will contain the address (coded in decimal) of the receiver unit sending the message or to which it is being sent by the controller. The first of these will be the most significant digit (0-9) while the next character will be the least significant digit (0-9). The address code for any receiver unit may be any digit pair from 00 to 99 provided that it is not used by any other unit connected to the bus. The controller has no address.

The next character of the message will be the beginning of the data field. This field may contain as few as one or as many as 73 characters. The data field will contain one or more messages. If more than one message is contained in the data field, each message will be separated from the next by a single blank (space) character. There is no maximum number of messages that may be included in the data field provided that the maximum number of characters is not exceeded.

The final character of the message will be a CR (carriage return). This character will follow the last character of the data field.

Example:

STX STX STX 1 5 F 1 2 0 0 0 0 0 SP M C CR

addr — data field

This message from the controller is addressed to receiver unit 15 and contains two messages: "F1200000" and "MC"

4.3.2 Message Types

All messages are divided into two major categories: Command Messages and Status Messages.

Command Messages are those messages that are sent from the controller to one of the receiver units and are subdivided into two classes: Radio Command Messages and Interface Command Messages.

Radio Command Messages contain commands that are passed to the receiver proper. They may command the receiver to change operational parameters or to report back operational status.

Interface Command Messages contain commands that are acted upon by the communications interface in the receiver unit. These commands cause the interface to change modes or other parameters.

Status Messages are those messages that are sent from one of the receiver units to the controller and are subdivided into two classes: Radio Status Messages and Interface Status Messages.

Radio Status Messages contain information about the operational status of the receiver proper. These messages are sent as a reply to Radio Command Messages that request a status report.

Interface Status Messages contain information about any errors or lack of errors caused by a previous Command Message or other source. When in the proper interface mode, the interface will respond to all command messages (except those Radio Command Messages that request an explicit Status Message and when there are no errors) with this class of message.

4.3.3 Message Protocol

The interface system will operate in one of three modes: Normal Mode, Acknowledge Mode, and Independent Mode. These modes are selected by sending the receiver unit(s) the appropriate Interface Command Message.

In Normal Mode, the receiver unit will process messages that are addressed to it but no response will be sent back unless the Command Message was a request for Status Message (Radio or Interface). The controller can verify that its Command Message(s) was received without error by sending a Command Message requesting a reply Status Message either immediately after sending the original Command Message, or after having sent Command Messages to other receiver units. This mode allows the fastest throughput of commands to a large group of receivers because the controller does not have to wait for each receiver unit to process the message(s) before moving on to the next receiver unit.

In Acknowledge Mode, a receiver unit will always respond to Command Messages with a Status Message after it has processed the Command Message. If the Command Message was for a Radio Status Message, and no errors or faults have been detected, the reply will be the requested Status Message. In all other cases, the receiver unit will respond with an Interface Status Message. This mode reduces maximum throughput because the controller must wait for the reply Status Message before issuing another command, but it simplifies the controller's job when it wants to verify the reception of its Command Messages and maximum throughput is not needed.

In Independent Mode the receiver unit will send a Status Message whenever a predefined condition occurs in its receiver such as a squelch break or a fault being detected. This will occur independently of any Command Messages. This mode is intended to be used only in non-controller systems with a terminal or printer unless the controller implements a method of handling contention. Several different sub-modes are possible for different predefined conditions. Independent mode is not defined further at this time.

4.3.4 Message Definition

In all cases the following messages are to be encoded in ASCII and inserted into the data field of transmissions as defined in the Message Format section previous. Messages from the controller may use lower or upper case for all alphabetic characters. The receiver units will always use upper case.

Interface Command Messages

MESSAGE	DEFINITION
:NORM	Set NORMAL interface mode
:ACKN	Set ACKNOWLEDGE interface mode
:IND1	Set INDEPENDENT mode 1
:?	Request Interface Status Message

Interface Status Messages

OK:NORM	No errors, NORMAL Mode
OK:ACKN	No errors, ACKNOWLEDGE Mode
OK:IND1	No errors, INDEPENDENT Mode 1
LE:PRTY	Line error - parity
LE:FRMG	Line error - framing
LE:OVRN	Line error - overrun
IE:OVFL	Interface error - buffer overflow
IE:UNKN	Interface error - unrecognized message
RE:FALT	Radio error - fault has been detected

Radio Command Messages

The following Commands follow as closely as possible the normal front panel operating key press sequences. For further details on these commands, see the Manual Operation section of the Technical Manual for the receiver.

F1234567	Change receiver operating Frequency. Digits 1 through 7 represent the seven digits of the receiver operating frequency with 1 representing the most significant (10 MHz digit) and 7 representing the least significant (10 Hz). (Range: 0000000 through 3000000)

M*	Change receiver operating Mode. * represents a one character code chosen from the following set: L for LSB, U for USB, A for AM, C for CW, F for FM.
W#	Change receiver IF BandWidth. # represents a one character number to select the IF bandwidth ranging from 0 for the narrowest bandwidth up to 5 for the widest bandwidth.
A#	Change receiver AGC Hold Time. # represents a one character number to select the AGC hold time ranging from 0 for the shortest hold time up to 3 for the longest hold time and 4 for no AGC. (Manual or Remote gain control only in state 4).
B-123	Change the BFO offset. - represents the sign (+ or -) and 1 through 3 represent the significant figures of the BFO offset with 1 representing the kHz units, 2 the 100 Hz, and 3 the 10 Hz increments. Valid in CW mode only. (Range: -999 through +999)
I-123	Change the IF Shift. - represents the sign (+ or -) and 1 through 3 represent the significant figures of the IF shift with 1 representing the kHz units, 2 the 100 Hz, and 3 the 10 Hz increments. (Range: -999 through +999)
G123	Change Manual Gain. Digits 1 through 3 represent the significant figures of the IF gain reduction in dB with 1 representing the 100 dB, 2 the 10 dB, and 3 the unit dB increments. Changing the Manual Gain turns the AGC off. (Range: 0 through 127)
L123	Change the Threshold Level. Digits 1 through 3 represent the significant figures of the signal level stopping sweep or scan or for opening squelch with 1 representing the 100 dB, 2 the 10 dB, and 3 the unit dB increments of the threshold level in dB below one milliwatt. (Range: 0 through 127)
D#	Change Dwell Time. # represents a one character number to select the dwell time after signal detection during scan or sweep operations. (Range: 0 through 9)
P##	Change SteP Size. The first # represents the kilohertz and the second # represents the 100 hertz increment of the step size to be used in sweep operation. (Range: 00 through 99)
O-123	Change the threshold Offset used in scan or sweep operation. - represents the sign (+ or -) and 1 through 3 represent the significant figures of the Offset with 1 representing the 100 dB, 2 the 10 dB, and 3 the 1 dB increments. (Range: -127 through +127)

SK or NSK	SKip Flag. SK sets the skip flag and NSK removes the skip flag for scan operations. Command must be followed by a store operation to be effective in a later scan.
ST##	STore current operating parameters into memory channel. ## represents the two digits of the memory channel being stored to. (Range: 00 through 99)
RC##	ReCall operating parameters from memory channel. ## represents the two digits of the memory channel from which to recall the parameters. Recalled data is entered immediately. This command is also used to set the starting channel for a scan or sweep operation in which case it is followed by a Scan or Sweep command.
SC##	Begin SCan of memory channels. ## represents the two digits of the highest memory channel to be scanned. The scan begins at the memory channel most recently recalled with the RC## command. (Range: 00 through 99)
SW##	Begin SWeep of frequency bands. ## represents the two digits of the highest odd numbered memory channel from which to take the sweep stop frequency. The sweep starts at the frequency of the channel most recently recalled with the RC## command. (Range: 00 through 99)
K	Cancel the command in progress.
SP	StoP the Scan or Sweep operation in progress but save parameters
C	Continue a stopped Scan or Sweep operation
CL	Clear all 100 memory channels to default parameters. Note that the receiver takes approximately 15 seconds to complete this command. No other Radio Command Messages should be sent during this time.
T	Allow Local operation (enable front panel with Local/Remote switch in Remote position).
X	Remote control operation only (disable front panel with Local/Remote switch in Remote position).
F?	Request current frequency.
M?	Request current mode.
W?	Request current IF Bandwidth.
A?	Request current AGC Hold Time.
B?	Request current BFO setting.

I?	Request current IF Shift setting.
G?	Request current Manual Gain setting.
L?	Request current Threshold Level setting.
D?	Request current Dwell Time.
P?	Request current SteP Size.
O?	Request the current threshold Offset.
S?	Request reply Radio Status Message of the received signal strength.
C?	Request report of all parameters that are now different from those reported in the last Radio Status Message.
R?	Request reply Radio Status Message of all operating parameters.

Radio Status Messages

All Radio Status Messages use the same format as the Radio Command Message for that parameter. For example, the reply to the Radio Command Message "B?" (current BFO setting) is "B-123" in the same format as the Radio Command Message to change the BFO. When more than one parameter is being reported, the individual parameters are seperated by a blank (space) character. The Reply to the R? command is as follows:

F1234567 B+009 I+099 G027 L127 W4 A4 MC D9 P12 O-020 S123

The final parameter in the above message is the Signal Strength parameter. This also is the format for the reply to the S? Radio Command Message. Digits 1 through 3 represent the significant digits of the signal strength in dB below one milliwatt where 1 represents the 100 dB, 2 represents the 10 dB, and 3 represents the unit dB increments. (Range: 0 through 127)

5.0 OPERATIONAL MAINTENANCE

Operational maintenance procedures are limited to occasional cleaning of the unit when required, isolation of faulty modules when the faults occur, and replacement of the faulty modules by complete module replacement. No internal adjustments or component replacement is to be performed at the operational level -- these functions are performed by an authorized repair depot.

5.1 FAULT ISOLATION

When operating the receiver from the front panel, the operator should be alert to potential fault conditions that would prevent the unit from operating normally. Many types of faults will cause the FAULT annunciator to be illuminated but other types of faults will not cause the fault condition to be sensed internally. A serious lack of sensitivity or low noise level should be suspected to be due to a non-sensed fault condition.

When operating the receiver from the remote control bus, the bus controller should monitor the fault condition on the bus. If this condition is observed to be set true (that is to the fault condition), the receiver can be assumed to be inoperative. If the receiver is set to receive a known test signal and no output is detected, the receiver can also be assumed to be inoperative. In the former case, the fault detectors within the various modules and the fault indicating light emitting diodes (LEDs) on the top surface of the modules can be used to isolate the fault to the failed module. If the receiver is inoperative and the fault condition is not indicated on the bus or by the module indicators, external test equipment can be used to isolate the failed module. Of course, suspected modules can be simply replaced one at a time with known good modules until the failed module is located.

Many cases of suspected fault are simply the failure of the AC power to the unit. However, this can be discovered relatively easily. Insure that the front panel circuit breaker is in the ON position and that the displays on the front panel are illuminated. If the displays are not illuminated, insure that AC power is available to the rear panel power connector.

One possibility that should never be overlooked in the event of an indicated fault is that the external frequency reference (if used) may be inoperative or that the rear panel reference selector switch may be in the wrong position. Try placing the reference selector in the INT position and examining the status of the unit again.

If a fault is suspected, remove the top cover from the unit by turning all 1/4 turn captive fasteners counter-clockwise and lifting off the cover. Use a #2 Phillips screwdriver in good condition and press down on the handle of the screwdriver to insure good contact with the fastener head to avoid damage either to the fastener or to the screwdriver.

Insure that power is applied to the unit and that the unit is set to a valid frequency within its range and that all other parameters are set to normal values. If no response is obtained from the unit and it has been determined that AC power is available, the Panel Interface or CPU modules may be suspected. If either one of these modules have failed, no response will be obtained.

Several modules contain fault detectors and indicators. Note that not all modules have fault LEDs installed. Only those modules that generate or use internally generated signals are tested for faults and display the fault condition. The modules with fault detectors are: Power Supply, 1st IF, Detector, Output Loop, Step Loop, Fine Loop, BFO, and Reference.

In the event of a fault indication, inspect the LEDs on the tops of the modules and determine if one or more are illuminated. Note that modules for two separate receivers are in the one chassis assembly. The fault isolation tables presented herein are also summarized by the tables inside the top cover of the receiver.

If only one fault indicator is illuminated, go to section 5.1.1. If more than one fault indicator is illuminated, go to section 5.1.2. If no fault indicators are illuminated and a suitable signal generator, oscilloscope, and other test equipment is available, go to section 5.1.3.

5.1.1 One Fault Indicator Illuminated

If only one of the fault indicators is illuminated, a good assumption is that the failure is within the indicated module. In the event of a failure in the wiring or in the output circuitry of another module, the other module listed below should also be investigated for possible failure. The following tables identify the possible failure modes.

LIGHT ON	FAILURE MODE
Power Supple Module	Low voltage from power supply
1st IF Module	Loss of 1st or 2nd Local Oscillator signal
Detector Module	Loss of BFO Signal
Output Loop Module	Loss of phase lock
Step Loop Module	Loss of phase lock
Fine Loop Module	Loss of phase lock
BFO Module	Loss of phase lock

LIGHT ON	OTHER MODULES WITH POSSIBLE FAILURES
1st IF Module	Output Loop Module, Reference and 2nd LO Module
Detector Module	BFO Module
Output Loop Module	Step Loop Module, Fine Loop Module, Reference Module
Step Loop Module	Reference Module
Fine Loop Module	Reference Module

5.1.2 Multiple Fault Indicators Illuminated

If multiple fault indicators are illuminated, finding the failed module is obviously more complicated. A simple process of reasoning should identify the most likely source of the problem. The power supply is obviously involved with all modules but other sources of multiple faults may not be so obvious. The following table may serve to help find the one failed module.

LIGHTS ON	SUSPECT MODULE
1st IF and Output Loop Modules only	Output Loop Module
1st IF and Reference Modules only	Reference Module (2nd LO)
Output Loop and Step Loop Modules only	Step Loop Module
Output Loop and Fine Loop Modules only	Fine Loop Module
Reference and Fine, Step, or BFO Modules	Reference Module or external ref.
Detector and BFO Modules only	BFO Module
Fine, Step, and Output Loop Modules	Reference Module or external ref.

5.1.3 No Fault Indicators Illuminated

If no fault indicators are illuminated and the unit still does not operate correctly, the trouble most likely lies within one of the modules without fault detectors. This generally will be within one of the modules in the received RF path; namely the Preselector, 1st IF, 2nd IF, or Detector modules. A complete failure of the receiver at all frequencies, bandwidths, and modes could be caused by a failure in any of the above modules. Certain types of partial failures, however, can be attributed to specific modules by following the following diagnostic table.

SYMPTOMS OF FAILURE	SUSPECT MODULE
No Display	Power Supply Module Display Board Panel Interface
No Function at all	CPU Module
Inoperative on one band only (reference section 2.1.4)	Preselector Module
Inoperative on one bandwidth only	2nd IF Module
Inoperative on one detector mode only	Detector Module

In the event that the suspect module cannot be isolated by the above table, certain rear panel monitor connections can be used to locate the possible problem. The minimum test equipment required will be an RF signal generator covering at least part of the frequency range to 30 MHz and an oscilloscope or other signal monitoring instrument having usable response to at least 40 MHz.

The following text describes one possible procedure to follow in order to isolate faults not resulting in fault light operation. A table summarizing these tests is presented on the bottom of this page.

Set the receiver to 0.0000 MHz and observe the output signal at the 1st IF monitor jack with the Oscilloscope. This signal should be 40.455 MHz with a level of approximately 300 millivolts peak-to-peak. This observation will confirm the operation of the 1st LO portions of the frequency synthesizer (Step, Fine, and Output Loop modules) and will confirm the operation of the 1st LO driver and 1st IF monitor amplifiers in the 1st IF module.

Set the receiver to any convenient frequency above 10 MHz using the remote control bus. The output level on the Oscilloscope connected to the 1st IF Monitor jack should be less than 50 millivolts peak to peak.

Apply a signal at a level of -10 dBm (0.07 volts RMS into 50 Ohms) to the Antenna connector of the receiver section being tested at that frequency set above. The output level on the Oscilloscope connected to the 1st IF Monitor jack should be approximately 250 millivolts peak-to-peak. If it is, the gain through the preselector module and the 1st mixer section of the 1st IF module is probably satisfactory. If this observation is not made, suspect the Preselector or 1st IF modules and replace one or both of them.

If the signal observation made just above is verified to be approximately 250 millivolts peak-to-peak, connect the Oscilloscope to the 2nd IF monitor connector. Insure that the receiver AGC is turned on and that 0 dB gain reduction is programmed into the receiver. Reduce the amplitude of the signal applied to the Antenna connector towards -100 dBm. The signal on the Oscilloscope should be approximately 600 millivolts peak-to-peak over the entire range at a frequency of 455 kHz. If it is not, suspect the 1st IF, 2nd IF, or detector modules and replace them.

- NO FAULT LEDS INDICATING; ALL BANDS, BANDWIDTHS, AND DETECTORS INOPERATIVE

VERIFY AC POWER AVAILABLE AND FRONT PANEL LIGHT ILLUMINATED _____

VERIFY REFERENCE SELECTOR IN INTERNAL POSITION _____

VERIFY BUS INTERFACE AND CPU MODULES OPERATIONAL _____

TESTS USING SIGNAL GENERATOR AND OSCILLOSCOPE:

FREQUENCY	SIGNAL	TEST POINT	VALID OBSERVATION	SUSPECT IF NOT VALID
0.000	NONE	1st IF MON	300 mv p-p, 40.455 MHz	1st IF Module
10 MHz	NONE	1st IF MON	50 mv p-p, 50.455 MHz	1st IF Module
10 MHz	-10 dBm	1st IF MON	250 mv p-p, 40.455 MHz	Preselector, 1st IF
10 MHz	-10 dBm	2nd IF MON	600 mv p-p, 455 kHz	1st IF, 2nd IF, Det.
10 MHz	-100dBm	2nd IF MON	600 mv p-p, 455 kHz	Detector Module

5.2 MODULE REPLACEMENT

The procedure for replacement of any of the shielded modules is very easy but care should be taken to avoid damaging any of the connectors or fasteners.

CAUTION

Switch OFF the power to the unit before removing or replacing a module.

When a suspected failed module is located, loosen the 1/4 turn captive fasteners located at the base of the module by using a #2 Phillips screwdriver in good condition. Press down firmly on the screwdriver handle and turn the fastener 1/4 turn counter-clockwise. The fastener should be observed to pop free and rise slightly. Using a module extraction tool or a pair of flat bladed screwdrivers, pry up gently on the top ears of the module to release the module from the connectors and lift the module free of the assembly.

Replacement of a module is the reverse of the above procedure, taking great care to avoid damaging the connectors when reinstalling the module. Insure that the module is correctly located in the chassis and oriented to the front of the unit and that the connectors on the bottom of the module and the connectors on the chassis assembly are aligned. The module position in the chassis is indicated on the outline and mounting drawing and the diagonal stripe on the top of the module also serves to indicate the correct module position. The stripe should form a continuous line from front to rear in the chassis with no noticeable offset.

Note that all connectors have a D shape. Be sure that the wide sides of the D are aligned on both connectors. On the modules with both a coaxial cable connector and an ordinary wire connector, the connector without the coaxial cables should be mated first. When both connectors are aligned, press the module firmly down to seat the connectors. Using the #2 Phillips screwdriver again and pressing firmly down, turn the captive fasteners clockwise 1/4 turn until they are locked into position.

When all modules have been replaced and the unit is restored to an operating condition, replace the top cover. Using the #2 Phillips screwdriver and pressing firmly down, turn the captive fasteners clockwise 1/4 turn until they are locked into position.

6.0 THEORY OF OPERATION

This section outlines the general theory of operation of the receiver. The specific operation of the various circuit boards and modules is presented in the appendix to this manual. Refer to the Block Diagram in Figure 6-1 for the modules and circuits discussed in this section.

6.1 RECEIVER SECTION

For the purposes of this discussion, the receiver section consists of those modules that process the incoming signal. The synthesizer and control sections are separately discussed. The modules in the receiver section are the Preselector, 1st IF, 2nd IF, and Detector modules plus the audio board.

6.1.1 Preselector Module

The incoming signal is applied through the rear panel RF connector to the Preselector Module. If power is applied to the unit and if the RF signal level is below approximately 1 watt, the signal is applied to the half-octave filter section through a protective relay. The RF detector will sense excess RF power and open the relay to protect the filters if required. The module is also protected by a gas tube transient suppressor that will conduct in the presence of very high voltage transients, such as those caused by static electrical discharge, as well as an initial high level signal pulse occuring before the protection relay has had a chance to open.

The half-octave bandpass filters serve to exclude out-of-band energy that could result in receiver spurious responses and also serve to reduce the local oscillator signal that may be conducted from the mixer in the 1st IF module. The filters operating above 1.6 MHz are PIN diode switched while the filters for the lower frequencies are relay switched. Relay switching is used for the lower frequencies as PIN diodes have excess distortion at low frequencies. PIN diodes are used at the higher frequencies to minimize switching time while changing frequencies and also for long term reliability reasons.

The preselector module also includes a low noise, high dynamic range, grounded gate FET amplifier. This amplifier serves to compensate for the loss in the preselector filters and the 1st mixer and thus preserve a low noise figure but it's gain is held to a low value in order to hold the signals applied to other circuits in the receiver to a minimum level and thus insure maximum dynamic range consistant with the required noise figure. The amplifier is switched out of the circuit when frequencies below 1.6 MHz are selected as it is not needed in these frequencies and the compromises required to operate in the lower frequencies would degrade the performance in the most needed 1.6 to 30 MHz range.

6.1.2 1st IF Module

The signal applied to the 1st IF module is filtered through a 30 MHz low pass filter designed to reject the local oscillator signal and prevent it from being radiated from the antenna as well as rejecting signals at the 1st IF frequency of 40.455 MHz from being impressed on the receiver.

The 1st IF module converts the input signal to the 1st intermediate frequency centered on 40.455 MHz in the first mixer. This is a very high level double-balanced diode mixer operating with +27 dBm (1/2 watt) of local oscillator signal. The output of this mixer is amplified with a grounded gate FET amplifier designed to terminate the mixer at all signal frequencies and to present a low noise figure with moderate gain.

A signal is output from the 1st IF module after the mixer but before the filter for test purposes or for analysis by other equipment.

The 1st IF filter serves to exclude signals outside a nominal 10 kHz bandwidth from the remainder of the receiver -- particularly the 2nd mixer.

The output from the 1st IF filter is attenuated (when required by signal level) by a PIN diode attenuator and amplified in another grounded gate FET amplifier exhibiting low noise figure and moderate gain. The PIN diode attenuator is only used to reduce the signal level when input signals greater than approximately -80 dBm are applied to the unit.

The second mixer converts the signal at the 1st intermediate frequency (40.455 MHz) to the second intermediate frequency (455 kHz) by mixing it with the 2nd LO signal at 40.000 MHz. This mixer is also followed by a grounded gate FET amplifier serving to terminate the mixer in a 50 Ohm load while exhibiting a low noise figure and moderate gain.

6.1.3 2nd IF Module

The 2nd IF module contains the 6 selectable bandwidth IF filters and the first stage of significant gain. The amplifier stage before the filters has only moderate gain and serves mainly to isolate the filters from the input port. The amplifier stage after the filter has approximately 50 dB of signal gain and can be controlled in gain over a 50 dB range.

6.1.4 Detector Module

The detector module is used to demodulate the signal in the manner selected and to derive the signals used for automatic gain control and signal detection. The signal input to this module is first amplified by an amplifier having a maximum gain of approximately 50 dB.

Amplitude modulated and pulse type signals are demodulated in the envelope detector. The output from this detector is itself peak detected and used for AGC and metering purposes. An averaging circuit is used to derive the AGC signal when receiving amplitude modulated signals with the AM mode selected.

Suppressed and reduced carrier signals are demodulated in the product detector. This circuit mixes the incoming signal with the BFO signal and the resulting difference signal is the desired demodulated signal.

Frequency modulated signals are demodulated in the FM detector. This circuit mixes the 2nd IF signal at approximately 455 kHz with another signal from the BFO module (in the synthesizer section) at 500 kHz. The resulting signal at approximately 45 kHz is applied to a pulse count type discriminator for demodulation. This type of discriminator is used because of its superior linearity as compared to other types and the signal is converted to a lower frequency before demodulation to optimize the stability and gain of the discriminator.

The output from the FM detector is used in two ways. When the FM mode is selected, its AC coupled output is applied to the audio circuit. At all times, its DC coupled output signal is applied to the FM video line for monitoring by external equipment. In addition, the FM video signal can be monitored by the CPU module (in the computer section) for metering purposes.

The AGC circuit is a hold or hang type circuit with selectable hold time constants. This type of AGC circuit has the characteristic of holding the IF gain constant for a period of time after the signal is sensed to be removed instead of immediately increasing the gain. When receiving voice type signals, this characteristic has the effect of eliminating the noise increase between syllables and can thus considerably improve the apparent signal to noise ratio on this type of signal. When used on signals exhibiting rapid fading, the shorter hold times can be selected.

The gain control voltage from the CPU module is applied to this module in order to achieve manual or remote gain control. When this mode is selected, the automatic gain control circuits are disconnected. In this mode, the output of the peak detector is monitored and manual or remote gain control is used to control the signal amplitude in the middle of the detector's output range. Only a few dB of manual gain control is required to control the signal amplitude over the entire useful range of this detector.

6.1.5 Audio Board

The Audio board contains the 600 Ohm balanced line transformer, the headphone amplifier, and the analog select switch for metering purposes. The detector for the audio level meter function is also contained on this board. The Audio board is mounted directly behind the Display board in the front panel area.

6.2 SYNTHESIZER SECTION

The synthesizer section is used to derive the various signals used for signal conversion and demodulation. The modules in the synthesizer section are the Output Loop, Step Loop, Fine Loop, Reference, and BFO modules.

6.2.1 Output Loop Module

The Output Loop module provides the 1st LO signal to the 1st mixer (in the 1st IF module) by phase locking a voltage controlled oscillator to the sum of the Step and Fine Loop module frequencies. This module contains three voltage controlled oscillators (VCOs) operating over the range of 40.455 to 70.455 MHz, a mixer taking the difference between the Step Loop and Output Loop signals, and a phase detector operating on the output signal from the mixer and the Fine Loop signal. Logic circuits are included to insure that the Output Loop locks only to the sum of the Step and Fine Loop signals and not to the difference frequency.

6.2.2 Step Loop Module

The step loop operates over the range of 40.400 to 70.400 MHz in 100 kHz steps by phase locking a VCO to a reference frequency of 100 kHz. This module contains three VCOs to cover the range and a complex integrated circuit that serves to vary the number by which the VCO frequency is divided (divide by N). This IC also contains a divider for the 1 MHz reference signal (divide by R) and the required phase detector as well as the control for the two modulus frequency divider (divide by A). A shift register is used to capture serial data from the CPU module (also used to program the variable dividers) in order to provide coarse tuning voltages to the Step and Output Loop modules.

6.2.3 Fine Loop Module

The Fine Loop module provides a signal to the Output Loop module in the range of 55 to 155 kHz in 10 Hz steps. It does this by dividing the output of one of three VCOs operating from 55 to 155 MHz by a factor of 1000. This technique allows for a VCO reference frequency of 10 KHZ (thus allowing for rapid phase lock loop acquisition) with an output step size of 10 Hz. The division by 1000 also substantially improves the spectral purity and frequency jitter of the output signal. The same complex IC as used in the Step Loop is used here and the shift register is used to select the VCO in use in all three synthesizer loop modules.

6.2.4 Reference Module

The Reference module provides the stable 1 MHz signal required by all synthesizer modules. This module can use the internal temperature compensated crystal oscillator (TCXO) or can use an externally supplied reference signal. A low power oven controlled crystal oscillator (OCXO) may also supplied on special order for applications where the normal 1 part per million accuracy is not considered sufficient and an accuracy of 1 part in 10 million is required. The standard design for this receiver uses an internal and external 10 MHz reference frequency. On special order, a reference module using an internal and external frequency of 1 MHz can be obtained.

The Reference module also provides the 2nd LO signal at 40 MHz by using a voltage controlled crystal oscillator (VCXO) operating at 20 MHz and comparing 1/40 of this signal frequency with 1/2 of the 1 MHz reference frequency (500 kHz). The second harmonic of the VCXO at 40 MHz is used for the 2nd LO signal. Operation in this manner insures adequate pull range in the VCXO under all conditions of crystal tolerance and temperature.

6.2.5 BFO Module

The BFO module provides a signal in the range of 445 to 465 kHz in 10 Hz steps to the product detector in the Detector module. It does this by dividing the output of one VCO in the range of 44.5 to 46.5 MHz by a factor of 100. The reference frequency for the VCO is 1 kHz so the output step size is then 10 Hz. The same type of complex IC used in the Step and Fine Loop modules is used in this module. The 500 kHz signal required by the Detector module is supplied by dividing the 1 MHz reference signal by a factor of 2.

6.3 CONTROL SECTION

The control section of the receiver is that section that performs all of the control functions including interface to the remote control bus, synthesizer data, receiver band and bandwidth, AGC and detector select, and all front panel controls and displays. The modules in the control section are CPU, Panel Interface, Bus Interface, and the Display board.

6.3.1 CPU Module

The CPU module contains the microprocessor with its associated program memory, a small amount of random access memory used for temporary registers and calculations, the analog to digital (A/D) converter used for the metering functions, the digital to analog (D/A) converter for providing remote or manual gain control, and port drivers to provide serial data to the synthesizer modules as well as parallel outputs to the receiver modules. All functions of the receiver are under the control of the program memory contained within the CPU module.

6.3.2 Panel Interface Module

The panel interface module contains the output ports to operate the displays, the input ports to sense the keypad and adjustment knob operations, the channel memory to store up to 100 channels of frequency and other information, and the temporary memory to store the frequency and other parameters upon loss of power and to restore the receiver to its last condition upon restoration of power.

The channel memory and the temporary memory both use non-volatile mode storage techniques that do not require a battery or other source of power to retain the information. The storage life for this information is essentially unlimited but the components have a write cycle limitation of several 10s of thousands of cycles. It can be expected that these components may have to be replaced after several years of operation -- particularly if the power is repeatably cycled. For this reason, these components are placed in sockets.

6.3.3 IEEE-488 Bus Interface Module

The IEEE-488 Bus interface module contains its own microprocessor and program memory to interface with the control bus plus a set of output ports that are read by the microprocessor in the CPU module as data. The IEEE-488 Bus interface module handles all handshaking on the bus without disturbing the operation of the CPU. This module also contains a dedicated IEEE-488 interface integrated circuit and bus transceivers.

6.3.4 Serial Bus Interface Module

The Serial Bus Interface module is similar to the IEEE-488 Interface module in that it also contains its own microprocessor and program memory plus a set of interface lines that are read by the microprocessor in the CPU module as data. The interface integrated circuit in this module is a programable serial data interface chip. Conversion to bus voltage levels is performed by other integrated circuits located on the bus connector board mounted on the rear panel of the receiver.

6.3.5 Display Board

The Display board contains all of the LED display elements plus the digit select and segment select drivers. The display is organized as 3 groups of 6 digits having 8 segments each. Normal intensity digits are turned on for 2 milliseconds every 16 milliseconds (a refresh rate of 62.5 Hz) while the intensified digit (when enabled) is turned on for 6 milliseconds every 16 milliseconds. Current switching transistors and current limiting resistors are located on the rear side of this board.

This board also contains connectors for interface of the keypad signals to the motherboard. No function is performed on these signals except for the connection to the motherboard.

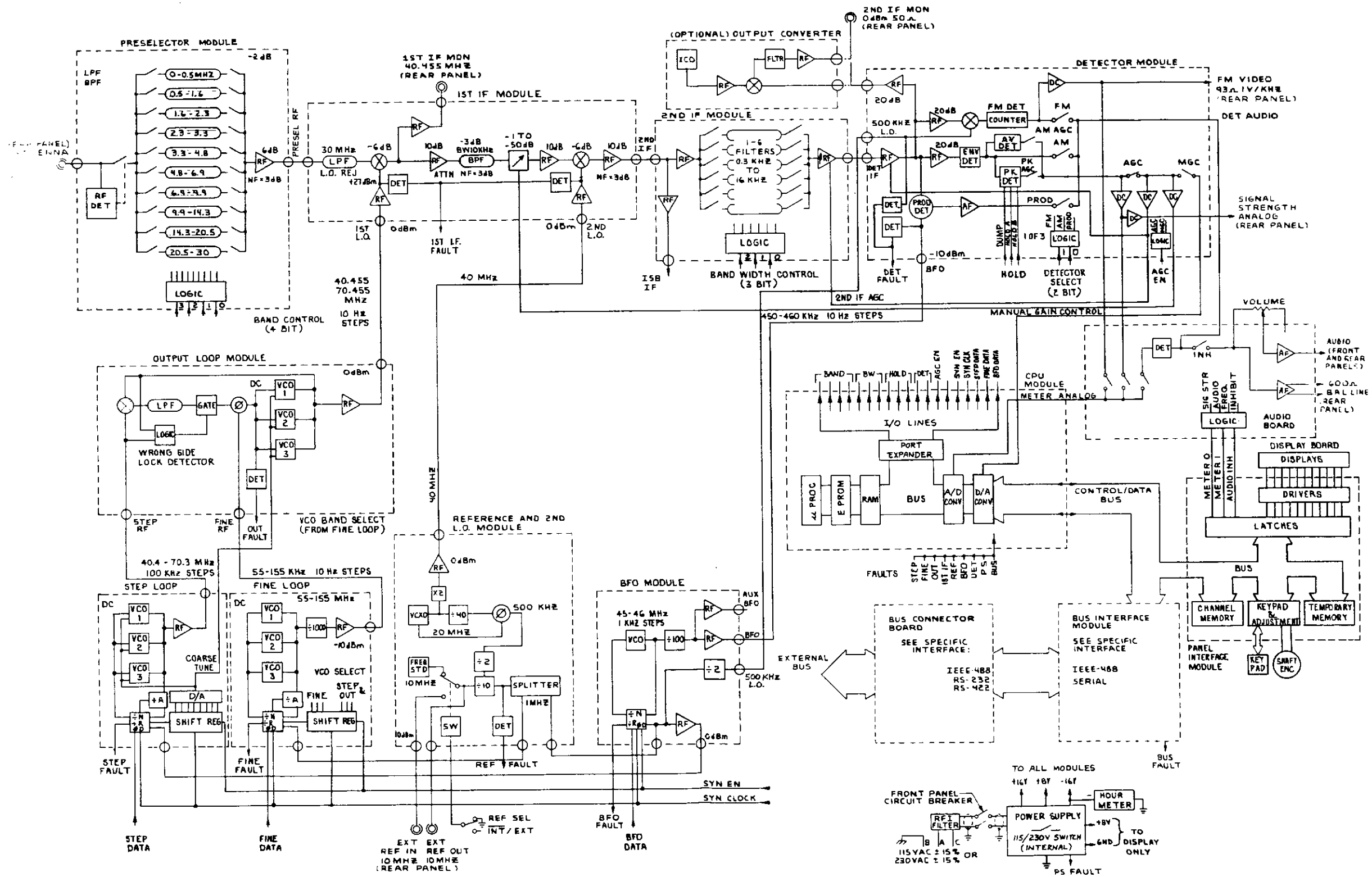


FIGURE 6-1
BLOCK DIAGRAM

7.0 REPLACEABLE MODULES

The following list of modules, boards, and components constitute the repair parts available at the operational maintainence level. Board level components are normally replaced only at the depot maintainence level and are not listed in this manual except for a few listed below. Part numbers listed for modules, boards, and components are assigned by the manufacturer, Cubic Communications Inc.

Description	Number	Remarks
Power Supply Module	2140-1124	
Preselector Module	2140-1101	
First IF Module	2140-1102	Filter not included
Second IF Module	2140-1103	Filters not included
Detector Module	2140-1104	
Output Loop Module	2140-1105	Original design
Output Loop Module	2140-1149	Improved design
Step Loop Module	2140-1150	Original design
Step Loop Module	2140-1106	Improved design
Fine Loop Module	2140-1107	
BFO Module	2140-1109	
Reference and 2nd LO Module	2140-1135	10 MHz Reference less oscillator
Reference and 2nd LO Module	2140-1146	1 MHz Reference less oscillator
CPU Module less Program	2140-1110	Program Memory required per options
Panel Interface Module	2140-1116	
IEEE-488 Bus Interface Mod.	2140-1112	
IEEE-488 Bus Connector Plate	2142-1107	Dual, for R-3030
IEEE-488 Bus Connector Plate	2721-1106	Single, for R-3080
Serial Interface Module	2140-1151	
RS-422 Connector Plate	2140-1152	
RS-232 Connector Plate	2140-1153	
Output IF Converter Bd.	2143-2001	
Audio Conn. and Terminal Bd.	2145-2001	
R-3030 Front Panel Assy.	2143-1102	Complete with display and audio boards
R-3080 Front Panel Assy.	2721-1102	Complete with display and audio boards
Display Board	2140-2016	
Audio Board	2140-2019	Fixed line level
Audio Board	2140-2067	Adjustable line level, speaker amp.
Keypad Assy.	2140-4301	Needs overlay
Keypad Overlay	180-004	Apply to keypad
Display Filter	2142-1506	
Large Knob	211-095	Adjustment knob, R-3030
Small Knob	211-096	Volume control
Crank Knob	2721-4005	Adjustment knob, R-3080
Circuit Breaker Assembly	2143-1107	
Shaft Encoder Assembly	2140-1122	
Phone Jack	342-035	
Potentiometer (Volume)	052-197	
Toggle Switch (Remote)	172-081	
Hour Meter Assembly	2140-1119	

See the notes on the next page.

1st IF Filter Note:
The 1st IF filter is soldered to the circuit board. Should replacement be required, it must be replaced with the same type. Two different types of filters are available:

BW 10 kHz 487-076 BW 20 kHz 487-084

2nd IF Filter Note:
The 2nd IF amplifier filters are soldered to the circuit board. Should replacement be required, they must be replaced by the identical type and bandwidth only. Replacement filters are available using the following part numbers:

BW	Part No.	BW	Part No.	BW	Part No.
0.3	487-089	2.7L	487-086	6.0	487-088
0.5	487-068	2.7U	487-087	8.0	487-072
1.0	487-069	3.2	487-095	16	487-075
2.0	487-070	4.0	487-071		

Reference Oscillator Note:
The oscillator assembly in the Reference and 2nd LO Module is soldered to the circuit board. Should replacement be required, it must be replaced with the same type. Three different types of oscillators are available:

1 MHz Temperature Compensated Crystal Oscillator	485-005
10 MHz Temperature Compensated Crystal Oscillator	485-008
10 MHz Oven Stabilized Crystal Oscillator	485-009

The oven stabilized crystal oscillator can be installed in the 2140-1135 module only if the A revision to the 2140-2042 circuit board is installed internally to the module. The no revision board will not accept the oven stabilized oscillator while the A revision board will accept either oscillator.

CPU Module Note:
The program memory chip to be installed in a socket in the CPU module must be specified for the installed receiver configuration. The serial bus and IEEE-488 bus require a different program memory chip as does any non-standard filter configurations. If an older version program memory chip is being replaced, the program number and revision letter must be specified. Otherwise, the current version program memory chip will be supplied by the manufacturer. These numbers can be found on labels applied to the program chip as well as the CPU module housing.

If required, extender modules may be obtained in order to test or adjust circuit modules while connected to the receiver mother board. These modules have the following identification numbers:

CPU, Bus Interface	2140-1113	2 25 pin connectors
Panel Interface	2140-1114	2 37 pin connectors
Preselector thru Detector	2140-1115	1 25 Pin, 1 5 contact coax connector
Power Supply	2140-1137	1 25 Pin, 1 2 contact H.V. connector

Connectors, wire harnesses, motherboards, and other items are also replaceable at the operational level. Consult the factory for details.

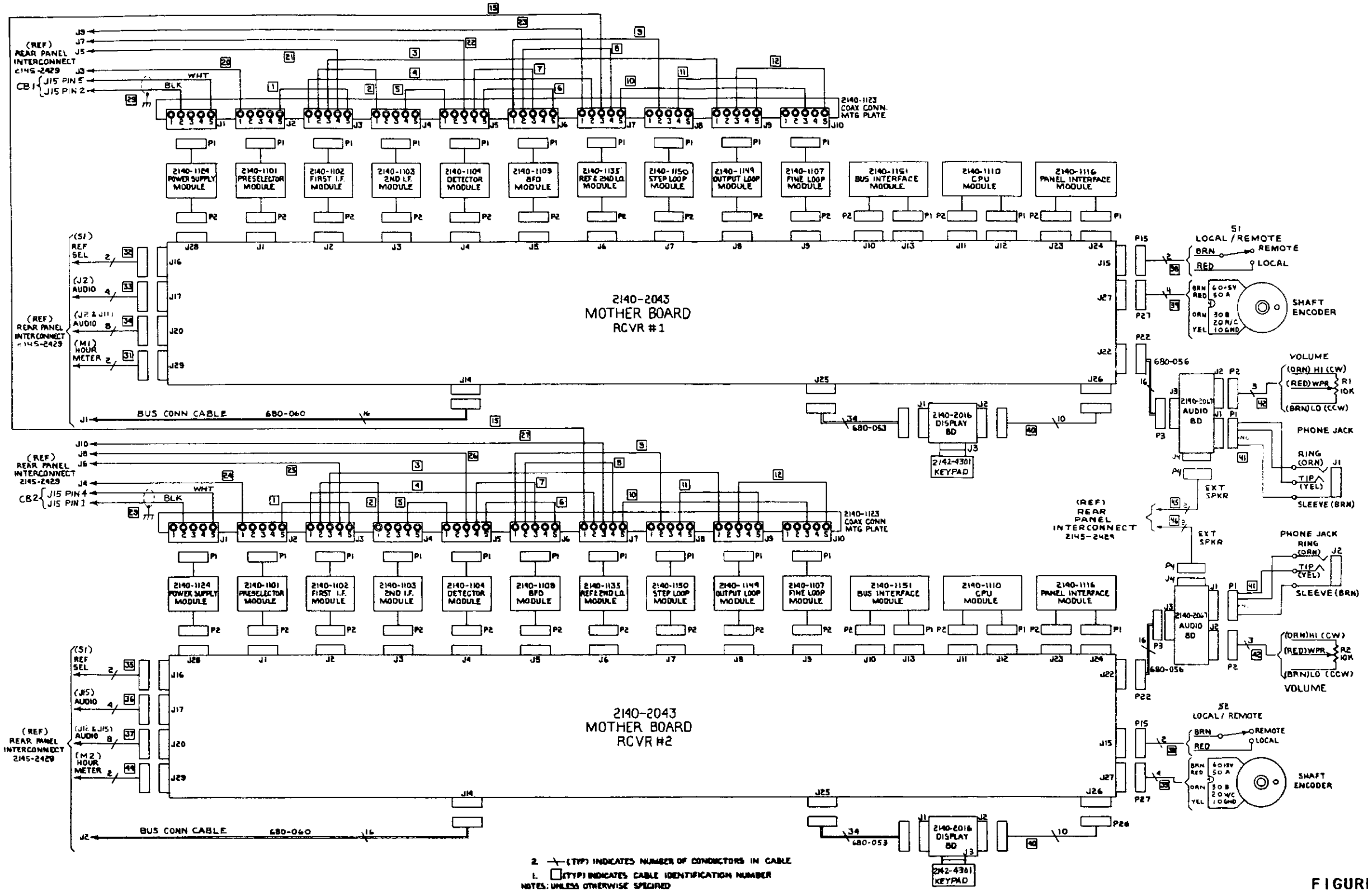


FIGURE 7-1
R-3030 CHASSIS INTERCONNECT

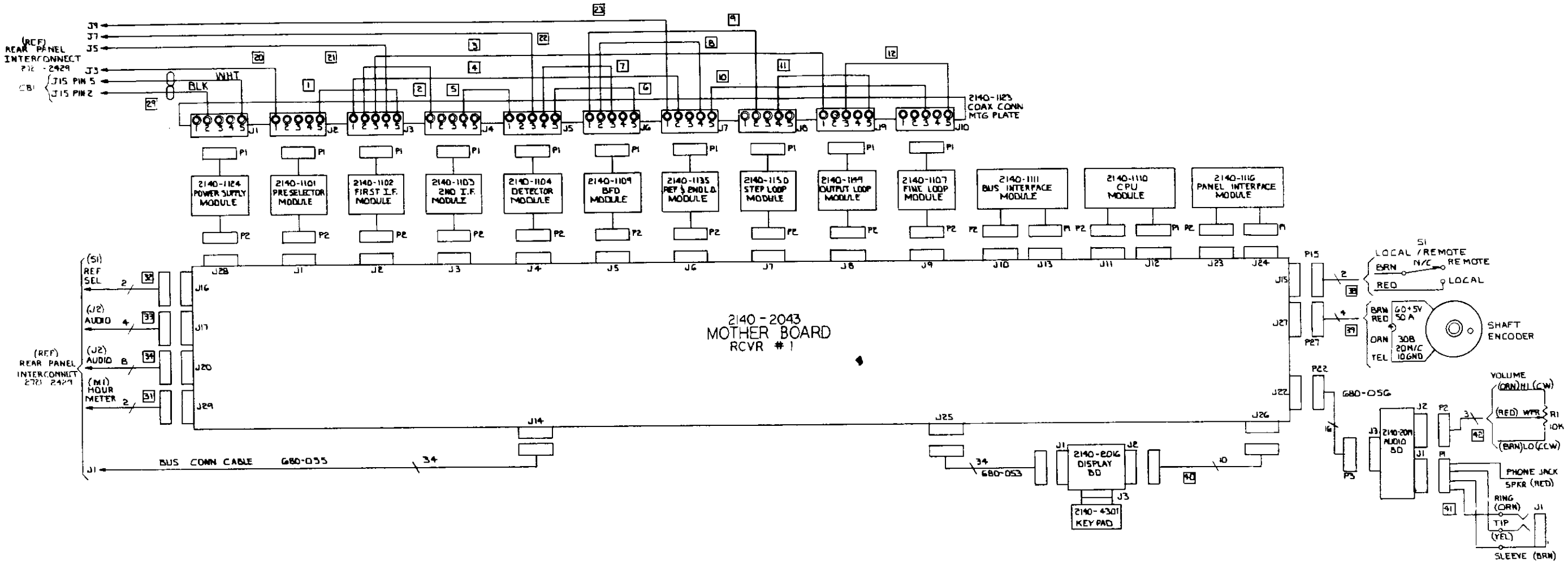


FIGURE 7-2
R-3080 CHASSIS INTERCONNECT

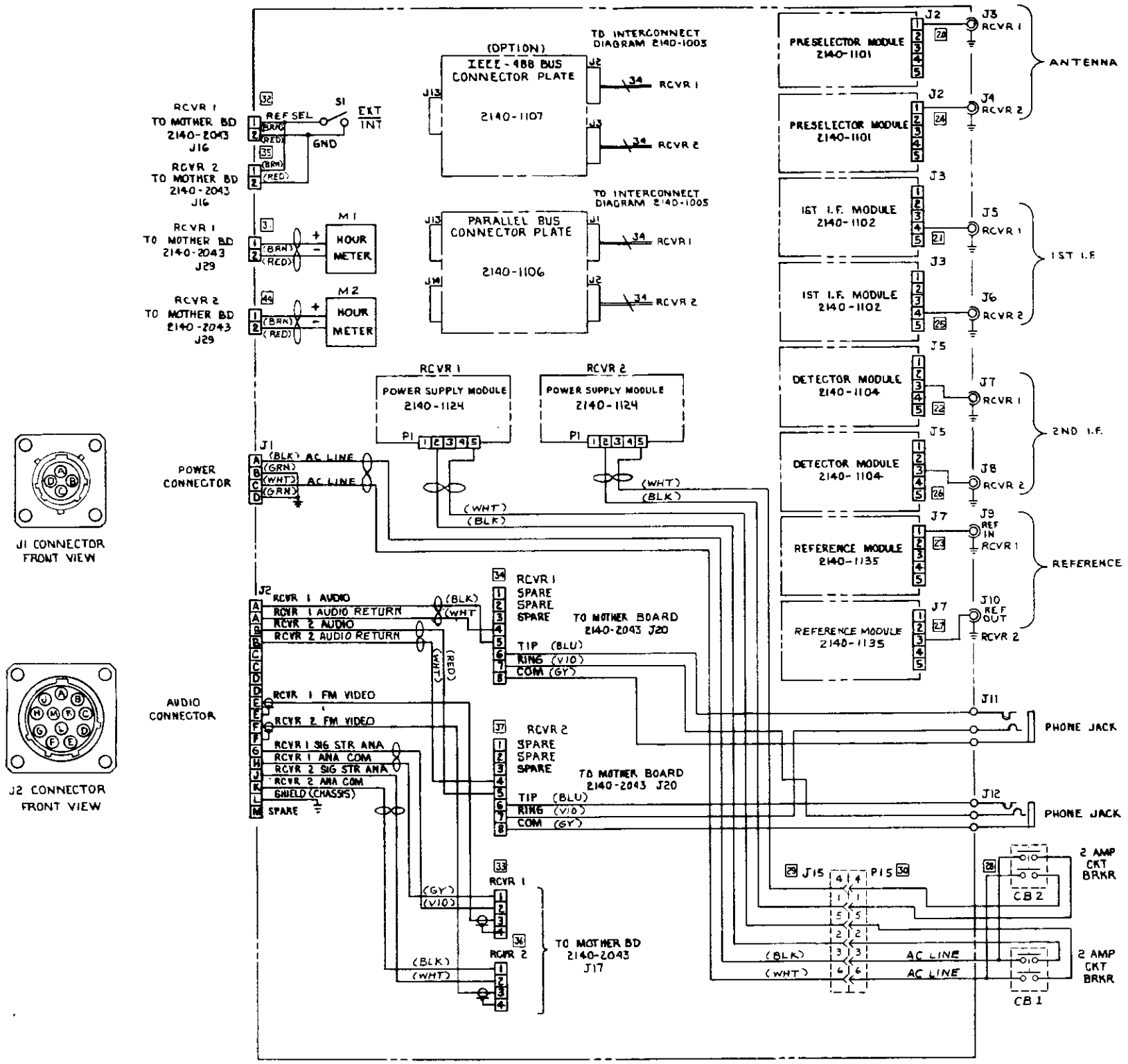


FIGURE 7-3
R-3030 REAR PANEL INTERCONNECT
12 PIN MS CONNECTOR

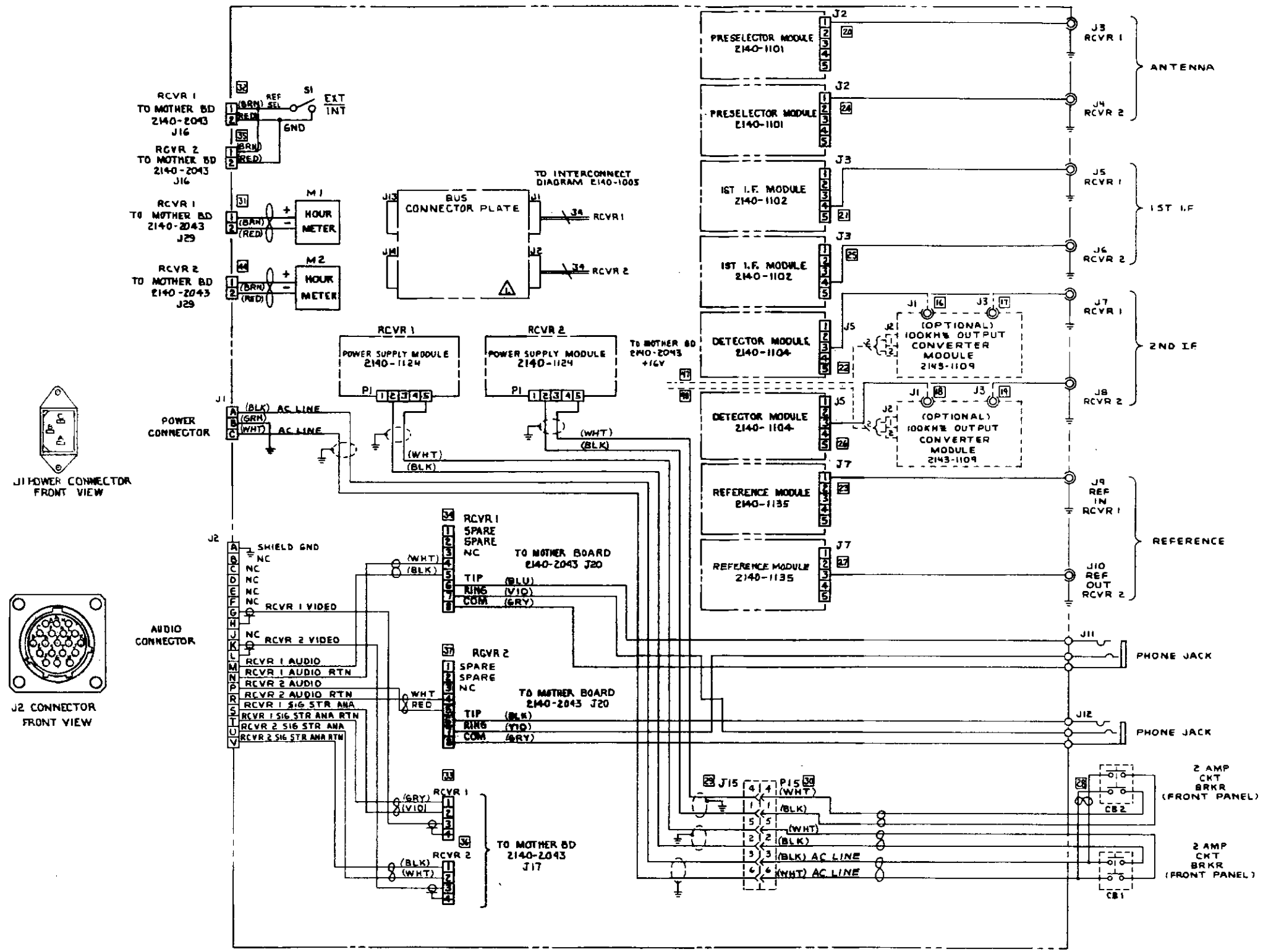


FIGURE 7-4
R-3030 REAR PANEL INTERCONNECT
19 PIN MS CONNECTOR

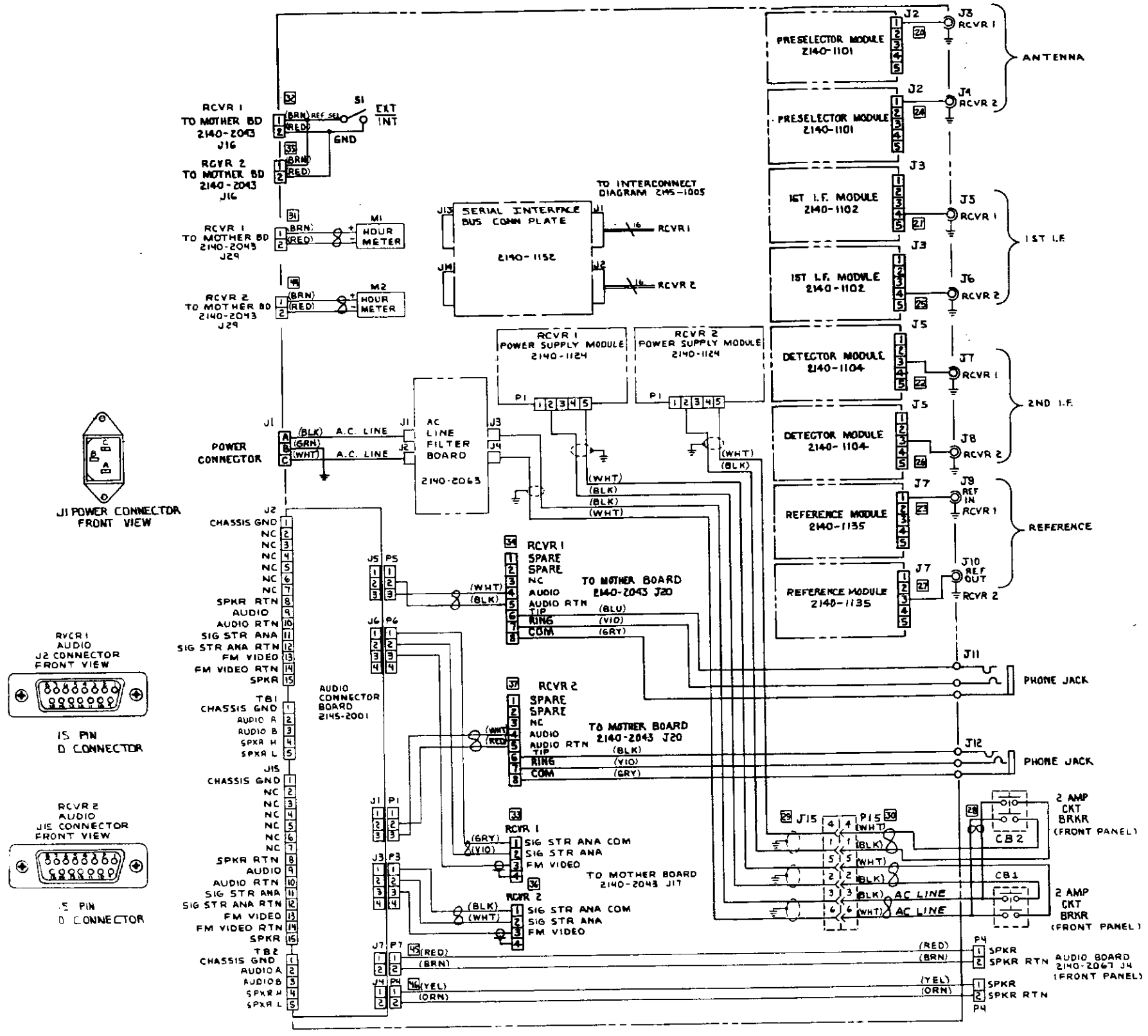


FIGURE 7-5
R-3030 REAR PANEL INTERCONNECT
D AUDIO CONNECTORS

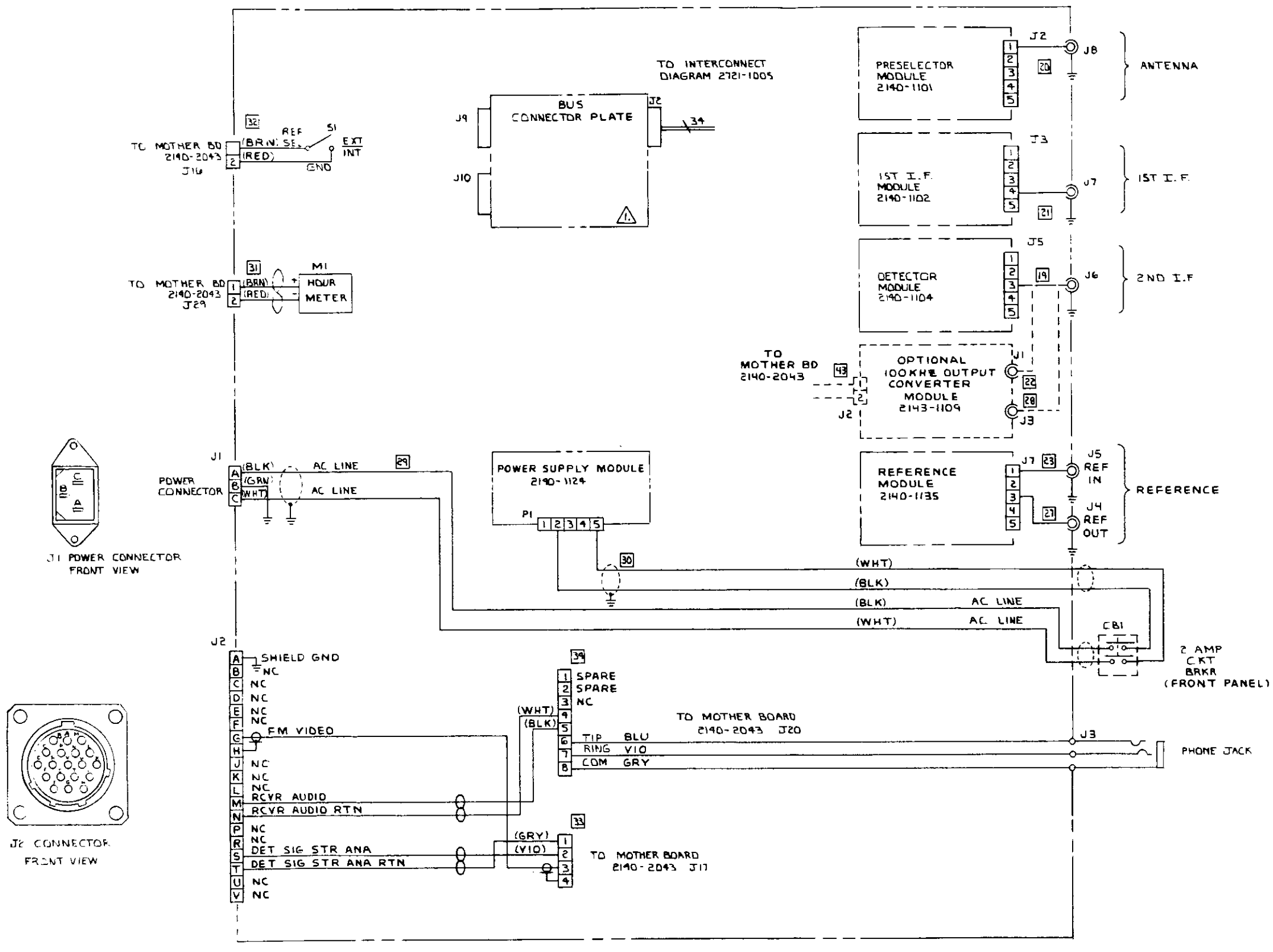


FIGURE 7-6
R-3080 REAR PANEL INTERCONNECT
19 PIN MS CONNECTOR

APPENDIX

DETAILED CIRCUIT DESCRIPTION

This appendix to the manual describes the functions of the various components and circuits of the circuit boards and shielded module assemblies. Complete component assembly location drawings and schematic diagrams are included for each module or circuit board as are parts lists organized by schematic component designator. The part number listed in the parts lists is that assigned by the receiver manufacturer, Cubic Communications, Inc. The manufacturer's name and part number listed is that of one possible manufacturer of the part -- others may be found on the circuit boards.

The distinction between circuit boards and modules in this section is simply that complete board and hardware assemblies in the completely shielded enclosures are referred to as modules. Boards may be located within modules or mounted separately.

Each individual module or board is described in an individual section of this appendix to the manual. The module names, assembly numbers, board assembly numbers, and board schematic numbers are as given below. Refer to the text section for a description of the baord or module and to the appropriate drawings as required. The module parts lists have a 12## number sequence while the board parts lists have a 24## number sequence where ## is the same as the corresponding assembly number.

NAME	MODULE	BOARD	SCHEMATIC
PRESELECTOR MODULE	2140-1101	2140-2001	2140-2401
1ST IF MODULE	2140-1102	2140-2002	2140-2402
2ND IF MODULE	2140-1103	2140-2003	2140-2403
DETECTOR MODULE	2140-1104	2140-2004	2140-2404
OUTPUT LOOP MODULE (EARLY)	2140-1105	2140-2005	2140-2405
OUTPUT LOOP MODULE (LATE)	2140-1149	2140-2061	2140-2461
STEP LOOP MODULE (EARLY)	2140-1106	2140-2006	2140-2406
STEP LOOP MODULE (LATE)	2140-1150	2140-2062	2140-2462
FINE LOOP MODULE	2140-1107	2140-2007	2140-2407
BFO MODULE	2140-1109	2140-2009	2140-2409
CPU MODULE	2140-1110	2140-2010	2140-2410
IEEE-488 BUS MODULE	2140-1112	2140-2013	2140-2413
PANEL INTERFACE MODULE	2140-1116	2140-2018	2140-2418
POWER SUPPLY MODULE	2140-1124	2140-2041	2140-2441
REFERENCE MODULE (10 MHz)	2140-1135	2140-2042	2140-2442
REFERENCE MODULE (1MHz)	2140-1146	2140-2051	2140-2451
SERIAL BUS MODULE	2140-1151	2140-2064	2140-2464
IEEE-488 CONNECTOR BOARD (DUAL)		2140-2021	2140-2421
IEEE-488 CONNECTOR BOARD (SINGLE)		2140-2056	2140-2456
RS-422 CONNECTOR BOARD		2140-2065	2140-2465
RS-232 CONNECTOR BOARD		2140-2066	2140-2466
OUTPUT CONVERTER BOARD		2143-2001	2143-2401
DISPLAY BOARD		2140-2016	2140-2416
AUDIO BOARD (FIXED LINE LEVEL)		2140-2019	2140-2419
AUDIO BOARD (ADJUSTABLE LINE LEVEL)		2140-2067	2140-2467
AC LINE FILTER BOARD (R-3030A Only)		2140-2063	2140-2463

PRESELECTOR MODULE

The Preselector module performs the task of filtering the input signal through a set of bandpass filters having a bandwidth of approximately one-half octave and providing amplification to compensate for the losses in these filters.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The incoming RF signal from the rear panel connector is applied to the module to the coaxial connector in position 1 of P1 on the Preselector Module. Protective relay K1 is initially open when the receiver is turned off but is energized (closed) when the receiver is powered up by the current applied to the base of Q2 through resistor R21. In the event of RF signal levels in excess of approximately 1 watt, the voltage divider of R19 and R20 will apply the signal to diode CR12 which conducts, turning Q1 on. This turns Q2 off and opens the relay, thus protecting the circuitry in the module from excess power. The module is also protected by a gas tube transient suppressor, E1, that will conduct in the presence of very high voltage transients, such as those caused by static electrical discharge, as well as initially high level signal pulses occuring before the protective relay has had a chance to open.

C93 couples the RF signal to one of the 8 bandpass filters above 1.6 MHz or one of the 2 low pass filters below 1.6 MHz. Taking, for example, the bandpass filter for the highest frequency band, 20.5 to 30 MHz, PIN diodes CR1 and CR2 are turned on -- all other diodes are turned off by means of the voltage developed across R1 and R6 respectively. The signal is transformed to a higher impedance by C1 and C2, resonated by L4, and coupled via resonant circuit L3 and C83 to L5, and transformed down to the nominal impedance by C3 and C4. The other bandpass filters are similar while the filters operating below 1.6 MHz are conventional low pass filters.

The half-octave bandpass filters serve to exclude out-of-band energy that could result in receiver spurious responses and also serve to reduce the local oscillator signal that may be conducted from the mixer in the 1st IF module. The filters operating above 1.6 MHz are PIN diode switched while the filters for the lower frequencies are relay switched. Relay switching is used for the lower frequencies as PIN diodes have excess distortion at low frequencies.

BDC to decimal decoder U3 selects the proper filter through line driver U2 for the bandpass filters, or Q3 and Q4 for the lowpass filters. The resulting filtered RF is coupled by C67 to the input of the low-noise, high dynamic range, grounded gate FET amplifier Q5. Constant current biasing is accomplished by Q6 and associated components. The amplifier is switched out of the circuit by relays K6 and K7 (through diodes CR23 or CR24) when frequencies below 1.6 MHz are selected. The output from the module is passed through the coaxial cable connector inserted in position 5 of P2.

ADJUSTMENTS: No adjustments are required in normal service. In the event of damage to any of the bandpass filters, the following adjustments may be made at the repair depot only using a suitable sweep signal generator, detector, and display device. A tracking signal generator and associated spectrum analyzer are recommended.

Apply the input signal to the rear panel RF input connector. Observe the output signal at the coaxial cable connector in position 5 of P1 in the 1st IF Module location (with the module removed from the receiver chassis).

FREQUENCY	ADJUST	ADJUSTMENT CRITERIA
25 MHz	L3,L4,L5	Maximum flat bandpass between 20.5 and 30 MHz
16 MHz	L8,L9,L10	Maximum flat bandpass between 14.3 and 20.5 MHz
12 MHz	L11,L12,L13	Maximum flat bandpass between 9.9 and 14.3 MHz
8 MHz	L14,L15,L16	Maximum flat bandpass between 6.9 and 9.9 MHz
6 MHz	L17,L18,L19	Maximum flat bandpass between 4.8 and 6.9 MHz
4 MHz	L20,L21,L22	Maximum flat bandpass between 3.3 and 4.8 MHz
3 MHz	L23,L24,L25	Maximum flat bandpass between 2.3 and 3.3 MHz
2 MHz	L26,L27,L28	Maximum flat bandpass between 1.6 and 2.3 MHz
1 MHz	None	Maximum flat bandpass between 0.5 and 1.6 MHz

CONNECTIONS:

P1, position 1 -- RF input, 0 to 30 MHz
P1, position 5 -- RF output, 0 to 30 MHz
P2, pin 1 -- + 16 VDC
P2, pin 6 -- Band select 0, 5V logic levels
P2, pin 9 -- Band select 1, 5V logic levels
P2, pin 8 -- Band select 2, 5V logic levels
P2, pin 7 -- Band select 3, 5V logic levels

The band select lines have logic signal levels as follows:

FREQUENCY	3	2	1	0
0.0-0.5 MHz	LOW	LOW	LOW	LOW
0.5-1.6 MHz	LOW	LOW	LOW	HIGH
1.6-2.3 MHz	LOW	LOW	HIGH	LOW
2.3-3.3 MHz	LOW	LOW	HIGH	HIGH
3.3-4.8 MHz	LOW	HIGH	LOW	LOW
4.8-6.9 MHz	LOW	HIGH	LOW	HIGH
6.9-9.9 MHz	LOW	HIGH	HIGH	LOW
9.9-14.3 MHz	LOW	HIGH	HIGH	HIGH
14.3-20.5 MHz	HIGH	LOW	LOW	LOW
20.5-30.0 MHz	HIGH	LOW	LOW	HIGH

1st IF MODULE

The 1st IF module converts the input signal to the first intermediate frequency of 40.455 MHz, filters this signal, and converts the 1st IF signal to the second intermediate frequency of 455 kHz. The gain of this module is controlled by the automatic or manual gain control functions at the higher levels of gain reduction in excess of approximately 50 dB gain reduction.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

Signal from the Preselector Module is applied to the 1st IF module through the coaxial cable connector in position 5 of P1. The signal is filtered through a multisection lowpass filter having attenuation notches. This filter is comprised of inductors L1, L2, L3, and L4 and associated capacitors.

Z1 is a very high level double-balanced diode mixer, utilizing a +27 dBm (0.5 watt) 1st LO signal of 40.455 to 70.455 MHz. The input signal in the range of 0 to 30 MHz is upconverted to 40.455 MHz in this mixer. The mixer output is split at this point; one signal is used to drive amplifier Q11 and emitter-follower Q10 for external monitoring purposes, the other to drive low-noise/moderate gain, grounded gate FET amp Q2. Constant-current biasing for Q2 is provided by Q3 and associated components. The LO signal level is detected by CR7 and is used both for 1st LO power leveling and fault detection purposes.

The first IF filter F1 serves to exclude signals outside a nominal 10 kHz bandwidth from the remainder of the receiver. The filter output passes through the PIN diode attenuator formed by CR1, CR2 and CR3, before going to the second grounded gate FET amplifier Q4. The PIN diode attenuator is driven by U1A and Q1. Constant-current biasing for Q4 is provided by Q5 and associated components. PIN diode attenuation occurs only when input signal levels are greater than approximately -80 dBm or when the signal gain is reduced by more than 50 dB.

The 1st IF signal output of Q4 at 40.455 MHz is coupled by C31 to the input of the second mixer Z2. This mixer uses the +17 dBm 2nd LO signal at 40.000 MHz to produce the 2nd IF signal centered around 455 kHz. Again, a low noise, moderate gain grounded gate FET transistor (Q6) is used to terminate the mixer in a 50 ohm load. Bias for Q6 is provided by Q8, and associated components. The output signal at 455 kHz is passed through emitter follower transistor Q7 to the output coaxial cable connector in position 2 of P1.

The 1st LO signal that is applied to the first mixer Z1 at a level of +27 dBm, initially arrives on the board from the Output Loop Module at a level of 0 dBm via the coaxial cable connector in position 3 of P1. The 1st LO is amplified by Q16 to a level determined by the automatic level control network consisting of detector diode CR7, operational amplifier U2A, transistor amplifier Q15, and PIN diode CR9. LO Level control R60 sets a DC reference for U2A. Q14 drives transformer T5, the center-tapped input transformer to a push-pull Class B amplifier formed by Q12 and Q13. Output transformer T4 drives the LO port (pin 8) of the first mixer Z1. A failure in the LO signal or LO driver circuitry as detected by CR7 will result in the FAULT line being set low and the FAULT LED being illuminated.

The 2nd LO signal on the coaxial cable connector in position 1 of P1 is a 0 dBm signal at 40.000 MHz. The output of 2nd LO amplifier Q9 drives the LO port (pin 1) of the second mixer, Z2, at a level of +17 dBm. A fault detecting circuit consisting of CR11 and U1B and associated components monitor the level of the 2nd LO signal and lights the fault LED if the level drops too low in a similar manner as a fault in the 1st LO driver.

ADJUSTMENTS: No adjustments are required in normal service. In the event of damage to any of the components, the following adjustments may be made using a suitable sweep signal generator, spectrum analyzer, and oscilloscope with a 10 to 1 probe.

1st LO Level:

Before beginning the test, verify that the output from the Output Loop Module applied to the coaxial connector in location 3 of P1 in the 1st IF module is approximately 0 dBm.

Connect the oscilloscope probe to pin 8 on Z1 with the ground lead to the nearest circuit ground. Adjust potentiometer R60 on the 1st IF Module for an indicated level of 10 v p-p at all receiver frequencies from less than 1 MHz to 30 MHz. If a variation is noted over the frequency range, adjust R60 as required for minimum deviation from 10 v p-p over the frequency range.

1st IF Monitor:

Connect the spectrum analyzer to the rear panel 1st IF Monitor jack. With all receiver modules installed, set the receiver frequency to 0.0000 MHz. Adjust L13 for maximum level on the spectrum analyzer at 40.455 MHz.

2nd IF Output:

Connect the spectrum analyzer to the coaxial cable connector in position 1 of P1 in the 2nd IF module location (with the 2nd IF module removed). Set the receiver frequency to 0.000 MHz. Set the spectrum analyzer to observe 455 kHz and adjust T2 for maximum level on the spectrum analyzer.

Input Filter:

This procedure requires a preselector module modified to bypass all bandpass filters and is normally performed only at the factory. The output of a tracking signal generator is applied to the input of the specially modified preselector module and the input to a spectrum analyzer from pin 1 on mixer Z1 is applied through a 1000 ohm resistor. For more details, the factory test procedure is available.

Adjust the spectrum analyzer controls to sweep the tracking signal generator from 0 to 50 MHz. Adjust L1, L2, L3, and L4 for a maximally flat response from 0 to 30 MHz with maximum attenuation at 40 MHz and above. The maximum attenuation in the range of 2 to 30 MHz should be not more than 2 dB below the frequency of minimum atenuation.

CONNECTIONS:

P1, position 1 -- 2nd LO input. 40.000 MHz, 0 dBm
P1, position 2 -- 2nd IF output, 455 kHz
P1, position 3 -- 1st LO input, 40.455 to 70.455 MHz, 0 dBm
P1, position 4 -- 1st IF monitor output, 40.455 MHz
P1, position 5 -- RF input, 0 to 30 MHz

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 12 -- Fault, low for fault (common with other fault lines)
P2, pin 13 -- -16 VDC (not used in this module)
P2, pin 22 -- 1st IF AGC, 0 to +8 VDC

2nd IF MODULE

The 2nd IF module filters the signal at 455 KHz through one of 5 selectable filters and provides approximately 50 dB of signal gain to this signal. The gain in this module is controlled using the automatic or manual gain control functions.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The 2nd IF signal, originating in the 1st IF Module, appears at the coaxial connector in position 1 of P1 and made available to the gates of the field effect transistor (FET) stages Q2, Q5, Q8, Q12, Q15, and Q20. Additionally, Q17 is used to provide an independent output that is not filterd for use in other model receivers using this module that also have an independent sideband mode. This output is made available on the coaxial cable connector in position 2 of P1.

Filters FL1 through FL6 are used to provide the required bandwidth for the receiver. The filter bandwidths shown are nominal and other bandwidths may be substituted on special order.

Filter selection is made by BCD to Decimal Decoder U1, which brings the Q line corresponding to the desired bandwidth HI, while the remaining 5 lines stay LO. If (for illustration) Filter 1 were selected, FET switch Q1 would pull its drain LO, putting a LO on the source of Q2, causing it to conduct, thus enabling that filter. Common-emitter amplifier Q3 would also be enabled thus providing signal to integrated circuit amplifier U2. The gain of U2 may be controlled under automatic AGC, or manual gain control. Maximum gain may be up to 50 dB. Q10 provides the output signal through the coaxial cable connector in position 4 of P1.

ADJUSTMENTS: No adjustments are normally required. If U2 or T1 are replaced, T1 may be adjusted for maximum level while receiving a signal.

CONNECTIONS:

P1, position 1 -- 2nd IF input, 455 KHz
P1, position 4 -- 2nd IF output, 455 KHz

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 4 -- BW 0, 5 V logic levels (selects filters in binary code)
P2, pin 5 -- BW 1, 5 V logic levels (selects filters in binary code)
P2, pin 7 -- BW 2, 5 V logic levels (selects filters in binary code)
P2, pin 10 -- 2nd IF AGC, 0 to +10 VDC
P2, pin 12 -- Fault (not used in this module)
P2, pin 13 -- - 16 VDC (not used in this module)

The filter select lines are activated in a binary coded fashion to select the desired filter in the manner shown below:

	BW2	BW1	BW0
Filter 1	L	L	L
Filter 2	L	L	H
Filter 3	L	H	L
Filter 4	L	H	H
Filter 5	H	L	L
Filter 6	H	L	H
BYPASS	H	H	L

DETECTOR MODULE

The Detector module demodulates the signal in any selectable mode and uses the amplitude of the signal to operate the automatic gain control and signal strength metering functions.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The signal at 455 kHz is applied to the module via the coaxial cable connector in position 1 of P1. The overall gain of the receiver is adjusted by means of potentiometer R9 so as to meet the requirements for AGC threshold, sensitivity, linearity, and other requirements.

U2 is an IF amplifier providing up to 50 dB of signal gain. Its output is filtered by the tuned circuits made up of L3, L4, and C31 so as to reduce any wideband noise contributed by the amplifiers on the detector side of the filters in the 2nd IF module.

The output of the filter is buffered by emitter follower Q3 and applied to the FM detector, envelope detector, and product detector circuits.

Begining with the FM Detector, a 500 kHz L.O. signal from the BFO module is applied to the coaxial cable connector in position 4 of P1. This signal is amplified by Q1 and applied to mixer U13 as the local oscillator signal for this mixer. The amplitude of the signal at this point is detected by CR1 and CR2 and used as one input the the module fault detector.

The signal from the IF amplifier is further amplified by Q2 and applied as the RF signal to mixer U13. The mixer takes the difference between the LO at 500 kHz and the signal at approximately 455 kHz and produces an output signal at approximately 45 kHz. U5 converts the analog signal at its input to a sequence of square waves at the same frequency. This process removes all amplitude variations in the signal and provides a trigger signal to U6.

U6A is a one-shot multivibrator triggered by the signal from U5. The output from U6 thus consists of a series of fixed width pulses having a frequency equal to the input frequency. The pulse width is chosen so that a signal at 45 kHz produces approximately a 37-63 duty cycle pulse wave. A lower frequency produces a lower duty cycle while a higher frequency produces a higher duty cycle.

The output from U6 is filtered by the fourth order lowpass filter comprised of U7A and U7B and associated capacitors and resistors. The output of this filter is then a DC voltage proportional to the deviation of the input frequency from the center frequency that can vary at a rate allowed by the low pass filter. This voltage is applied to buffer amplifier U12. R97 is adjusted so that the output voltage is 0 VDC for a signal exactly at the receiver tuned frequency. This signal is taken from the receiver as the FM VIDEO output for use by external equipment.

The output from the lowpass filter is also applied to audio select switch U8B for use by the internal audio amplifiers.

The signal for the envelope detector is amplified by Q4 and applied to the detector transistor, Q5. This is a so-called infinite impedance detector biased just to the edge of conduction by the current through R67 and R68 divided by R72 and CR6. The audio output from this detector is buffered by U4A and applied to audio switch U8B.

The DC output from this detector is averaged through U4B and R87-C65 for use as an AGC voltage when the AM mode is selected. The DC output is peak detected through CR7 for use as an AGC voltage when the LSB, USB, or CW modes are selected. R89 and C66 determine the attack time for peak AGC. C66 and R92 determine the discharge time for peak AGC.

The hold time for peak AGC action is determined by the timing of re-triggerable one-shot U6B. Variations in signal amplitude caused by modulation result in the one-shot being re-triggered through U4D and Q13. When these variations cease, the one-shot times out after a time determined by the value of C28, C67, and C68. These capacitors are selected by the Hold time select lines Hold 0 and Hold 1. For short hold time, only C28 is used. Medium hold time uses both C28 and C67 while long hold time uses C28 and C68. The Dump command (given by the CPU when AGC hold time is changed or during sweep and scan operations) times out U6B immediately and, in addition, Q15 discharges C66 in the shortest possible time.

Suppressed or reduced carrier signals are demodulated in the Product Detector. Emitter follower Q7 drives the Product Detector composed of Q8 and Q9. This circuit simply mixes the 450 to 460 kHz BFO signal with the IF to produce the desired audio signal. C53 then couples the signal to pin 11 of the Audio Select switch U8B. The BFO signal is amplified by Q10 prior to being used in the product detector.

Amplifier transistor Q6 is used to provide a sample of the IF signal for use by external equipment.

The audio signal desired and the AGC mode are selected through U8B and U8A respectively. These are dual 4 input by 1 output analog switches operating under control of the DET 0 and DET 1 signals. When both these signals are low, inputs X0 and Y0 are selected corresponding to AM mode with average AGC. When DET 0 is high and DET 1 is low, inputs X1 and Y1 are selected and the receiver uses the envelope detector with peak AGC. This mode is ordinarily only available using the parallel bus. When DET 0 is low and DET 1 is high, the FM mode is selected using X2 and Y2 while both DET 0 and DET 1 high selects the product detector with peak AGC using the X3 and Y3 inputs.

The selected audio output is amplified in integrated circuit U4C and passed to the audio board mounted behind the display board on the front panel.

The signal strength voltage from the selected detector is processed by operational amplifiers U11B and U11A. Meter zero and gain controls (R104 and R110 respectively) are used to set the signal stength voltage range between 0 and +5 V. The output from U11B is applied to the analog to digital converter in the CPU module by means of a metering analog switch on the audio board while the output from U11A is provided for use by external equipment.

Automatic or manual gain control for the receiver is determined by the state of the AGC EN signal applied through pin 17 of P2. When this signal is high, U9B (pins 3, 4, and 5) is on while U9A (pins 1, 2, and 13) is off by means of Q18 being turned on. This applies a voltage from the selected detector to U10B and U10A, the 2nd IF and 1st IF AGC amplifiers respectively and the gain is controlled automatically. When the AGC EN signal is low, the state of these two sections of U9 is reversed and the gain control voltage is derived from the digital to analog converter in the CPU module. This corresponds to manual gain control. R129 and R130 are used to convert the nominal 0 to +5 V output from the D/A converter to the values required by the gain control system.

The fault detection circuitry consists of dual comparator U3, transistors Q11 and Q12, Fault LED CR5 and associated components. U3A compares a sample of the BFO signal to a preset reference, while U3B samples the 500 kHz L.O. signal. In either case, an absence of signal produces a low output which is applied to the base of PNP transistor Q11. With Q11 turned on, LED CR5 is biased to conduct. Q11s collector goes high, turning NPN Q12 on. Q12s collector is pulled low, and this is applied to pin 12 of P2, the FAULT/ line to the CPU module. The BFO ON/OFF signal is used to disable the BFO fault detection circuitry in the AM and FM modes when the BFO signal is not used or applied to the module.

ADJUSTMENTS:

The following adjustments are normally made only after a component replacement following a repair. In the event that the Detector Module is placed in another receiver chassis or if the 1st IF or 2nd IF modules are replaced, it is possible that the AGC THRESHOLD, IF GAIN, METER ZERO, METER GAIN, MGC OFFSET, or MGC GAIN controls may require adjustment in order to make the audio output level or meter indications accurate. Do not make these adjustments unless it is absolutely necessary as some of the adjustments may interact.

Unless otherwise noted, all adjustments below are made with the receiver in CW mode with the frequency of the receiver set to the signal generator frequency and the BFO offset set to 1.00 kHz. Select the 2.0 kHz bandwidth, .25 second AGC, and IF shift of 0.000 kHz. The MGC controls are adjusted in manual gain adjust mode with the gain reduction set to the values indicated. The audio signal is observed at the 600 Ohm balanced output with a 600 ohm termination.

ADJ	FUNCTION		ADJUST FOR
L5	BFO tuning	--	maximum DC level at cathode of CR3
L3	SIGNAL tuning	--	maximum audio at P2, pin 11, -73 dBm input signal
L4	SIGNAL tuning	--	maximum audio at P2, pin 11,, -73 dBm input signal
R67	AGC THRESHOLD	--	0 dBm audio output, -73 dBm input signal
R9	IF GAIN	--	-17 dBm audio output with no signal input
R104	METER ZERO	--	bargraph indication of -100 dBm with -100 dBm input
R110	METER GAIN	--	bargraph indication of -20 dBm with -20 dBm input
R130	MGC OFFSET	--	0 dBm audio with signal = -100 dBm and gain = -27 dB
R129	MGC GAIN	--	0 dBm audio with signal = -20 dBm and gain = -107 dB
R97	FM OFFSET	--	0 bargraph indication (FREQ meter) on frequency

R67-R9, R104-R110, and R130-R129 may be interactive in adjustments

CONNECTIONS:

P1, position 1 -- IF input, 455 kHz
P1, position 3 -- IF monitor, 455 kHz, 0 dBm
P1, position 4 -- 500 kHz LO, 0 dBm
P1, position 5 -- BFO, 450 to 460 kHz, 0 dBm, CW, LSB, or USB modes only

P2, pin 1 -- +16 VDC
P2, pin 3 -- Ground
P2, pin 5 -- Detector Audio, 2 V p-p
P2, pin 8 -- Audio Common
P2, pin 9 -- MGC Voltage, 0 to + 5 VDC
P2, pin 10 -- 2nd IF AGC, 0 to + 10 VDC
P2, pin 11 -- Signal Strength Analog, 0 to + 5 VDC
P2, pin 12 -- FAULT/, low for fault
P2, pin 13 -- -16 VDC
P2, pin 14 -- DET 0, 5 V logic
P2, pin 15 -- DET 1, 5 V logic
P2, pin 16 -- Hold 0, 5 V logic
P2, pin 17 -- AGC Enable, +5 VDC for AGC, 0 for MGC
P2, pin 18 -- DUMP/, low pulse for dump
P2, pin 19 -- Hold 1, 5 V logic
P2, pin 22 -- 1st IF AGC, 0 to + 10 VDC
P2, pin 23 -- SIG STR, 0 to + 5 VDC
P2, pin 24 -- FM Video, 0 ± 1 Volt per kHz
P2, pin 25 -- BFO ON/OFF, low in CW, LSB, and USB, high in FM and AM

OUTPUT LOOP MODULE

The Output Loop module provides the 1st LO signal to the 1st mixer (in the 1st IF module) by phase locking a voltage controlled oscillator to the sum of the Step and Fine Loop module frequencies. This module contains three voltage controlled oscillators (VCOs) operating over the range of 40.455 to 70.455 MHz, a mixer extracting the difference between the Step Loop and Output Loop frequencies and a phase detector comparing this difference frequency with the Fine Loop frequency. Logic circuits are included to insure that the Output Loop locks only to the sum of the Step and Fine Loop signals and not to the difference frequency.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (40.4550 to 48.7499 MHz), MED range (48.7550 to 58.6499 MHz) and HI range (58.6550 to 70.4550 MHz). These ranges correspond to receiver tuned frequency 0 to 8.2990, 8.3 to 18.1990, and 18.2 to 30 MHz respectively.

These three circuits are nearly identical. Looking at the HI range VCO (for example), it is comprised of junction field effect transistor (JFET) Q1, transformer T1, trimmer capacitor C2, varactor diodes CR1 and CR2, and associated components. NPN Transistor Q2 is used to select the particular VCO under control of the VCO select lines on P2, pins 7, 8, and 9. Diode CR3 provides signal detection for oscillator amplitude control while PIN diode CR4 couples the output of the oscillator to the other circuits.

Coarse tuning voltage originates in the Step Loop Module, and fine control voltage is provided by the output of the Loop Amplifier U5A. The individual VCO Select lines come from the Fine Loop shift register (CPU driven) on P2 pins 7, 8 and 9. VCO Select requires a logic high to enable.

Emitter-follower amplifiers Q7 and Q19 serve as buffers for the output of the selected VCO to isolate the VCO from the other signals in the module. Feedback amplifier Q8 provides the output signal from this module via the coaxial cable connection in P1, position 1 for application to the 1st IF module.

The signal from Q19 is applied both to the mixer circuit of Z1 through amplifier Q12 and the wrong-side-lock detector of U2 through U1D.

The Step Loop signal, input on the coaxial cable at P1 position 5, is passed by emitter-follower Q9 and placed on Pin 1 of Mixer Z1. This signal is also applied to the wrong-side-lock detector U2 through U1A.

The mixer (Z1) takes the difference in frequency between the Step Loop and Output Loop frequencies and passes this difference frequency through the low pass filter of L6, L7, and capacitors C62, C63, and C65. This difference signal is then applied to the Level Shifter circuit composed of Q13, Q14 and associated components which transforms the analog signal to a logic level signal. The logic level output of the Level Shifter is then applied to the gates of U3 to the phase detector U4.

The second input of Phase Detector U4 orignates in the Fine Loop Module. The coaxial cable in P1, position 3 passes this 55 to 155 kHz signal to amplifier Q10, through NOR gate U3C and on to the pin 1 input port of U4. The difference frequency signal from Z1 is applied to pin 3 of U4.

Two of the outputs of this phase detector are operative. The U2 signal on Pin 12 drives the Out-of-Lock Fault Detector circuit through U5B and the UF and DF signals on pins 5 & 10 drive the Loop Amplifier, U5A. The output from U5A on pin 1 provides the Fine Control Voltage applied to varactors CR2, CR6 and CR10 in the three VCOs.

The fault output of Phase Detector U4 pulses low when the loop is not locked. U5 pin 7 goes high at this time, turning Q15 on, biasing fault LED CR14 to conduct and become illuminated. Similarly, transistor Q16 is turned on, placing a low on the Output Fault line on P2, pin 12.

The Wrong-side Lock Detector (U2) is a phase/frequency comparator whose emitter-coupled-logic (ECL) output signals are converted to 5 volt saturated logic levels by emitter coupled matched pair transistors Q11 and Q18. These transistors operate to pulse Q11 on and off at the difference frequency rate when the Output Loop frequency is greater than the Step frequency. CR13 conducts on the positive pulses, charging C47, and turning Q17 on. This places a low logic level at NOR gate U3B pin 6 allowing normal operation by passing the difference frequency signal from U3A. If U2 detects the Output frequency to be less than the Step frequency, Q11 turns off, as does CR13, placing a high at U3B, pin 6. This disables the input to U4, pin 3 and causes the selected VCO to be driven to a higher frequency.

When the wrong-side-lock detector circuit senses that the Output Loop frequency is higher than the Step Loop frequency, the phase detector, U4, operates so that the difference between the Output Loop and Step Loop frequencies is equal to the Fine Loop frequency and the difference frequency is phase locked to the Fine Loop frequency.

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP2. This test point is also connected to pin 14 on P2 on the module motherboard connector. Set the vertical controls to DC coupling, .5 V/division (including the probe division)

T3

Tune the receiver in turn to each of the following frequencies: 0.0 MHz, 3.9 MHz and 8.2 MHz. Observe the Oscilloscope and check if the voltage at TP2 remains inside the limits of 0.0 VDC ±2.0 V for each frequency . If not, observe the trend in voltage. If these voltages remain within 2.0 V of each other for each of the three frequencies, adjust T3 so the voltage at the middle of the 3 frequencies is 0.0 VDC.

T2, C11

Perform the procedure substituting the following frequencies:
8.3 MHz, 13.0 MHz, 18.1 MHz

If the voltage tends to increase with increase in frequency, reduce the capacitance (less mesh) of C11 a small amount and adjust T2 for 0.0 VDC at TP2 at the center frequency. If the voltage tends to decrease for an increase in frequency, increase the capacitance of C11 (more mesh) a small amount and adjust T2 for 0.0 VDC at TP2 at the center frequency. Repeat step 2 until first criterion is met (0.0 VDC ±2.0 V on all three frequencies).

NOTE: It is normal for C11 to be nearly fully meshed when done.

T1, C2

Perform the procedure substituting the following frequencies:
18.2 MHz, 23.8 MHz, 30.0 MHz

NOTE: Trimmer cap C2 should not be fully meshed when done.

The output level on the coaxial cable in position 1 should be between 140 and 300 mV peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 1 -- 1st LO output
P1, position 3 -- Fine Loop RF input to module
P1, position 5 -- Step Loop input to module

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (synthesizer enable signal, not used in this module)
P2, Pin 6 -- SYN CK (synthesizer clock signal, not used in this module)
P2, Pin 7 -- VCO LO (high to select)
P2, Pin 8 -- VCO HI (high to select)
P2, Pin 9 -- VCO MED (high to select)
P2, Pin 10 -- Coarse Tune Voltage
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test Point, loop control voltage

STEP LOOP MODULE

The Step Loop module provides a phase locked signal from 40.4 to 70.4 MHz in 100 kHz steps to the Output Loop module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (40.4 to 48.6 MHz), MED range (48.7 to 58.5 MHz) and HI range (58.6 to 70.4 MHz). These frequency ranges correspond to receiver tuned frequencies of 0 to 8.2999, 8.3 to 18.1999, and 18.2 to 30 MHz respectively.

These three circuits are nearly identical. Looking at the HI range VCO (for example), it is comprised of junction field effect transistor (JFET) Q1, transformer T1, trimmer capacitor C2, varactor diodes CR1 and CR2, and associated components. NPN Transistor Q2 is used to select the particular VCO under control of the VCO select lines on P2, pins 7, 8, and 9. Diode CR3 provides signal detection for oscillator amplitude control while PIN diode CR4 couples the output of the oscillator to the other circuits.

The output of the selected VCO is coupled by C30 to the base of NPN buffer Q7 and amplified by Q8 for input to the Output Loop Module. Q7s emitter output is also used to drive the frequency input of dual modulus prescaler U1, a divide by 20 or 21 device (selectable via pin 1). U2, which receives its frequency input from U1, is a multi-function synthesizer chip, incorporating programmable divider, reference divider, and phase detector into a single package. In addition to the 1 MHz Step Reference, U2 also receives data, clock and enabling inputs from the CPU under program control.

Shift register U4 provides Digital to Analog Converter U3 with the 8-bit information necessary for it to drive operational amplifier U5B. The output from U5B, pin 7, is an analog voltage (±8 V) used as input to the VCOs as a coarse tuning control voltage (TP1). In line with the coarse tuning voltage is a noise reduction filter composed of C29, R20, C56 and R36. Diodes CR17 through CR20 act as a speed-up circuit when new frequencies are selected.

Synthesizer circuit U2 generates the fine tuning control voltage at pin 5 (TP2) which is applied to the cathodes of varactors CR2, CR6 and CR10 and provides a lock detector signal for input to the one-shot multivibrator U6A. This lock detector signal input (from U2 pin 7) pulses when the loop is not locked. U6A and associated components form the fault detector circuit. When the U6A pin 7 output goes low during a no-lock condition, PNP transistor Q9 is biased to conduct, turning Fault indicator LED CR16 and transistor Q10 on, putting a low on the module Fault line.

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP2. Set the vertical controls to DC coupling, .5 V/division (including the probe division)

T3, C20

Tune the receiver in turn to each of the following frequencies: 0.0 MHz, 3.9 MHz and 8.2 MHz. Observe the Oscilloscope and check if the voltage at TP2 remains inside the limits of 2.5 VDC ±0.5 V for each frequency . If not, observe the trend in voltage. If these voltages remain within 0.5 V of each other for each of the three frequencies, adjust T3 so the voltage at the middle of the 3 frequencies is 2.5 VDC. If the voltage tends to increase with increase in frequency, reduce the capacitance (less mesh) of C20 a small amount and adjust T3 for 2.5 VDC at TP2 at the center frequency. If the voltage tends to decrease for an increase in frequency, increase the capacitance of C20 (more mesh) a small amount and adjust T3 for 2.5 VDC at TP2 at the center frequency. Repeat step 2 until first criterion is met (2.5 VDC ±0.5 V on all three frequencies).

T2, C11 Perform the procedure substituting the following frequencies: 8.3 MHz, 13.0 MHz, 18.1 MHz

T1, C2 Perform the procedure substituting the following frequencies: 18.2 MHz, 23.8 MHz, 30.0 MHz

The output level on the coaxial cable in position 4 should be between 0.45 and 1.4 V peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 2 -- Reference input, 1 MHz
P1, position 4 -- Step RF output from module to output loop

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- STEP DATA (Step Loop data)
P2, Pin 6 -- SYN CLK (Synthesizer data clock)
P2, Pin 7 -- VCO LO
P2, Pin 8 -- VCO HI
P2, Pin 9 -- VCO MED
P2, Pin 10 -- Coarse Tune Voltage
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

FINE LOOP MODULE

The Fine Loop module provides a signal from 55 to 154.99 kHz in 10 Hz steps to the Output Loop module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The three VCOs in this module are Hartley type oscillators, organized by frequency into a LO range (55.0 to 77.69 MHz), MED range (77.7 to 109.73 MHz) and HI range (109.74 to 154.99 MHz). These frequency ranges correspond to tuning of the receiver between 100 kHz increments with the LO range corresponding to xx.x0000 to xx.x2269 MHz, the medium range corresponding to xx.x2270 to xx.x5473 MHz, and the HI range corresponding to xx.x5474 to xx.x9999 MHz. xx.x represents any MHz and 100 kHz frequency. The oscillator generates these frequencies in 10 kHz steps.

These three circuits are nearly identical. Looking at the LO range VCO (for example), it is composed of JFET Q1, transformer T1, varactor CR1, and associated components. The individual VCO Select lines come from shift register U5 (CPU driven) at pins-11, 12 and 13. VCO Select requires a logic high to enable, applied to the base junctions of Q2, Q4 and Q6 for the LO, MED and HI ranges respectively.

The output of the selected VCO is coupled by C23 to emitter-follower Q7. The output is split at this point, one side driving Prescaler U3, the other inputing a Divide-by-1000 chain composed of U1 (divide by 40) and U2 (dual divide by 5). The 55 - 154.99 kHz output result (in 10 Hz increments) exits the module via the coaxial cable in P1, position 5 for input to the Output Loop Module.

U3 is a dual modulus prescaler (divide-by-32/33) device which both provides a signal to U4, and receives (a divide-by-A) instruction from U4. U4 is a multi-function synthesizer chip, incorporating programmable divider, reference divider and phase detector into a single package. In addition to the Prescaler frequency and 1 MHz Reference, U4 also receives data, clock and enabling inputs from the CPU under program control. Eight-bit shift register U5 interfaces incoming CPU serial data for VCO selection in all three Loop Modules, as well as data to multi-function U4 and the BFO ON/OFF data line (P2 pin 11) to the BFO Module itself.

The pin 7 (Lock Detector) output of U4 is a normally high signal which will pulse low in the event of an "out-of-lock" condition. Out of Lock Detector U7A (a retriggerable multivibrator) will sense this on its input and hold its pin 7 output low in response. PNP Fault Driver Q8 is biased on, enabling Fault LED CR11. With its base juction pulled high, NPN Q9 conducts and outputs a logic low from its collector to P2 pin-12 (FAULT/).

The pin 5 (Phase Detector) output of multi-function U4 is an analog voltage corresponding to the degree of phase or frequency error between the VCO frequency and the desired frequency. Loop Amp U6B then provides an amplified control voltage at pin 7 that is applied to the cathodes of varactors CR1, CR4 and CR7.

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP1. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

T1

Tune the receiver to 10.02269 MHz with the IF shift set to 0.00 kHz. Observe the Oscilloscope and check if the voltage at TP1 is + 2 ± 0.5 VDC. If it is not, adjust T1 as required to make it so. Tune the receiver to 10.0000 Mhz and verify that the voltage at TP1 is less than -9 VDC.

T2

Repeat the above procedure except tune the receiver to 10.05473 and 10.02270 MHz respectively.

T3

Repeat the above procedure except tune the receiver to 10.09999 and 10.05474 MHz respectively.

The output level on the coaxial cable in position 5 should be greater than 0.25 V peak to peak into a 50 Ohm load.

CONNECTIONS:

P1, position 3 -- Reference input, 1 MHz
P1, position 5 -- Fine RF output from module to output loop

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- FINE DATA (Fine Loop data)
P2, Pin 6 -- SYN CLK (Synthesizer data clock)
P2, Pin 7 -- VCO LO
P2, Pin 8 -- VCO HI
P2, Pin 9 -- VCO MED
P2, Pin 11 -- BFO ON/OFF signal to BFO module
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

BFO MODULE

The BFO module supplies a phase locked signal from 445.01 to 464.99 kHz in 10 Hz steps to the Detector module. It uses the 1 MHz reference frequency from the Reference module and serial data from the CPU module.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The 1 MHz Reference frequency enters the Module via the coaxial cable in P1, position 2 where it is split for use by the 500 kHz L.O. circuit, a buffer amplifier to distribute this signal to other modules in the receiver, and the Multi-function Synthesizer chip U3.

The 500 kHz LO signal is used in the Detector module. This signal is obtained by passing the 1 MHz signal through NPN buffer amplifier Q4 which drives the pin 3 clock input port of divide-by-two counter U1A. Its output from pin 1 is filtered and placed on the 500 kHz L.O. output cable in P1, position 3.

The reference signal is also coupled through C25 to RF amplifier Q5 and associated components and is routed to the output on P1, position 1. This signal is amplified and buffered in this module rather than the Reference module due to the lack of enough coaxial cable connectors in the Reference module.

The VCO in this module is a Hartley type oscillator nearly identical with the VCOs found in the three Loop Modules. Its output range is 44.501 to 46.499 MHz in 1 kHz steps, and is composed of JFET Q1, transformer T1, varactor diode CR1, and associated components. NPN transistor Q3 acts as a switch to disable the VCO on computer command (through the Fine Loop Module shift register). Diode CR2 detects the oscillator signal to provide amplitude control and amplifier Q2 isolates the VCO from the other stages thus improving the stability of the oscillator.

U5 and U6A, both divide-by-10 counters, use the VCO output to generate a BFO frequency one one-hundreth the VCO frequency. This signal at 445 to 465 kHz in 10 Hz steps is filtered and output at P1 position 5 for use by the Detector Module. U6B is used to provide an auxillary BFO output for other types or models of receivers using the same module.

Dual Modulus Prescaler U2 is driven by the VCO frequency as well. This is a divide-by-64 or 65 device (selectable via pin 1). U3, which receives its frequency input from U2, is a multi-function synthesizer chip, incorporating programmable divider, reference divider and phase detector into a single package. In addition to the 1 MHz Reference, U3 also receives data, clock and enabling inputs from the CPU under program control. The pin 5 Phase Detector output of U3 is an analog voltage that is applied to the cathode of varactor CR1 in the VCO circuit, and serves as an error correction signal for the oscillator. The pin 7 Lock Detector output of U3 is normally high, pulsing low when the VCO is not locked on frequency. If the oscillator is not locked, U4A pin 7 goes low, biasing PNP Q6 to conduct, lighting the Fault LED CR4. As the Q6 collector goes high, NPN Q7 conducts, putting a low on the data FAULT line.

ADJUSTMENTS: No adjustments are required in normal service. In the event of component replacement or drift in characteristics, the following VCO adjustments may be made:

Connect an Oscilloscope through a 10 to 1 probe to TP1. Set the vertical controls to DC coupling, .5 V/division (Including the probe division)

T1

Tune the receiver to any frequency with the BFO offset and IF shift set to 0.00 kHz. Observe the Oscilloscope and check if the voltage at TP1 is + 2.5 ± 0.25 VDC. If it is not, adjust T1 as required to make it so.

Adjust the BFO Offset from -9.9999 to + 9.9999 kHz while observing TP1. The voltage should remain above + 2 VDC and below +3 VDC.

The output level on the coaxial cable in positions 4 and 5 should be between 0.45 and 0.90 V peak to peak into a 50 Ohm load at 445 to 465 kHz.

The output level on the coaxial cable in position 3 should be between 0.45 and 0.90 V peak to peak into a 50 Ohm load at 500 kHz.

CONNECTIONS:

P1, position 1 -- Reference output, 1 MHz to Step Loop
P1, position 2 -- Reference input, 1 MHz from Reference Module
P1, position 3 -- 500 kHz LO output, to Detector Module
P1, position 4 -- AUX BFO output, 455 kHz spare (for other model receivers)
P1, position 5 -- MAIN BFO output, 455 kHz to Detector module

P2, Pin 1 -- + 16 VDC
P2, Pin 2 -- + 8 VDC
P2, Pin 3 -- Ground
P2, Pin 4 -- SYN EN (Synthesizer enable pulse to latch data)
P2, Pin 5 -- BFO DATA
P2, Pin 6 -- SYN CK (Synthesizer data clock)
P2, Pin 11 -- BFO ON/OFF from Fine Loop module
P2, Pin 12 -- Fault (Low in fault -- common with other faults in receiver)
P2, Pin 13 -- - 16 VDC
P2, Pin 14 -- Test point, Loop control voltage

CPU MODULE

The CPU module provides all the control signals to the various modules of the receiver from front panel control operations and data sent over the remote control bus.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

U5 is a microprocessor chip performing all the receiver control functions. The application of DC power is sensed at pin 33 by the charge on C4 through R8. CR1 is used to discharge C4 quickly when power is removed. MOS-FET switch transistor Q1 is used by the processor to reset itself during a powerdown sequence by the port line from U6. This prevents inadvertent control states from being set into the receiver circuits.

The processor clock is crystal controlled by the 4.9152 MHz crystal (Y1) between pins 10 and 11 and associated components. Address lines A8 through A15 are found on pins 1 through 8. Pins 12 through 19 are bi-directional multiplexed Address and Data lines AD0 through AD7. Pin 21 is the Non-Maskable Interrupt line, which provides the indication of incipient loss of power by means of the voltage comparator comprised of U10a and associated voltage divider components.

Address Latch U9 provides EPROM U4 with address line 0 - 7 data under a (low) enable pulse at pin 11, which originates in the microprocessor. The Address Latch Enable (U5, pin 30) line controls both the Address Latch U9 and the Programmable Peripheral Interface (U6 pin 11), as well as the Panel Interface Module and the IEEE-400 or Parallel Bus Interface Module. This line is held high to enable data, and low to enable address information.

Program Memory is stored in U4, an erasable programable read-only-memory (EPROM). Chip Enable (CE/) is provided by the processor on address line A14. Output Enable is a low put on pin 22 by the processor Read line (U5 pin 32). This line also enables U6, 7 and 8, as well as other devices in the Panel Interface and Bus Interface Modules. U3 is an Address Decoder generating Chip Select signals for U6, 7 and 8, as well as other devices in the Panel Interface and Bus Interface Modules.

U6 is a programmable device known by the acronym RIOT (RAM, I/O ports, Timer) which upon processor prompt, interface (or in this case Read) program data to Output or control devices in the Preselector, 2nd IF, Detector, Step Loop, Fine Loop and BFO Modules. Timing is taken from the U5 pin 9 Clock output. I/O or Memory (IO/M) selection, in addition to Read and Write instructions, arrive directly from the microprocessor.

U7 (DAC0832) is a Digital to Analog Converter which provides an analog Manual Gain Control Voltage (0 to +5 VDC through op amp U1) to the Detector Module, from parallel digital data on the bus. Analog to Digital Converter U8 (ADC0804) receives an analog 0 to +5V Meter level from the Detector Module (via the Audio Board), and makes the digital equivalent data available to the multiplexed bus.

ADJUSTMENTS: NONE

CONNECTIONS:

P1

Pin 1	--	+8 VDC
Pin 2	--	+16 VDC
Pin 3	--	-16 VDC
Pin 4	--	ADR/DAT1
Pin 5	--	ADR/DAT3
Pin 6	--	ADR/DAT5
Pin 7	--	ADR/DAT7
Pin 8	--	A9
Pin 9	--	A2
Pin 10	--	A0
Pin 11	--	RD/
Pin 12	--	EN4
Pin 13	--	ALE
Pin 14	--	GROUND
Pin 15	--	MGC VOLTAGE
Pin 16	--	ADR/DAT0
Pin 17	--	ADR/DAT2
Pin 18	--	ADR/DAT4
Pin 19	--	ADR/DAT6
Pin 20	--	SPARE
Pin 21	--	A10
Pin 22	--	A1
Pin 23	--	METER ANALOG
Pin 24	--	B1
Pin 25	--	EN5

P2

Pin 1	--	FAULT/
Pin 2	--	INTA/
Pin 3	--	IO/M
Pin 4	--	SYN EN
Pin 5	--	STEP DATA
Pin 6	--	BFO DATA
Pin 7	--	BAND 1
Pin 8	--	BAND 3
Pin 9	--	BW 1
Pin 10	--	AGC EN
Pin 11	--	DET 0
Pin 12	--	DUMP
Pin 13	--	HOLD 0
Pin 14	--	INTR/
Pin 15	--	WR/
Pin 16	--	RESET
Pin 17	--	SYN CLOCK
Pin 18	--	FINE DATA
Pin 19	--	BAND 0
Pin 20	--	BAND 2
Pin 21	--	BW 0
Pin 22	--	BW 2
Pin 23	--	SPARE
Pin 24	--	DET 1
Pin 25	--	HOLD 1

IEEE-488 BUS INTERFACE MODULE

The optional IEEE-488 Bus Interface module receives data from the remote control bus and makes it available to the CPU module.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

The operations of this module are under the control of its own microprocessor, U2. Timing for this processor is provided by the 5.76 MHz crystal connected between pins 2 & 3, and is made available to U4 (the IEEE-488 Interface Controller) and U1 (the Port Expander) from pin 1 Timing Out. Bi-directional data to and from the CPU Module (via the mother board and U1) is applied to pins 27 through 34. Multiplexed address/data is output from U2 on pins 12 through 19. Pin 39 is the dedicated Request To Talk (TO) line. The Bus Interface Fault line is pin 35, which when high (true) forward biases Q1, pulling its collector low, thus enabling (lighting) Fault LED CR1. ALE/ pin 11 is the Address Latch Enable.

U1 is a RAM and Port Expander chip identical to U6 found in the CPU Module. As on U2, pins 12 through 19 are multiplexed address/data lines from the CPU module. Pins 21 through 28 are bi-directional data lines to the microprocessor. Rear panel Address switches input Service Request, Talk Enable, Listen Enable, and address ID selection data to pins 29 through 36 of U1 (and hence, to U2). Bus Interface, Read, Write and Address Latch Enable are applied to U1 on pins 8 through 11. Pin 37 (RINT/) is an interrupt request line to the Interrupt Controller.

U6 is an Address Latch device. It simply latches (transfers) address data from the data bus to U3 (EPROM) Program Memory on command (LE/, pin 11). Program memory data is read onto the bus from data lines D0 through D7.

The IEEE-488 Interface Controller, U4, regulates sequencing of control and data intelligence (under U2 control) to and from the rear panel IEEE-488 bus connector (via U5 & 7). Address/data bus lines D0 through D7 are found on pins 12 through 19. Pin 1 is the bus transceiver control line (high to transmit, low to receive). U5 and U7 are Bus Transceivers interfacing U4 and the rear panel (through the Mother Board). U5 handles data information, and U7 handles control information.

ADJUSTMENTS: NONE

PANEL INTERFACE MODULE

The primary functions of the Panel Interface Module are to sense operation of keypad and adjustment knob controls, provide drive signals for the front panel displays, and provide retention of channel data and current status of the receiver during power off-on cycles.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

Function decoding is accomplished by way of U1, a one of eight decoder which selects the proper chip into which to latch data via address lines A8 - A10. The EN5 signal and the IO/M signal from the CPU module enable the decoder.

Data for the display light emitting diodes on the front panel is latched into integrated circuits U2 through U5. During a decode, the data present on data lines AD0 - AD7 is strobed on the rising edge of the decode pulse into 8-bit latches U2 through U5. The information is multiplexed at a 2 millisecond rate under control of interrupts in the CPU module. U2 through U4 are used to latch the data corresponding to individual segments of each of 3 display digits (or elements) while U5 is used to select one of 6 groups of digits. Each group of 3 digits is normally selected for 2 milliseconds every 16 milliseconds while the bright digit used during adjustment knob operations is selected for 6 milliseconds each 16 milliseconds.

The keypad encoder U6 provides column strobe output signals to and row input sensing from the front panel keypad. When a key press is sensed, an interrupt is generated on the data available output (pin 13) that sets flip/flop U15. This generates an interrupt through the interrupt controller U11 which alerts the CPU to read the keypad data on the data outputs AD0 through AD4. The scan rate of the keypad controller is determined by C3 and is approximately 60 Hz. The keypad debounce delay is determined by C2 and is set for a delay of approximately 50 milliseconds.

Integrated circuit U8 serves several functions. When selected by U1, this IC latches data from the CPU module. MET0 and MET1 (pin 19 and pin 18) are utilized as select lines for signals on the front panel audio board that are to be used for bargraph metering purposes. The INH line (pin 17) serves as a mute control for audio to the headphone jacks on the front and rear panels and is also applied to the audio board.

Two outputs from U8 are used to control the operation of the power down memory, U12. One output (pin 16) selects the recall operation on power up while another output (pin 15) directs U12 to store the current data on power down.

The encoder direction set output from U8 (pin 14) sets the state of the direction flip/flop U15 to the correct polarity when the receiver is powered up. Subsequent pulses from the front panel shaft encoder set or reset this flop/flop which alerts the CPU, through the interrupt controller U11, that the shaft encoder is being turned and in which direction.

The local/remote output from U8 (pin 13) sends pulses through resistor R1 to the interrupt controller, U11. When the switch is closed (local) no interrupts are generated and the CPU sets the local mode of operation. Opening the switch (remote) alerts the CPU to the remote mode of operation. Keyboard operations are disabled and the Remote operation is enabled in this mode.

Latching of address lines A0 through A7 is performed by U9 when the ALE (address latch enable) signal strobes the low order address lines into U9 from the address/data bus. Channel memory functions are accomplished by latching of address locations from U9 and chip select of U10 (pin 18) from function decoder U1 along with a low logic level on pins 20 or 21 during memory read and writes respectively. Address lines A8 through A10 are brought directly to U10.

Interrupt controller U11 is used to interrupt the CPU when a keypad operation, adjustment knob operation, or local/remote switch actuation occurs. The CPU then reads tha data from this chip to determine which operation has occurred and then acknowledges the interrupt to reset the controller.

The non-volatile random access memory (NOVRAM) U12 utilizes logic signals to control the presentation of four bit data bits on the bus. This prevents U12 from presenting its data on the bus during an active address cycle. Address selection is accomplished using address inputs A0 - A5 which are latched by U9. Pin 11, the write enable (WE/) controls the direction of data flow. Memory store and recall operations are directed by inputs latched in U8. Current data regarding frequency, mode, and other parameters are always written to the temporary memory portion of this chip. When an imminent loss of power is sensed, the CPU directs this temporary data to be stored. After a power up operation, the CPU calls for a recall operation to recall data from the non-volatile to the temporary memory portion of this chip. This data can then be read and used to restore the operation of the receiver to the conditions existing just before the power loss.

ADJUSTMENTS REQUIRED: NONE

CONNECTIONS AND SIGNALS:

P1

1	+8 VDC input
2	Segment F1 2 ms multiplex
3	Segment DP1 2 ms multiplex
4	AD1 Address and data bus
5	AD3 Address and data bus
6	AD5 Address and data bus
7	AD7 Address and data bus
8	A9 Address bus
9	Segment E1 2 ms multiplex
10	Segment C1 2 ms multiplex
11	RD/ Low for read
12	EN4/ Low for Channel Memory En.
13	ALE High for address true
14	No Connection
15	Segment A2 2 ms multiplex
16	Segment C2 2 ms multiplex
17	Segment E2 2 ms multiplex
18	Segment DP2 2 ms multiplex
19	Segment F2 2 ms multiplex
20	Ground
21	Segment G1 2 ms multiplex
22	AD0 Address and data bus
23	AD2 Address and data bus
24	AD4 Address and data bus
25	AD6 Address and data bus
26	A8 Address bus
27	A10 Address bus
28	Segment D1 2 ms multiplex
29	Segment B1 2 ms multiplex
30	Segment A1 2 ms multiplex
31	EN5/ Low for Port Enable
32	No Connection
33	No Connection
34	Segment B2 2 ms multiplex
35	Segment D2 2 ms multiplex
36	No Connection
37	Segment G2 2 ms multiplex

P2

1	No Connection
2	INTR Low for interrupt
3	MET1 Meter select (Binary)
4	No Connection
5	INTA Low for interrupt acknowledge
6	IO/M Low for memory, high for IO
7	DG5 2 ms out of 16 high
8	DG3 2 ms out of 16 high
9	DG1 2 ms out of 16 high
10	Segment F3 2 ms multiplex
11	Segment DP3 2 ms multiplex
12	Segment C3 2 ms multiplex
13	Segment A3 2 ms multiplex
14	Column 2 Keypad
15	Column 4 Keypad
16	Row 1 Keypad
17	Row 3 Keypad
18	Local Switch Ground for local
19	Encoder Phase B
20	+ 5 VDC
21	INH Low to inhibit audio
22	MET0 Meter select (Binary)
23	RINT Remote Interrupt
24	WR/ Low for write to memory or IO
25	DG6 2 ms out of 16 high
26	DG4 2 ms out of 16 high
27	DG2 2 ms out of 16 high
28	Segment E3 2 ms multiplex
29	Segment G3 2 ms multiplex
30	Segment D3 2 ms multiplex
31	Segment B3 2 ms multiplex
32	Column 1 Keypad
33	Column 3 Keypad
34	Column 5 Keypad
35	Row 4 Keypad
36	Row 2 Keypad
37	Encoder Phase A

POWER SUPPLY MODULE

The power supply module furnishes DC voltages to all modules from the AC power line. This power supply is a switching mode type to minimize power dissipation and heat build-up in the power supply and in the receiver chassis. All inputs and outputs are extensively filtered to prevent RF noise from the power supply from appearing in the signal path.

The power supply is packaged in a completely shielded module similar to the other modules in the receiver although the power supply module is slightly thicker than the other modules. This shielding serves also to isolate any RF noise generated in the power supply from the signal path.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

AC input voltage is applied to pins 2 and 5 of the high voltage input connector. This connector is similar to the coaxial connectors in many of the other modules except for the type of contact pin used. CR14 is a metal oxide varistor (MOV) used to clip high voltage transients that may be present.

The AC line radio frequency interference (RFI) filter is comprised of capacitors C28, C29, C30, bifilar wound dual RF choke L9, capacitors C25, C26, C27, separate RF chokes L7 and L8, and capacitor C21. Neon bulb DS1 and associated resistors is used to indicate a fault in the module under the control of optically isolated thrysistor U1 and will be discussed later.

Bridge rectifier CR13 converts the AC input voltage to DC and stores the resultant DC voltage in capacitors C20 and C22. Voltage selector switch S1 configures the rectifier for a full wave bridge in the 220 V position and for a full wave voltage doubler in the 110 V position. MOV device CR12 clips any high voltage transients that have passed through the initial MOV device while thermistors RT1 and RT2 limit the surge current into the capacitors when the unit is first turned on and the thermistors are cold or at the receiver ambient temperature.

The rectified DC voltage is applied to the primary winding (Pins 10 and 2) of power transformer T1 through field effect transistor (FET) Q4 and current sense resistor R26. The switching of Q4 under the control of integrated circuit U2 changes the DC voltage back into AC at a frequency of approximately 65 KHz with a controlled on-off ratio so as to regulate the effective voltage appearing across each of the transformer secondary windings. Diode CR2 together with C1, R8, and R9 provide transient suppression when Q4 is turned off.

When the unit is first turned on, FET Q1 is turned on by means of the voltage developed across R5 and R39. Zener diode CR1 limits the bias voltage applied to Q1 and Q2 is turned off initially. The conduction through Q1 provides an operating voltage for U2 which then pulses Q4 on and off to create the AC voltage. As a voltage is developed across the secondary winding between Pins 1 and 11 of T1, the DC voltage developed by CR3 across C24 then turns Q2 on and Q1 off. The operating voltage for U2 then is applied through CR5 and CR6. CR4 insures that the base-emitter junction of Q2 is never reverse biased by more than 0.7 volts.

The DC voltage across C24 is sensed by integrated circuit U2 and is used to control the duty cycle of the AC voltage across the primary of T1. The regulation of this voltage thus serves to control the other voltages as desired for use by the other modules in the receiver. The voltage across R26 is sensed to insure that the peak currents through Q4 are not excessive such as those that may result from a component failure in the power supply or a short circuit on the output of the power supply.

Each of the three desired output voltages is developed in essentially a similar manner. Refering to the connections shown to the right of transformer T1 on the schematic diagram, each supply consists of a half wave rectifier diode, a set of energy storage capacitors, and an RFI filter consisting of alternate capacitors and inductors. These rectifier convert the AC voltage appearing across the transformer back into DC at the desired lower voltages. Thus the transformer, switching transistor, and output rectifiers serve to form a DC to DC converter.

Each of the separate output voltages is sensed by comparison with a reference voltage developed by voltage regulator U3. The separate comparator sections of U4 are summed in an OR connection at the input (gate) of Q6. Any voltage sensed to be below its fault threshold will cause a low voltage at the gate of Q6 thus turning it off and turning Q5 on. This causes the FAULT / at pin 8 of P2 to be low and signal a fault to the CPU module.

The fault condition resulting in the turning off of Q6 would also result in the light emitting diode (LED) section of U1 to be turned off, thus turning off the thyristor section and allowing DS1 to become illuminated. With the unit operating normally, Q6 is turned on thus allowing conduction through the LED section of U1 and DS1 is not illuminated. Note that operating DS1 from the AC line in this manner allows a fault to be indicated (at least on the module) with the no other components operating.

ADJUSTMENTS REQUIRED: NONE

CONNECTIONS AND VOLTAGE LIMITS:

AC Line -- Pins 2 and 5 of P1 (High Voltage Inserts)
100 to 130 or 200 to 260 VAC RMS

Ground -- Pins 1, 13, 14, and 25 of P2

+16V -- Pins 10, 11, 22, and 23 of P2
+15 to +17 VDC

-16V -- Pins 3 and 16 of P2
-15 to -17 VDC

+8V -- Pins 5, 6, 18, and 19 of P2
+7.5 to +8.5 VDC

Fault -- Pin 8 of P2
Low indicates fault condition (common with other faults)

REFERENCE and 2nd LO MODULE, 10 MHz

The Reference module supplies the 1 MHz reference frequency to all synthesizer modules and the 40 MHz 2nd Local Oscillator signal to the 1st IF module. This module uses an internal 10 MHz TCXO or OCXO and an external 10 MHz reference.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

Y1 is a temperature compensated crystal oscillator (TCXO) or oven controlled crystal oscillator (OCXO) whose 10 MHz output is buffered by amplifier Q1 and applied to gate U1C. External reference signals (if used) are present at P1, on the coaxial cable in position 1, and drive buffer amplifier Q2. The output signal from Q2 is applied to gate U1A.

If the external reference selector signal (REF SEL) applied to pin 9 of connector P2 is not low or grounded (as determined by the position of the rear panel reference selector switch), U1A is enabled and the external reference is selected. If the REF SEL signal is low, U1C is enabled and the internal reference is selected. The selected signal is gated by U1B and applied to U3A where it is divided in frequency by 10. The resultant 1 MHz signal used as a source of the reference frequencies used in the Step and Fine Loop Modules, as well as the BFO Module. The optional 1 MHz reference module has the divide by 10 circuit of U3A bypassed.

The undivided reference signal is applied to amplifier Q3 via the low pass filter comprised of C11, L1, and C12. This filter removes all harmonics of the reference signal thus providing a sinusoidal signal to the REF OUT coaxial cable in connector position 3 of P1.

The 1 MHz signal is applied to U4B and U4C that act as buffer amplifiers for the signals applied to the BFO and Fine Loop modules respectively. These outputs are also filtered to remove harmonics of the 1 MHz signal.

The 2nd L.O. signal is generated by the 20 MHz Voltage Controlled Crystal Oscillator (VCXO) comprised of crystal Y2, NPN transistor Q4, varactor CR2 and associated components. The output from Q4 is multiplied in frequency by two by Q5 and filtered by the tuned circuit consisting of T1 and C28. This signal at 40 MHz is further amplified and filtered by Q6 and T2/C33 before passing through the low pass filter comprised of C36, L4, and C37 and being applied to the 2nd Mixer of the receiver in the 1st IF module.

The 20 MHz VCXO signal is divided by 40 in U6 and applied to one input of U4D. The 1 MHz reference signal is divided by 2 in U3B and applied to the other input of U4D. U4D acts as a phase detector and corrects the frequency of the VCXO as required to make the 2nd LO output signal at 40 MHz exactly 40 times the frequency of the 1 MHz reference signal.

ADJUSTMENTS:

Y1, adjustment screw

Insure that the rear panel REF SELECT switch is set to the INT position. Measure the frequency on the REF OUT coaxial cable in position 3 of P1. If this frequency is not exactly 10.000000 MHz, adjust the trimmer capacitor on Y1 through the hole in the top of the module. It will be necessary to remove the Phillips head screw to gain access to the adjustment and the screw should be replaced after the adjustment is made.

T1, T2

Adjust T1 and T2 for maximum 40 MHz output signal on the coaxial cable in position 2 of P1.

C24

Adjust C24 for a voltage of +2.5 ± 0.25 VDC on the testpoint connection to P2, pin 14.

CONNECTIONS:

P1, position 1 -- External Reference In, 10 MHz
P1, position 2 -- 2nd LO Out, 40 MHz
P1, position 3 -- Reference Out, 10 or 1 MHz
P1, position 4 -- BFO reference, 1 MHz
P1, position 5 -- Fine Loop Reference, 1 MHz

P2, pin 1 -- +16 VDC
P2, pin 2 -- + 8 VDC
P2, pin 3 -- Ground
P2, pin 9 -- Reference Selector (high for external, low for internal)
P2, pin 12 -- Fault (low for fault)
P2, pin 14 -- Test point, VCO control voltage

REFERENCE and 2nd LO MODULE, 1 MHz

The Reference module supplies the 1 MHz reference frequency to all synthesizer modules and the 40 MHz 2nd Local Oscillator signal to the 1st IF module. This version of the Reference and 2nd L.O. module uses an internal 1 MHz TCXO and an external reference of 1 MHz.

Refer to the module assembly drawing, board assembly drawing and the schematic diagram for this module.

Y1 is a temperature compensated crystal oscillator (TCXO) whose 1 MHz output is buffered by amplifier Q1 and applied to gate U1C. External reference signals (if used) are present at P1, on the coaxial cable in position 1, and drive buffer amplifier Q2. The output signal from Q2 is applied to gate U1A. If the external reference selector signal (REF SEL) applied to pin 9 of connector P2 is not low or grounded (as determined by the position of the rear panel reference selector switch), U1A is enabled and the external reference is selected. If the REF SEL signal is low, U1C is enabled and the internal reference is selected. The selected signal is gated by U1B. The 1 MHz signal used as a source of the reference frequencies used in the Step and Fine Loop Modules, as well as the BFO Module.

The reference signal is applied to amplifier Q3 via the low pass filter comprised of C11, L1, and C12. This filter removes all harmonics of the reference signal thus providing a sinusoidal signal to the REF OUT coaxial cable in connector position 3 of P1.

The 1 MHz signal is applied to U4B and U4C that act as buffer amplifiers for the signals applied to the BFO and Fine Loop modules respectively. These outputs are also filtered to remove harmonics of the 1 MHz signal.

The 2nd L.O. signal is generated by the 20 MHz Voltage Controlled Crystal Oscillator (VCXO) comprised of crystal Y2, NPN transistor Q4, varactor CR2 and associated components. The output from Q4 is multiplied in frequency by two by Q5 and filtered by the tuned circuit consisting of T1 and C28. This signal at 40 MHz is further amplified and filtered by Q6 and T2/C33 before passing through the low pass filter comprised of C36, L4, and C37 and being applied to the 2nd Mixer of the receiver in the 1st IF module.

The 20 MHz VCXO signal is divided by 40 in U6 and applied to one input of U4D. The 1 MHz reference signal is divided by 2 in U3B and applied to the other input of U4D. U4D acts as a phase detector and corrects the frequency of the VCXO as required to make the 2nd LO output signal at 40 MHz exactly 40 times the frequency of the 1 MHz reference signal.

ADJUSTMENTS:

Y1, adjustment screw

Insure that the rear panel REF SELECT switch is set to the INT position. Measure the frequency on the REF OUT coaxial cable in position 3 of P1. If this frequency is not exactly 1.000000 MHz, adjust the trimmer capacitor on Y1 through the hole in the top of the module. It will be necessary to remove the Phillips head screw to gain access to the adjustment and the screw should be replaced after the adjustment is made.

T1, T2

Adjust T1 and T2 for maximum 40 MHz output signal on the coaxial cable in position 2 of P1.

C24

Adjust C24 for a voltage of +2.5 ± 0.25 VDC on the testpoint connection to P2, pin 14.

CONNECTIONS:

P1, position 1 -- External Reference In, 10 MHz
P1, position 2 -- 2nd LO Out, 40 MHz
P1, position 3 -- Reference Out, 10 or 1 MHz
P1, position 4 -- BFO reference, 1 MHz
P1, position 5 -- Fine Loop Reference, 1 MHz

P2, pin 1 -- +16 VDC
P2, pin 2 -- + 8 VDC
P2, pin 3 -- Ground
P2, pin 9 -- Reference Selector (high for external, low for internal)
P2, pin 12 -- Fault (low for fault)
P2, pin 14 -- Test point, VCO control voltage

DISPLAY BOARD

The display board contains all of the front panel display components and drivers for these components. The data is latched to the Display board from the Panel Interface module and converted to current levels necessary to drive the display LEDs.

Refer to the board assembly drawing and the schematic diagram for this board.

The display is organized as 3 groups of 6 digits having 8 segments each. Normal intensity digits are turned on for 2 milliseconds every 16 milliseconds (a refresh rate of 62.5 Hz) while the intensified digit (when enabled) is turned on for 6 milliseconds every 16 milliseconds.

U1 through U4 are 8-channel drivers that receive Panel Interface Module data on J1. U1 serves as a driver for the PNP digit group driver transistors Q1 through Q6. These transistors, when biased to conduct, enable a group of 3 digits (i.e. Q1 enables DS1, 7 and 13).

Segment drivers U2 through U4 will, upon receipt of data, place logic levels on their parallel outputs necessary to illuminate the selected segments of the display elements. Since only one digit group at a time is enabled, the data from one segment driver is directed to only one digit. Bargraph displays CR1 and CR2 as well as annunciators CR3 through CR8 are treated as segments of digits. The resistors serve to control the current to each display LED.

ADJUSTMENTS REQUIRED: NONE

CONNECTIONS: J1 ONLY

PIN	SIGNAL	PIN	SIGNAL
1	+8 RTN (Ground at power supply)	18	A1
2	+8 RTN (Ground at power supply)	19	DP3
3	DP2	20	+ 8 VDC
4	DP1	21	G3
5	G2	22	+ 8 VDC
6	G1	23	F3
7	F2	24	DG6
8	F1	25	E3
9	E2	26	DG5
10	E1	27	C3
11	D2	28	DG4
12	D1	29	D3
13	C2	30	DG3
14	C1	31	B3
15	B2	32	DG2
16	B1	33	A3
17	A2	34	DG1

AUDIO BOARD

The Audio board provides amplification of the audio signal from the Detector Module for application to the headphones jacks and the 600 Ohm balanced line audio output from the receiver, the detection of audio signal level for metering purposes, and the signal selection gate for metering purposes.

Refer to the assembly drawing and the schematic diagram for this board.

The audio signal from the Detector Module enters at J3 pin 16 and is applied to both the Metering Select and the Audio Inhibit circuitry. U3B simply acts as a switch to pass or inhibit the audio signal under CPU control to provide the squelch function. The Audio Inhibit line on J3 pin 12 is set high to enable the signal at the U3B output. A low on this line disables (inhibits) the signal.

C24 couples the audio signal both to the front panel volume control potentiometer (through J2/P2), and to buffer amplifier U2A. U2B drives the primary of transformer T1, which produces a 600 ohm balanced line signal. L1, L2 and C5 through C8 form a filter designed to exclude external RF signals from the audio amplifiers. Audio from the Volume Control on the front panel drives amplifier U6, whose filtered output signal is made available to the front panel headphone jack via J1.

Meter Select switch U3A serves as a 1-pole/4-throw switch under CPU control. When selected, the audio signal is processed by detector U1B (with CR2 and CR3), peak detector U1C (with CR4 and C3) and associated components for analog level, and is subsequently routed to U3 pin 13. The FM video signal at P3 pin 14 is converted to a 0 to +5V signal level by U1A, and is routed to U3 pin 12 in the same manner as the detected Audio signal. The Signal Strength analog line from the Detector module is connected to U3 pin 11.

The CPU module selects the desired signal for metering purposes via the MET 0 and MET 1 select lines on J3, pins 10 and 11 respectively. The selected signal is thus made available to the A/D converter on the CPU module via the Meter Analog line on J3, pin 13. The signal strength signal is used for squelch as well as scan or sweep stop purposes in addition to front panel bargraph metering while the other signals are selected only when those metering functions are required.

ADJUSTMENTS: NONE

CONNECTIONS:

J1 Headset Jack connection

1 Audio ground for headphones
2 Optional speaker connection
3 Ring contact on Headset jack
4 Tip contact on Headset jack

J2 Volume Control connection

1 Audio ground (Volume Control low)
2 Volume Control wiper
3 Volume Control high

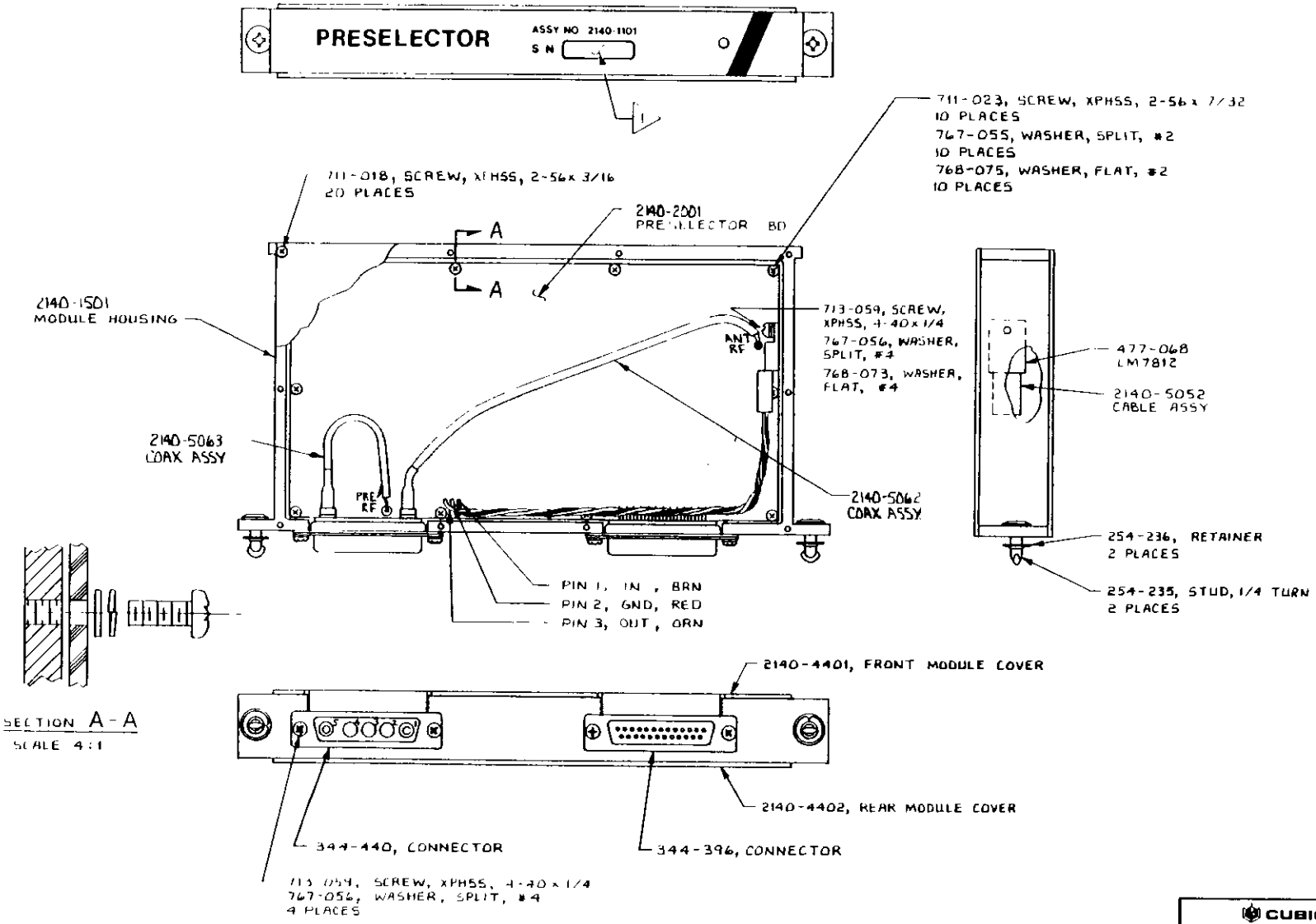
Note: Ground connections to board only, not to chassis

CONNECTIONS: (Continued)

J3 -- connector to motherboard

Pin 1 -- 600 Ohm balanced audio (Paired with Pin 3)
Pin 2 -- Headphones audio, tip
Pin 3 -- 600 Ohm balanced audio (Paired with Pin 1)
Pin 4 -- Headphones audio, ring
Pin 5 -- - 16 VDC
Pin 6 -- Audio Ground (Not chassis ground except at detector module)
Pin 7 -- No connection
Pin 8 -- Audio Ground (Not chassis ground except at detector module)
Pin 9 -- + 16 VDC
Pin 10 -- MET 0 (Binary meter selection)
Pin 11 -- MET 1 (Binary meter selection)
Pin 12 -- Audio Inhibit (Low when audio inhibited)
Pin 13 -- Meter Analog (0 to + 5 VDC to CPU)
Pin 14 -- FM Video (From Detector)
Pin 15 -- Signal Strength analog (From Detector)
Pin 16 -- Detector Audio (From Detector)

REVISION			
LTR	DESCRIPTION	DATE	APPD



1 RUBBER STAMP SERIAL NUMBER

NOTES: UNLESS OTHERWISE SPECIFIED

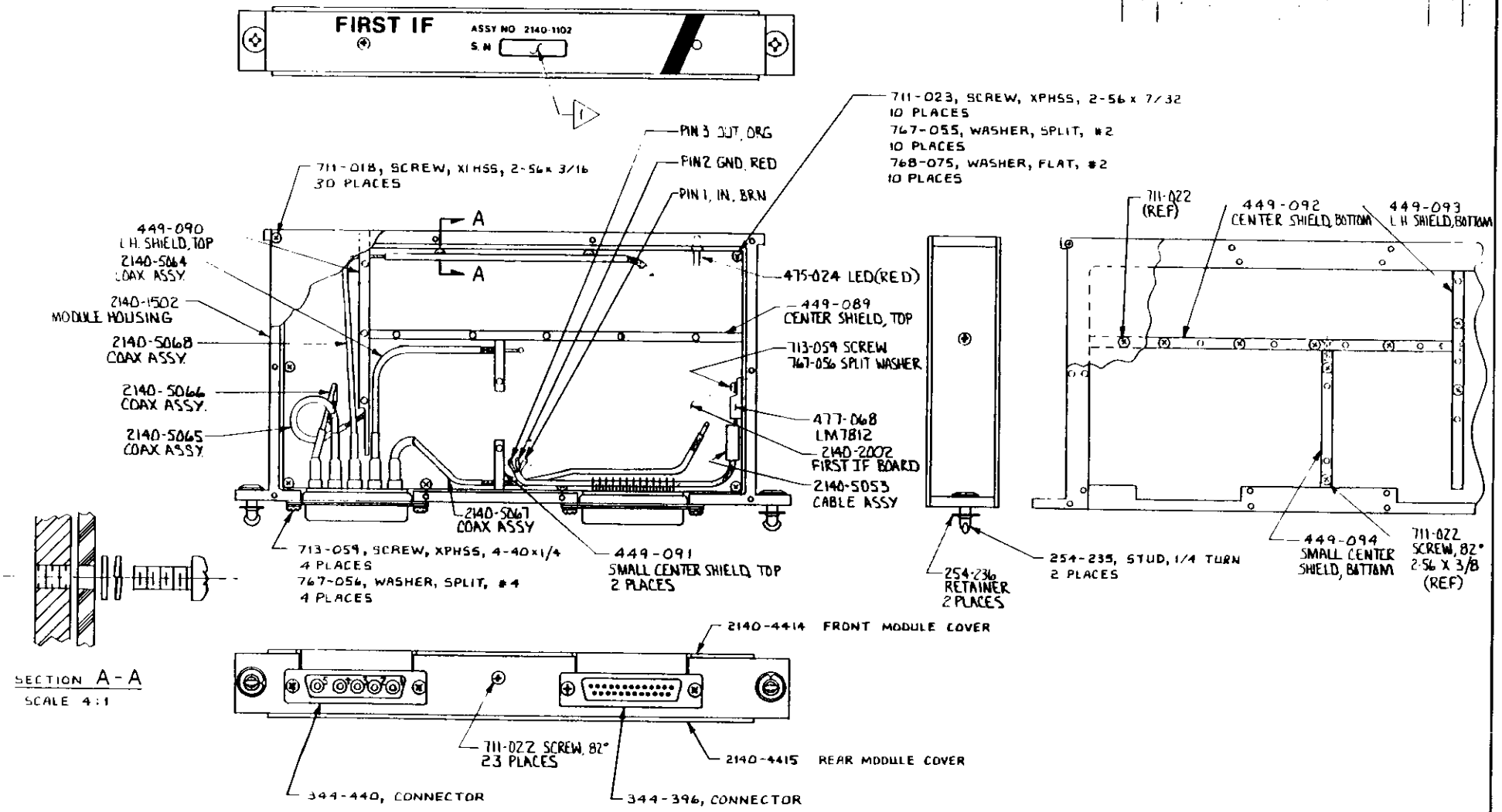
CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

SCALE	1/1	APPROVED BY:	DRAWN BY
DATE	12-17-84		REVISED

PRESELECTOR MODULE

N/A	QTY	MODEL	REV	DRAWING NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD



1 RUBBER STAMP SERIAL NUMBER

CUBIC COMMUNICATIONS
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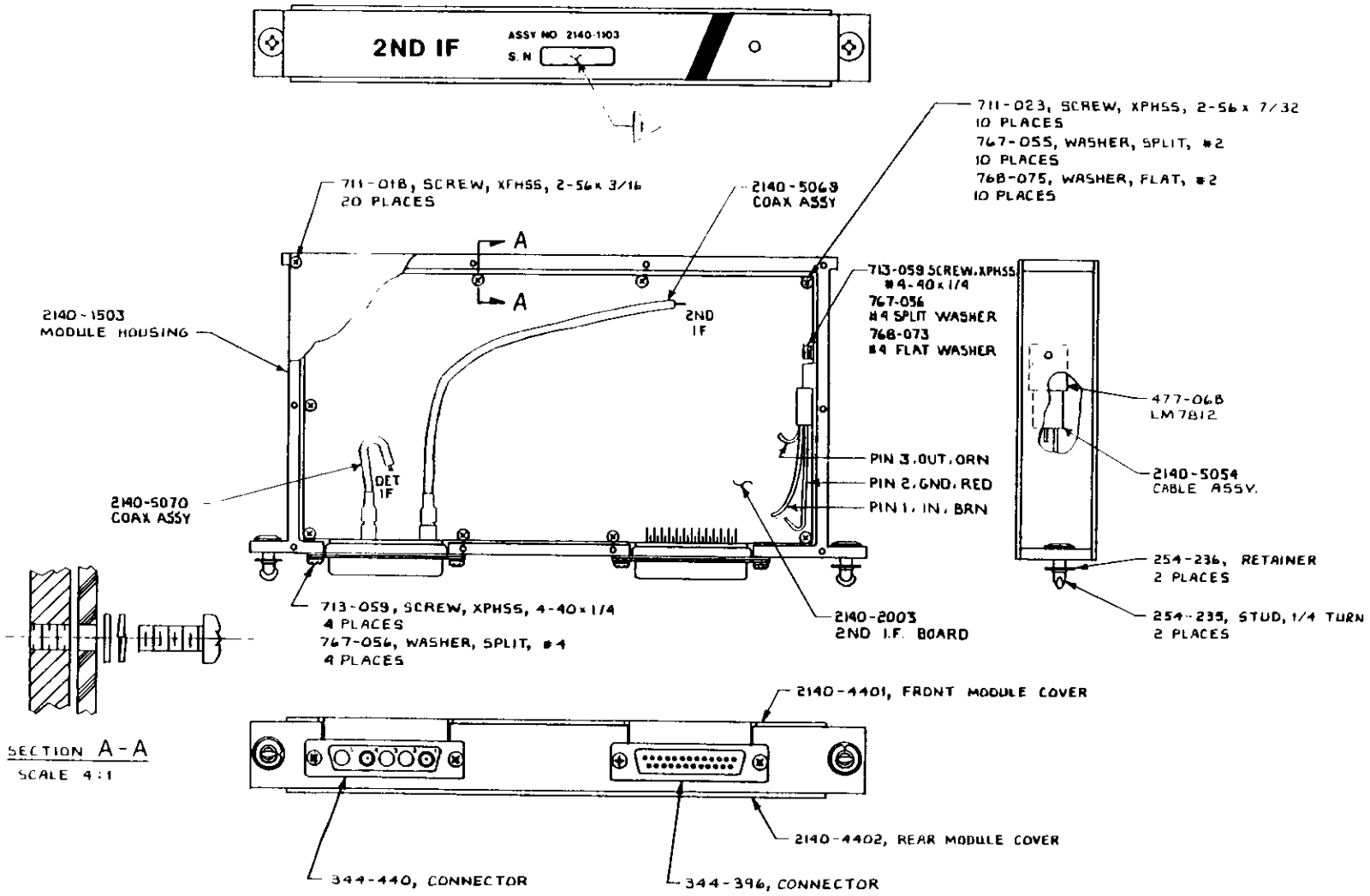
305 Airport Rd Oceanside CA 92054

SCALE 1/1	APPROVED BY:	DRAWN BY RC
DATE 12-17-84		REVISED

FIRST IF MODULE

REVISION			
LTR	DESCRIPTION	DATE	APPD



1 RUBBER STAMP SERIAL NUMBER.

CUBIC COMMUNICATIONS

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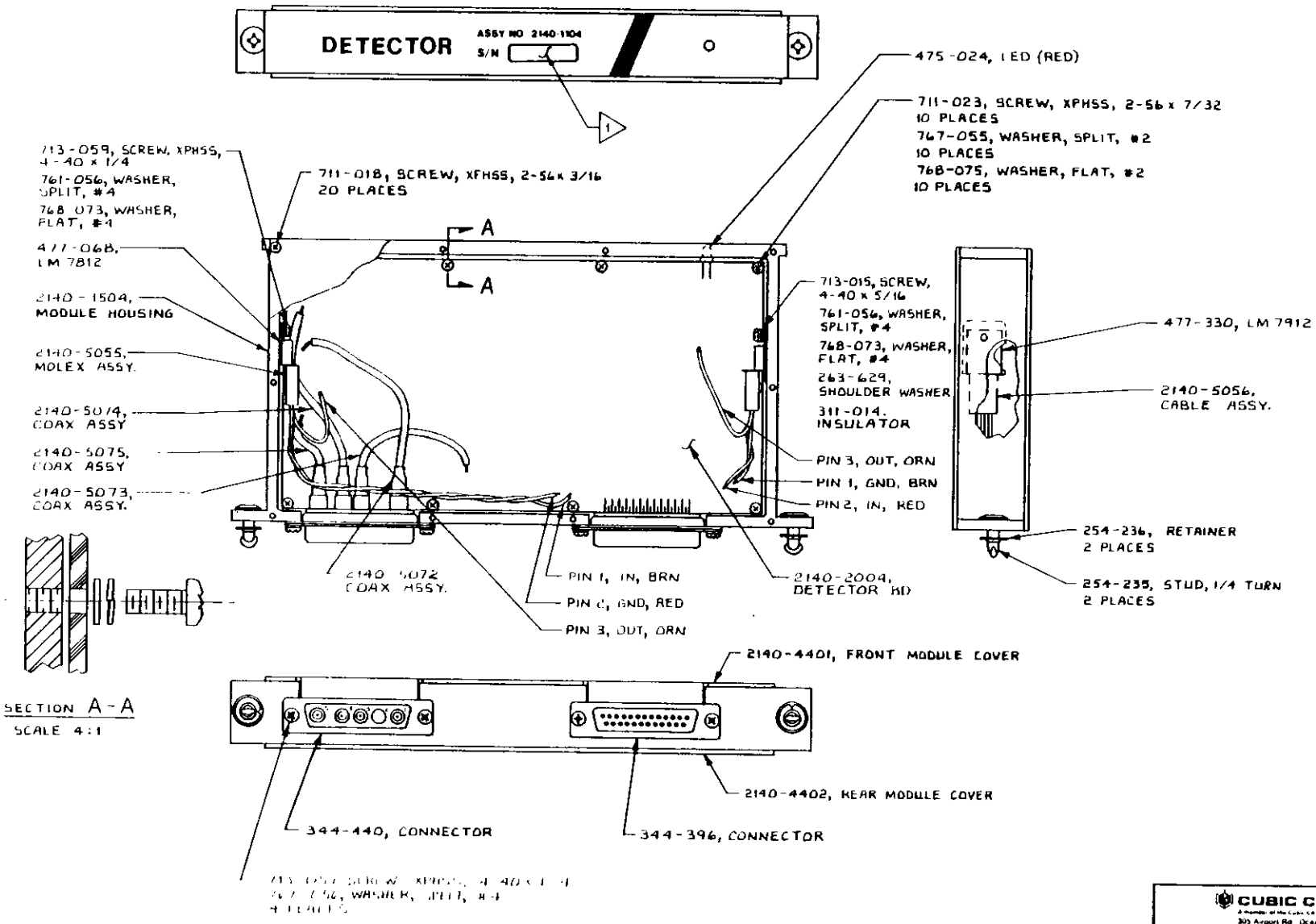
305 Airport Rd Oceanside CA 92054

SCALE 1/1	APPROVED BY:	DRAWN BY E ROBLES
DATE 1-10-85		REVISED

2ND I.F. MODULE

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140-13, CHANGED COAX CABLE NUMBERS, ADDED REVISION LETTER "A" E.D.R. 1-23-85	1/24/85	



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305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY:	DRAWN BY: [illegible]
DATE: [illegible]		REVISED

DETECTOR MODULE

[illegible] NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD
S			

475-064 (REQUIRED)

711-023, SCREW, XPHSS, 2-56 x 7/32
10 PLACES
767-055, WASHER, SPLIT, #2
10 PLACES
768-075, WASHER, FLAT, #2
10 PLACES

711-018, SCREW, XPHSS, 2-56 x 3/16
20 PLACES

713-015, SCREW, XPHSS, 4-40 x 5/16
767-056, #4 SPLIT WASHER
768-073, #4 FLAT WASHER

477-032, 7805

2140-1505, MODULE HOUSING

2140-5057, CABLE ASSY

2140-5076, COAX ASSY

2140-5077, COAX ASSY

2140-5078, COAX ASSY

PIN 3. OUT. ORN
PIN 2. GND. RED
PIN 1. IN. BRN
PIN 1. IN. BRN
PIN 2. GND. RED
PIN 3. OUT. ORN

713-059, SCREW, XPHSS, 4-40 x 1/4
4 PLACES
767-056, WASHER, SPLIT, #4
4 PLACES

2140-2005, OUTPUT LOOP BD.

477-068, 7812A

2140-5058, CABLE ASSY

254-236, RETAINER
2 PLACES

254-235, STUD, 1/4 TURN
2 PLACES

SECTION A-A
SCALE 4:1

2140-4401, FRONT MODULE COVER

2140-4402, REAR MODULE COVER

344-440, CONNECTOR

344-396, CONNECTOR

2> APPLY 3145 RTV (CLEAR) DOW-CORNING TO AREA INCLOSED BY DASH LINE

1> RUBBER STAMP SERIAL NUMBER

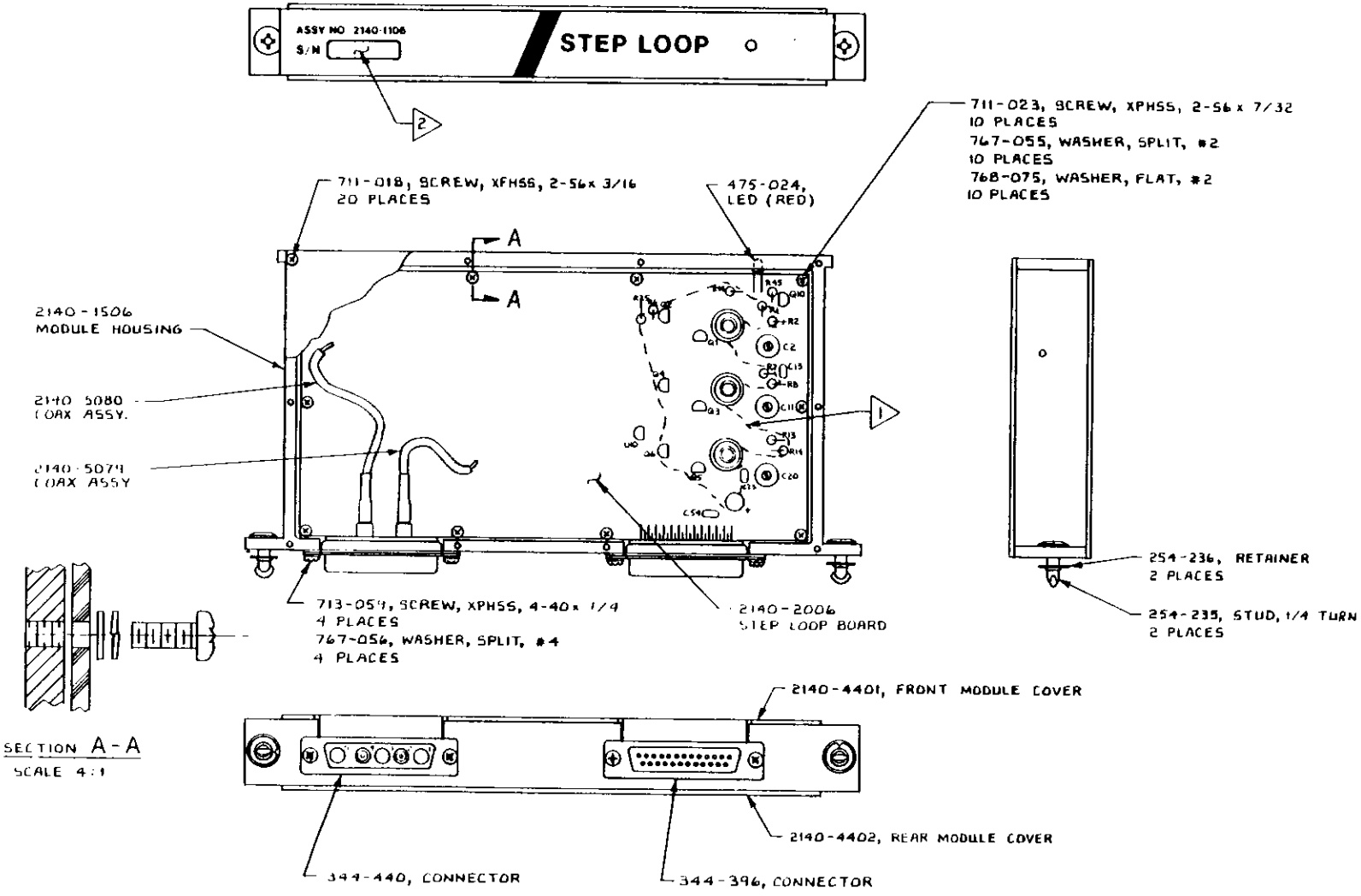
NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS		
305 Airport Rd Oceanside CA 92054		
SCALE 1/1	APPROVED BY:	DRAWN BY E. ROBLES
DATE: 1-10-85		REVISED

OUTPUT LOOP MODULE

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140-13, CREATED SHEET 2 E.O.R. 1-23-85	1-23-85	



SHEET 1 OF 2

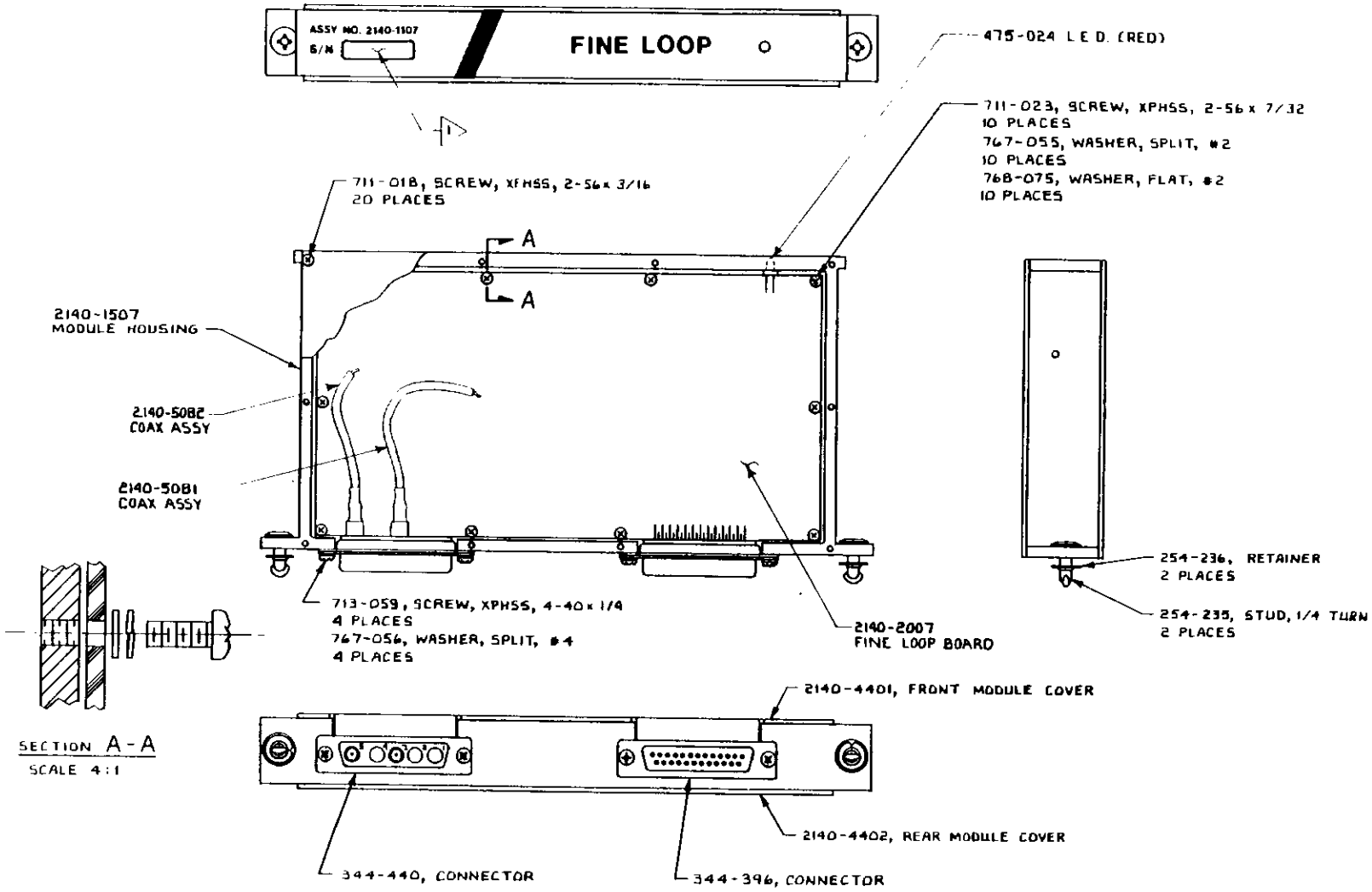
CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE 1/1 | APPROVED BY | DRAWN BY R. ROY

DATE 1-23-85 | REVISED

STEP MODULE

REVISION			
LTR	DESCRIPTION	DATE	APPD
	[illegible]		



SHEET 1 OF 2

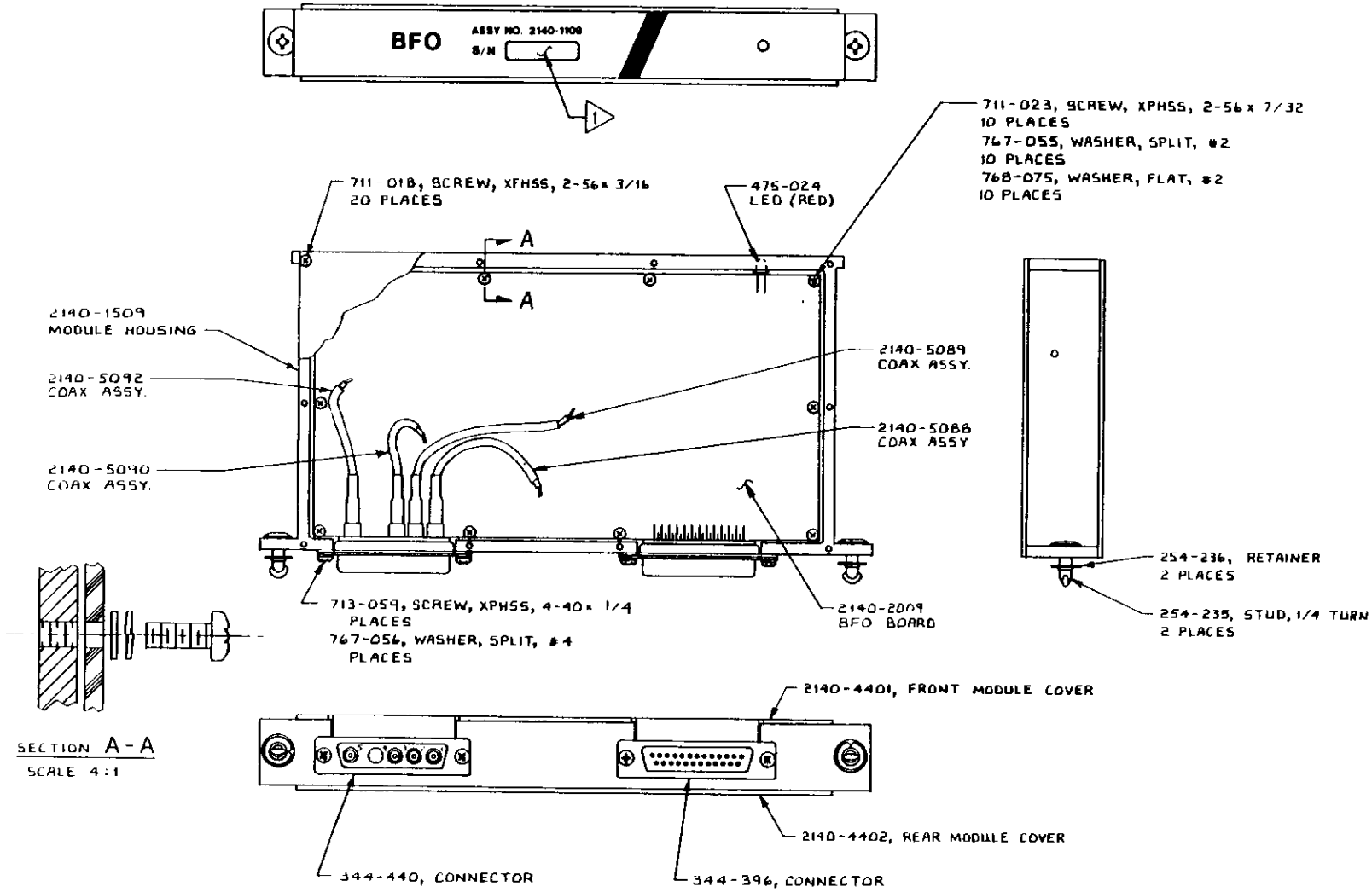
CUBIC COMMUNICATIONS
A Subsidiary of the Cubic Corporation
305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY:	DRAWN BY: E. ROBLES
DATE: 1-8-85		DESIGN

FINE LOOP MODULE

1 RUBBER STAMP SERIAL NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140-13, CHANGED COAX CABLE NUMBERS, ADDED REVISION LETTER "A" & CREATED SHEET 2 E.O.R. 1-23-85	1/24/85	
B	ECN #2140-129, DELETED 2140-5091 COAX ASSY E.O.R 4-11-85	4/16/85	



1 > INDICATES STAMPED SERIAL NUMBER

NOTE: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

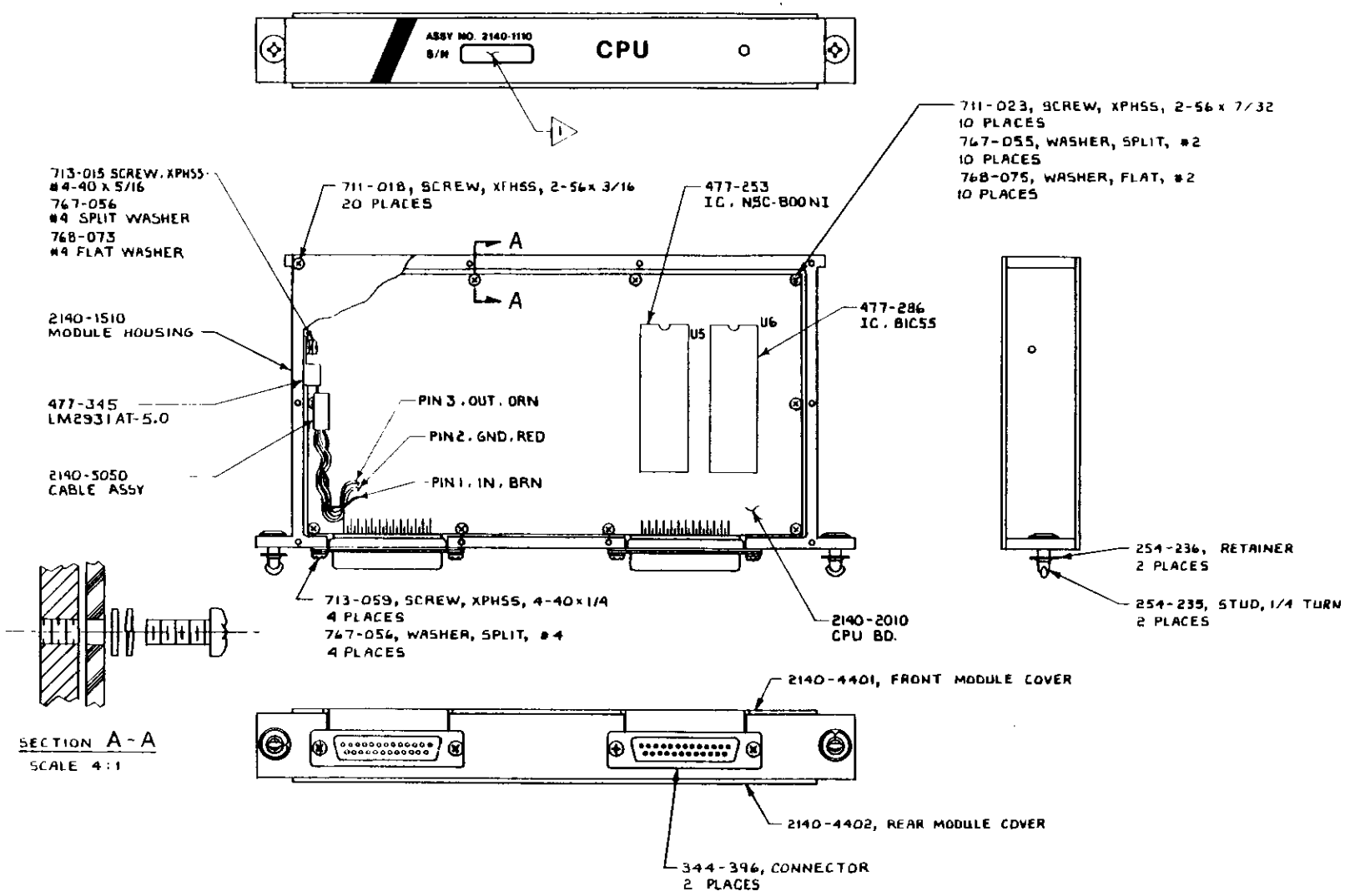
CUBIC COMMUNICATIONS
A Member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

SCALE 1/1	APPROVED BY:	DRAWN BY R RDE
DATE 1-8-85		REVISED

BFO MODULE

N/A	QTY	MODEL	ASY	DRAWING NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	[illegible]		
	[illegible]		
B	[illegible]		



SECTION A-A
SCALE 4:1

1. RUBBER STAMP SERIAL NUMBER

NOTES: UNLESS OTHERWISE SPECIFIED

CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY:	DRAWN BY: E.ROBLES
DATE: 1-9-85		REVISED

CPU MODULE

N/A	SIZE	MODEL	REV	DRAWING NUMBER
2143-1010	A2	R-2307/U	B	2140-1110

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN#2140-159, DELETED 2143-3004 E-PROM (U3) 7-17-85 MPK	7-17-85	

713-015 #4-40 X 5/16 XPHSS SCREW
767-056 #4 SPLIT WASHER
768-073 #4 FLAT WASHER

711-018, SCREW, XPHSS, 2-56 x 3/16
20 PLACES

477-286
(8155)

711-023, SCREW, XPHSS, 2-56 x 7/32
10 PLACES
767-055, WASHER, SPLIT, #2
10 PLACES
768-075, WASHER, FLAT, #2
10 PLACES

2140-1512
MODULE HOUSING

U1 U2 U3 U4

475-024
LED(RED)
CR1

477-032
(7805)

2140-5060
MOLEX ASSY

ORN(OUT)
RED(GND)
BRN (IN)

477-271
(8291 GPIB)

477-217
(8039)

713-059, SCREW, XPHSS, 4-40 x 1/4
4 PLACES
767-054, WASHER, SPLIT, #4
4 PLACES

2140-2013
IEEE 488 BUS BOARD

254-236, RETAINER
2 PLACES

254-235, STUD, 1/4 TURN
2 PLACES

SECTION A-A
SCALE 4:1

2140-4401, FRONT MODULE COVER

2140-4402, REAR MODULE COVER

344-396, CONNECTOR
(TYP) 2 PLACES

CUBIC COMMUNICATIONS	
305 Airport Rd Oceanside CA 92054	
SCALE: 1/1	APPROVED BY:
DATE: 2-18-85	DRAWN BY: RK
	REVISED

IEEE 488 BUS INTERFACE MODULE ASSY

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140 [illegible] CHANGE [illegible]		
B	ECN # 2140 [illegible] ADDED SHEET 2		
C	[illegible]		
D	[illegible]		

713-015 SCREW, XPHSS
4-40 x 5/16
767-056
#4 SPLIT WASHER
768-073
#4 FLAT WASHER

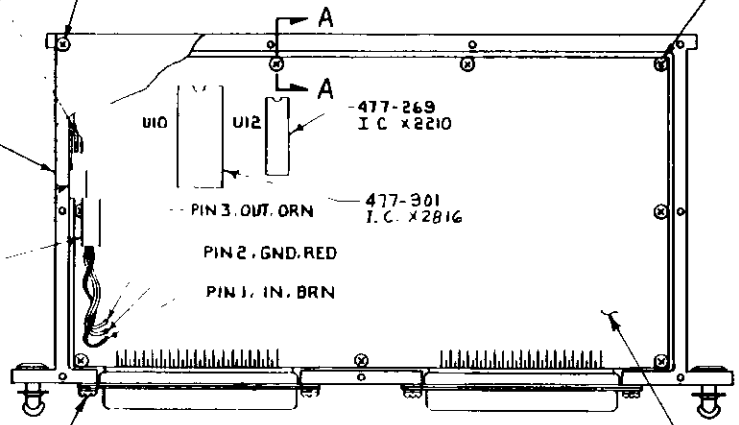
711-018, SCREW, XPHSS, 2-56 x 3/16
18 PLACES

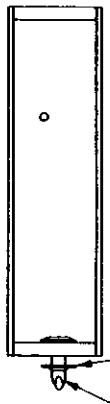
711-023, SCREW, XPHSS, 2-56 x 7/32
9 PLACES
767-055, WASHER, SPLIT, #2
9 PLACES
768-075, WASHER, FLAT, #2
9 PLACES

2140-1516
MODULE HOUSING

477-032
7805

2142-5051
CABLE ASSY



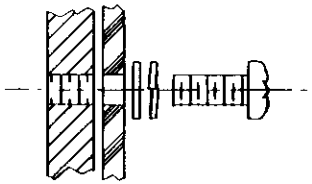


254-236, RETAINER
2 PLACES

254-235, STUD, 1/4 TURN
2 PLACES

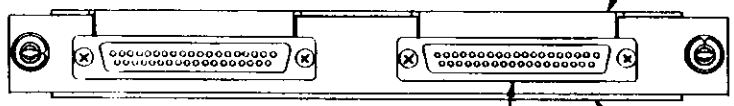
713-059, SCREW, XPHSS, 4-40 x 1/4
4 PLACES
767-056, WASHER, SPLIT, #4
4 PLACES

PANEL INTERFACE BD.
2140-2018



SECTION A-A
SCALE 4:1

2140-4403, FRONT MODULE COVER



2140-4404, REAR MODULE COVER

344-444, CONNECTOR
2 PLACES

1 RUBBER STAMP SERIAL NUMBER

NOTES: UNLESS OTHERWISE SPECIFIED

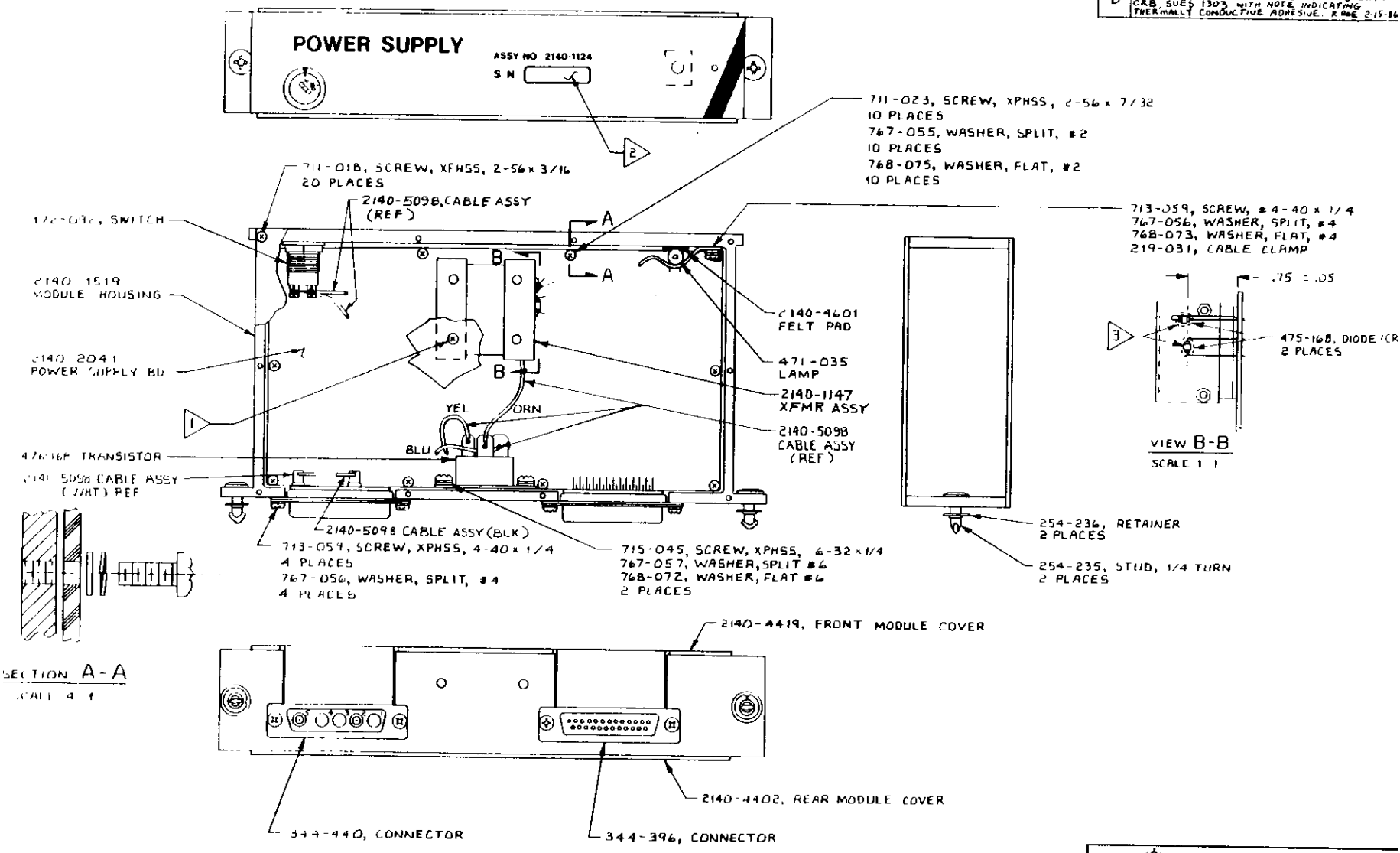
CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY: DEJ	DRAWN BY: E. ROBLES
DATE: 1-14-85		REVISED

PANEL INTERFACE MODULE

N/A	QTY	MODEL	REV	DRAWING NUMBER
2147-4010	2/3	P-2140-4404	D	2140-1116

REVISION	
LTR	DESCRIPTION
A	ECN # 2140-13, CHANGED COAX CABLE NUMBERS, ADDED REVISION LETTER "A" E.D.R. 1-23-85
B	ECN # 2140-134, CHANGED 2140-5099 CABLE ASSY (WHT) TO 2140-5098 E.D.R. 4-10-85
C	ECN # 2140-153, ADDED 2140-1147 XFMR ASSY. AJG 6-12-85
D	ECN # 2140-216A, ADDED VIEW SHOWING CR7 & CR8, SUES 1303, WITH NOTE INDICATING THERMALLY CONDUCTIVE ADHESIVE.



1 > DIODES TO BE SECURED AGAINST XFMR BRACKET WITH THERMALLY CONDUCTIVE ADHESIVE (ITEM 29)

2 > RUBBER STAMP SERIAL NUMBER

3 > USE 713-003, SCREW, XPHSS, 100, #4-40 x 5/8, (4)

NOTE:

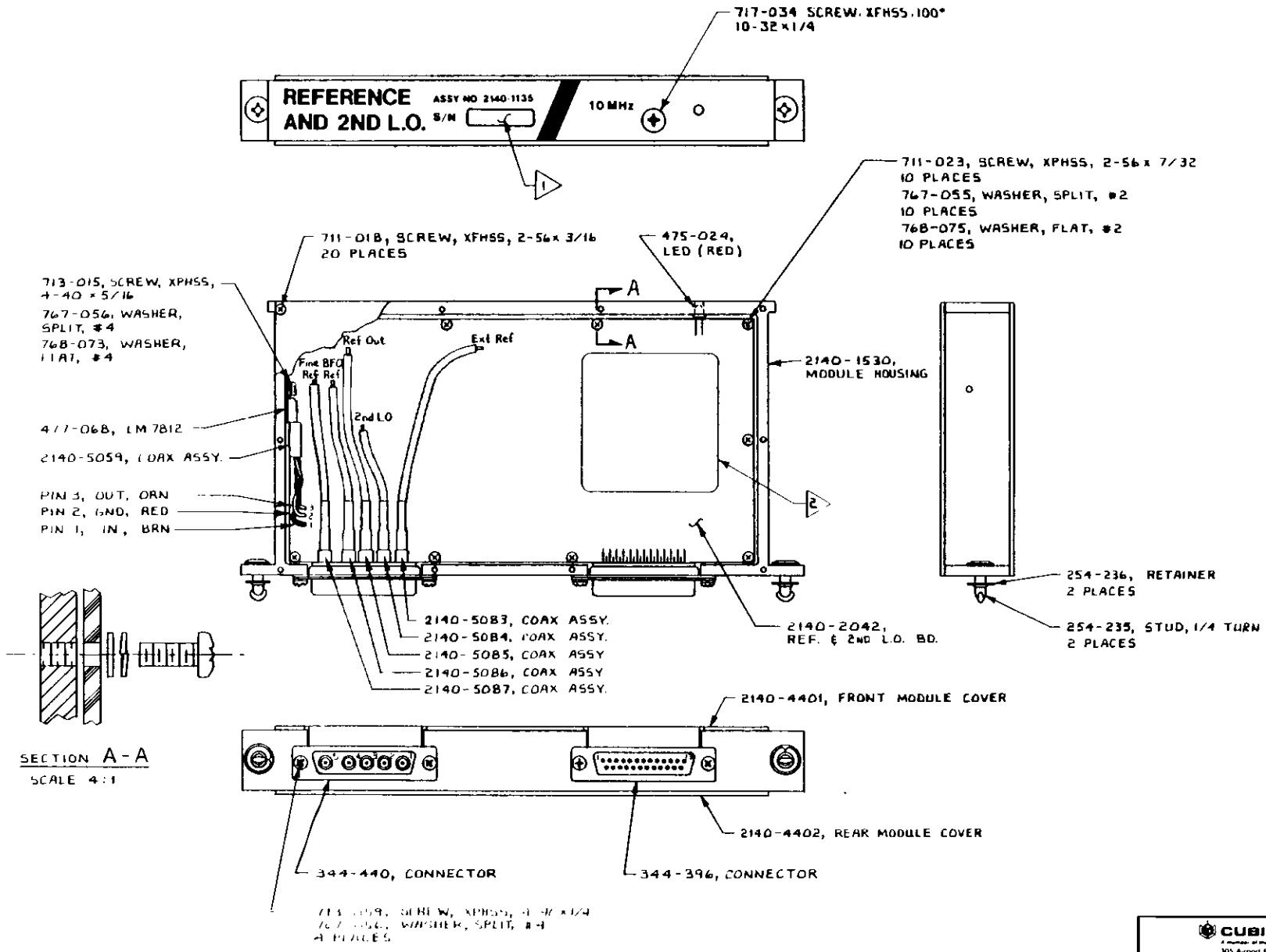
CUBIC COMMUNICATIONS

SCALE 1 1 | APPROVED BY | DRAWN BY

DATE 12-20-84 | REVISED

POWER SUPPLY MODULE

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140-13. CHANGED COAX CABLE NUMBERS ADDED REVISION LETTER "A", ADDED NOTE 2. E.D.R. 1-23-85		



2. REMOVE SCREW FROM J2XG BEFORE INSTALLING BOARD IN MODULE.

1. RIBBED SIDE OF KNOB TOWARDS

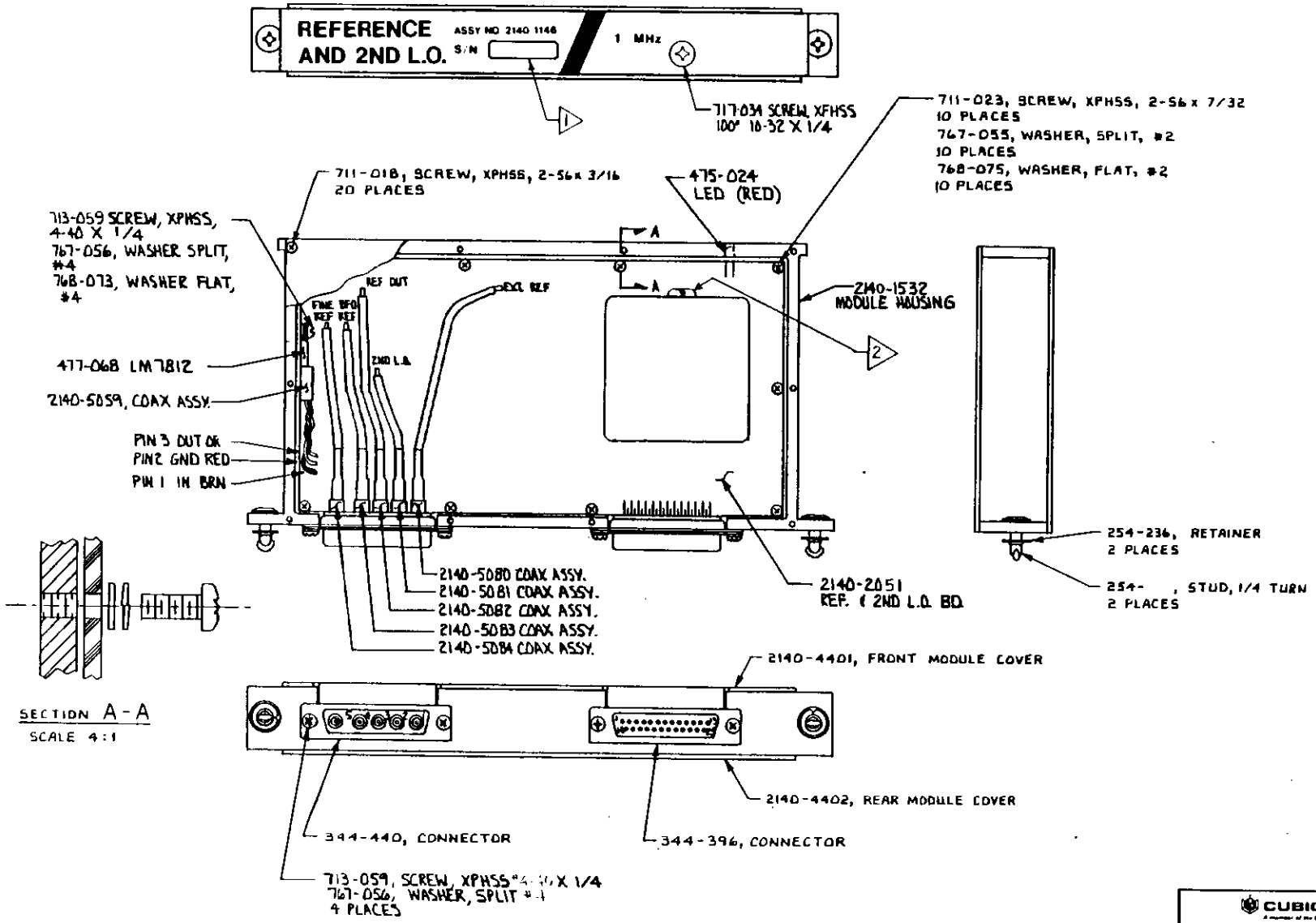
CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd. Oceanside CA 92054

SCALE 1/1	APPROVED BY:	DRAWN BY K. KOIL	
DATE 1-25-84		REVISED	

REF & 2ND LO MODULE

N/A	QTY	MODEL	REV	DRAWING NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD



2 > REMOVE SCREW FROM TCXO BEFORE INSTALLING BOARD IN MODULE.

1 > RUBBER STAMP SERIAL NUMBER.

NOTES: UNLESS OTHERWISE SPECIFIED

CUBIC COMMUNICATIONS

A member of the Cubic Corporation family of companies

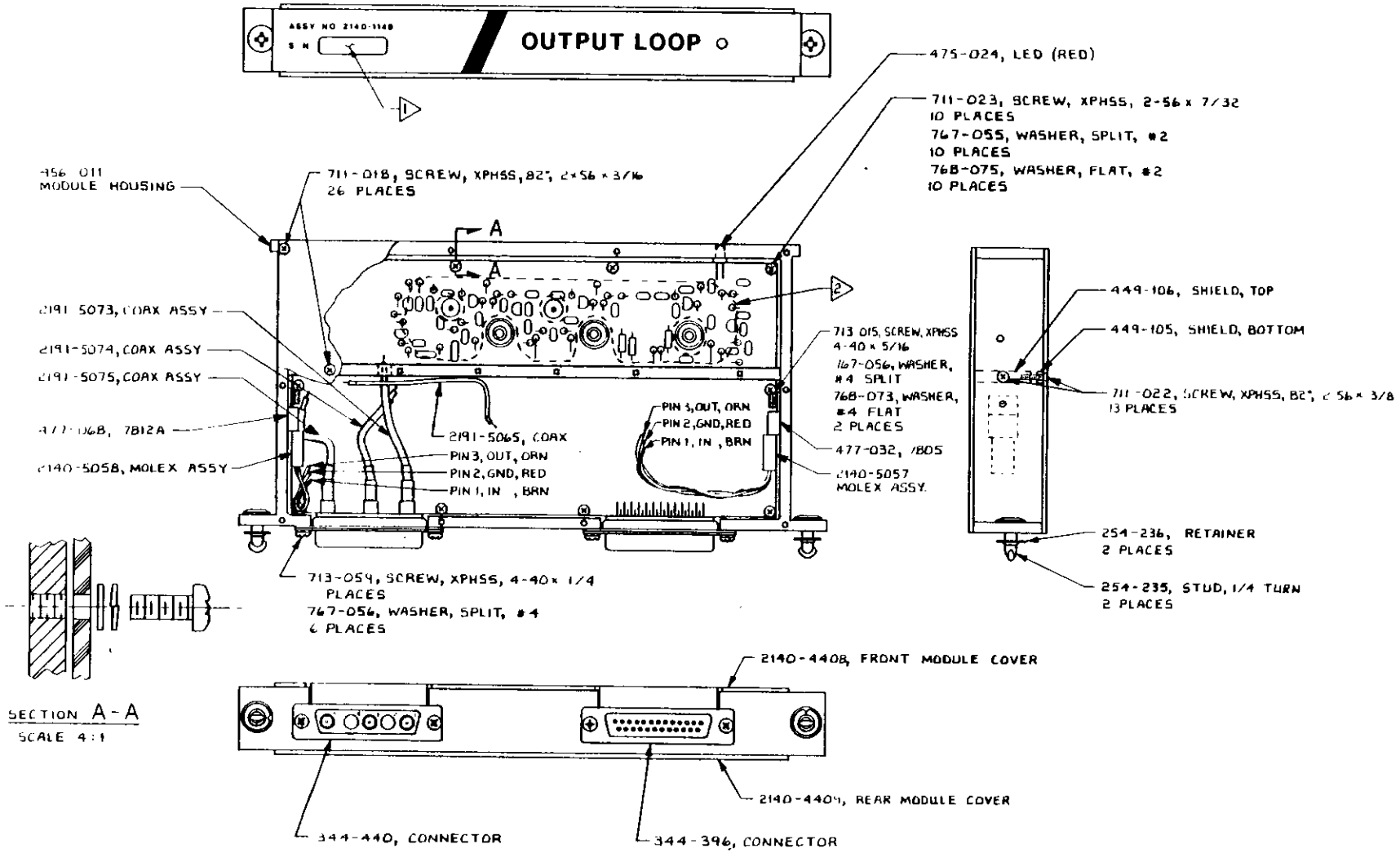
305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY:	DRAWN BY
DATE: 3 / /		REVISED

REF & 2ND L.O. MODULE (1MHz)

N/A	SIZE	MODEL	REV	DRAWING NUMBER

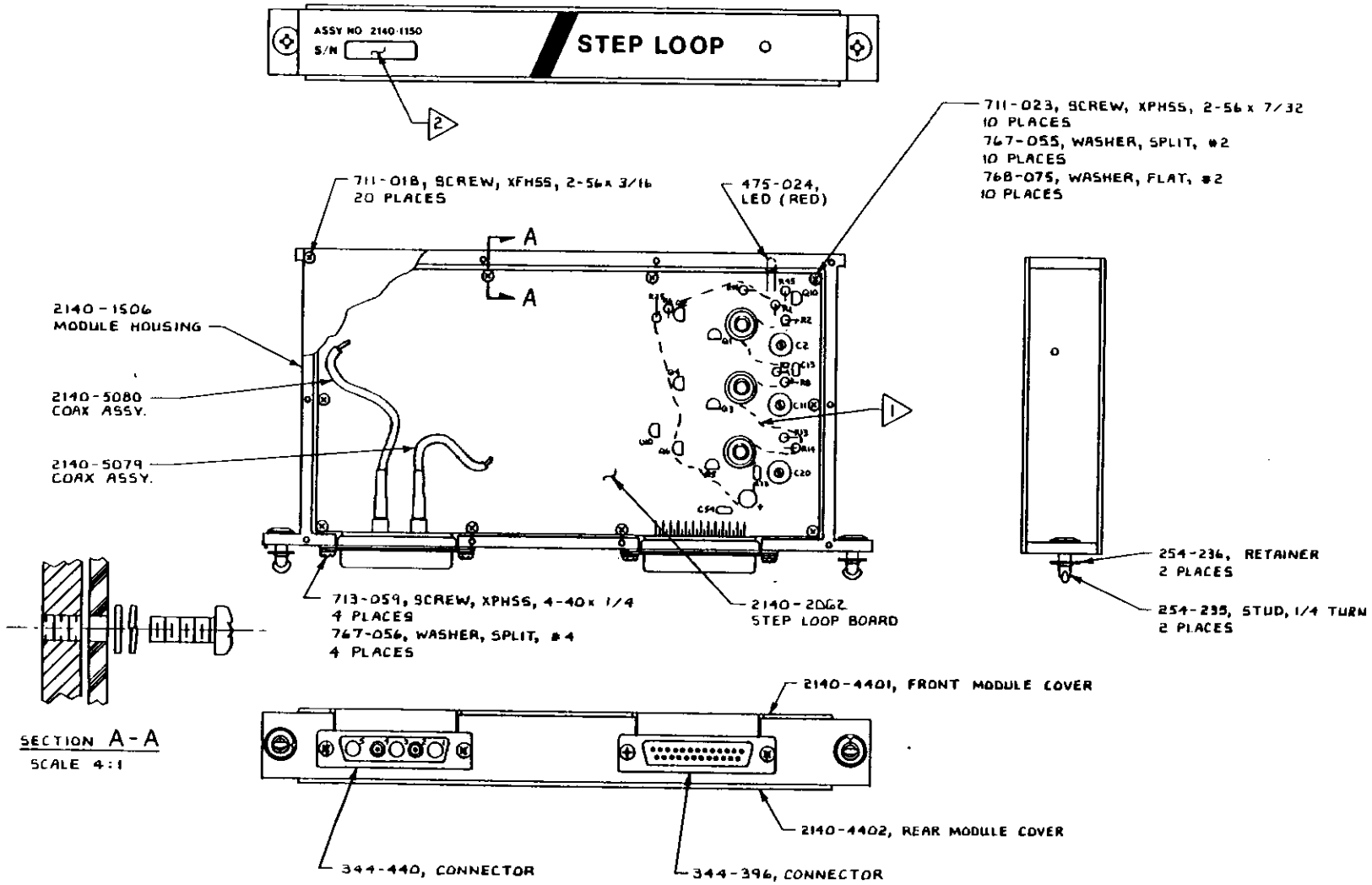
REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN #2140-193: REV. B/M. R.RUE 12-4-85		



CUBIC COMMUNICATIONS

SCALE 1/1	APPROVED BY	DRAWN BY R. RUE
DATE 11-27-85		REVISED

OUTPUT LOOP MODULE



SHEET 1 OF 2

N/A	QTY	MODEL
2144-1010	2	R-3030
2145-1010	2	R-3030A
2541-1010	1	R-3050
2721-1010	1	R-3080

CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

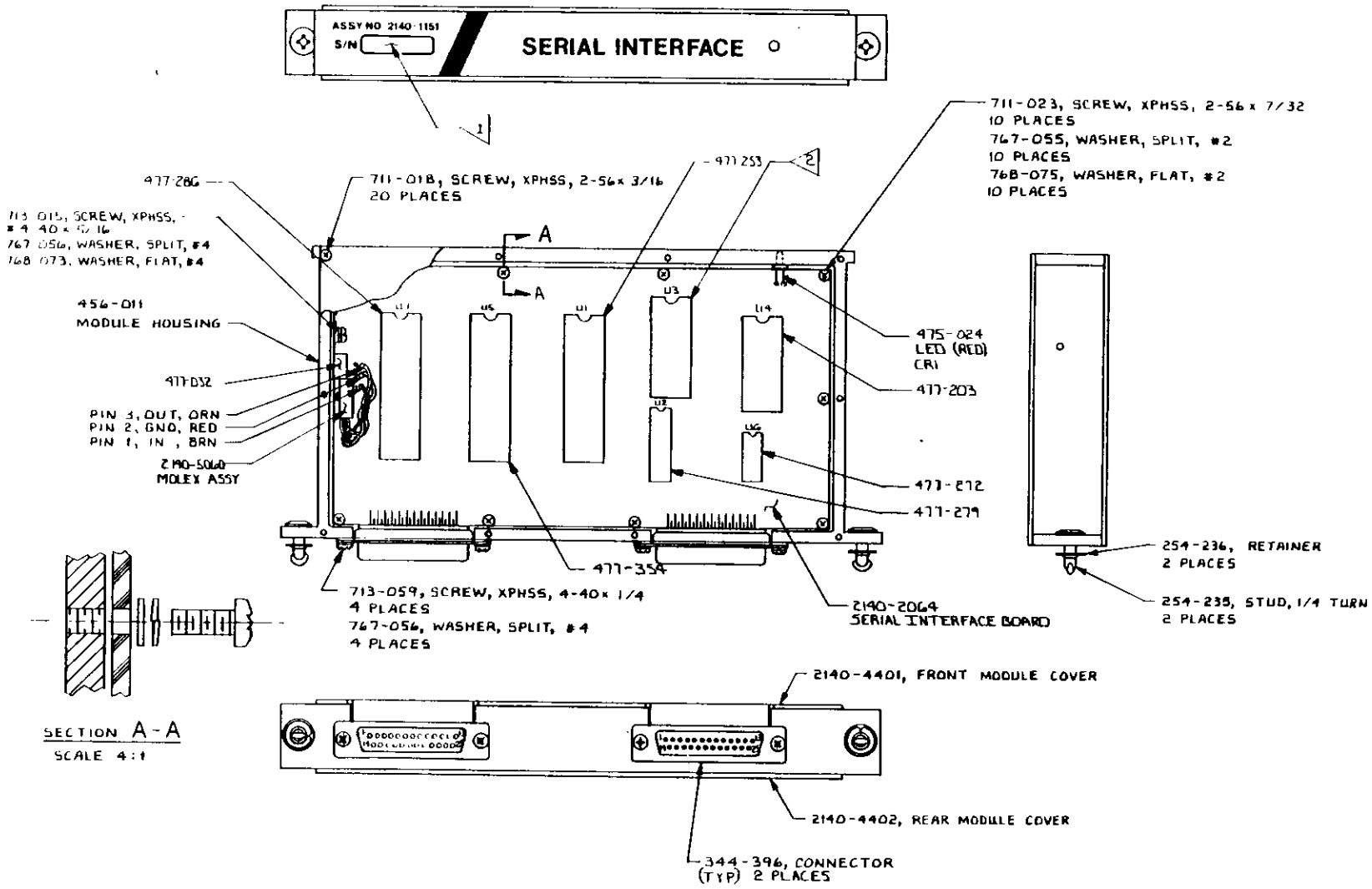
SCALE: 1/1 | APPROVED BY: | DRAWN BY R. ROE
DATE: 10-30-85 | REVISED

STEP LOOP MODULE

2> RUBBER STAMP SERIAL NUMBER.

1> APPLY 3145 RTV (CLEAR) DOW-CORNING TO AREA INCLOSED BY DASH LINE

REVISION			
LTR	DESCRIPTION	DATE	APPD



2 > 113 E PROM INSTALLED PER OPTION LIST. REFER TO BILL OF MATERIALS 2145-3002

1 > RUBBER STAMP SERIAL NUMBER.

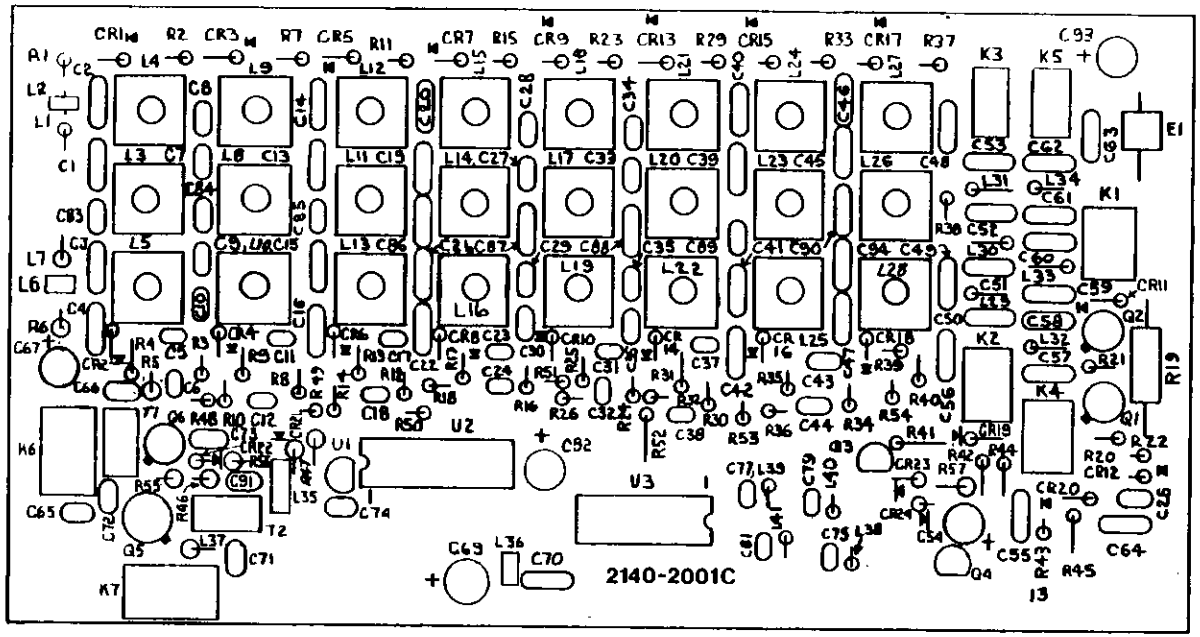
NOTES: UNLESS OTHERWISE SPECIFIED.

CUBIC COMMUNICATIONS
A member of the Cubic Corporation family of companies
305 Airport Rd Oceanside CA 92054

SCALE: 1/1	APPROVED BY	DRAWN BY MK
DATE: 11-22-85		REVISED

SERIAL INTERFACE MODULE ASSY

REDUCE TO 8.000 ± .005



6. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. REF: SCHEMATIC NO. 2140-2401
2. REF: CKT BD NO. 2140-2101.
1. SCREEN COMPONENT SIDE USING 2140-2001

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

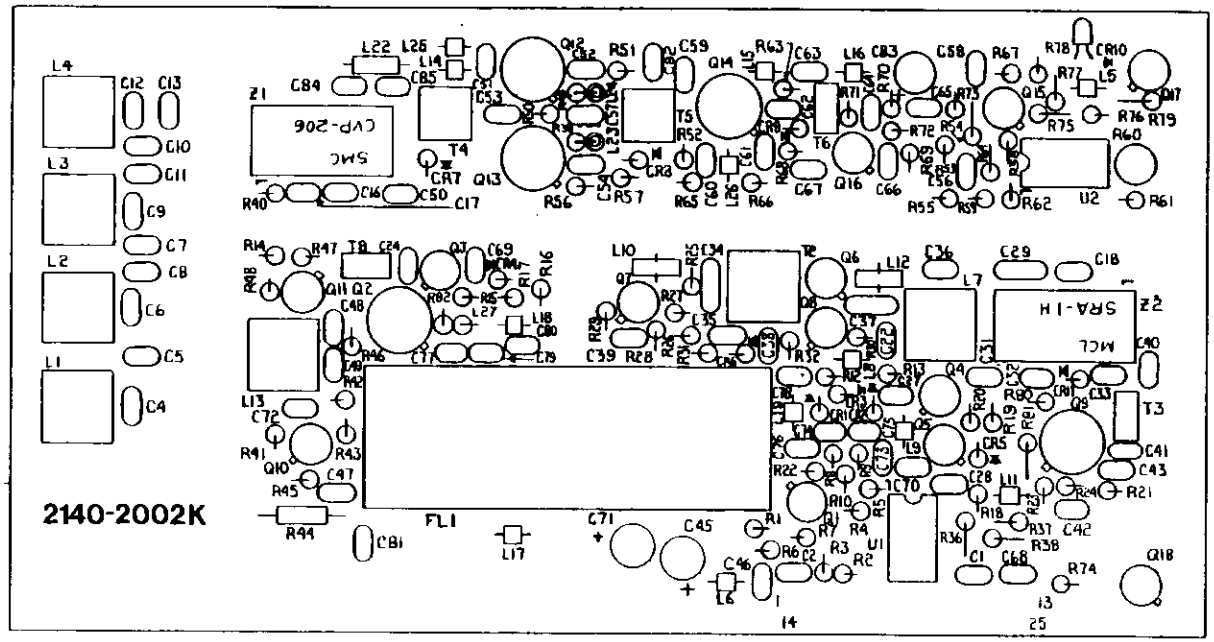
SCALE: 2:1 | APPROVED BY: | DRAWN BY E. BRUNT

DATE: 6-25-84 | REVISED E.D.R.

PRESELECTOR BOARD ASSY

REDUCE TO 6.740 ± .005

REVISION			
LTR	DESCRIPTION	DATE	APPD
E	REVISED & UPDATED 8-24-84		
F	REVISED & UPDATED E.O.R. 9-13-84	9/14/84	
G	ECN # 2140-2, R53 WAS 5.6K, R58 WAS 10K, R61 WAS 5.6K & R71 WAS 39Ω. SHEET 2 AFFECTED AUG 11-14-84	11/14/84	
—	ECN # 2140-36: ADDED NOTES ▷4▷ TO SHEET 2. AFFECTED COMPONENTS FLAGED. E.O.R. 2-7-85		
H	ECN # 2140-501 RB1,100 WAS L21,1T. CHANGED SYMBOL FOR RB1; T3,3T,3T WAS 8T,1T; C41, 100pF WAS 68pF, R21,39 WAS 68. DELETED L21 FROM NOTE ▷ SHEET 2. E.O.R. 2-8-85	2/11/85	
J	ECN # 2140-54, AFFECTED SHT 2, R69 390 WAS R69 100 E.O.R. 2-19-85	2/19/85	
—	ECN # 2140-92, AFFECTED SHT 2, ADDED VALUE 15 TO R49 E.O.R. 3-15-85	3/19/85	
—	ECN # 2140-120, AFFECTED SHT 2, C2 .0047uF WAS .0047uF E.O.R. 3-30-85	3/30/85	
—	ECN # 2140-128, SHEET 1: ADDED POLARITY TO Q7, SHEET 2: ADDED VALUE 390Ω TO R27 ADDED POLARITY TO Q7 E.O.R 4-5 85	4/5/85	
—	ECN # 2140-137, CORRECTED PICTURE OF T8 ON SHT 2 T8 2T:4T CHG WAS T8 4T:2T E.O.R 4-15 85	4/15/85	
K	ECN # 2140-141, SHT 1: RELOCATED C77 & C79 DELETED T7, ADDED RB2 & L27 SHT 2: C77 27pF WAS .0047 ADDED RB2 470 & L27 0 4/7 E.O.R 4-30-85	4/30/85	
—	ECN # 2140-196, ON SHT 2, 6A9, G12, B13 & G14, JUMPERS WAS WIRES 1/61-11-86	11-6-86	



1. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS
3. RESISTANCE VALUES IN OHMS 1/4W, 5%
4. REF SCHEMATIC 2140-2402
5. REF CKT BOARD NO. 2140-2102
6. SCREEN COMPONENT SIDE USING 2140-2002

NOTES UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

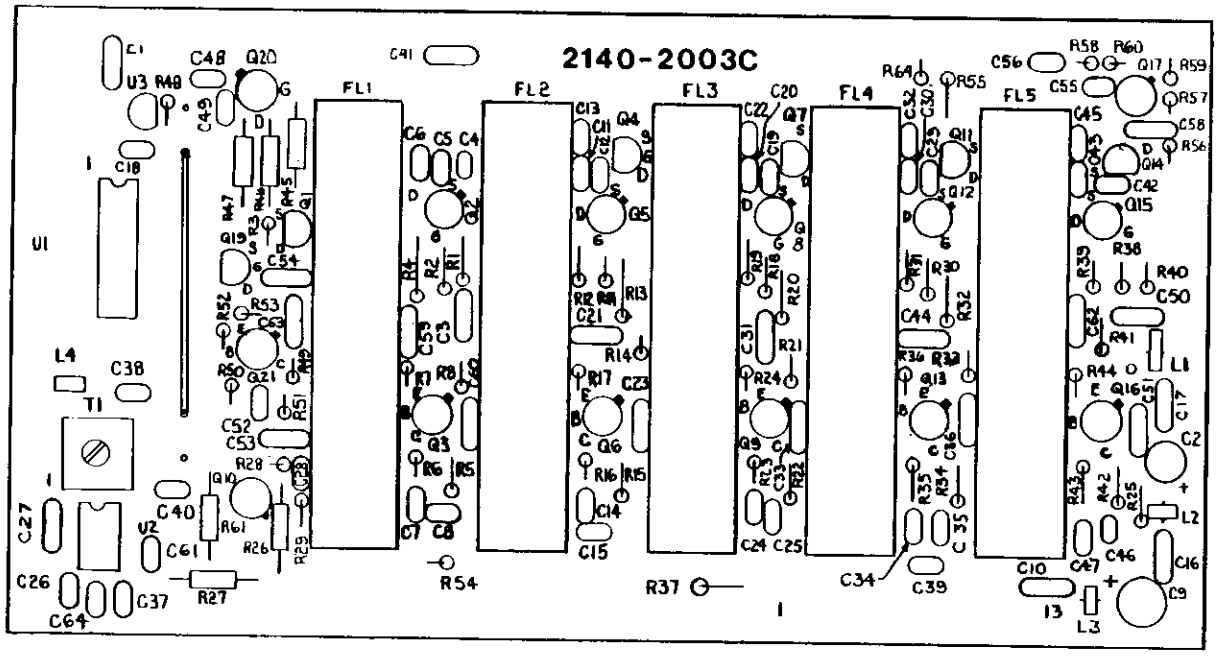
CUBIC COMMUNICATIONS

SCALE 2:1	APPROVED BY:		DRAWN BY E. BIGGLES
DATE 4-25-84			REVISED

FIRST IF BOARD ASSY

N/A			DRAWING NUMBER 2140-2002

REDUCE TO 4.000 ± .005



6. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. REF: SCHEMATIC NO 2140-2403
2. REF: CKT BD NO. 2140-2103
1. SCREEN COMPONENT SIDE USING 2140-2003

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

SCALE: 2:1 | APPROVED BY: | DRAWN BY: E. BRUER

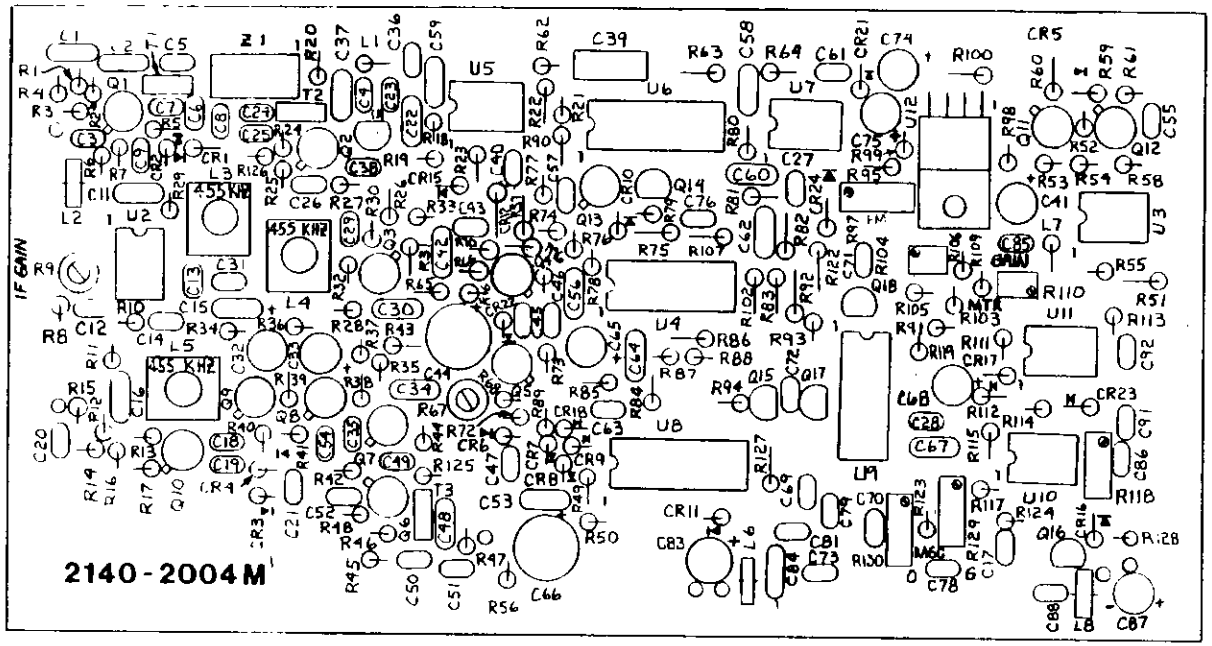
DATE: 9-10-84 | REVISED: E.D.R

2ND I.F. BOARD ASSY

REVISIONS

LTR	DESCRIPTION	DATE	APPD
C	REVISED & UPDATED	7/17/84	
D	REVISED & UPDATED EDR 9-11-84	9/11/84	JEP
E	ECN 2140-4, REVISED DWG. #, WAS U13, REVERSED C83 + SIGN ADDED TO SYM. TO CR10 AJG 11-29-84	11/29/84	AJG
—	ECN # 2140-20 R91 ADDED 1K; R22, 47K WAS 470; R52 ADDED 10K; R87, 100K WAS 10K, CR13 ADDED POLARITY MARKING. THIS REVISION AFFECTS SHEET 2 OF 2 ONLY. RRUE 1-22-85	1/22/85	AJG
F	ECN # 2140-27, C7 ADDED .0047, C48 & C23 ADDED .033, R70 ADDED 3.6K; R82 270K WAS 820. CORRECTED CR10 DIODE SYMBOL SHTS 1 & 2 AFFECTED AJG 2-4-85	2/4/85	AJG
—	ECN # 2140-38: ADDED NOTE [D] TO SHEET 2; AFFECTED COMPONENTS FLAGED R RUE 2-7-85	2/5/85	AJG
G	ECN # 2140-55: SHEET 2 CHANGE R84, 100K WAS 180K. R RUE 2-14-85	2/14/85	AJG
H	ECN # 2140-66, ON SHT 2, CHG R62 FROM 10K 1% TO 8.25K, 1%, CHG R95 FROM 17.5K, 5% TO 3.32K, 1%, CHG R100 FROM 10K, 1% TO 82.5K, 1%, CHG R98 FROM 4.42K TO 3.9K AJG 2-22-85	2/22/85	AJG
J	ECN # 2140-80, R62 8.66K WAS 8.25K, R83, 22K WAS 27K, R95, 750 & R98 3.9K, ON 2ND, IN 914 B WAS R96, 2.2K THIS AFFECTS SHT 2 AJG 3-4-85	3/4/85	AJG
K	ECN # 2140-86, REVISED PICTURE OF R104, R110, R95, R130, R129, SHT 2 C96, 097 WAS 0.1 E.D.R 3-8-85	3/8/85	AJG
L	ECN # 2140-134: ADD R118 TO ADJ POT WAS 10K R RUE 7-8-85	7/8/85	AJG
M	ECN # 2140-211: R70, 3.0K WAS 3.6K. R71, 33Ω WAS 47Ω, R89, 470Ω WAS 220Ω. ADD R96, 1K. ADD CR12, IN914B MK 2-12-86	2/12/86	AJG

REDUCE TO 6.000 ± .005



1. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%.
5. REF DES GO TO 2140-2004
6. SHOWN COMPONENT SIDE OF DWG 2140-2004
7. REF 2140-2404 SCHEMATIC DWG

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

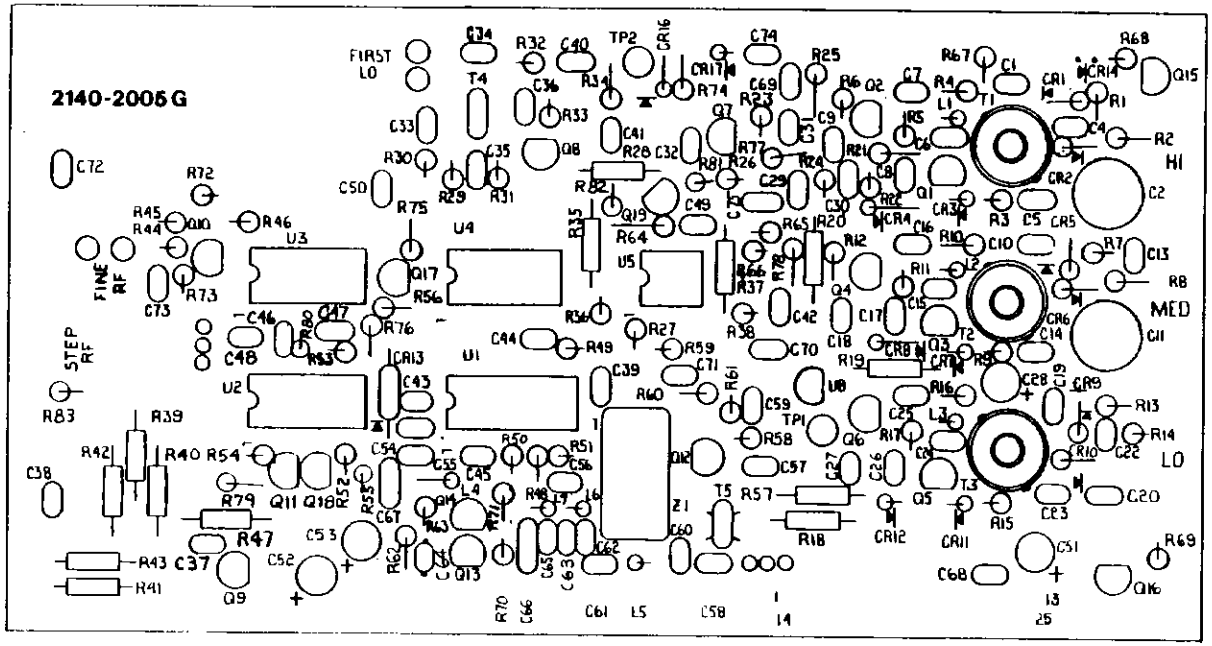
SCALE 2:1	APPROVED BY:		DRAWN BY R RUE
DATE 7-17-84			REVISED 1-24-84

DETECTOR BOARD ASSY

SIZE	REF	MODEL	REV	DRAWING NUMBER
				2140-2004

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED E.D.R 9-13-84	9/1/84	JEL
B	ECN #2140-7, REVISED PICTURE OF CR1, CR2, CR5, CR6, CR9 & CR10 AJG 12-13-84	12/12/84	JEL
C	ECN #2140-11, ADDED Q18, R79, R80, REVISED PICTURE OF Q11, C46, R53, R54, R42, R47, R52, R54, & R55. ADDED R81, R82 & R83. ADDED Q19 & C64 ECN # 2140-23, CR1, 5, 6, 9 & 10 BB609B WAS MV209 E.D.R 1-24-85	1/25/85	JEL
—	ECN #2140-46: ADDED NOTES 4 & 5 AFFECTED COMPONENTS PLACED. R. ROE 2-11-85	2/11/85	JEL
D	ECN # 2140-54, ON SHT 2 - R31, 1K WAS 220. AJG 2-14-85	2/14/85	JEL REW
E	ECN # 2140-73, ON SHT 2, R28, 470Ω W/5.1KΩ. AJG 2-27-85	2/27/85	JEL
—	ECN # 2140-94, ADDED NOTE 6 Q11 & Q18 TRANSISTORS ETC. TO SHT 2, ON SHT 2, C64, .01μF WAS .001μF E.D.R 3-18-85	3/18/85	JEL
F	ECN # 2140-125, SHT 1 CORRECTED PICTURE OF C20, SHT 2 CH 40-15pF WAS 3.5-23pF. CORRECTED PICTURE OF C10 E.O.R. 9-4-85	4-5-85	JEL JW
G	ECN # 2140-167: RELOCATED Z-17 CLOSE TO Q9. R. ROE 8-4-85		

REDUCE TO 7.000 ±.005



2. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. REF. SCHEMATIC NO. 2140-2405
2. REF: CKT BD NO 2140-2105.
1. SCREEN COMPONENT SIDE USING 2140-2005

NOTES: UNLESS OTHERWISE SPECIFIED

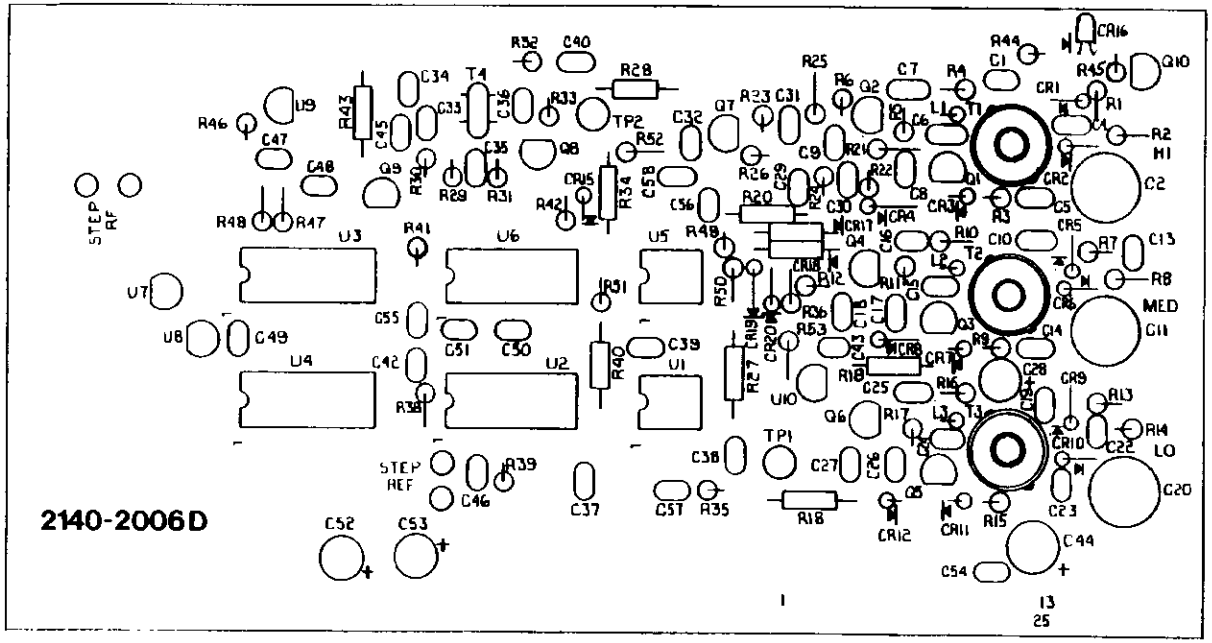
SHEET 1 OF 2

CUBIC COMMUNICATIONS

OUTPUT LOOP BOARD ASSEMBLY

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED E.O.R. 9-14-84	9/14/84	JEL
B	ECN # 2140-8, REVISED PLATING OF CR1,CR2,CR5,CR6,CR9&CR10 AJG 12-13-84	12/13/84	JEL
—	ECN # 2140-20, R5 ADDED 22; R3, 100K WAS 10; R1, 100K WAS 10; R6, 100K WAS 100; R7, 100K WAS 100; R8, 100K WAS 10; R4 ADDED 100K; R17, 100K WAS 100; R15, 100K WAS 100; R13, 100K WAS 100; R14, 100K WAS 100. R.R.E 1-22-85	1/22/85	JEL
C	ECN # 2140-23 CR1,2,5,6,9&10 BB6098 WAS MV209 E.O.R. 1-24-85	1/25/85	JEL
—	ECN # 2140-47 ADDED NOTES ▷ ▷ TO SHT 2, AFFECTED COMPONENTS FLAGED E.O.R. 2-11-85	2/11/85	JEL
D	ECN # 2140-131, SHT 2, C1 82 pF WAS 47pF, C10 100 pF WAS 68 pF C19 180 pF WAS 150 pF, T1 3T WAS 6T E.O.R. 4-8-85	4-8-85	JEL

REDUCE TO 7.000 ±.005



6. INDUCTANCE VALUES IN MICROHENRIES.
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%.
3. REF. SCHEMATIC 2140-2406
2. REF: CKT BOARD NO. 2140-2106
1. SCREEN COMPONENT SIDE USING 2140-2006

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

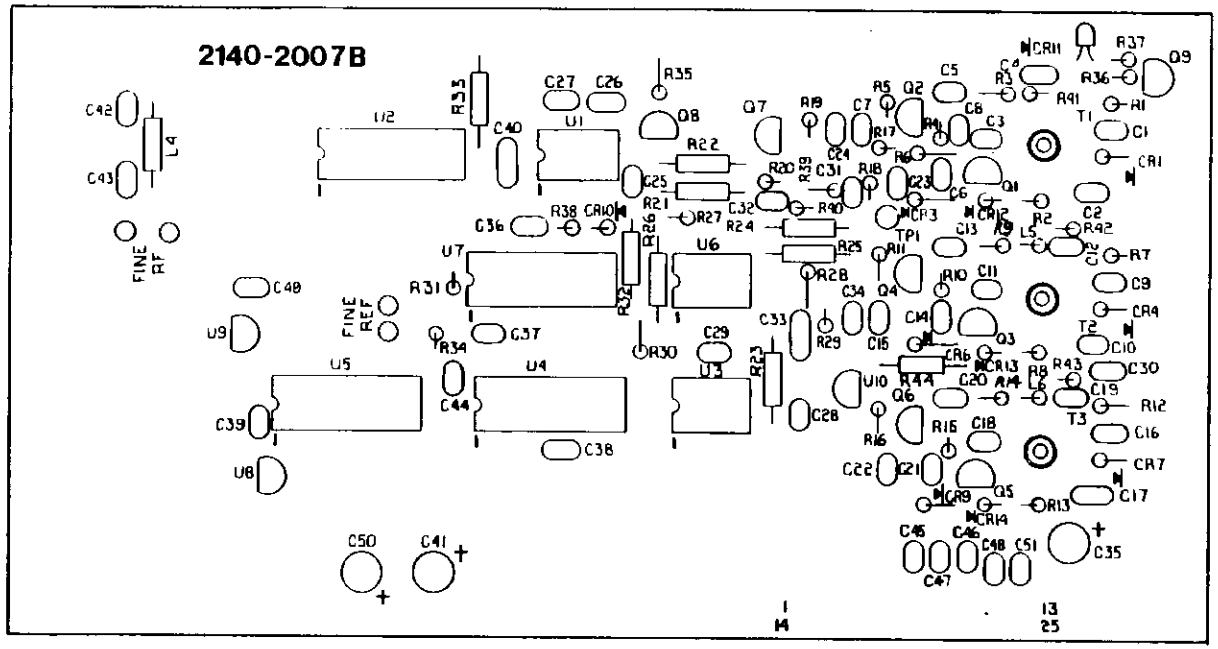
SCALE: 1:1	APPROVED BY:	DRAWN BY E. RIDLEY
DATE 1-13-89		REVISED

STEP LOOP BOARD ASSEMBLY

N/A		MODEL	REV	DRAWING NUMBER

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED E.D.R. 3-21-84		
B	REVISED & UPDATED E.D.R. 10-11-89		
—	[illegible]		
—	[illegible]		
—	[illegible]		
—	ECN #2140-164 [illegible]	11/6/[illegible]	

REDUCE TO 7.000 ± .005



6. INDUCTANCE VALUES IN MICROHENRIES.
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%.
3. REF: SCHEMATIC 2140-2407
2. REF: CKT BOARD NO. 2140-2107
1. SCREEN COMPONENT SIDE USING 2140-2007.

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

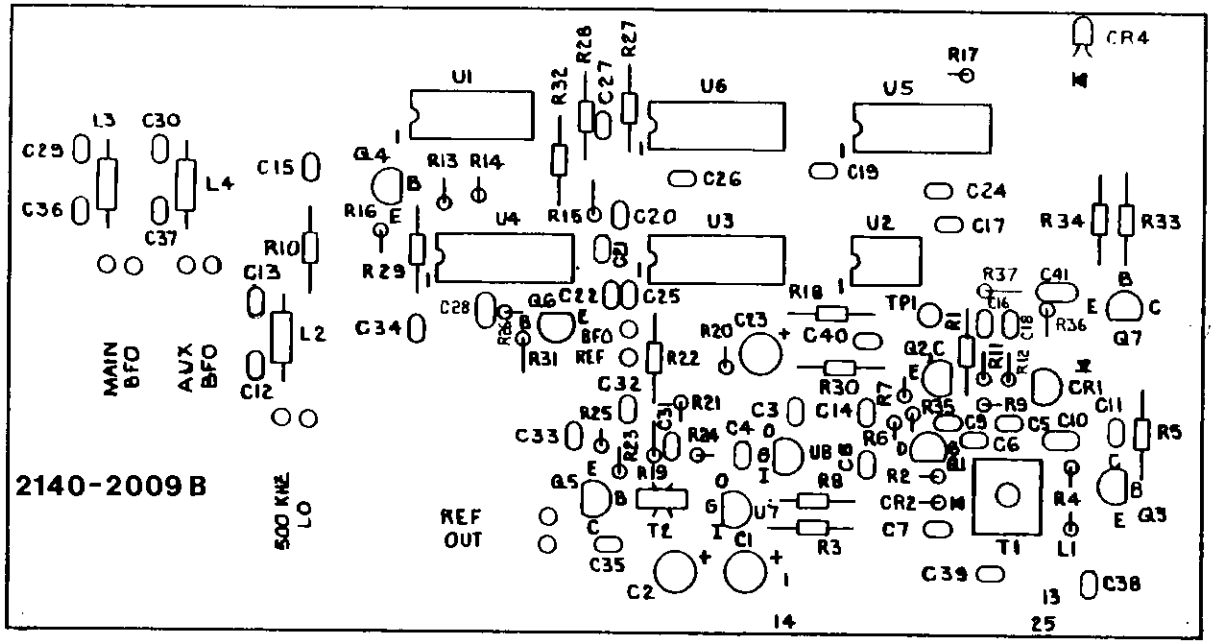
SCALE: 2:1	APPROVED BY:	DRAWN BY: E. ROBLES
DATE: 10-11-84		REVISED

FINE LOOP BOARD ASSEMBLY

N/A	QTY	MODEL	REV	DRAWING NUMBER

REDUCE TO 8.000 ± .005

LTR	REVISIONS DESCRIPTION	DATE	APPD
P	REVISED & UPDATED E.O.R. 9-24-84		
—	ECN # 2140-39 DES GNATION NO. U7 WA JB DESIGNATION NO UR WAS U7 E.O.R. 9-24-85		
P	ECN # 2140-39 ADDED NOTE 5 AFFECTED [illegible]		



6. INDUCTANCE VALUES IN MICROHENRIES.
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%.
3. REF: SCHEMATIC NO. 2140-2409
2. REF: CKT BOARD NO. 2140-2109
1. SCREEN COMPONENT SIDE USING 2140-2009

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

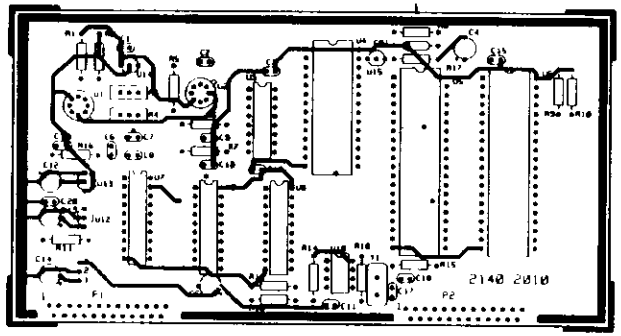
CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE 2:1	APPROVED BY	DRAWN BY E. Bunker
DATE 9-24-84		REVISED E.O.R.

BFO BOARD ASSEMBLY

N/A	QTY	MODEL	REV	DRAWING NUMBER

REVISIONS			
NO	DESCRIPTION	DATE	APPROVED
—	[illegible]		

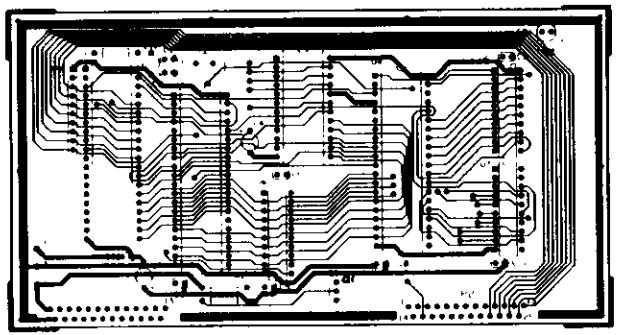


1. REF SCHEMATIC NO 2140-2410.
4. REF CIRCUIT BOARD NO 2140-2110.
3. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS
1. RESISTANCE VALUES IN OHMS 1/4W, 5%

UNLESS OTHERWISE SPECIFIED.

USED ON	DIMENSIONS ARE IN INCHES OVER INDICATED FINISHES TOLERANCES: ± DECIMAL .03, ± DECIMAL .010, ANGULARITY 1°	CUBIC COMMUNICATIONS
	PREPARED TEX	CPU BOARD ASSY
	CHECKED	SIZE C; CODE IDENT NO; NUMBER 2140-2010; REV
	DEPT APPVL	SCALE FULL; DO NOT SCALE PRINTS; SHEET
	DEPT APPVL	

REVISION			
LTR	DESCRIPTION	DATE	APPD
–	ECN # 2140-154: ADDED NOTE 1 R ROE 6-14-85		



COMPONENT SIDE SHOWN

2140-2013 : A

SHEET 1 OF 2

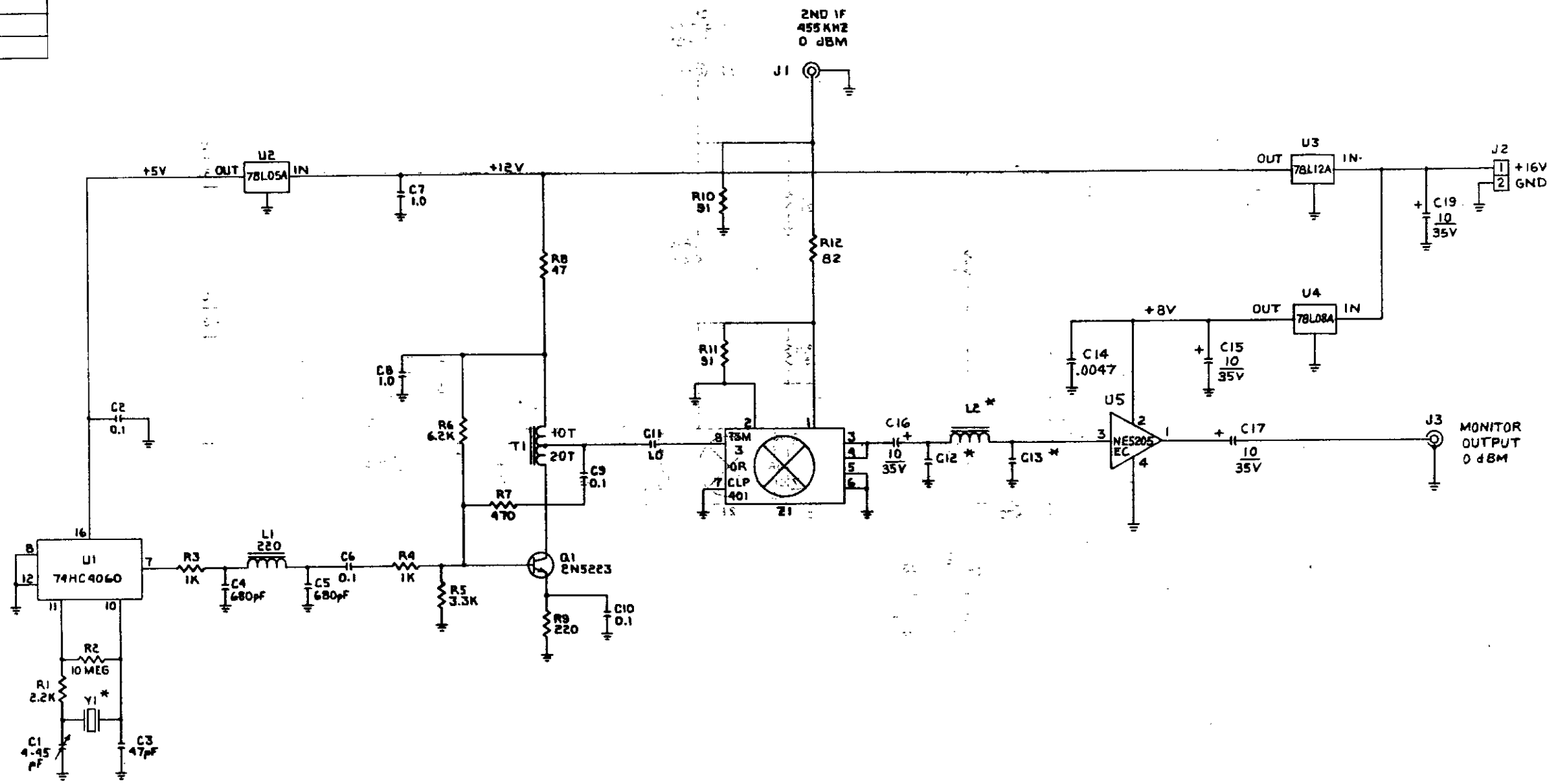
USED ON	DIMENSIONS ARE IN INCHES UNLESS INDICATED OTHERWISE TOLERANCES TWO PLACE DECIMAL .010 THREE PLACE DECIMAL .003 ANGULARITY 1°	CUBIC COMMUNICATIONS **ASSEMBLY DRAWING** IEEE 488 INTERFACE MOD
	DRAWN TEX 4 10 85 CHECKED ENGR APPR MFG APPR	SIZE C · DRAWING NO. 2140-20 3 · REV A SCALE NONE · WEIGHT · SHEET 1 OF 2

1. COMPONENTS LISTED ARE TO BE BONDED TO CIRCUIT BD. AFTER TEST USING PROCESS SPEC # 0900-1004. C4, C7, C12 & Y1 (SEE SHT 2)

NOTES: UNLESS OTHERWISE SPECIFIED

OUTPUT FREQ	Y1	L2	C12	C13
100 KHz	8.86MHz	56	.047	.047
5 KHz	7.52MHz	470	.15	.15

LTR	DESCRIPTION	DATE	APPD
A	ECN#2140E-151, REVISED CIRCUIT, R12 WAS 100Ω, R10, R11 WERE 82Ω. AJG 6-19-15	4/14/15	JER



LAST REF. DESIGNATION USED:
R18. C20. Q2. U3. L2. T2. Y1. Z1

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES IN OHMS 1/4 W. 5%
2. CAPACITANCE VALUES IN MICROFARADS.
3. INDUCTANCE VALUES IN MICROHENRIES.
4. *-SEE CHART ABOVE FOR VALUES.

CUBIC COMMUNICATIONS

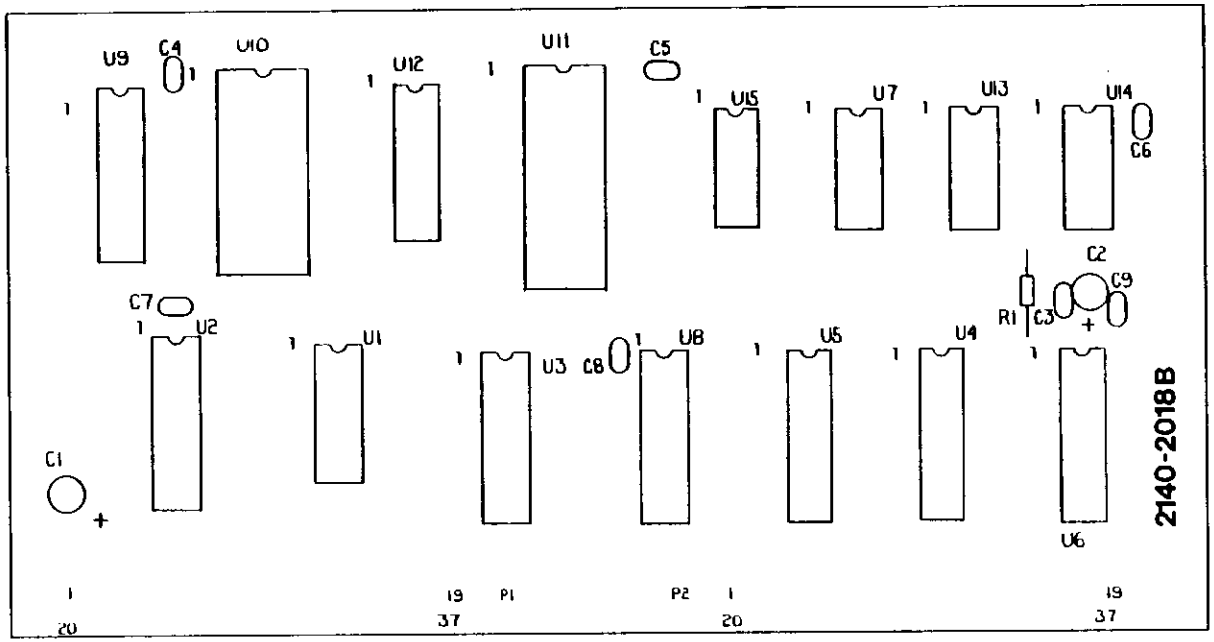
SCALE: NONE	DRAWN BY:	CHECKED BY: JER	APPROVED BY: E. ROBLES
DATE: 4-22-85			

OUTPUT CONVERTER BD. . SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
2143-2001			A	2143-2401

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED	6/26/84	JEL
—	ECN # 2140-44, ADDED NOTE 5 TO SHT 2, AFFECTED COMPONENTS FLAGED, E.D.R 2-8-85	2/8/85	JEL
B	ECN # 2140-89, CHG AFFECTS ASSY SHT 2 B-B/11 ONLY E.D.R. 3-4-85	3/4/85	JEL

REDUCED TO 6.740 ±.005



5. INDUCTANCE VALUES IN MICROHENRIES.
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. SCREEN COMPONENT SIDE USING 2140-2018
2. REF CKT BOARD NO. 2140-2118
1. REF. 2140-2418 SCHEMATIC

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

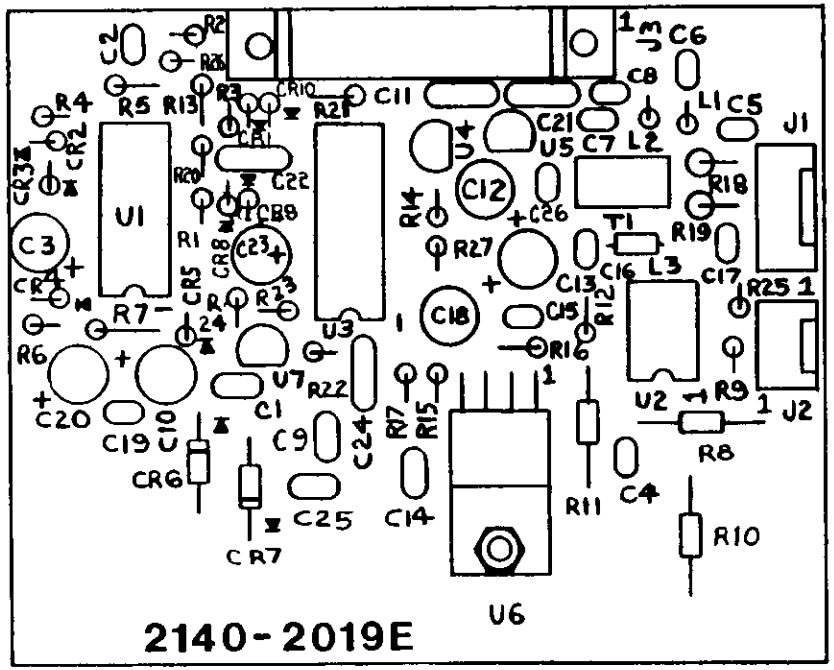
SCALE 2:1	APPROVED BY	DRAWN BY J. ROBLES
DATE 6-26-84	6/26/84	REVISED

PANEL INTERFACE BOARD

T/A	QTY	MODEL	REV	DRAWING NUMBER
2140-1116	1/2/2	R-S-5140	D	2140-2018

REVISION			
LTR	DESCRIPTION	DATE	APPD
B	REVISED & UPDATED	10/2/84	JEL
C	ECN #2140-9, CORRECTED TRACE ON ARTWORK AJG 12-15-84	12/15/84	JEL
—	ECN #2140-45: ADDED NOTE 1 ON SHEET 2. AFFECTED COMPONENTS FLAGED R.ROE 2-8-85		
D	ECN # 2140-91, ADDED CR10 DIODE. (1) IN34A E.D.R. 3-13-85	3/14/85	CAW JEL REW
—	ECN # 2140-102, CR8 VALUE IN5221B WAS IN5231B ON SHEET 2. E.D.R. 3-19-85	3/19/85	CAW JEL
E	ECN # 2140-122, ON SHT 2, CR10 IN5819 WAS IN34A. E.D.R. 3-30-85	3/30/85	CAW

REDUCE TO 4.000 ± .005



SHEET 1 OF 2

5. REF: SCHEMATIC NO. 2140-2419.
4. REF: CIRCUIT BOARD NO. 2140-2119
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED.

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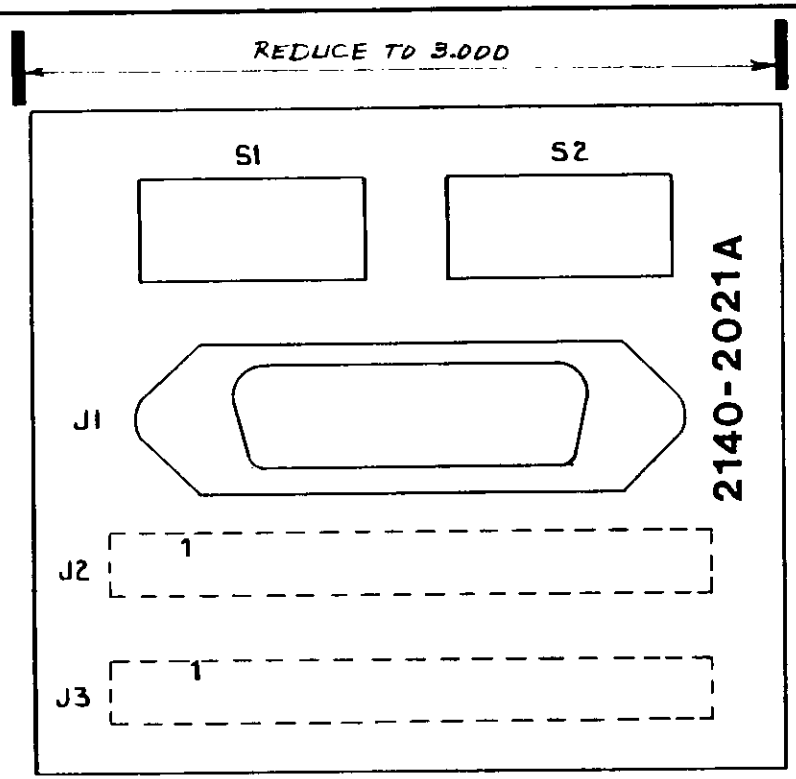
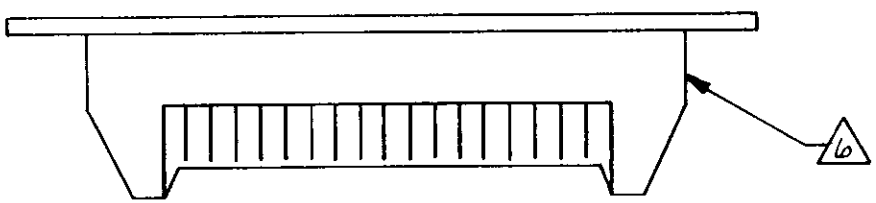
SCALE: 2:1	APPROVED BY: REW 1-22-84 JEL	DRAWN BY: E. BRINER
DATE: 12-4-84		REVISED

AUDIO BOARD ASSY

N/A	QTY	MODEL	REV	DRAWING NUMBER
2142-1102	212	R-2307/U	E	2140-2019





REVISIONS			
LTR	DESCRIPTION	DATE	APP'D
A	ECN#2140-170: REVISED ARTWORK + SCHEMATIC RWB 11-22-85	11-22-85	ER

⚠6 NOTE ORIENTATION OF CONNECTORS J2 / J3 (TYP. FARSIDE)

5. REF: SCHEMATIC NO. 2140-2421.
4. REF: CIRCUIT BOARD NO. 2140-2121.
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED.

CUBIC COMMUNICATIONS
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305 Airport Rd Oceanside CA 92054

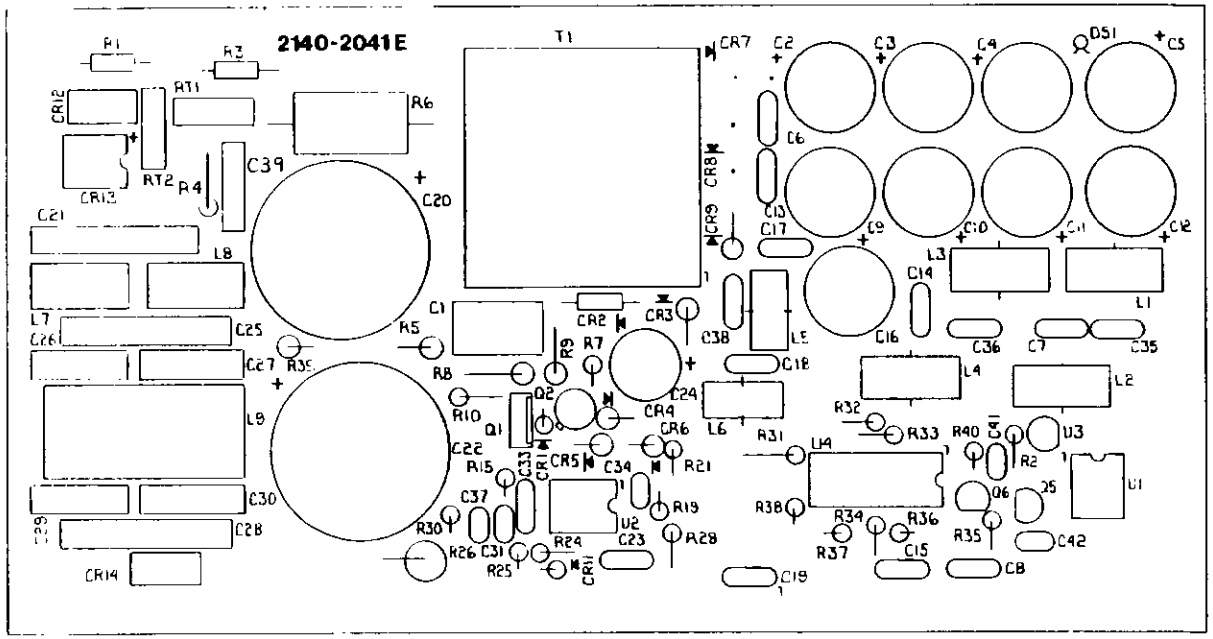
SCALE: 2:1	APPROVED BY: ER	DRAWN BY E. BRINK
DATE: 12-4-84		REVISED

IEEE 488 BUS CONNECTOR BOARD ASSY.

N/A	QTY	MODEL	REV	DRAWING NUMBER
2142-1103	2	R-3030	A	2140-2021

LET	REVISION	DATE	APPD
A	ECN # 2140-41 AND 41, DELETED FIGURE E OF 45 & 044 CMPS. THIS CHG AFFECTS SHT 1 & 2 AUG 2-4-85		
—	ECN # 2140-41: ADDED NOTE 1 TO SHEET 2. AFFECTED COMPONENTS FLAGED. R.ROE 2-6-85		
B	ECN # 2140-51 ADDED C39 & SYMBOL, MOVED R4 R.ROE 4-12-85		
C	ECN # 2140-160 ON SHT 2, R15, 16K 1/4W 1%		
D	ECN # 2140-204: SHT 2: REVISED R21 27K TO 19.1K 1% R28 4.7K TO 3.32K 1% DELETED RT1 & RT2 FROM NOTE 1 R.ROE 2-11-86		
E	ECN # 2140-216 A: DELETE DRAWING AND PART DESCRIPTION OF CR7 & CR8. R.ROE 2-19-86		

REDUCE TO 6.740 ± .005



6. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. REF SCHEMATIC NO 2140-2041
2. REF CKT BOARD NO 2140-2141
1. SCREEN COMPONENT SIDE USING 2140-2041

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

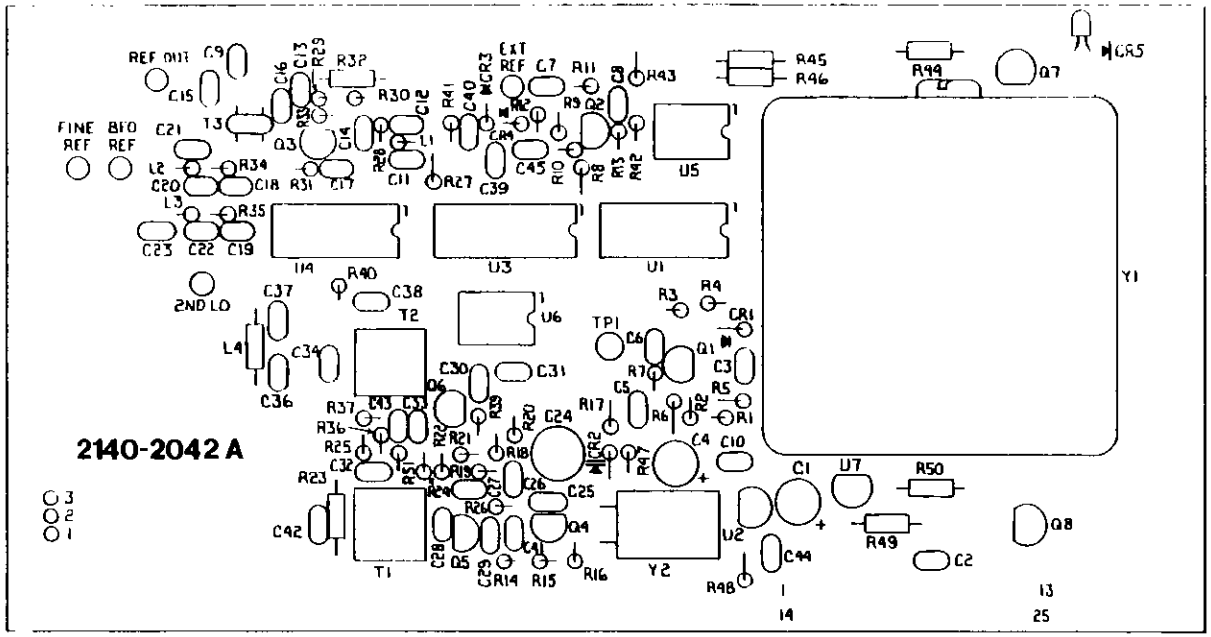
SCALE 2:1	APPROVED BY	DRAWN BY E ROBLES
DATE 10-2-84		REVISED

POWER SUPPLY BOARD

N/A	QTY 1/2	MODEL R-3020/30/40	REV	DRAWING NUMBER 2140-2041

REVISION			
LTR	DESCRIPTION	DATE	APPD
-	ECN # 2140-40. ADDED NOTE [illegible] TO SH. [illegible]. AFFECTED COMPONENTS FLAGGED [illegible] AS		
-	[illegible]		
A	[illegible] ARTWORK [illegible]		

REDUCE TO 6.740 ± .005



6. INDUCTANCE VALUES IN MICROHENRIES.
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%.
3. REF: SCHEMATIC NO. 2140-2442
2. REF: CKT BOARD NO. 2140-2142
1. SCREEN COMPONENT SIDE USING 2140-2042

NOTES: UNLESS OTHERWISE SPECIFIED

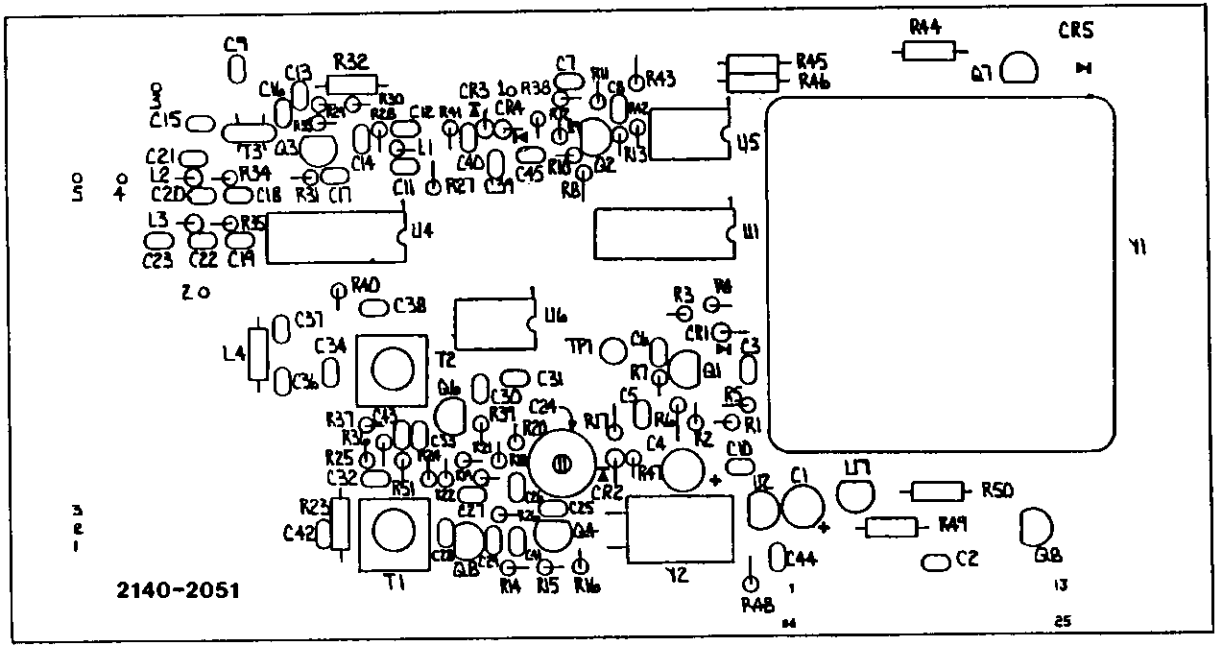
SHEET 1 OF 2

CUBIC COMMUNICATIONS

SCALE: 2:1	APPROVED BY: [illegible]	DRAWN BY E ROBLES
DATE: 10-4-84		REVISED

REFERENCE & 2ND L.O. BOARD

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-U35	1/C	R-3080/30	A	2140-2042



6. COMPONENTS LISTED ARE TO BE BONDED TO CIRCUIT BOARD AFTER TEST USING PROCESS SPEC 0900-1004. C1, C4, T3
5. REF. SCHEMATIC NO. 2140-2451
4. REF: CIRCUIT BOARD NO. 2140-2151
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

SHEET 1 OF 2

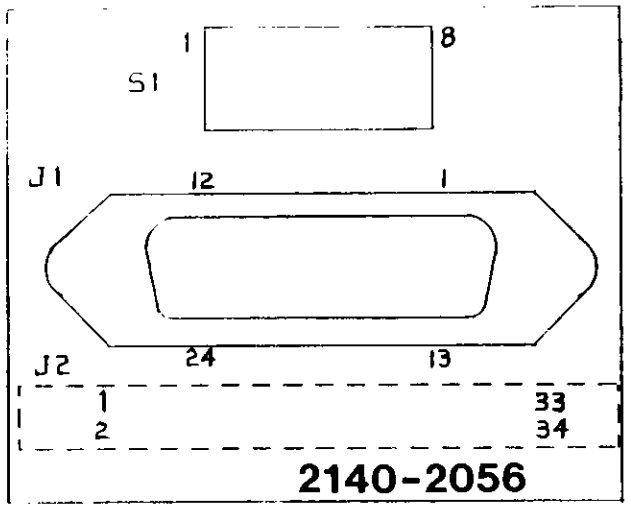
CUBIC COMMUNICATIONS

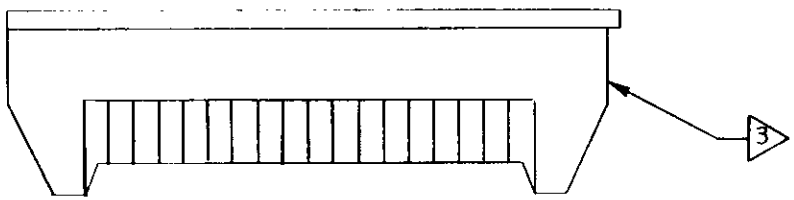
SCALE 2:1	APPROVED BY	DRAWN BY RC
DATE 3-25-85		REVISED

REF & 2ND L.O BOARD ASSY. (1 MHz)

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-1145	1	R-250/U		2140-2051

REVISIONS			
LTR	DESCRIPTION	DATE	AP





SHEET 1 OF 2

3 NOTE ORIENTATION OF CONNECTOR J2 (FARSIDE)
2. REF: SCHEMATIC NO. 2140-2456.
1. REF: CIRCUIT BOARD NO. 2140-2156
NOTES: UNLESS OTHERWISE SPECIFIED.

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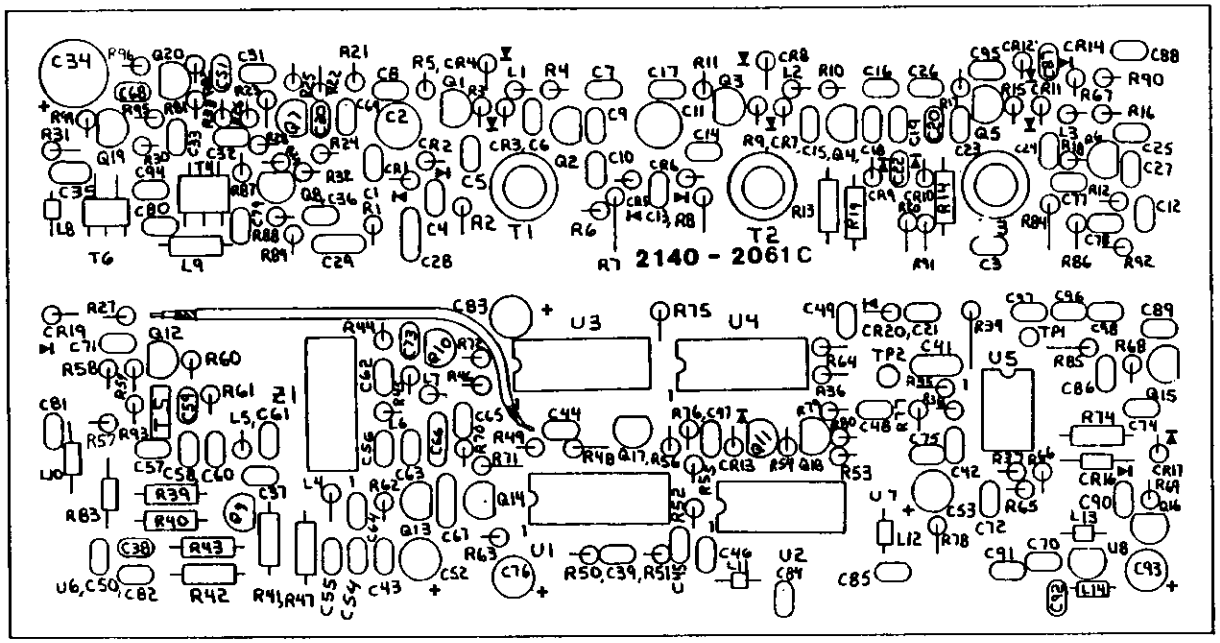
SCALE 2/1	APPROVED BY R. ROE 8-9-85	DRAWN BY R. ROE
DATE 7-16-85		REVISED

IEEE-488 BUS CONNECTOR BOARD ASSY.

N/A	QTY	MODEL	REV	DRAWING NUMBER
		R-3050/70/80		2140-2056



SHEET 1 OF 2

6. REF: SCHEMATIC NO. 2140-2461
5. REF: CKT BOARD NO. 2140-2161
4. SCREEN COMPONENT SIDE USING 2140-2061
3. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS
1. RESISTANCE VALUES IN OHM 1/4W, 5%

CUBIC COMMUNICATIONS

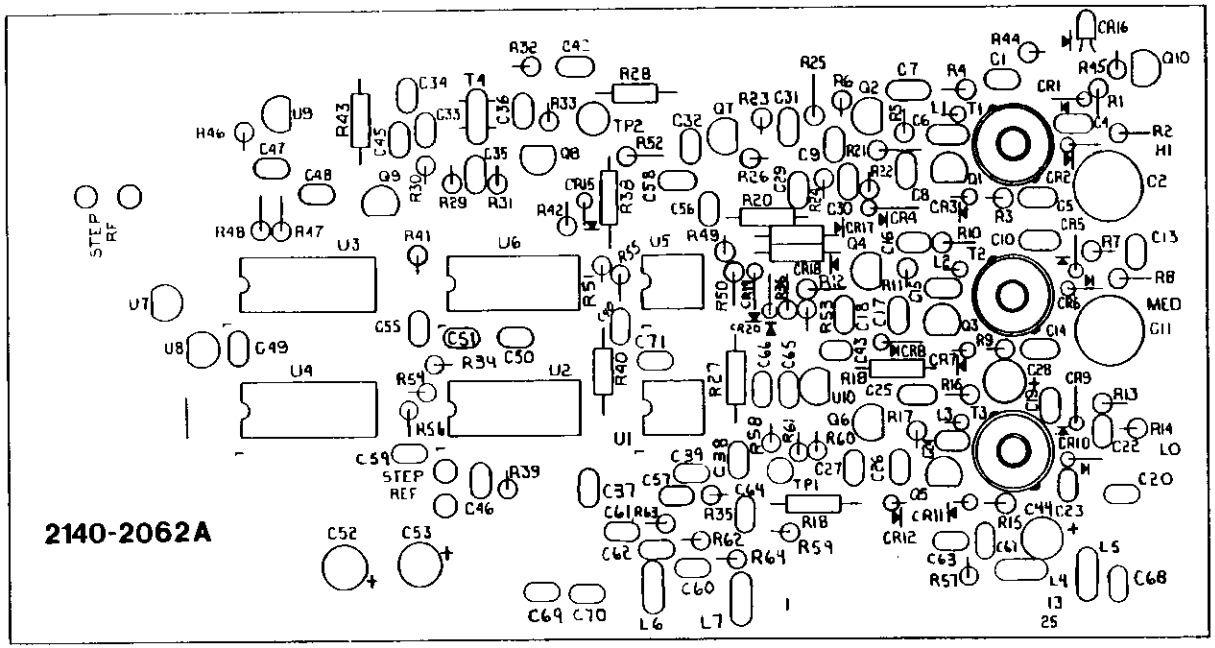
305 Airport Rd Oceanside CA 92054

SCALE NONE	APPROVED BY	DRAWN BY RWB
DATE 8 20 85		REVISED

OUTPUT LOOP BOARD ASS'Y

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-1148		A 3030 50 A0	C	2140-2061

REDUCE TO 7.000 ±.005



6. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4W, 5%
3. REF: SCHEMATIC 2140-2406
2. REF: CKT BOARD NO. 2140-2106
1 SCREEN COMPONENT SIDE USING 2140-2006

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

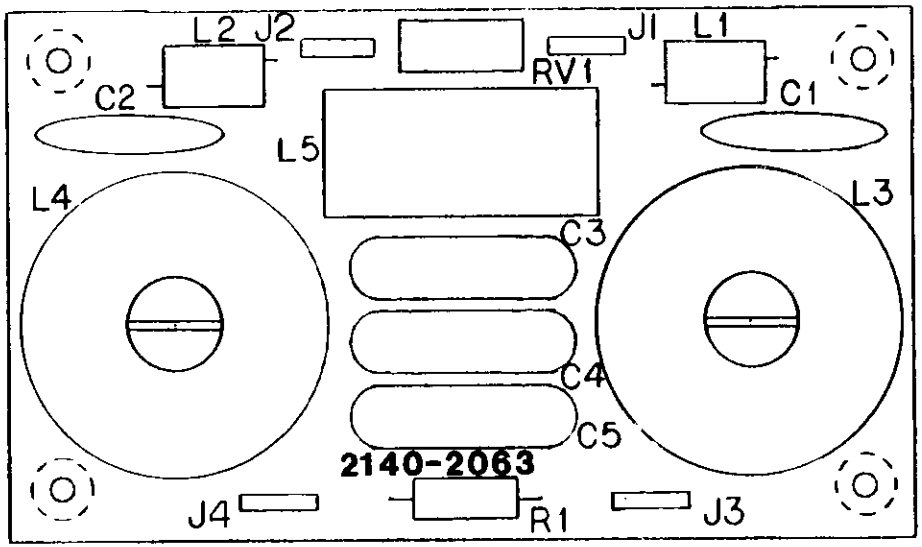
305 Airport Rd Oceanside CA 92054

SCALE: 2:1	APPROVED BY:	DRAWN BY RWB
DATE: 10-8-85		REVISED

STEP LOOP BOARD ASSEMBLY

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-2062	1/A	2140-2006	A	2140-2062

REVISIONS			
LTR	DESCRIPTION	DATE	APPD



SHEET 1 OF 2

6 COMPONENTS LISTED ARE TO BE BONDED TO CIRCUIT BOARD AFTER TEST USING PROCESS SPEC 0900-1004 C1, C2, C3, C4, C5, L1, L2, RV1 (REV. SHEET 2).
5 INDUCTANCE VALUES IN MICROHENRIES (REF. SHEET 2)
4 CAPACITANCE VALUES IN MICROFARADS (REF SHEET 2)
3. RESISTANCE VALUES IN OHMS, 1/4 W, 5% (REF. SHEET 2)
2 REFERENCE: SCHEMATIC NO. 2140-2463
1 REFERENCE: CKT BOARD NO. 2140 - 2163
NOTES: UNLESS OTHERWISE SPECIFIED.

N/A	QTY	MODEL
2191-1103	1/1	R-3040
2551-1010	1/1	R-3070
2145-1101	1/1	R-3030A

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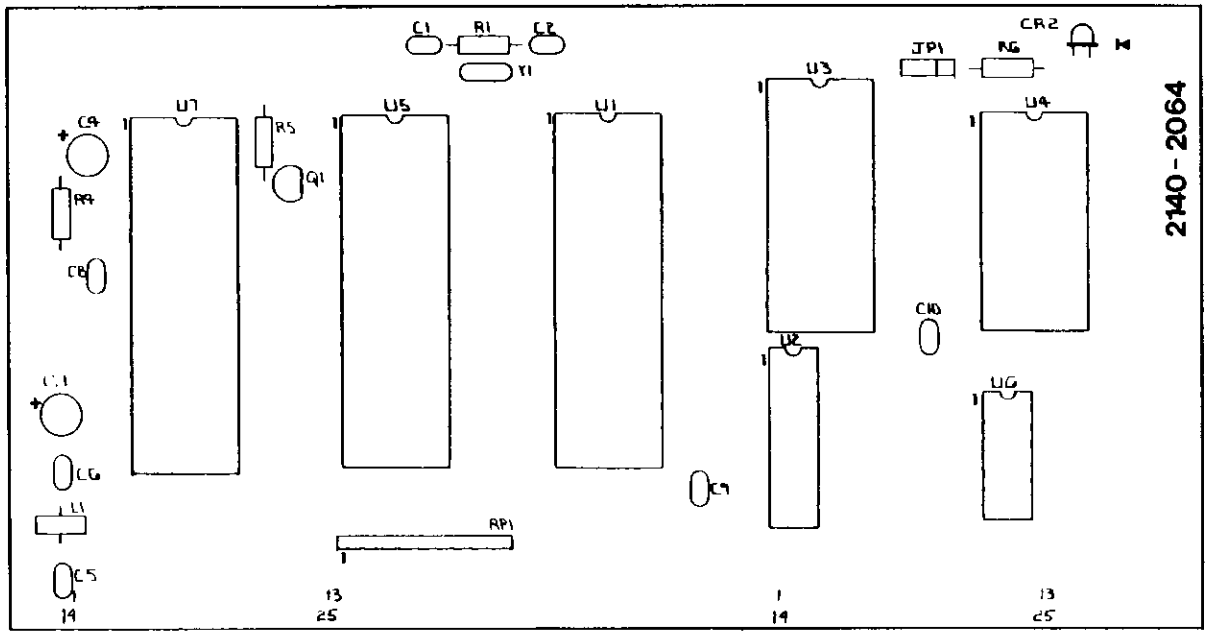
SCALE 2:1	APPROVED BY RJW 10-30-85 EE	DRAWN BY R. ROE
DATE 10-29-85		REVISED

AC LINE FILTER BOARD

N/A	QTY	MODEL	REV	DRAWING NUMBER
—	—	—		2140-2063

BRUNING 40-10

REVISION			
LTR	DESCRIPTION	APPD	DATE



1. COMPONENTS LISTED ARE TO BE BONDED TO CIRCUIT BOARD AFTER TEST USING PROCESS SPEC 0900-1004. C1, C11, Y1 (REF SHEET 2)
3. REFERENCE SCHEMATIC NO 2900-2960
4. REFERENCE CIRCUIT BOARD NO 2140-2064.
5. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10% (SEE SHEET 2)
2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10% (SEE SHEET 2)
1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT (SEE SHEET 2)

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS

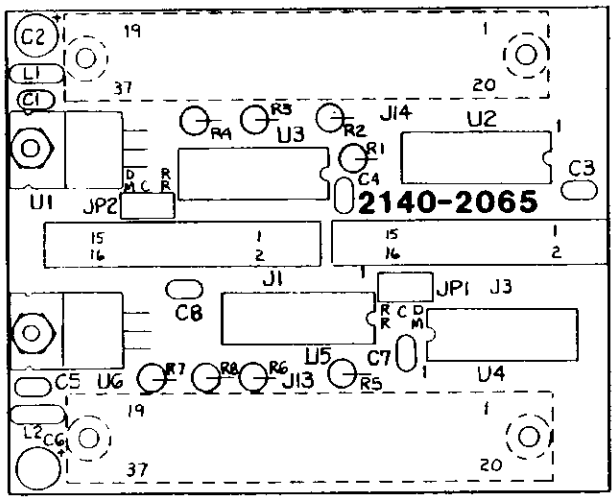
305 Airport Rd Oceanside CA 92054

SCALE 2/1	APPROVED BY	DRAWN BY TM
DATE 11-21-85	DATE	REVISED

SERIAL INTERFACE BOARD

SIZE	CAGE	MODEL	REV	DRAWING NUMBER
A		15-301510		2900-2064

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
–	ECN# 2140-214: CHANGED STANDOFFS TO UNDER SIDE OF BOARD. RWB 2-12-86		



SHEET 1 OF 2

1. COMPONENTS LISTED ARE TO BE BONDED TO CIRCUIT BD. AFTER TEST USING PROCESS SPECIFICATION 0900-1004: C2, C6, L1, L2. (REF. SHEET 2)
5. INDUCTANCE VALUES ARE IN MICROHENRIES (REF SHEET 2)
4. CAPACITANCE VALUES ARE IN MICROFARADS. (REF SHEET 2)
3. RESISTANCE VALUES ARE IN OHMS, ¼W, 5% (REF SHEET 2)
2. REF SCHEMATIC NO 2140-2465
1. REF CKT BD NO. 2140 2065

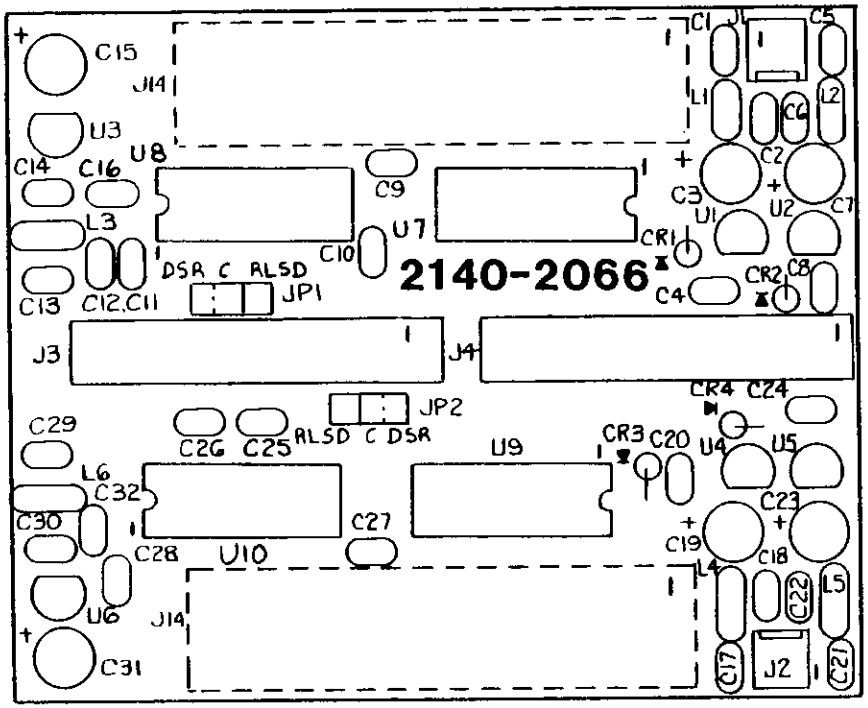
NOTES: UNLESS OTHERWISE SPECIFIED

CUBIC COMMUNICATIONS
305 Airport Rd. Oceanside CA 92054

SCALE 2:1	APPROVED BY K RUE 12-2-85	DRAWN BY	KC
DATE 12-2 85		REVISED	

RS-422-A CONNECTOR BD ASSY

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-	1	R 3030 SERIES	–	2140-2065



SHEET 1 OF 2

7. COMPONENTS LISTED ARE TO BE BONDED USING PROCESS SPECIFICATION 0900-1004 : L1-6, C3,7,15,19,23,31.
6. J13 & J14 INSTALLED ON RS-232-C CONN PLATE ASSY 2140-1153.
5. REF SCHEMATIC NO. 2140-2466.
4. REF CIRCUIT BD NO 2140-2066
3. INDUCTOR VALUES ARE IN MICROHENRIES (μH), 10%
2. CAPACITOR VALUES ARE IN MICROFARADS (μF), 10%
1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT.
NOTES: UNLESS OTHERWISE SPECIFIED

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305 Airport Rd Oceanside CA 92054

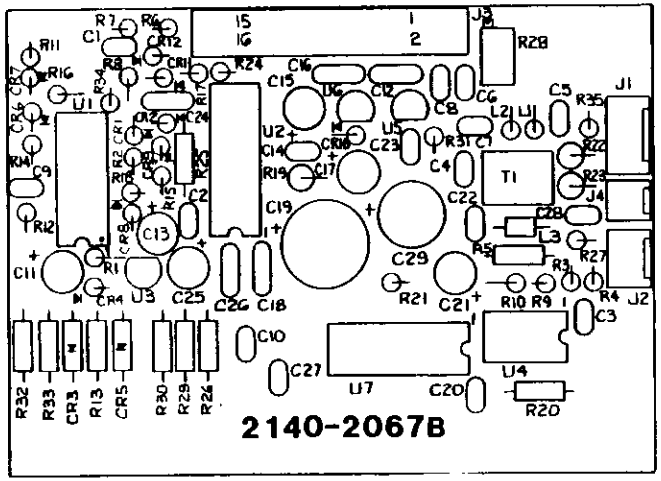
SCALE 2:1	APPROVED BY 12-12-85	DRAWN BY KC
DATE 12-9-85		REVISED

RS-232-C CONNECTOR BOARD ASSY

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-1153		R-3030		2140-2066

BRUNING 4C-10

REVISIONS			
LTR	DESCRIPTION	DATE	APP'D
A	ECN#2140-203: EXCHANGED R18 & CR8 RWB 1-22-86	1-22-86	
B	ECN# 2140-218: ROTATED U3 180°. RWB 2-19-86 ECN# 2140-221: REVISED C22 .0047μF TO 0.1μF. RWB 2-20-86	2-20-86 CD	



SHEET 1 OF 2

1. COMPONENTS LISTED ARE TO BE BONDED TO CKT BD AFTER TEST USING PROCESS SPECIFICATION 0900-1004, L3, C11, 13, 15, 17, 19, 21, 25, 29.
5. REF SCHEMATIC NO. 2140-2467
4. REF CIRCUIT BD NO. 2140-2167
3. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10%
2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10%
1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT.

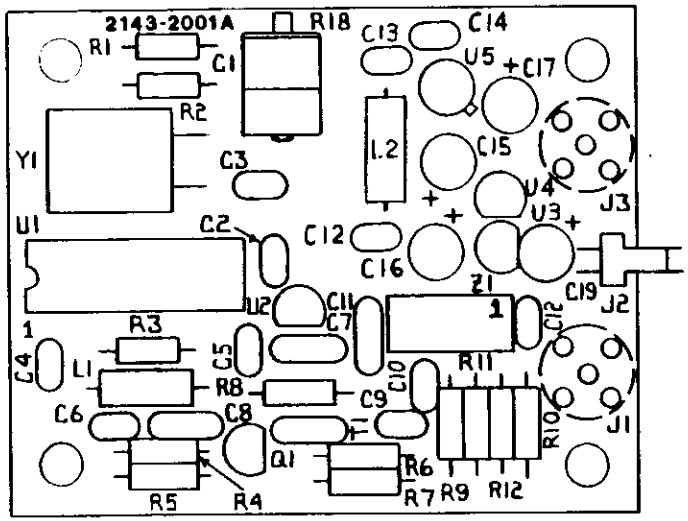
CUBIC COMMUNICATIONS
305 Airport Rd. Oceanside CA 92054

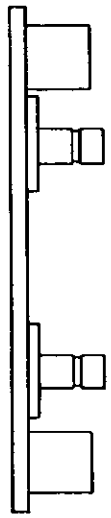
SCALE 2:1	APPROVED BY (12-7-85)	DRAWN BY KC
DATE 12-3-85		REVISED

AUDIO BOARD

N/A	QTY	MODEL	REV	DRAWING NUMBER
2145-1102		R-3030A	B	2140-2067

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	ECN # 2140-151 : COMPLETELY REVISED. R.ROE 6-18-85	6/19/85	JS2





7. C12, C13, Y1, L2 VALUES DETERMINED BY OUTPUT FREQUENCY. SEE SCHEMATIC 2143-2401.
6. INDUCTANCE VALUES IN MICROHENRIES
5. CAPACITANCE VALUES IN MICROFARADS.
4. RESISTANCE VALUES IN OHMS 1/4 W, 5%.
3. REF: SCHEMATIC NO. 2143-2401.
2. REF: CKT BD NO. 2143-2101.
1. SCREEN COMPONENT SIDE USING 2143-2001.

NOTES: UNLESS OTHERWISE SPECIFIED

SHEET 1 OF 2

CUBIC COMMUNICATIONS
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SCALE 2:1	APPROVED BY	DRAWN BY E.ROBLES
DATE 4-23-85		REVISED

OUTPUT CONVERTER BD. ASSEMBLY

N/A	QTY	MODEL	REV	DRAWING NUMBER
2143-1109	1/2		A	2143-2001

BRUNING 40-10

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED		
B	REVISED & UPDATED E.D.R. 9-2-84		
C	ECN # 2140-25. DELETED C76, C78, C80 & C82 ALL .01 CAPS REVERSED POSITION OF C66 & C72. E.D.R 1-29-85		
D	ECN # 2140-283. REVISED Q5 CP-640 W/S CAPACITOR RWB 8-13-86		

P1
LOCATED ON
2140-1101 MODULE

OUTSIDE VIEW

ANT RF
0-30MHz

L1 3.9mH, L2 160, R1 220

CR1–CR18 UM9401

BAND J: 20.5-30 MHz
BAND I: 14.3-20.49 MHz
BAND H: 9.9-14.24 MHz
BAND G: 6.9-9.85 MHz
BAND F: 4.8-6.89 MHz
BAND E: 3.3-4.75 MHz
BAND D: 2.3-3.29 MHz
BAND C: 1.6-2.29 MHz
BAND B: .5-1.599 MHz
BAND A: 0-0.499 MHz

R47–R52 10K; R53 10K; R54 10K

K1 12V; K2 12V; K3 12V; K4 12V; K5 12V; K6 12V; K7 12V

CR11 1N4005; CR12 1N914B; CR21 1N4005; CR22 1N814B

Q1 2N2222A; Q2 2N2222A; Q3 VN10KM; Q4 VN10KM; Q5 CP640; Q6 2N2222A

T1 6T:12T; T2 15T:15T

R46 2.7K; R55 15; R56 180; R57 47

C65 0.1; C66 0.1; C67 10 20V; C72 0.1; C73 0.1; C91 0.1

L35 160; L36 160µH; L37 0.82

C69 10 35V; C70 1.0

U1 78L05A

C74 0.1; C92 10 20V

U2 UDN2981A

U3 4028B

L38 33; L39 33; L40 33; L41 33

C75 0.1; C77 0.1; C79 0.1; C81 0.1

C93 10 20V; C54 68 15V; C55 1.0; C56 1.0; C63 1.0; C64 1.0

R19 10K 1W; R20 2.2K; R21 10K; R22 10K; R23 820; R24 47; R25 820; R26 820; R27 47; R28 820; R29 820; R30 47; R31 820; R32 47; R33 820; R34 47; R35 820; R36 47; R37 820; R38 47; R39 820; R40 47; R41 47; R42 390; R43 100; R44 390; R45 47

C1 200pF; C2 200pF; C3 200pF; C4 200pF; C5 0.1; C6 0.1; C7 270pF; C8 270pF; C9 270pF; C10 270pF; C11 0.1; C12 .01; C13 430pF; C14 430pF; C15 430pF; C16 430pF; C17 0.1; C18 .01; C19 620pF; C20 620pF; C21 620pF; C22 620pF; C23 0.1; C24 .01; C25 .0033; C26 0.1; C27 820pF; C28 820pF; C29 820pF; C30 820pF; C31 0.1; C32 .01; C33 1200pF; C34 1200pF; C35 1200pF; C36 1200pF; C37 0.1; C38 .01; C39 1800pF; C40 1800pF; C41 1800pF; C42 1800pF; C43 0.1; C44 0.1; C45 2700pF; C46 2700pF; C47 2700pF; C48 1.0; C49 1.0; C50 .0033; C51 .0047; C52 .0047; C53 .0033; C57 .01; C58 .01; C59 .0047; C60 .01; C61 .0047; C62 .01

L3 12pF 2.8 0.57; L4 0.57; L5 0.57; L6 160; L7 3.9mH; L8 5.9 0.75; L9 0.75; L10 18pF 0.75; L11 5.4 0.75; L12 0.75; L13 27pF 5.4; L14 6.5 1.0; L15 1.0; L16 36pF 1.0; L17 12 1.9; L18 1.9; L19 50pF 1.9; L20 17 2.8; L21 2.8; L22 75pF 2.8; L23 21 5.4; L24 5.4; L25 150pF 5.4; L26 30 5.4; L27 5.4; L28 200pF 5.4; L29 .56; L30 .56; L31 .56; L32 18; L33 18; L34 18

P2
OUTSIDE VIEW

LOCATED ON
2140-1101
MODULE

5 INDUCTANCE VALUES IN MICROHENRIES.
4 CAPACITANCE VALUES IN MICROFARADS.
3 □ REFERS TO COAX CONN PIN NO.
2. REF: ASSY DWG 2140-2001.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED
C25	CR24 E1
C68	R57 Q7
C74	C94 U4
C78	L41
C80	K7
C82	

CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE: ~ | APPROVED BY | DRAWN BY C. BRINER
DATE 12-4-84 | REVISED

PRESELECTOR MODULE SCHEMATIC

N/A	QTY	MODEL R-3020/R-2307/U	REV D	DRAWING NUMBER 2140-2401

REVISION		
LTR	DESCRIPTION	DATE APPD
F	REVISED & UPDATED E.D.R 5-12-84	
G	ECN#2140-2 R33 WAS 10K R34 WAS 10K R35 WAS 3.3K	
H	ECN#2140-50 C41 100PF R81 100 R8 100 WAS 1.2K R9 2.2K R22 6.2K	
J	ECN #2140-54 R64 100 E.D.R	
K	ECN #2140-[illegible]	
—	ECN#2140-288	
L	ECN#2140-283 R64 680 WAS 100	

1ST I.F. AGC

PRE RF

FIRST I.F MON 40.455 MHZ

2ND I.F. 455 KHZ

GROUND

+16V

2ND L.O. 0 dBm 40.000 MHZ

0 dBm 1ST L.O. 40.455-70.455 MHZ

FAULT

P1 OUTSIDE VIEW

LOCATED ON 2140-1102 MODULE

P2

LOCATED ON 2140-1102 MODULE

OUTSIDE VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
2. REF ASSEMBLY DRAWING 2140-2002
3. ☐ REFERS TO COAX CONN PIN NUMBER
4. CAPACITANCE VALUES IN MICROFARADS.
5. INDUCTANCE VALUES IN MICROHENRIES.

REFERENCE DESIGNATORS NOT USED

R33, C3, L20, R34, R35, L21, T1, J11

REFERENCE DESIGNATORS LAST USED

Z2	U3	Q18
L27	T8	
CR10	RB2	
FL1	C83	

CUBIC COMMUNICATIONS

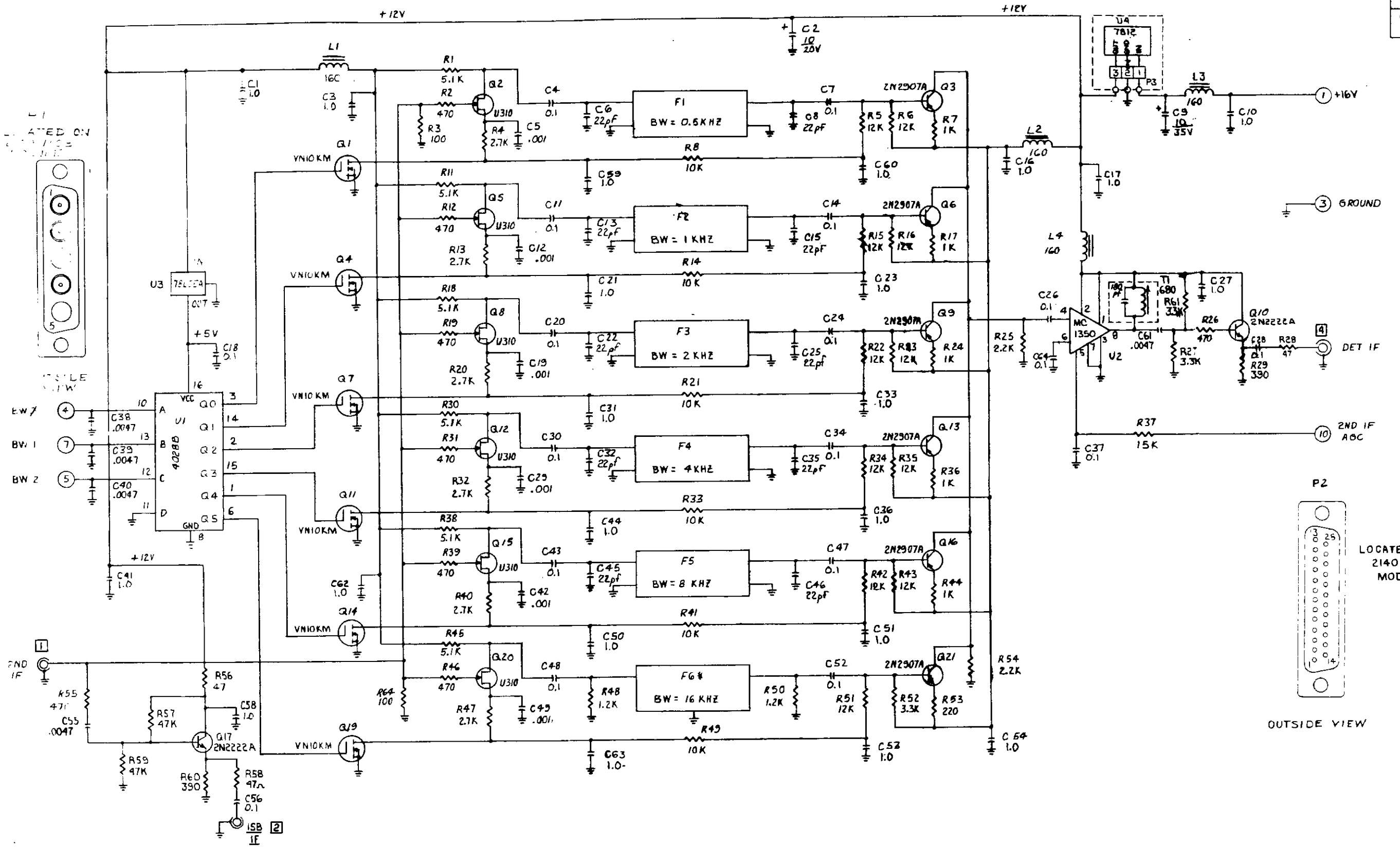
305 Airport Rd Oceanside CA 92054

SCALE ~ | APPROVED BY JEZ | DRAWN BY E.BAKER | DATE 12-4-84 | REVISED E.D.R

1 ST IF MODULE SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-2002		R-3020/R-2307/U	L	2140-2402

REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED & UPDATED		
B	REVISED & UPDATED E.D.R. 9-10-84	9/11/84	EER
C	ECN # 2140-85 ADDED C17 1.0uF E.D.R. 3-7-85	3/7/85	EER



* THIS FILTER IS OPTIONAL.

[ ] REFERS TO COAX CONN PIN NUMBER.

3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED
R62, R10, R9	C64 U3
C57, C1,	L4 P3
Q18	F6
	Q21
	R64

CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE ~	APPROVED BY EER	DRAWN BY E.BRINER
DATE 12-5-84	REV 9-27--	REVISED E.D.R.

2ND I.F. MODULE SCHEMATIC

N/A	QTY	MODEL R-3020/R-2307/U1	REV C	DRAWING NUMBER 2140-2

FM DETECTOR

REVISION			
LTR	DESCRIPTION	DATE	APP
A	REVISED & UPDATED		
B	REVISED & UPDATED		
C	REVISED & UPDATED 8-24-84		
D	REVISED & UPDATED E.O.R. 9-11-84	9/11/84	
E	ECN # 2140-4, RECORD CHANGE 2: WAS U13 R ROE 2-27-85		
F	ECN # 2140-27, CHANGED CR10,21,22,23 & 24 TO 1N4005 SYM ON ASSY DWG SHT# 1&2 OR ASSY DWG AFFECTED. A/6 2-4-85	3/1/85	
G	ECN # 2140-55: CHANGED R84, WAS 180K. R ROE 2-19-85	4/1/85	
H	ECN # 2140-66: CHANGED R62, WAS 8.66K, 1% TO 8.45K, 1%; R95 WAS 3.32K, 1% TO 3.57K, 1%; R100, WAS 82.5K, 1% TO 78.7K, 1%; R102 WAS 4.7K TO 2.2K		

L	ECN # 2140-183A, R117, 22K WAS 27K; R118, 10K POT. WAS 10K KE6156A. R ROE 11-5-83	11-7-83	
M	ECN # 2140-211, R70, 3.0 WAS 3.6K; R71, 33Ω WAS 47Ω; R89, 470Ω Ω WAS 220Ω; ADD R96, 1K, ADD CR12 IN914B.	9/1/84	
J	ECN # 2140-80, R62 8.66K WAS 8.25K; R83 22K WAS 27K; R97, 7.87K WAS 7.5K; C4-34, WAS 39 WAS 47K, 2.2K. A/6 8-4-85	9/1/85	
K	ECN # 2140-86, REVISED 8/M 2TEM #3268. ASSY DWG. E.O.R. 3-8-85	9/1/85	

2140-1109

2140-1104

P1 OUTSIDE VIEW

LOCATED ON 2140-1104 MODULE

P2 OUTSIDE VIEW

LOCATED ON 2140-1104 MODULE

4 ☐ REFERS TO COAXIAL CONNECTOR PART NUMBER.

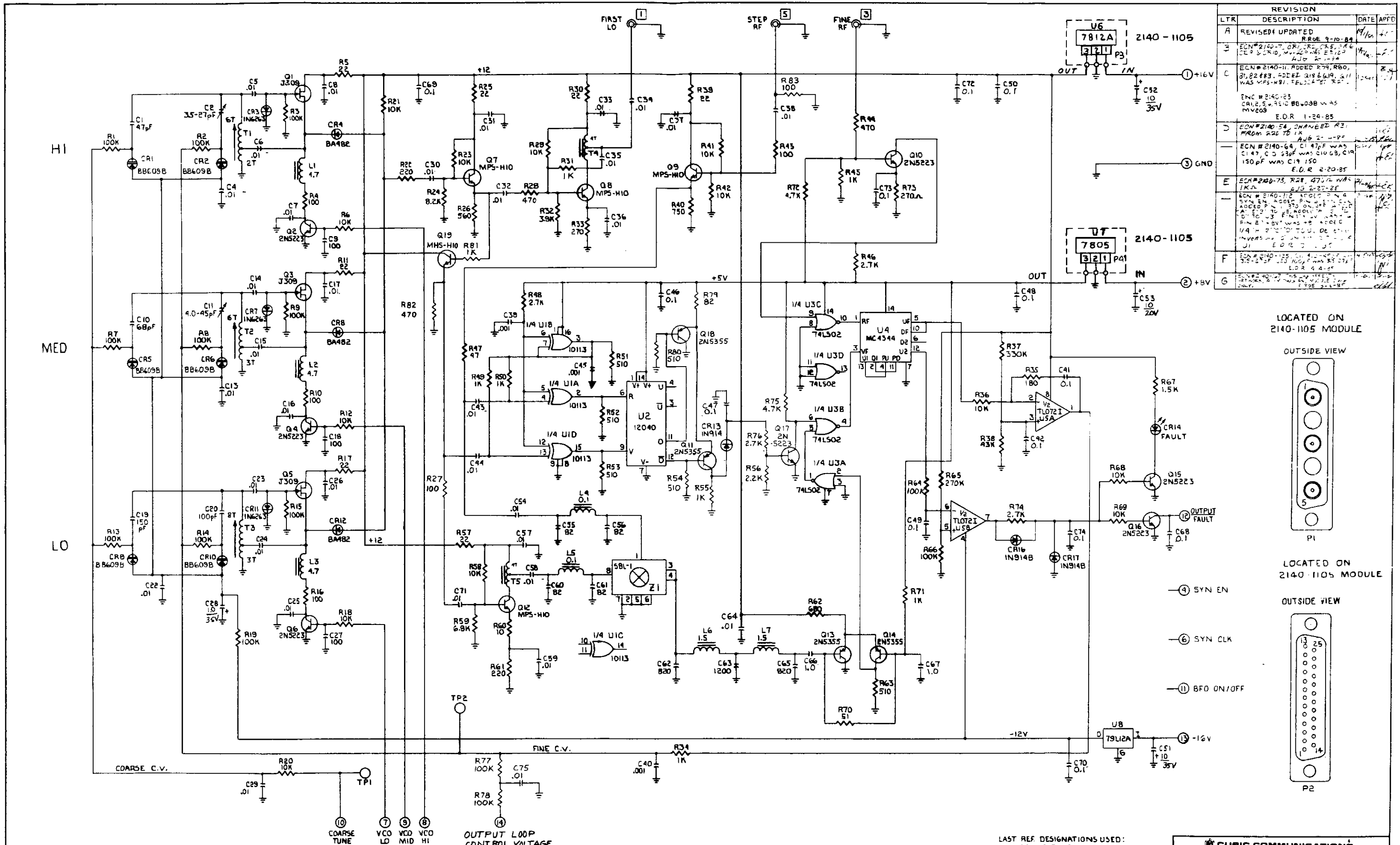
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

* DETECTOR SELECT
00 = AM W/AV. AGC
01 = AM W/PK AGC
10 = FM
11 = SSB

CUBIC COMMUNICATIONS
305 Airport Rd. Oceanside CA 92054

REFERENCE DESIGNATORS LAST USED	SCALE NONE	APPROVED BY	DRAWN BY K. R.
C93, CR24, L9, Q18, R130, T4, U15	DATE 9-11-84		REVISED E.O.R.
REFERENCE DESIGNATORS NOT USED	DETECTOR MODULE SCHEMATIC		
C80, R116, C77, R108, C82, R101, R121, R120, CR13, CR14	N/A	QTY	MODEL R-3020/30
	SIZE	DRAWING NUMBER	



REVISION			
LTR	DESCRIPTION	DATE	APPD
A	REVISED/ UPDATED R.ROE 9-10-84		
B	ECN # 2140-71, ORIG. REL. CR5, 6, 16, 17 & U6, U7 WAS MV2209, MV2209 WAS EE1/2 A.J.O 2-1-85		
C	ECN # 2140-11, ADDED R79, R80, R81, R82 & R83, ADDED Q18 & Q19, Q11 WAS MPS-H81, RELOCATED REF. ENC # 2140-63 CR12, 5 & 9 WAS BB609B WAS MV2209 E.O.R 1-28-85		
D	ECN # 2140-54, CHANGED R21 FROM 220 TO 1K A.J.O 2-27-85		
—	ECN # 2140-64, C1 47pF WAS C147, C3 68pF WAS C10 68, C19 150pF WAS C19 150 E.O.R 2-20-85		
E	ECN # 2140-73, R28, 470Ω WAS 1KΩ A.J.O 2-27-85		
—	ECN # 2140-112, ADDED R79 WAS R79 & R80, ADDED R80, CHANGED R79 TO 82Ω, ADDED R81, CHANGED R82 TO 470Ω, CHANGED C46 TO 0.1 CHANGED C47 TO 0.1, CHANGED C48 TO 0.1, CHANGED C49 TO 0.1, CHANGED C50 TO 0.1, CHANGED C51 TO 10/35V, CHANGED C52 TO 10/35V, CHANGED C53 TO 10/20V E.O.R 3-27-85		
F	ECN # 2140-125 C41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53 WAS 33pF NPO WAS 27pF E.O.R 4-4-85		
G	ECN # 2140-137 THIS ECN REFERS TO ARTWORK A.D.V WAS ECN 2140-112 E.O.R 5-1-85		

LAST REF. DESIGNATIONS USED:
R83, C75, CR17, Q19, U8, L7, Z1, T5

DESIGNATORS NOT USED:
C3, C12, C61, CR15, C44

4 ☐ REFERS TO COAX CONN PIN NUMBER
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

CUSIC COMMUNICATIONS
305 Airport Rd. Oceanside, CA 92054

SCALE: NONE	APPROVED BY		DRAWN BY: E.ROELOFS
DATE: 12-5-84			REVISED: 9-10-84

OUTPUT LOOP MODULE SCHEMATIC

	QTY	MODEL	REV	DRAWING NUMBER
N/A		5-7220/30/40	G	E-40-2405

LTR	REVISION	DATE	APPD
D	ECN # 2140-131, C1 82pF WAS 47pF C10 100pF WAS 68pF, C19 180pF WAS 150pF, T1 5T WAS 6T E.D.R. 4-8-85	4-8-85	

LTR	REVISION	DATE	APPD
A	REVISED & UPDATED R. ROE 9-10-84		
B	ECN # 2140-8, CR1, CR2, CR5, CR6, CR9 & CR10, MV209 WAS BB109 AUG 12-11-24		
C	ECN # 2140-23 CR1,2,5,6,9 & 10 BB609B WAS MV209 E.D.R. 1-24-85		
—	ECN # 2140-64, C1 47pF WAS C1 47, C10 68pF WAS C10 68, C19 150pF WAS C19 150 E.D.R. 2-20-85		

HI
58.6-70.4 MHZ

MED
48.7-58.5 MHZ

LOW
40.4-48.6 MHZ

STEP REF

STEP RF

LOCATED ON
2140-1106 MODULE
OUTSIDE VIEW

P2

OUTSIDE VIEW

P1

LOCATED ON
2140-1106 MODULE

LAST REF DESIGNATIONS USED:
R33, C58, Q10, CR20, U10, T4, L3

NOTES: UNLESS OTHERWISE SPECIFIED.
1. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
3. RESISTANCE VALUES IN OHMS 1/4W, 5%.
4. [ ] REFERS TO COAX CONN PIN NUMBER.

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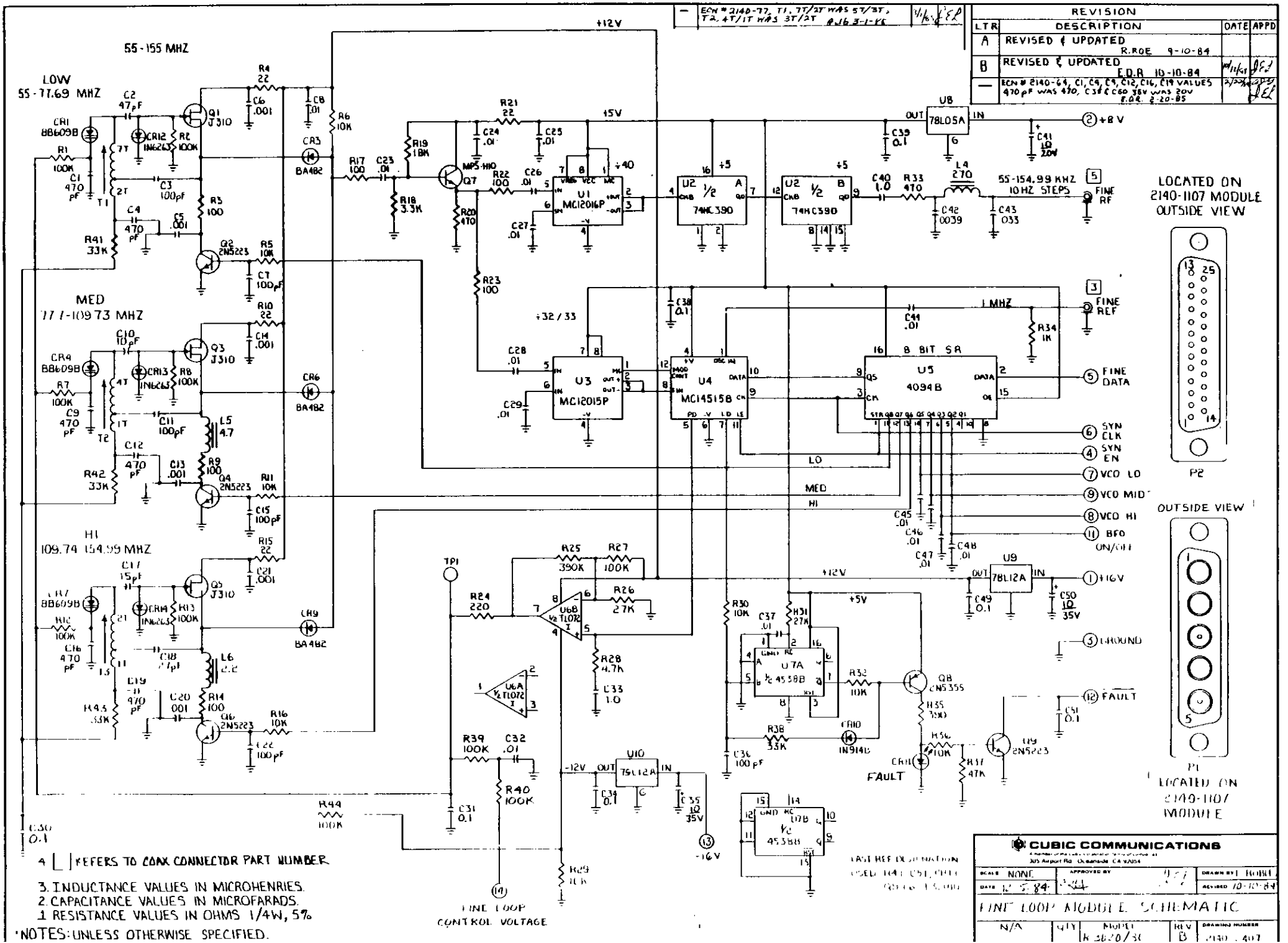
305 Airport Rd Oceanside CA 92054

SCALE: NONE	APPROVED BY	DRAWN BY: E. ROBLES
DATE: 12-5-84		REVISED 9-10-84

STEP LOOP MODULE SCHEMATIC

	QTY	MODEL	REV	DRAWING NUMBER
N/A		R-3020/30/40	C	2140-2406


REVISION
LTR DESCRIPTION DATE APPD
A REVISED & UPDATED R.ROE 9-10-84
B REVISED & UPDATED E.D.A 10-10-84
— ECN # 2140-64, C1, C9, C9, C12, C16, C19 VALUES 470 pF WAS 470, C38 & C50 35V WAS 20V E.D.A. 2-20-85
55 - 155 MHZ
LOW 55 - 77.69 MHZ
MED 77.1 - 109.73 MHZ
HI 109.74 154.99 MHZ
+12V
+15V
+5V
-12V
-16V
+8 V
+16V
+40
+32 / 33
1 MHZ
8 BIT SR
LO
MED
HI
FAULT
55 - 154.99 KHZ 10 HZ STEPS
FINE RF
FINE REF
FINE DATA
SYN CLK
SYN EN
VCO LO
VCO MID
VCO HI
BFO ON/OFF
GROUND
FAULT
FINE LOOP CONTROL VOLTAGE
LOCATED ON 2140-1107 MODULE OUTSIDE VIEW
P2
P1
OUTSIDE VIEW
LOCATED ON 2140-1107 MODULE
4 REFERS TO COAX CONNECTOR PART NUMBER
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1 RESISTANCE VALUES IN OHMS 1/4W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED.
CUBIC COMMUNICATIONS
FINE LOOP MODULE SCHEMATIC
SCALE NONE
DRAWN BY ROBLE
DATE 12-5-84
REVISED 10-10-84
N/A
MODEL 2620/30
REV B
DRAWING NUMBER 2130 - 407

LTR	DESCRIPTION REVISION	DATE	APPD
A	REVISED & UPDATED R. ROE 4-10-84	4/10/84	
B	ECN # 2140-49, REF DESIGNATIONS R37 WAS R35, R36 WAS R37 E.O.R 2-7-85		
—	ECN # 2140-110, ADDED PIN 3 AND GND SYMBOL, ADDED PIN 13 AND -16V, CONNECTED TRACE FROM P.N. 13 TO PIN 12 U4B (GND). STEP REF WAS REF OUT. E.O.R. 3-22-85		

BFO REF — 1 MHZ

500 KHZ LO

+16V

+8V

+5V

STEP REF

P2 — OUTSIDE VIEW — LOCATED ON 2140-1109 MODULE

P1 — OUTSIDE VIEW — LOCATED ON 2140-1109 MODULE

U1A ½ 4013B — U1B ½ 4013B — U2 MC12017P — U3 MC145158 — U4A ½ 4538B — U4B ½ 4538B — U5 SP8630B — U6A ½ 74HC390 — U6B ½ 74HC390 — U7 78L08 — U8 78L05

Q1 J309 — Q2 MPSH10 — Q3 2N5223 — Q4 2N5223 — Q5 2N5223 — Q6 2N5355 — Q7 2N5223

CR1 MV2107 — CR2 IN6263 — CR4 FAULT

T1 — 4T C7, 1T .01 — T2 — R16 R, R19 680

L1 10 — L2 82 — L3 82 — L4 82

÷64/65 — ÷10 — ÷10 — ÷10

44.5-46.5 MHZ 014-058

SYN EN — BFO DATA — SYN CLK — MAIN BFO — BFO ON/OFF — AUX BFO — FAULT

BFO CONTROL VOLTAGE

TP1

NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
2. CAPACITANCE VALUES IN MICROFARADS.
3. INDUCTANCE VALUES IN MICROHENRIES.
[ ] = PARTS TO COAX CONNECTOR PART NUMBER.

REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED		
CR3	T2	CR4	P2
	R37	Q7	L4
	C41	P52	CR4
	TP1	U6	

CUBIC COMMUNICATIONS
309 Airport Rd Oceanside CA 92054

SCALE	APPROVED BY	DRAWN BY
DATE 12-5-84	LEK	REVISED 9-6-89

BFO MODULE SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
		R-3020/30	E	2140-2403

LTR	DESCRIPTION	DATE	APP'D
-	ECN #2140-147, ON U11 - 5.0 LM2931AT-5.0 TO LM 2931AT-5.0	ALG 5-31-95	

U5 NSC-800

U9 74HC573

U4 27C64/27128

U6 8155

U8 ADC0804

U7 DAC0832

U2 CA 3130

U1 CA 3140

U14 79L05

U3 74HC138

U10 ½ 258

U12 78L12A

U13 79L12A

U11 LM2931AT-5.0

P1

P2

OUTSIDE VIEW

OUTSIDE VIEW LOCATED ON 2140-1110 MODULE

LOCATED ON 2140-1110 MODULE P1

	POWER SUPPLY CONNECTION PINS				
	I.C.	+5	GND	+12	-12
U5	NSC 800	40	20		
U9	74HC573	20	10		
U3	74HC138	16	8		
U4	PRGM MeM	28	14		
U6	8155	40	20		
U2	3130		4	7	
U8	ADC0804	20	10		
U7	DAC0832		10	20	
U1	314-0			7	4
U10	258	8	4		

REFERENCE DESIGNATORS	
LAST USED	NOT USED
R18 U14 C20 P2 Q1 CR1 Y1	R1,2,3,4,

NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
2. CAPACITANCE VALUES IN MICROFARADS.
3. INDUCTANCE VALUES IN MICROHENRIES.

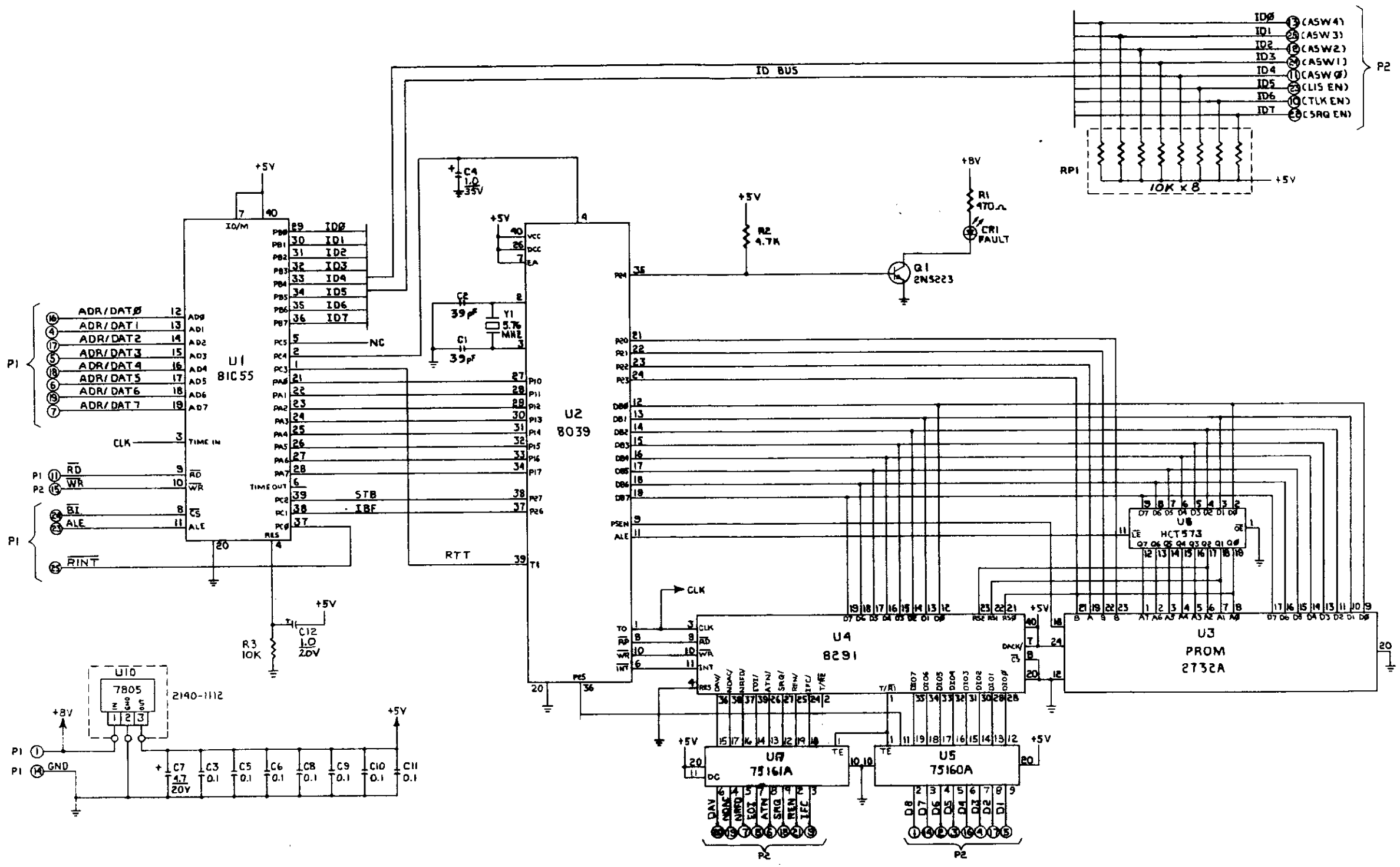
CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE	APPROVED BY	DRAWN BY BRINER
DATE 12-5-84		REVISED E.C.R

CPU MODULE SCHEMATIC

N/A	QTY	MODEL R-3020/30	REV	DRAWING NUMBER 2140-2410

REVISION			
LTR	DESCRIPTION	DATE	APPD
—	ECN # 2 ADD 3 JUMPERS PIN 2 TO +5V PIN 3 TO U1 PIN 7 C2 WAS VCC +5V IS NOW RELOCATED TO PIN 40 OF U1 PIN 40 OF U1 IS NOW +5V ONLY AS R1 = 3V GND FROM TOP RIGHT OF SCREW MOVED NEARBY TO TRACE OF TCLK CHANGED TO TOP OF TBOS AND REORDERED TO SEQUENTIAL NUMBERING E.D.R. 3-30-85	3 MAR 85	
A	ECN # 3 ADD 33Ω RESISTOR IN SERIES WITH LINES 5 THROUGH 8 OF P1 TO REDUCE OVERSHOOT & RINGING ON THESE LINES. ALSO ADD 1 JUMPER FROM PIN 1 OF U1 TO PIN 2 OF U1 AND ONE JUMPER FROM PIN 1 OF U2 TO PIN 2 OF U2 E.D.R. 4-29-85	29 APR 85	



3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

REF. DESIGNATOR LAST USED:
R3, Q1, C12, CR1, U10, Y1

CUBIC COMMUNICATIONS				
SCALE NONE	APPROVED BY		DRAWN BY E. ROBLES	
DATE 12-5-84			REVISED	
IEEE-488 BUS MODULE SCHEMATIC				
N/A 2140-2013	QTY 1	MODEL R-3030	REV A	DRAWING NUMBER 2140-2413

REVISION		
LTR	DESCRIPTION	DATE (YR-MO-DA)
A	REVISED & UPDATED	
B	REVISED & UPDATED	
C	REVISED & UPDATED	
D	ECN#2140-23, 2140-2043, 2140-2015 J2, J3 AND ADDED J26, ROW 1 etc. RWB 4-3-85	
E	ECN#2140-46, ADDED J1 +8V, +8V, 16V ORG	

+8V

C1 33 16V

U1 ULN2803A

R1 1K Q1 TIP42 | R2 1K Q2 TIP42 | R3 1K Q3 TIP42 | R4 1K Q4 TIP42 | R5 1K Q5 TIP42 | R6 1K Q6 TIP42

R7 220 R8 220 R9 220 R10 220 R11 220 R12 220

J1

TO MOTHERBOARD 2140-2015 J25

D61	34	A2	17
D62	32	B2	15
D63	30	C2	13
D64	28	D2	11
D65	26	E2	9
D66	24	F2	7
+8V	22	G2	5
+8V	20	DP2	3
A1	18	+8RTN	1
B1	16		
C1	14		
D1	12		
E1	10		
F1	8		
G1	6		
DP1	4		
+8RTN	2		
A3	33		
B3	31		
D3	29		
C3	27		
E3	25		
F3	23		
G3	21		
DP3	19		

U2 ULN2803A — R13 68, ½W R14 68, ½W R15 68, ½W R16 68, ½W R17 68, ½W R18 68, ½W R19 68, ½W R20 68, ½W

DS1 F7 | DS2 F6 | DS3 F5 | DS4 F4 | DS5 F3 | DS6 F2 — MAN 3420A

U3 ULN2803A — RZ1 68, ½W RZ2 68, ½W RZ3 68, ½W R24 68, ½W RZ5 68, ½W R26 68, ½W R27 68, ½W R28 68, ½W

DS7 F1 | DS8 M | DS9 BW10 | DS10 BW1 | DS11 AGC10 | DS12 AGC1 — MAN 3420A

U4 ULN2803A — R29 68, ½W R30 68, ½W R31 68, ½W R32 68, ½W R33 68, ½W R34 68, ½W R35 68, ½W R36 68, ½W

DS13 CH10 | DS14 CH1 — MAN 3420A

CR1 MV54164

CR2 MV54164

MV57173X6

CR3 (AUDIO)
CR4 (FREQ)
CR5 (REM)
CR6 (FAULT)
CR7 (KPAD)
CR8 (SKIP)

J2 J3

1	COL 1	1
2	COL 2	2
3	ROW 1	3
4	ROW 4	4
5	COL 3	5
6	ROW 3	6
7	ROW 2	7
8	COL 4	8
9	COL 5	9
10		

TO MOTHER BD 2140-2043 J26

TO KEYPAD

3. INDUCTANCE VALUES IN MICROHENRIES
2. CAPACITANCE VALUES IN MICROFARADS
. RESISTANCE VALUES IN OHMS, ¼W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATORS LAST USED	
J3	Q6
U4	R36
DS14	
CR8	

CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

SCALE ~ | APPROVED BY | DRAWN BY E.RAINEY | DATE 10-6-84 | REVISED

DISPLAY BOARD SCHEMATIC

N/A		MODEL	LTR	DRAWING NUMBER
2140-2016		R-3030	E	2140-416

LTR	DESCRIPTION	DATE	APPD
—	ECN #2140-155, ADDED PIN 20(P2), +5V, CONNECT TO PIN 3, U16. REMOVED C1 4.7uF FROM OUT-PUT U16. ADDED C1 .1uF TO INPUT U16. ADDED PIN 14(VCC) AND PIN 7 (GND) TO U7, U13 & U14. R.ROE 6-17-85	6/17/85	

LTR	DESCRIPTION	DATE	APPD
—	ECN #2140-119, ADDED LABEL 'G' TO PIN 9 TO U1. ADDED 'OSC' TO PIN 8 & 'MB' TO PIN 7 ON U6. PIN 15 WAS 'PIN 11' ON U1. PIN 2 ROW 3 WAS 'ROW 1' PIN 9 'ROW 1' WAS 'ROW 3' ON U6. ADDED A '78' TO 'D' TO U12, U13. DELETED 'FRONT PANEL' LOCAL REMOTE AND SWITCH PICTURE. P2 PIN 18 'LOCAL' WAS 'LOCAL SWITCH'. ADDED 'A' & 'C' TO U14. ADDED U16 & PICTURE. ADDED 10 U2, U3, U4, U5, U8 PIN 11 'CLK' PIN 10 'OE'. PIN 10 TO GND. ADDED TRACE TO PIN 11-U8. ADDED JUNCTION DOT ON TWO LINE BETWEEN PIN 6 - P2 & PIN 6 - U1. RELOCATED PIN 13 & 14 OF U8 TO OPPOSITE SIDE OF CHIP FROM SIDE. ADDED PIN 12 'NC' TO U8. P1 - PIN 1 'SW' WAS 'SW'. ADDED 'OUT' & '5V' TO LEFT OF U16. ADDED C6, C7, RELOCATED U13A TO SURFACE OF ZONE ON U13. RELOCATED PIN 6, E3 TO BOTTOM OF U1. ADDED PIN 8 'GND' & PIN 16 'VCC' TO U1. ADDED TRACE FROM PIN 16-U1 TO PIN 20-U8. ADDED 'NC' TO PIN 23 - C8 & 'NC' TO PIN 24 - P2. PIN 14 COND. AB TO PIN 27. CABLE - 'NC' TO PIN 25 - 'NC' TO PIN 15. CABLE - 'NC' TO PIN 13 - 'NC' TO PIN 10 ON U11. ADDED OE TO PIN 6 - C11 - PIN 7 - U10 PIN 19. R1 TO PIN 4, D1 TO PIN 5, OE TO PIN 7, OE & NC'S TO PIN 12, R2 TO PIN 13, R3 TO PIN 10, OE & GND'S PIN 7 TO U15, PIN 4 WAS 'SW' & ADDED 'OUT' & 'NC'. PIN 12 & 'NC' TO U12 / PIN 11 & 'NC' & 'EN' ADDED OE TO PIN 1. ONE NO PIN 9 ON U9, 'INTR' WAS 'INTR' ON U1, PIN 20 WAS PIN 2 4-1-85	4-1-85	PM

LTR	DESCRIPTION	DATE	APPD
A	REVISED PER ECO		
-	ECN #2140-78, ADDED 'MB' TO PIN 7 OF U6 & 'MB' TO PIN 7 OF U7. ADDED 'MB' TO PIN 7 OF U8. ADDED 'MB' TO PIN 7 OF U9. ADDED 'MB' TO PIN 7 OF U10. ADDED 'MB' TO PIN 7 OF U11. ADDED 'MB' TO PIN 7 OF U12. ADDED 'MB' TO PIN 7 OF U13. ADDED 'MB' TO PIN 7 OF U14. ADDED 'MB' TO PIN 7 OF U15. ADDED 'MB' TO PIN 7 OF U16. ADDED 'MB' TO PIN 7 OF U17. ADDED 'MB' TO PIN 7 OF U18. ADDED 'MB' TO PIN 7 OF U19. ADDED 'MB' TO PIN 7 OF U20. ADDED 'MB' TO PIN 7 OF U21. ADDED 'MB' TO PIN 7 OF U22. ADDED 'MB' TO PIN 7 OF U23. ADDED 'MB' TO PIN 7 OF U24. ADDED 'MB' TO PIN 7 OF U25. ADDED 'MB' TO PIN 7 OF U26. ADDED 'MB' TO PIN 7 OF U27. ADDED 'MB' TO PIN 7 OF U28. ADDED 'MB' TO PIN 7 OF U29. ADDED 'MB' TO PIN 7 OF U30. ADDED 'MB' TO PIN 7 OF U31. ADDED 'MB' TO PIN 7 OF U32. ADDED 'MB' TO PIN 7 OF U33. ADDED 'MB' TO PIN 7 OF U34. ADDED 'MB' TO PIN 7 OF U35. ADDED 'MB' TO PIN 7 OF U36. ADDED 'MB' TO PIN 7 OF U37. ADDED 'MB' TO PIN 7 OF U38. ADDED 'MB' TO PIN 7 OF U39. ADDED 'MB' TO PIN 7 OF U40. ADDED 'MB' TO PIN 7 OF U41. ADDED 'MB' TO PIN 7 OF U42. ADDED 'MB' TO PIN 7 OF U43. ADDED 'MB' TO PIN 7 OF U44. ADDED 'MB' TO PIN 7 OF U45. ADDED 'MB' TO PIN 7 OF U46. ADDED 'MB' TO PIN 7 OF U47. ADDED 'MB' TO PIN 7 OF U48. ADDED 'MB' TO PIN 7 OF U49. ADDED 'MB' TO PIN 7 OF U50. ADDED 'MB' TO PIN 7 OF U51. ADDED 'MB' TO PIN 7 OF U52. ADDED 'MB' TO PIN 7 OF U53. ADDED 'MB' TO PIN 7 OF U54. ADDED 'MB' TO PIN 7 OF U55. ADDED 'MB' TO PIN 7 OF U56. ADDED 'MB' TO PIN 7 OF U57. ADDED 'MB' TO PIN 7 OF U58. ADDED 'MB' TO PIN 7 OF U59. ADDED 'MB' TO PIN 7 OF U60. ADDED 'MB' TO PIN 7 OF U61. ADDED 'MB' TO PIN 7 OF U62. ADDED 'MB' TO PIN 7 OF U63. ADDED 'MB' TO PIN 7 OF U64. ADDED 'MB' TO PIN 7 OF U65. ADDED 'MB' TO PIN 7 OF U66. ADDED 'MB' TO PIN 7 OF U67. ADDED 'MB' TO PIN 7 OF U68. ADDED 'MB' TO PIN 7 OF U69. ADDED 'MB' TO PIN 7 OF U70. ADDED 'MB' TO PIN 7 OF U71. ADDED 'MB' TO PIN 7 OF U72. ADDED 'MB' TO PIN 7 OF U73. ADDED 'MB' TO PIN 7 OF U74. ADDED 'MB' TO PIN 7 OF U75. ADDED 'MB' TO PIN 7 OF U76. ADDED 'MB' TO PIN 7 OF U77. ADDED 'MB' TO PIN 7 OF U78. ADDED 'MB' TO PIN 7 OF U79. ADDED 'MB' TO PIN 7 OF U80. ADDED 'MB' TO PIN 7 OF U81. ADDED 'MB' TO PIN 7 OF U82. ADDED 'MB' TO PIN 7 OF U83. ADDED 'MB' TO PIN 7 OF U84. ADDED 'MB' TO PIN 7 OF U85. ADDED 'MB' TO PIN 7 OF U86. ADDED 'MB' TO PIN 7 OF U87. ADDED 'MB' TO PIN 7 OF U88. ADDED 'MB' TO PIN 7 OF U89. ADDED 'MB' TO PIN 7 OF U90. ADDED 'MB' TO PIN 7 OF U91. ADDED 'MB' TO PIN 7 OF U92. ADDED 'MB' TO PIN 7 OF U93. ADDED 'MB' TO PIN 7 OF U94. ADDED 'MB' TO PIN 7 OF U95. ADDED 'MB' TO PIN 7 OF U96. ADDED 'MB' TO PIN 7 OF U97. ADDED 'MB' TO PIN 7 OF U98. ADDED 'MB' TO PIN 7 OF U99. ADDED 'MB' TO PIN 7 OF U100.		
B	ECN #2140-89, CE [illegible] 10uF 20V E.O.R. 3-9-[illegible]		

DATA BUS

P1
ALE
WR
P2

74HC574 U2 — P1
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
1D 2D 3D 4D 5D 6D 7D 8D — 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
19 SEG A1, 18 SEG B1, 17 SEG C1, 16 SEG D1, 15 SEG E1, 14 SEG F1, 13 SEG G1, 12 SEG DP1
Vcc 20, CLK OE 11 1, 10

74HC574 U3 — P1
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
19 SEG A2, 18 SEG B2, 17 SEG C2, 16 SEG D2, 15 SEG E2, 14 SEG F2, 13 SEG G2, 12 SEG DP2
Vcc 20, CLK OE 11 1, 10

74HC574 U4 — P2
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
19 SEG A3, 18 SEG B3, 17 SEG C3, 16 SEG D3, 15 SEG E3, 14 SEG F3, 13 SEG G3, 12 SEG DP3
Vcc 20, CLK OE 11 1, 10

74HC574 U5 — P2
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
19 DG1, 18 DG2, 17 DG3, 16 DG4, 15 DG5, 14 DG6, 13 NC, 12 NC
Vcc 20, CLK OE 11 1, 10

74C923 U6 — P2
ADØ 19, AD1 18, AD2 17, AD3 16, AD4 15
A B C D E — Y1 Y2 Y3 Y4 Y5 X1 X2 X3 X4 KB
1 COL 1, 2 COL 2, 3 COL 3, 4 COL 4, 5 COL 5, 12 ROW 3, 11 ROW 2, 9 ROW 1, 8 ROW 4
DA 13, OE 14, OSC 7, 6, 10
Vcc 20
C2 33/15V, C3 0.1

74HC574 U8 — P2
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
1D 2D 3D 4D 5D 6D 7D 8D — 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
19 MET Ø, 18 MET 1, 17 INH, 16, 15, 14, 13, 12 NC
Vcc 20, CLK OE 11 1, 10
C6 0.1

74HC573 U9
ADØ 2, AD1 3, AD2 4, AD3 5, AD4 6, AD5 7, AD6 8, AD7 9
1D 2D 3D 4D 5D 6D 7D 8D — Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
19, 18, 17, 16, 15, 14, 13, 12
Vcc 20, OE 1, LE 10, 11
C5 0.1

X2816A U10
ADØ 9, AD1 10, AD2 11, AD3 13, AD4 14, AD5 15, AD6 16, AD7 17
D0 D1 D2 D3 D4 D5 D6 D7 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
8 7 6 5 4 3 2 1 23 22 19
CE 18, Vcc 24, WE 21, OE 20, 12
C4 0.1

8259A U11
ADØ 11, AD1 10, AD2 9, AD3 8, AD4 7, AD5 6, AD6 5, AD7 4
DØ D1 D2 D3 D4 D5 D6 D7 — IR7 IR6 IR5 IR4 IR1 IR0 IR2 IR3
NC 12, VCC 28, GND 14, A0 27, 25 NC, 24 NC, 23, 22, 19, 18, 20, 21, 16 NC
WR 2, RD 3, CS 1, SP/EN 15 NC, CAS2 13 NC, CAS1, INT 17, INTA 26, 19

X2210 U12
ADØ 12, AD1 13, AD2 14, AD3 15
DØ D1 D2 D3 — A5 A4 A3 A2 A1 AØ RW STB
18 NC, 17 NC, 16, 2, 3, 4, 5, 6, 10
WE 11, CE 1, NC 1

74HC138 U1
ENS 5, A8 1, A9 2, A10 3, E2 4, E1, E3 6 1
A B C — H G F E D C B A
7 15 14 13 12 11 10 9

U13A 1/4 74HC32 — 2, 1, 3
U13B 1/4 74HC32 — 4, 5, 6
U13C 1/4 74HC32 — 9, 10, 8
U13D 1/4 74HC32 — 12, 13, 11
U14A 1/6 74HC14
U14B 1/6 74HC14 — 4, 3
U14C 1/6 74HC14 — 5, 6
U14D 1/6 74HC14 — 8, 9
U14E 1/6 74HC14 — INTR 10, INTA 11
U14F 1/6 74HC14 — 13, 12
U7A 1/4 74HC30 — 2, 1, 14, 3
U7C 1/4 74HCØØ — 10, 9, 8
U7D 1/4 74HCØØ — 12, 13, 11
U78 1/4 74HCØØ — 5, 4, 6

4013 U15
D2 Vcc, C1, S1, R1, D1, S2, Q1, Q2, R2, C2
9 14, 3, 6, 4, 5, 8, 12, 1, 2, 13, 10, 11

P1
RD
EN4
ADØ
AD1
AD2
AD3
AD4
AD5
AD6
AD7
DATA BUS

P1
IO/M

P2
RINT
LOCAL

ENC PHASE B
ENC PHASE A

+5V
C7 .1
C8 .1
C9 .1
C1 4.7
R1 10K

P1 + 5V
GND

OUTSIDE VIEW P2
LOCATED ON 2140-1116 MODULE

OUTSIDE VIEW P1
LOCATED ON 2140-1116 MODULE

U16 7805 — 3 2 1 P3 — IN OUT

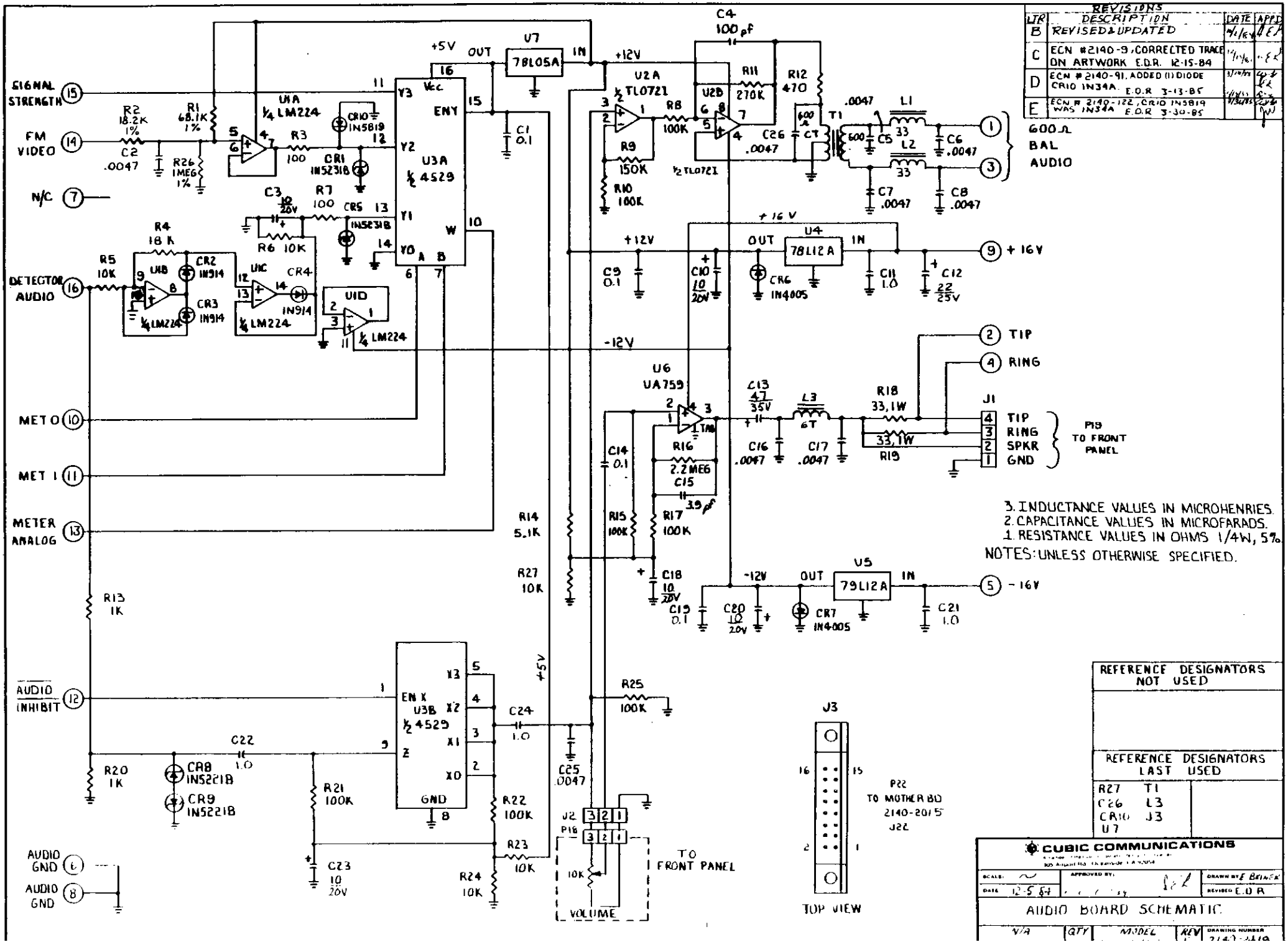
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054

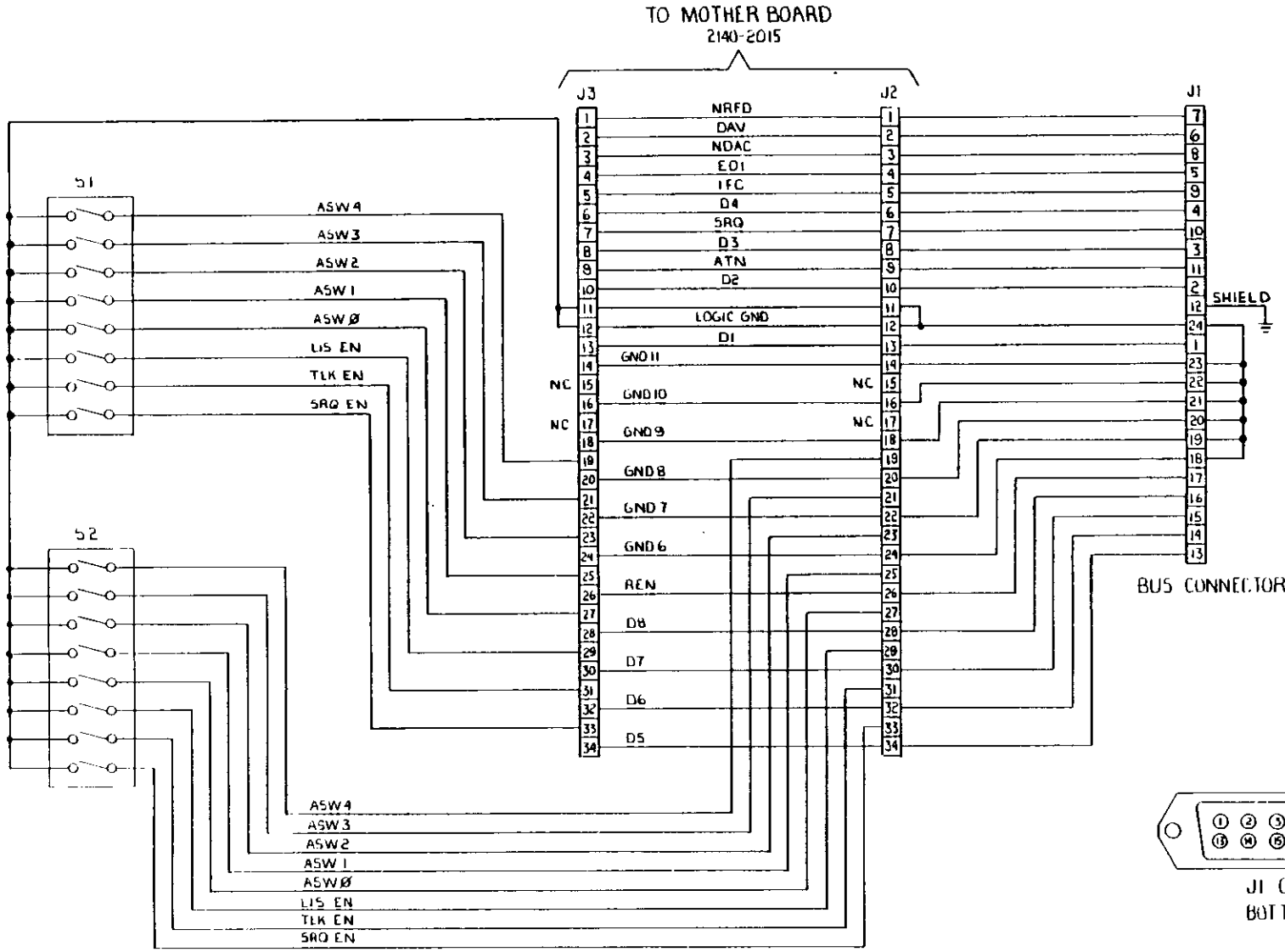
SCALE	APPROVED BY	DRAWN BY
DATE 12-5-84		REVISED

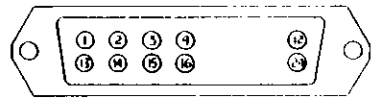
PANEL INTERFACE MODULE SCHEMATIC

N/A	QTY	MODEL R-3030/40	REV E	DRAWING NUMBER 2140-2416

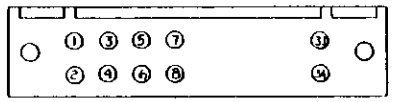

REVISIONS
LTR DESCRIPTION DATE APPD
B REVISED & UPDATED 9/16/84
C ECN #2140-9, CORRECTED TRACE ON ARTWORK E.O.R. 12-15-84 12/19/84
D ECN # 2140-91, ADDED (1) DIODE CR10 IN34A. E.O.R 3-13-85 3/19/85
E ECN # 2140-122, CR10 IN5819 WAS IN34A E.O.R 3-30-85 4/3/85
SIGNAL STRENGTH
FM VIDEO
N/C
DETECTOR AUDIO
MET 0
MET 1
METER ANALOG
AUDIO INHIBIT
AUDIO GND
AUDIO GND
+5V
+12V
-12V
+16V
-16V
U1A 1/4 LM224
U1B 1/4 LM224
U1C 1/4 LM224
U1D 1/4 LM224
U3A 1/2 4529
U3B 1/2 4529
U2A 1/2 TL0721
U2B 1/2 TL0721
U4 78L12A
U5 79L12A
U6 UA759
U7 78L05A
CR1 IN5231B
CR2 IN914
CR3 IN914
CR4 IN914
CR5 IN5231B
CR6 IN4005
CR7 IN4005
CR8 IN5221B
CR9 IN5221B
CR10 IN5819
T1
L1
L2
L3
600Ω BAL AUDIO
TIP
RING
SPKR
GND
P19 TO FRONT PANEL
J1
J2 P18
J3
P22 TO MOTHER BD 2140-2015 J22
TO FRONT PANEL
VOLUME
TOP VIEW
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED.
REFERENCE DESIGNATORS NOT USED
REFERENCE DESIGNATORS LAST USED
R27 T1
C26 L3
CR10 J3
U7
CUBIC COMMUNICATIONS
AUDIO BOARD SCHEMATIC
DRAWN BY E. BRIACK
REVISED E.O.R
DATE 12-5-84
SCALE: ~
N/A QTY MODEL REV
DRAWING NUMBER 2140-2119

REVISIONS			
LTR	DESCRIPTION	DATE	APP'D
A	ECN# 2140-170: REVISED GND WIRING TO CONNECTORS PWB 112-84	11/21/85	JEL





J1 CONNECTOR
BOTTOM VIEW



J2 & J3 CONNECTORS
BOTTOM VIEW

3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED.

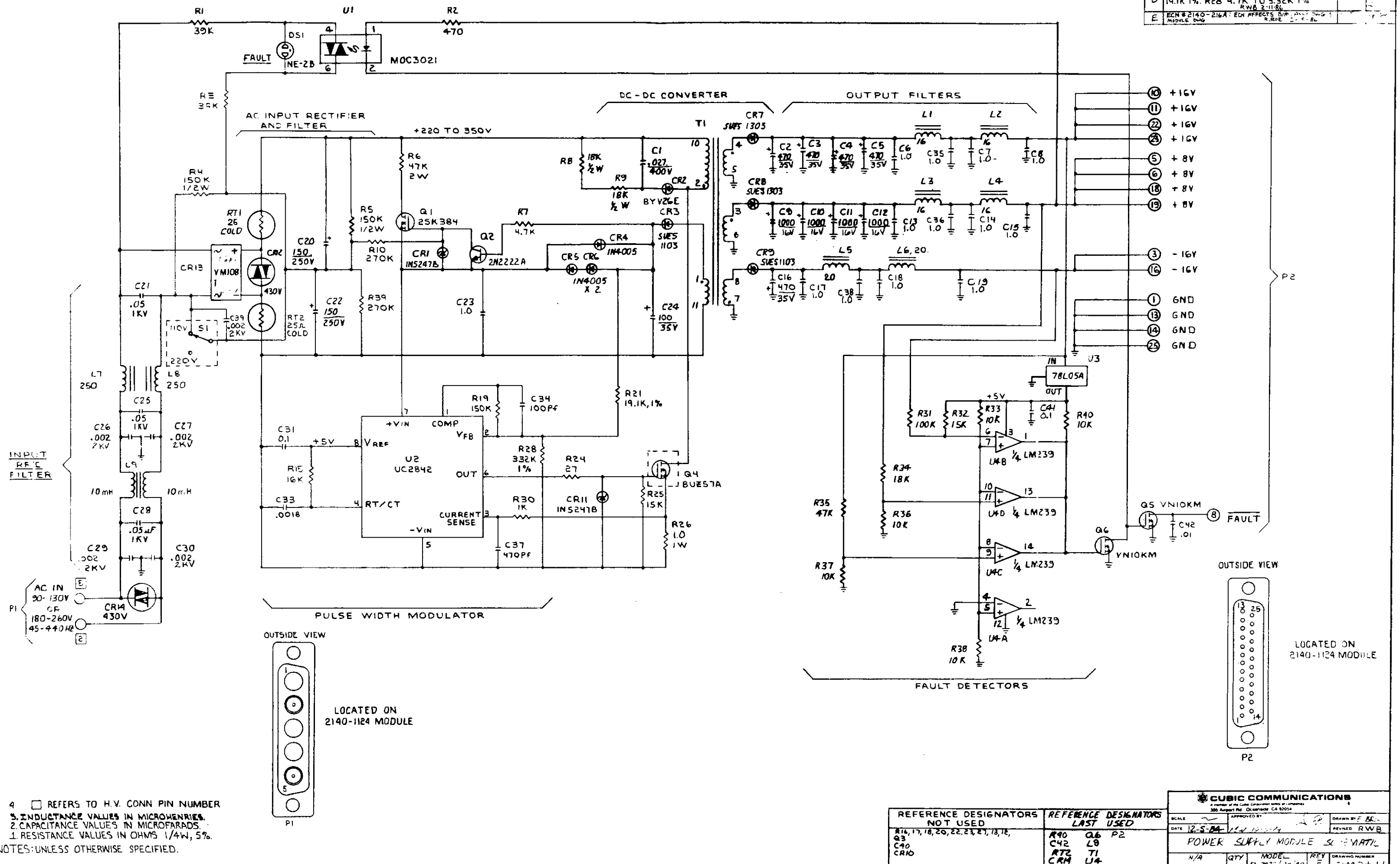
CUBIC COMMUNICATIONS

SCALE NONE	APPROVED BY		DRAWN BY L. ROLL
DATE 12-5-84			REVISED

IEEE-488 BUS CONNECTOR BD SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-2021	1	R-3030	A	2140-2021

LET	REVISION	
A	ECN#2140-31, DELETED C48 & C44 ... 2KV. 4JG 2-4-75	
B	ECN#2140-51, ADDED C37, .002, 2KV. RJOE 2-12-85	
C	ECN#2140-60, R5 ... RWB 2-25-85	
D	ECN#2140-206: REVISED R21 21K TO 19.1K 1%. R28 4.7K TO 3.32K 1% RWB 2-18-86	
E	ECN#2140-216A: ECN AFFECTS B/M ... MODULE DWG. RJOE 2-6-86	



4 ☐ REFERS TO H.V. CONN PIN NUMBER
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATORS NOT USED	REFERENCE DESIGNATORS LAST USED	
R14, 17, 18, 20, 22, 23, 27, 13, 18, Q3 C40 CR10	R40	Q6 P2
	C42	L8
	RT2	T1
	CR14	U4

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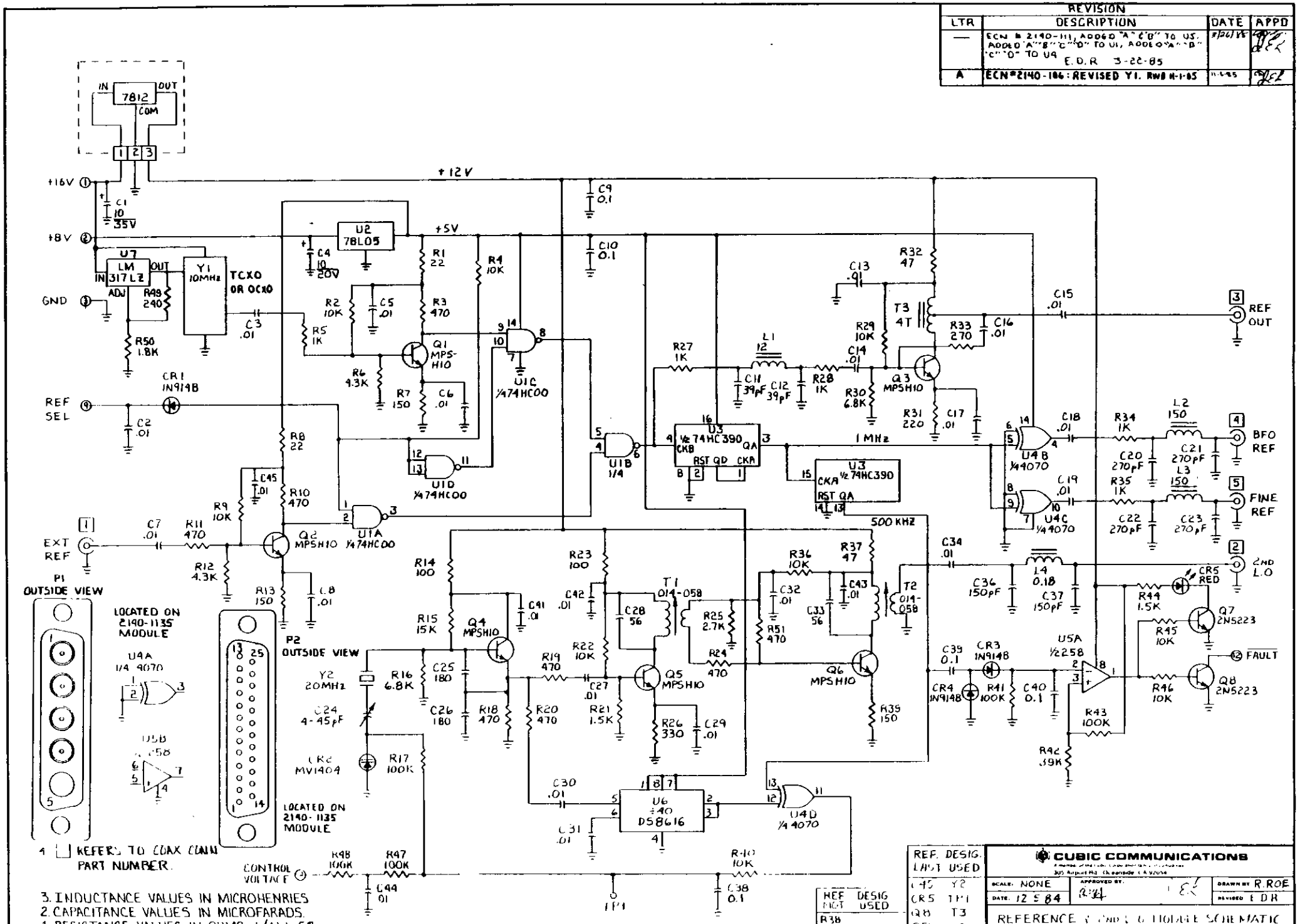
SCALE ~	APPROVED BY		DRAWN BY E BR...
DATE 12-5-84			REVISED RWB

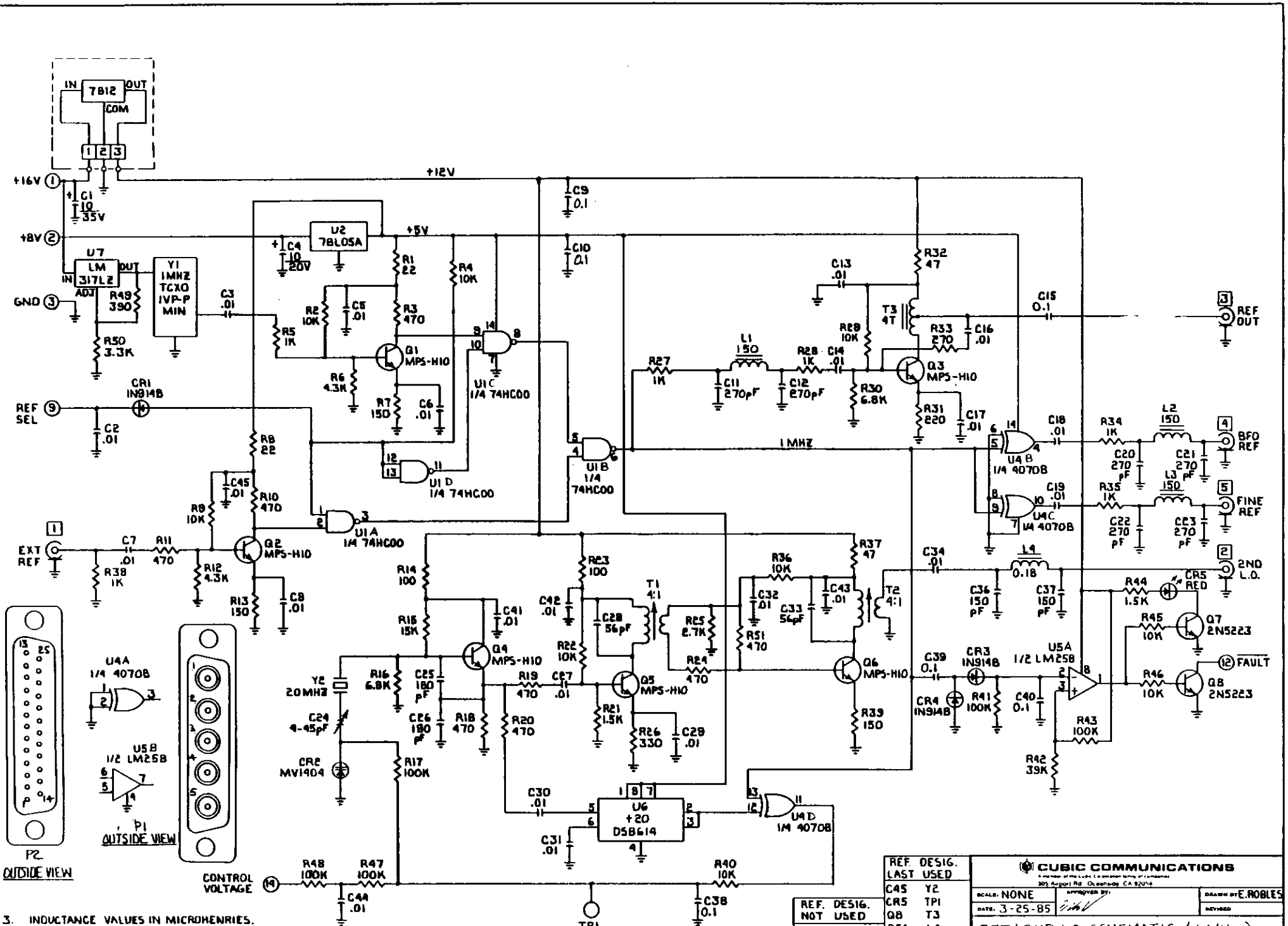
POWER SUPPLY MODULE SCHEMATIC

N/A	QTY	MODEL R-3020/3040	REV E	DRAWING NUMBER 2140-2+ 1



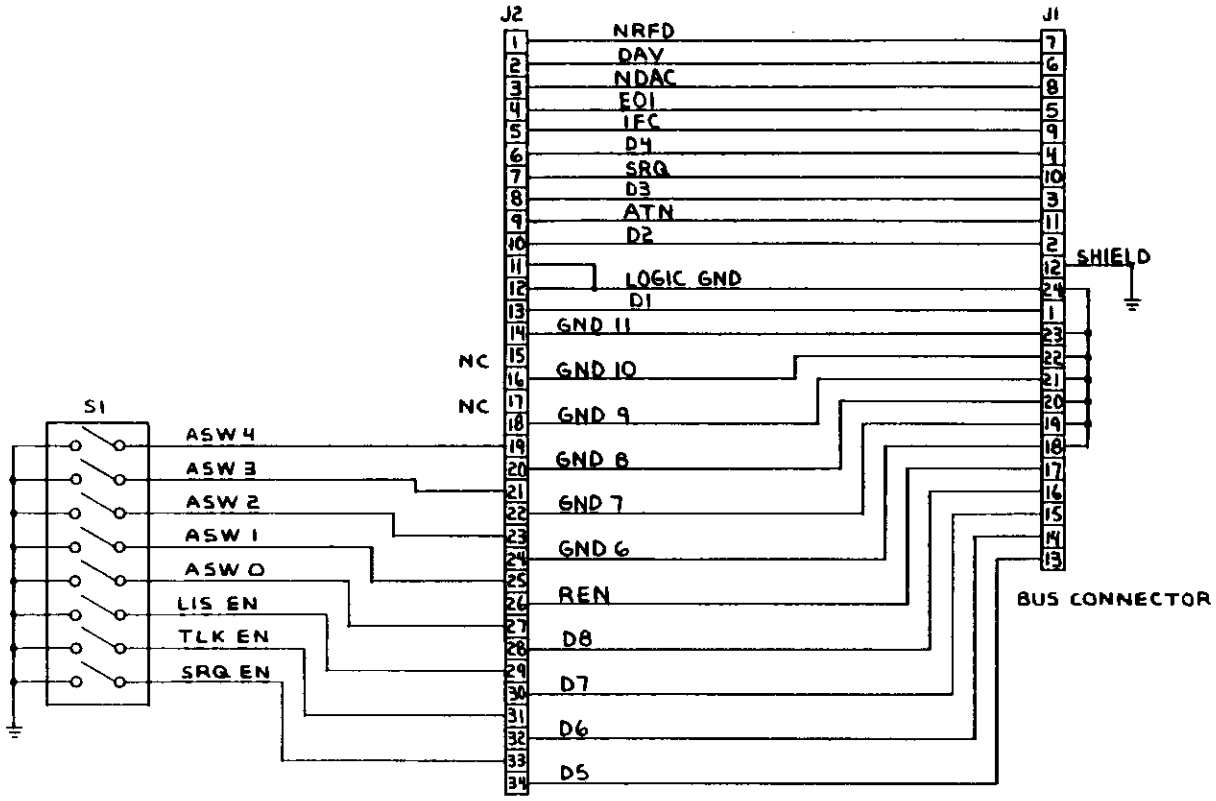
1. REFERS TO COAX CABLE PART NUMBER.

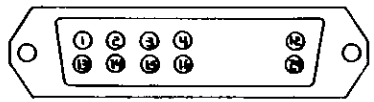
NOTES: UNLESS OTHERWISE SPECIFIED.
2. CAPACITANCE VALUES IN MICROFARADS.
3. INDUCTANCE VALUES IN MICROHENRIES
.1 RESISTANCE VALUES IN OHMS 1/4W, 5%


U7 LM 317LZ
7812
78L05A
+16V
+12V
+8V
+5V
GND
Y1 1MHZ TCXO 1VP-P MIN
R49 390
R50 3.3K
C1 10 35V
C4 10 20V
C9 0.1
C10 0.1
R1 22
R2 10K
R3 470
R4 10K
R5 1K
R6 4.3K
R7 150
C5 .01
C6 .01
C3 .01
Q1 MPS-H10
U1C 1/4 74HC00
U1D 1/4 74HC00
U1B 1/4 74HC00
U1A 1/4 74HC00
CR1 IN914B
REF SEL
C2 .01
R8 22
R9 10K
R10 470
C45 .01
Q2 MPS-H10
EXT REF
C7 .01
R11 470
R12 4.3K
R13 150
C8 .01
R38 1K
R32 47
C13 .01
T3 4T
R28 10K
R33 270
C16 .01
C15 0.1
L1 150
R27 1K
C11 270pF
C12 270pF
R28 1K
C14 .01
R30 6.8K
Q3 MPS-H10
R31 220
C17 .01
C18 .01
U4B 1/4 4070B
1MHZ
C19 .01
U4C U4 4070B
R34 1K
L2 150
C20 270 pF
C21 270 pF
L3 150
R35 1K
C22 270 pF
C23 270 pF
REF OUT
BFO REF
FINE REF
2ND L.O.
R37 47
C34 .01
L4 0.18
C36 150 pF
C37 150 pF
R36 10K
C32 .01
C43 .01
C33 56pF
T2 4:1
R51 470
R23 100
R14 100
R15 15K
C41 .01
C42 .01
C28 56pF
T1 4:1
R25 6.7K
R24 470
R22 10K
Q4 MPS-H10
Q5 MPS-H10
Q6 MPS-H10
R19 470
C27 .01
R21 1.5K
R26 330
C29 .01
R20 470
R18 470
C26 180 pF
R16 6.8K
C25 180 pF
Y2 20MHZ
C24 4-45pF
CR2 MV1404
R17 100K
R39 150
C39 0.1
CR3 IN914B
CR4 IN914B
R41 100K
C40 0.1
U5A 1/2 LM258
R43 100K
R42 39K
R44 1.5K
CR5 RED
R45 10K
Q7 2N5223
R46 10K
Q8 2N5223
FAULT
U4A 1/4 4070B
U5B 1/2 LM258
P1 OUTSIDE VIEW
P2 OUTSIDE VIEW
U6 +20 DS8614
C30 .01
C31 .01
U4D 1/4 4070B
CONTROL VOLTAGE
R48 100K
R47 100K
C44 .01
TP1
R40 10K
C38 0.1
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS, 1/4W, 5%
NOTES: UNLESS OTHERWISE SPECIFIED
5 ○ REFERS TO CONNECTOR PIN NUMBER.
4. □ REFERS TO COAX CONNECTOR PIN NUMBER.
REF. DESIG. NOT USED
U3, R52, R53, R54, C35
REF. DESIG. LAST USED
C45 Y2
CR5 TP1
Q8 T3
R54 L4
U7
CUBIC COMMUNICATIONS
SCALE: NONE
DATE: 3-25-85
DRAWN BY: E. ROBLES
REF & 2ND L.O. SCHEMATIC (1 MHz)
N/A
QTY
MODEL R-2307/U
REV
8140-2451

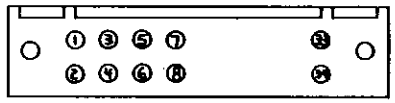
REVISIONS			
LTR	DESCRIPTION	DATE	APP'D
—	ECN#2140-197 : REMOVED GND SYM. PIN 18, J1. REMOVED CONNECTION BETWEEN PIN 12, J1 AND LOGIC GND. ADDED J1 DESIGNATOR PER ECN 1-8-85	1-11-85	

TO MOTHER BOARD





J1 CONNECTOR
BOTTOM VIEW



J2 CONNECTOR
BOTTOM VIEW

CUBIC COMMUNICATIONS
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305 Airport Rd Oceanside CA 92054

SCALE NONE	APPROVED BY K ROE 8-9-85 RG 9/26/85	DRAWN BY RWB
DATE 7-23-85		REVISED

IEEE-488 BUS CONN SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
2140-2056		R-3050/70/80		2140-2456

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	ECN #2140-189: CHANGED R34, 10K WAS R31, 10K. R. ROE		
B	ECN #2140-193: CHANGED R54, 1.8K WAS 510. R80, 1.8K WAS 510. R. ROE		
C	ECN #2140-207: CHANGED R33, 33 WAS 82. MK 1-24-86 ECN #2140-207-1: CHANGED R33, 33 WAS 82. MK 1-24-86 NEWEST ECO REV C		

H1

MED

LO

FIRST LO

STEP RF

FINE RF 45-145KHz

U6 7812 P3 — Z140-1105 — L11 4T — +12V OUT — IN — ① +16V

U7 7805 P4 — Z140-1105 — L12 4T — +5V OUT — IN — ② +8V

③ GND

OUTSIDE VIEW — P1

N/C — ④ SYN EN

N/C — ⑥ SYN CLK

N/C — ⑪ BFO ON/OFF

OUTSIDE VIEW — P2

U8 79L12A — L14 4T — -12V — ⑬ -16V

⑫ OUTPUT FAULT

COARSE C.V.

FINE C.V.

TP1

TP2

⑩ COARSE TUNE

⑦ VCO LO

⑨ VCO MID

⑧ VCO HI

⑭ OUTPUT LOOP CONTROL VOLTAGE

4. □ REFERS TO COAX CONN PIN NUMBER
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

REFERENCE DESIGNATION LAST USED	CUBIC COMMUNICATIONS		
C98, CR20, L14, Q20, R96, T6, U8, Z1	SCALE: NONE	DRAWN BY: R. ROE	
REFERENCE DESIGNATION NOT USED	DATE: 7-17-85	REVISED	
	OUTPUT LOOP MODULE SCHEMATIC		
	N/A: 2140-2061	QTY	MODEL: R3030 50.30
	REV: C	DRAWING NUMBER: 2140-24	

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	ECN #2140-192 REV -NTR ENG ONLY. CHG IS TO ASSY DWG AND MODULE DWG. R.BOE 11-21-85	11-22-85	JSD

HI
58.6-70.4 MHZ

MED
48.7-58.5 MHZ

LOW
40.4-48.6 MHZ

STEP REF

STEP REF

LOCATED ON
2140-1106 MODULE

OUTSIDE VIEW

P2

OUTSIDE VIEW

P1

LOCATED ON
2140-1106 MODULE

STEP LOOP CONTROL VOLTAGE

LAST REF. DESIGNATIONS USED:
R64, C71, Q10, CR20, U10, T4, L7

4. ☐ REFERS TO COAX CONN PIN NUMBER
3. INDUCTANCE VALUES IN MICROHENRIES.
2. CAPACITANCE VALUES IN MICROFARADS.
1. RESISTANCE VALUES IN OHMS 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED.

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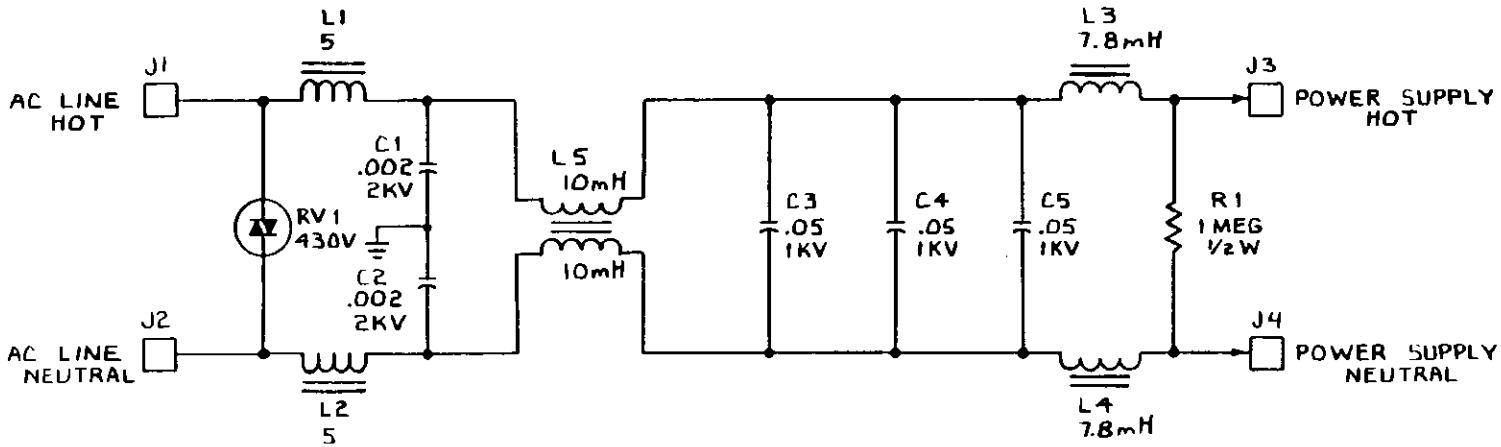
SCALE: NONE	APPROVED BY:	DRAWN BY: RWB
DATE: 10-7-85		REVISED

STEP LOOP MODULE SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
		R-3020/30/40/50/80	9	2140-24 02

REVISIONS			
LTR	DESCRIPTION	DATE	APPD



3. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10%

2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10%

1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT

NOTES: UNLESS OTHERWISE SPECIFIED

CUBIC COMMUNICATIONS

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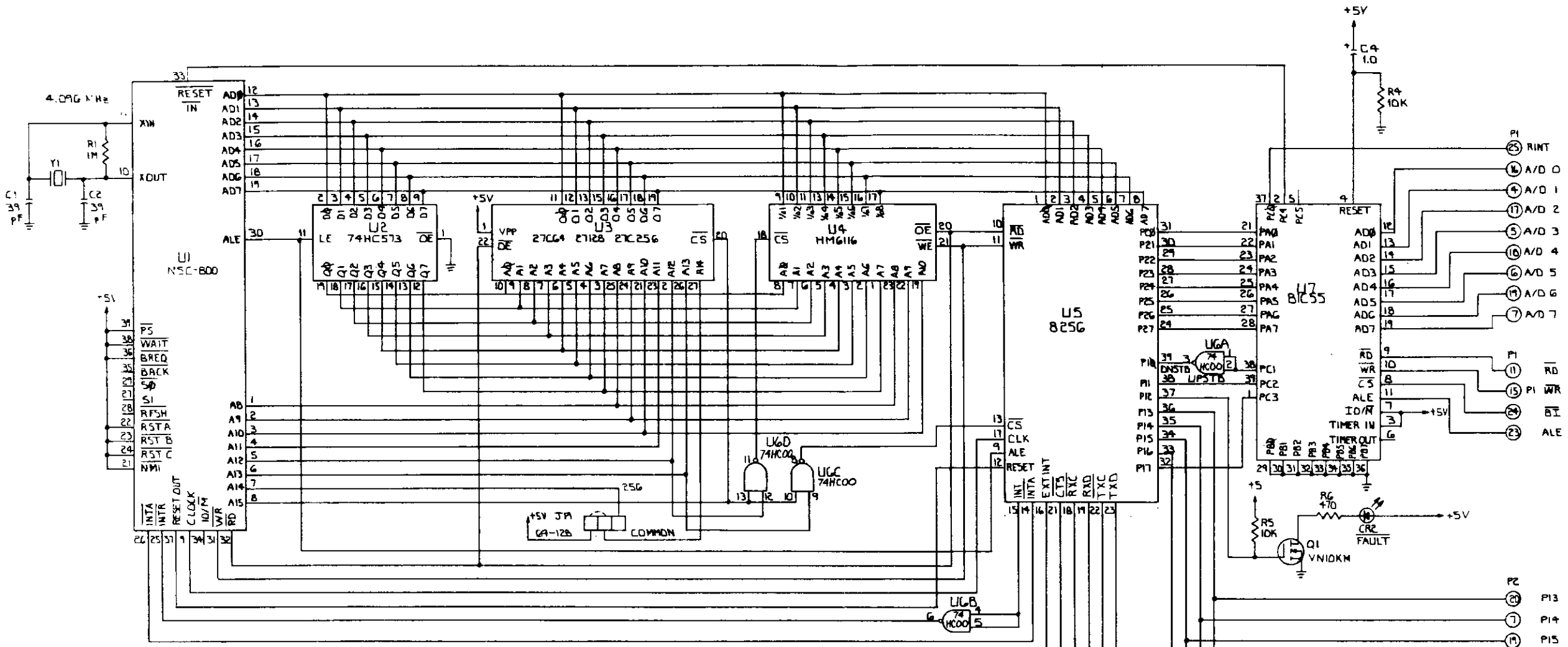
305 Airport Rd Oceanside CA 92054

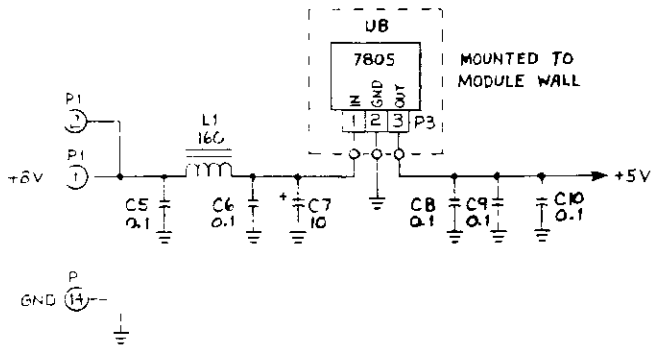
SCALE: NONE	APPROVED BY KEW 10-30-85 REL	DRAWN BY R. ROE
DATE: 10-28-85		REVISED

AC LINE FILTER BRD

N/A	QTY	MODEL	REV	DRAWING NUMBER
				2140-2463

REVISIONS			
LTR	DESCRIPTION	DATE	APP'D





IC	+5V	GND
NSC800	40	20
74HC573	20	10
27C256	28	14
6116	24	12
8256	40	20
8155	40	20
74HC00	14	7

P1 ÷ P2
OUTSIDE VIEW

LOCATED ON 2140-1151 MODULE

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT
2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10%
3. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10%

REFERENCE DESIGNATORS LAST USED	CUBIC COMMUNICATIONS		
R6, C10, U8, Q1, CR2, Y1, RP1	SCALE NONE	APPROVED BY	DRAWN BY MK
REFERENCE DESIGNATORS NOT USED	DATE 11-5-85		REVISED
R2, R3, C3, CR1,	SERIAL INTERFACE BOARD		
	N/A	QTY	MODEL R-3030A
	REV		DRAWING NUMBER 2140-2464

REVISIONS			
LTR	DESCRIPTION	DATE	APPD

U1 7805 IN OUT GND
C2 10 20V
C1 0.1
L1 160
C3 0.1
U2 26LS31
J1
P14 1
P13 2
P15 3
TXD 4
5
RXD 6
CTS 7
RXC 8
P16 9
EXTINT 10
GND 11
GND 12
TXC 13
+8V 14
15
16
R1 100, 1/2 W OPTIONAL
R2 100, 1/2W OPTIONAL
R3 100, 1/2W OPTIONAL
R4 100, 1/2W OPTIONAL
DM C RR
JP2
U3 26LS32B
C4 0.1

J14 RCVR 2 RS-449/RS-422-A DTE
1 SHIELD
2 SI A'
3 NC
4 SD A
5 ST A'
6 RD A'
7 RS A
8 RT A'
9 CS A'
10 LL A
11 DM A'
12 TR A
13 RR A'
14 RL A
15 IC A'
16 SF A
17 TT A
18 TM A'
19 SG C
20 RC B'
21 NC
22 SD B
23 ST B'
24 RD B'
25 RS B
26 RT B'
27 CS B'
28 IS A
29 DM B'
30 TR B
31 RR B'
32 SS A
33 SQ A'
34 NS A
35 TT B
36 SB A'
37 SC C

J1, J3
TOP VIEW

OUTSIDE VIEW
J13, J14

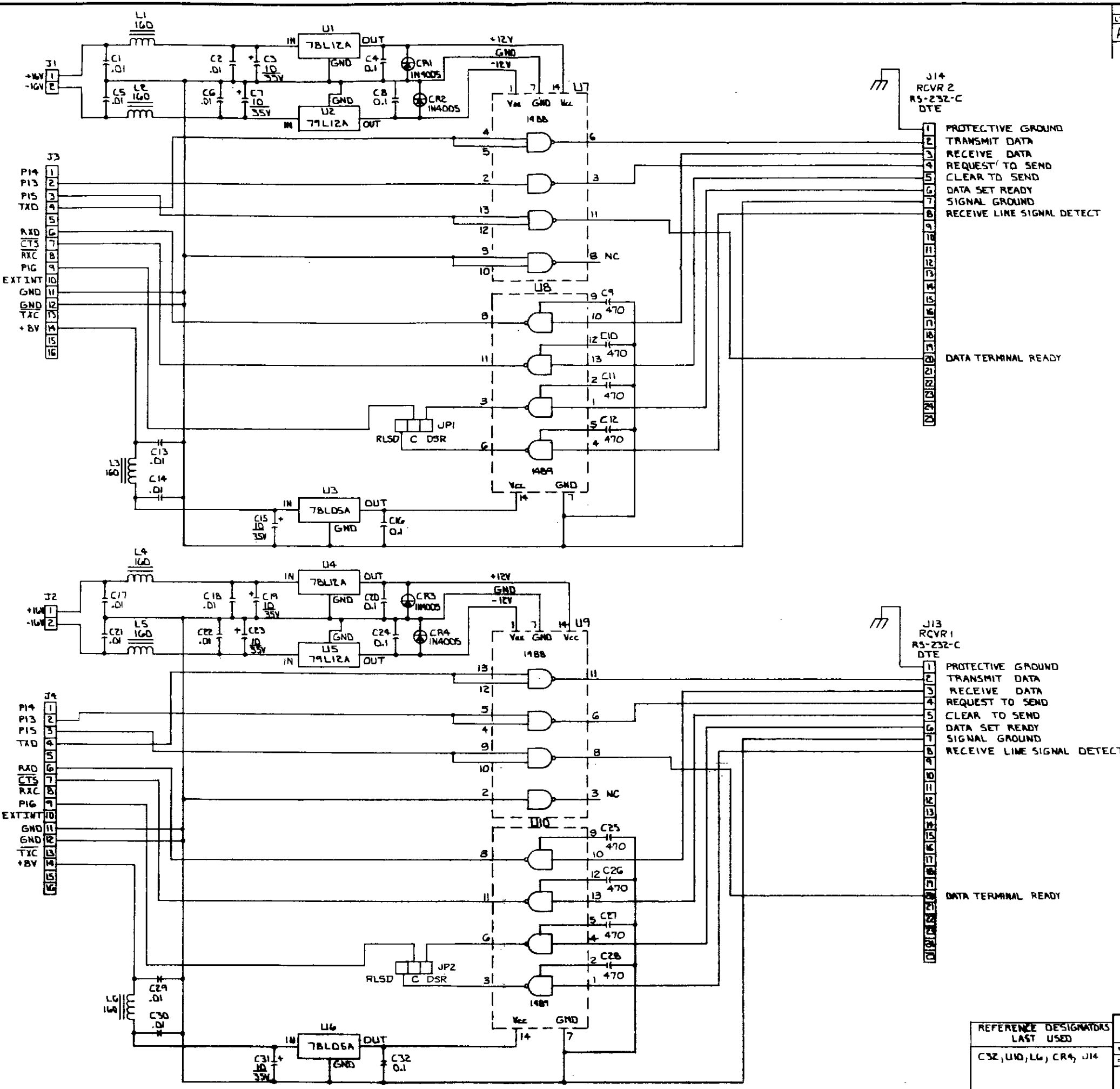
U6 1805 IN OUT GND
C6 10 20V.
C5 0.1
L2 160
C7 0.1
U4 26LS31
J3
P14 1
P13 2
P15 3
TXD 4
5
RXD 6
CTS 7
RXC 8
P16 9
EXTINT 10
GND 11
GND 12
TXC 13
+8V 14
15
16
R5 100.1/2W OPTIONAL
R6 100, 1/2W OPTIONAL
R7 100, 1/2W OPTIONAL
R8 100, 1/2W OPTIONAL
DM C RR
JP1
U5 26LS32B
C8 0.1

J13 RCVR 1 RS-449/RS-422-A DTE
1 SHIELD
2 SI A'
3 NC
4 SD A
5 ST A'
6 RD A'
7 RS A
8 RT A'
9 CS A'
10 LL A
11 DM A'
12 TR A
13 RR A'
14 RL A
15 IC A'
16 SF A
17 TT A
18 TM A'
19 SG C
20 RC B'
21 NC
22 SD B
23 ST B'
24 RD B'
25 RS B
26 RT B'
27 CS B'
28 IS A
29 DM B'
30 TR B
31 RR B'
32 SS A
33 SQ A'
34 NS A
35 TT B
36 SB A'
37 SC C

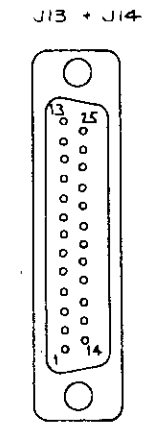
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT
2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10%
3. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10%

REF DESIGNATOR LAST USED	CUBIC COMMUNICATIONS, a member of the Cubic Corporation family of companies, 305 Airport Rd Oceanside CA 92054			
U6, C8, R8, J14	SCALE: NONE	APPROVED BY: R. RUE 12-5-85		DRAWN BY: RW8
	DATE: 12-2-85			REVISED: KC
	RS-422-A CONNECTOR BD. SCHEMATIC			
	N/A	QTY	MODEL: A-3030 SERIES	REV
	DRAWING NUMBER: 2140-2465			

REVISIONS			
LTR	DESCRIPTION	DATE	APPD
A	ECN# 2140-219: ADDED PIN 6 TO U7, PIN 11 TO U9. RWB 2-20-86	2-21-86	

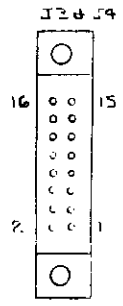


J13 + J14



OUTSIDE VIEW

J13 & J14



TOP VIEW

3. INDUCTOR VALUES ARE IN MICROHENRIES (uH), 10%
2. CAPACITOR VALUES ARE IN MICROFARADS (uF), 10%
1. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT

NOTES: UNLESS OTHERWISE SPECIFIED

REFERENCE DESIGNATORS LAST USED
C32; U10; L6; CR4; J14

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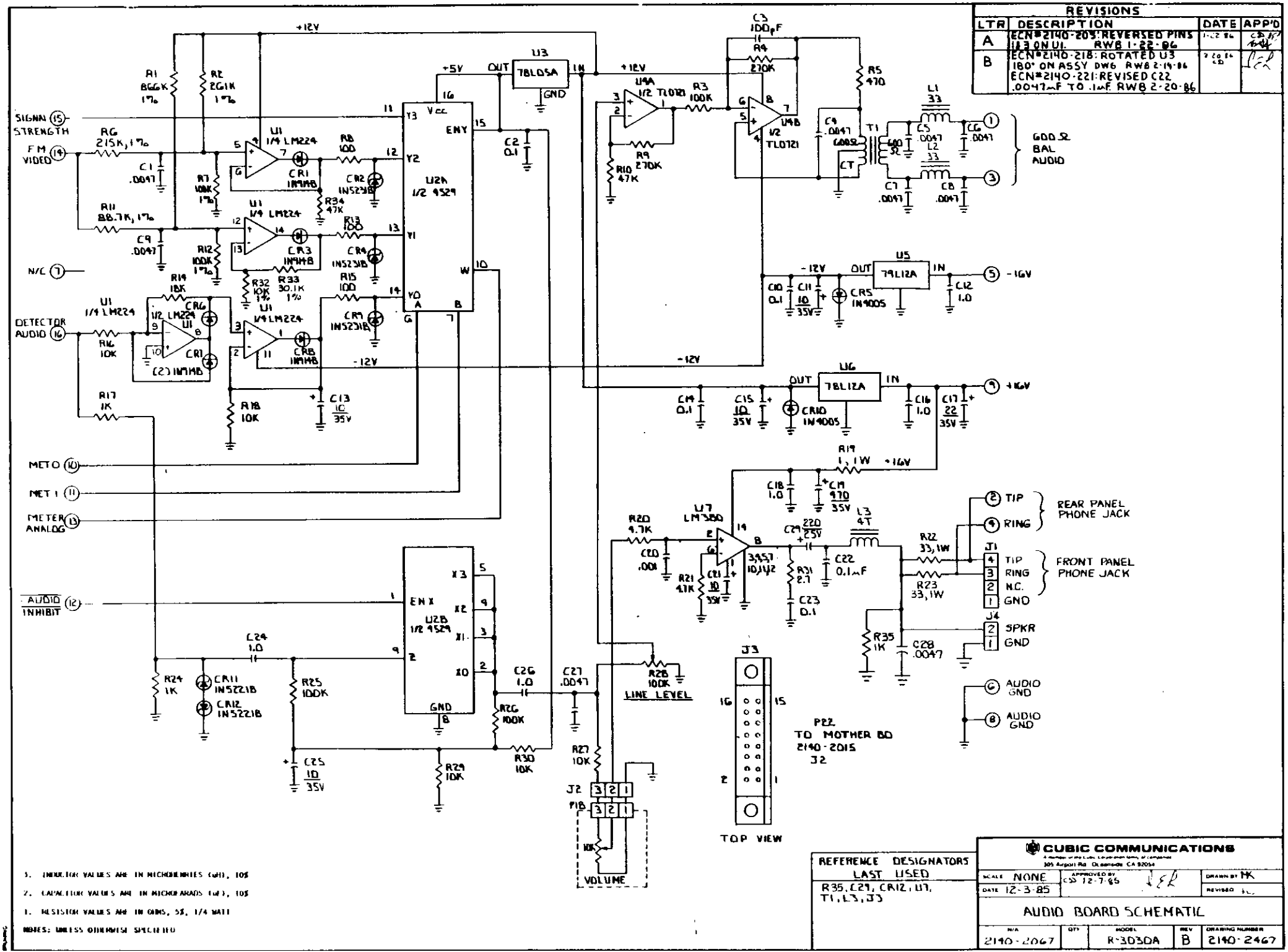
FSCM 59532

SCALE	NONE	APPROVED BY	DEL
DATE	11-26-85	DRAWN BY	MK
		CHECKED	

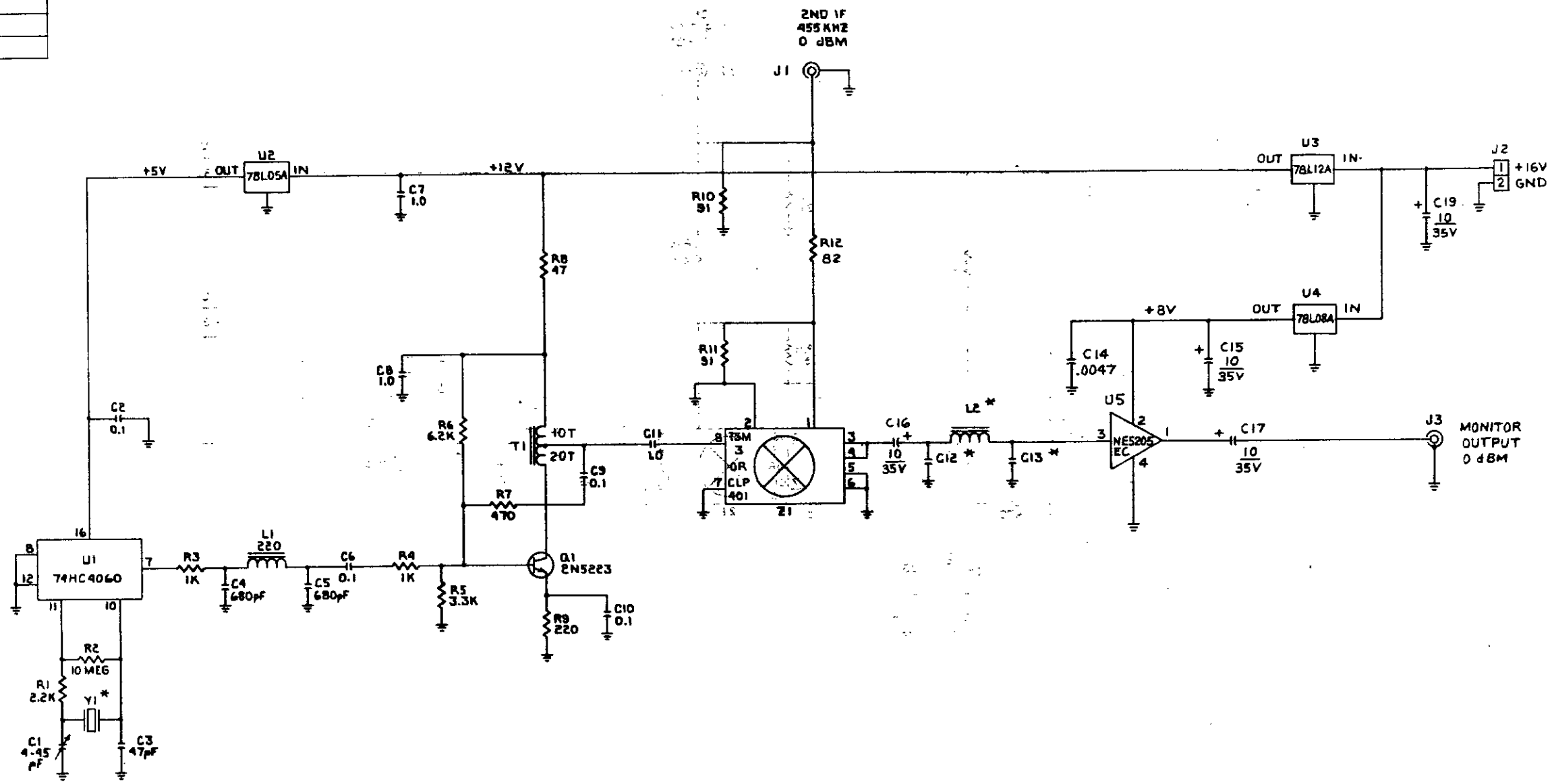
RS-232-C CONNECTOR BD. SCHEMATIC

NEXT ASSEMBLY	QTY	MODEL	REV	DRAWING NUMBER
		R-303D	A	2140-2906


REVISIONS
LTR | DESCRIPTION | DATE | APP'D
A | ECN#2140-205: REVERSED PINS U3 ON U1. RWB 1-22-86 | 1-22-86 | CSS
B | ECN#2140-218: ROTATED U3 180° ON ASSY DWG RWB 2-19-86 ECN#2140-221: REVISED C22 .0047μF TO .1μF. RWB 2-20-86 | 2-20-86 CSS | CSS
+12V
+5V
-12V
-16V
+16V
SIGNAL STRENGTH
FM VIDEO
DETECTOR AUDIO
N/C
METO
MET 1
METER ANALOG
AUDIO INHIBIT
LINE LEVEL
VOLUME
600Ω BAL AUDIO
REAR PANEL PHONE JACK
FRONT PANEL PHONE JACK
TIP
RING
N.C.
GND
SPKR
AUDIO GND
P22 TO MOTHER BD 2140-2015 32
TOP VIEW
U1 1/4 LM224
U2A 1/2 4529
U2B 1/2 4529
U3 78L05A
U4A 1/2 TL072
U4B 1/2 TL072
U5 79L12A
U6 78L12A
U7 LM380
T1
L1 33
L2 33
L3 4T
R1 866K 1%
R2 261K 1%
R3 100K
R4 270K
R5 470
R9 270K
R10 47K
R11 88.7K 1%
R12 100K 1%
R13 100
R14 100K 1%
R15 100
R16 10K
R17 1K
R18 10K
R19 1, 1W
R20 4.7K
R21 4.7K
R22 33, 1W
R23 33, 1W
R24 1K
R25 100K
R26 100K
R27 10K
R28 100K
R29 10K
R30 10K
R31 2.7
R34 47K
R35 1K
R36 10K
R37 100K 1%
R38 10K 1%
C1 .0047
C2 0.1
C3 100pF
C4 .0047
C5 .0047
C6 .0047
C7 .0047
C8 .0047
C9 .0047
C10 0.1
C11 10 35V
C12 1.0
C13 10 35V
C14 0.1
C15 10 35V
C16 1.0
C17 22 35V
C18 1.0
C19 470 35V
C20 .001
C21 10 35V
C22 0.1μF
C23 0.1
C24 1.0
C25 10 35V
C26 1.0
C27 .0047
C28 .0047
C29 220 25V
CR1 IN914B
CR2 IN5231B
CR3 IN914B
CR4 IN5231B
CR5 IN4005
CR6 IN914B
CR7 IN5231B
CR8 IN914B
CR9 IN4005
CR10 IN4005
CR11 IN5221B
CR12 IN5221B
(2) IN914B
J1
J2
J3
J4
P1B
1. INDUCTOR VALUES ARE IN MICROHENRIES (μH), 10%
2. CAPACITOR VALUES ARE IN MICROFARADS (μF), 10%
3. RESISTOR VALUES ARE IN OHMS, 5%, 1/4 WATT
NOTES: UNLESS OTHERWISE SPECIFIED
REFERENCE DESIGNATORS LAST USED
R35, C29, CR12, U7, T1, L3, J3
CUBIC COMMUNICATIONS
305 Airport Rd Oceanside CA 92054
SCALE NONE
DATE 12-3-85
APPROVED BY CSS 12-7-85
DRAWN BY MK
REVISED
AUDIO BOARD SCHEMATIC
N/A 2140-2067
QTY
MODEL R-3030A
REV B
DRAWING NUMBER 2140-2467

OUTPUT FREQ	Y1	L2	C12	C13
100 KHz	8.86MHz	56	.047	.047
5 KHz	7.52MHz	470	.15	.15

LTR	DESCRIPTION	DATE	APPD
A	ECN#2140E-151, REVISED CIRCUIT, R12 WAS 100Ω, R10, R11 WERE 82Ω. AJG 6-19-15	4/14/15	JER



LAST REF. DESIGNATION USED:
R18. C20. Q2. U3. L2. T2. Y1. Z1

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE VALUES IN OHMS 1/4 W. 5%
2. CAPACITANCE VALUES IN MICROFARADS.
3. INDUCTANCE VALUES IN MICROHENRIES.
4. *-SEE CHART ABOVE FOR VALUES.

CUBIC COMMUNICATIONS

SCALE: NONE	DRAWN BY:	CHECKED BY: JER	APPROVED BY: E. ROBLES
DATE: 4-22-85			

OUTPUT CONVERTER BD. . SCHEMATIC

N/A	QTY	MODEL	REV	DRAWING NUMBER
2143-2001			A	2143-2401