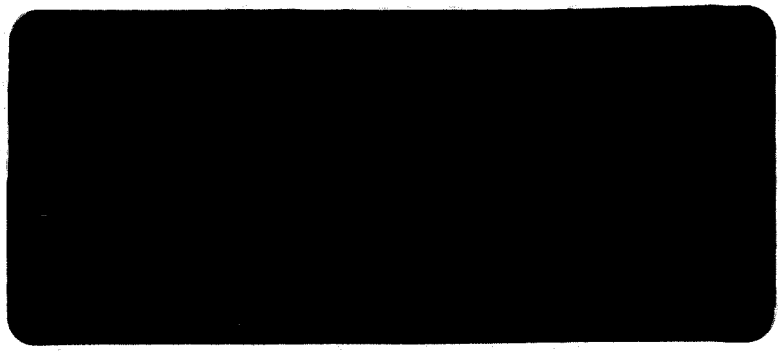

TECHNICAL MANUAL

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DEPOT MANUAL
RA6778C
LF/HF RECEIVER

NOTE

This manual contains detailed technical information on the Theory of Operation and the Maintenance procedures associated with the RA6778C Receiver. Refer to the Station Servicing Manual for information on Installation and Operating procedures.

Prepared

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CHAPTER 1
RECEIVER ASSEMBLY AND ALIGNMENT

1.1 INTRODUCTION

The RA6778C Communications Receiver is shown in Figure 1.1. A detailed description of the overall receiver, its specifications, operation, installation and general theory of operation are given in the RA6778C Station Servicing Manual. The station servicing manual also contains general procedures for the isolation of faults to a defective module. This manual contains the detailed theory of operation and detailed testing, repairing, adjusting and aligning procedures for each of the modules used in the receiver. Also, contained in this chapter are alignment procedures for the RA6778C Receiver as a complete assembly.

1.2 RECEIVER ASSEMBLY AND MODULES

Figure 1-2 is a top view (with covers removed) and Figure 1-3 is a bottom view (with covers removed) of the RA6778C Receiver. A rigid, die-cast, full width chassis provides the basis for the main frame of the receiver. Essentially all receiver circuitry, including front panel controls and displays, are contained on modules mounted on the chassis. Table 1-1 lists all the modules used in the RA6778C receiver. It should be noted that modules A6, A7, All and A23 are each made up of two separate boards. Mounted within compartments on the underside of the chassis are the mixer modules and a portion of the frequency synthesizer circuitry modules. On the top side close to the front panel are the front panel and control modules. The power supply and frequency standard modules are also mounted on the top side.

The following chapters in this manual contain detailed descriptions of operation for each module in the RA6778C receiver. Also, detailed procedures are given for testing, adjusting and aligning each module in its Racal test fixture. Schematic diagrams and photographs of all module boards, showing location of components, are also provided.

1.3 RECEIVER ALIGNMENT

This section contains alignment procedures for the RA6778C Receiver as a complete assembly. Under normal operating conditions the receiver will maintain the factory alignment over a long period of time. Re-alignment should, therefore, only be carried out where a known mis-alignment exists. Refer to the Station Servicing Manual for operating instructions.

Should it be necessary to re-align the complete receiver, the following procedures should be followed in the order given. Before attempting to re-align an individual sub-assembly it must be ascertained, where applicable, that the preceding assemblies are functioning correctly.

If the specified performance cannot be attained by alignment, then a fault must be suspected and reference should be made to Chapter 5, Troubleshooting Procedures, in the Station Servicing Manual.

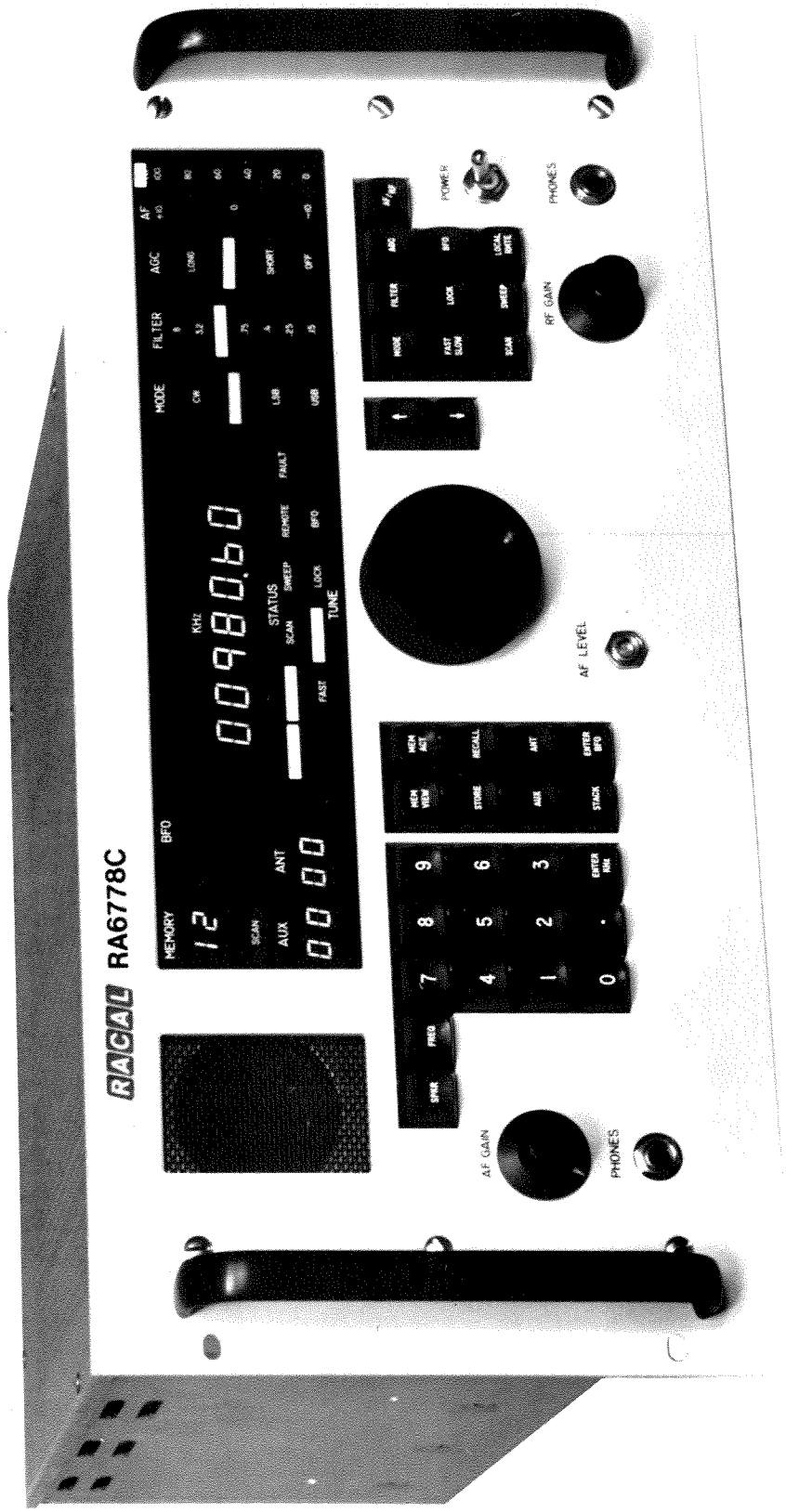


Figure 1-1. Overall View, RA6778C Receiver

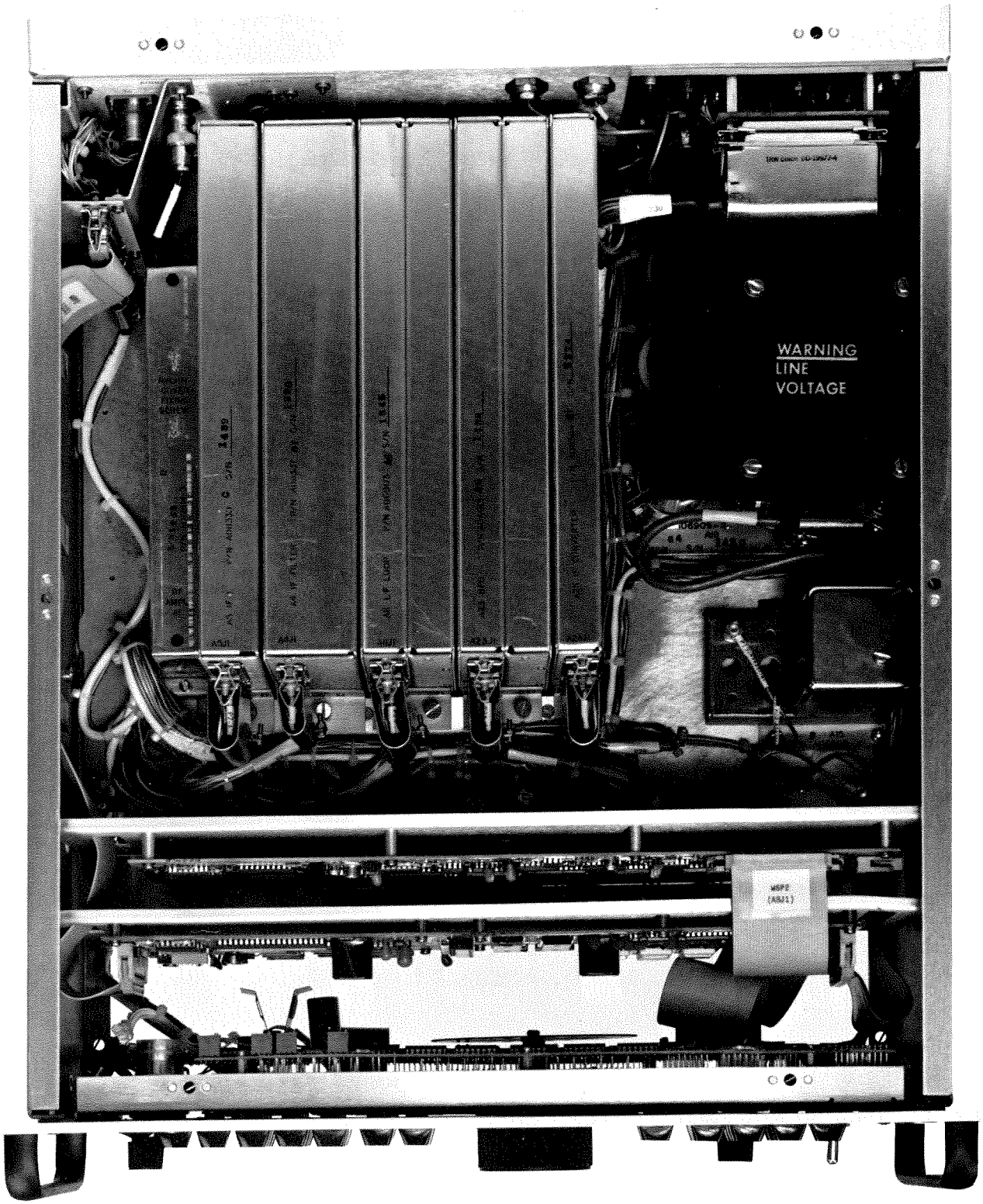


Figure 1-2. Top View, RA6778C Receiver

TABLE 1-1
RA6778C Modules

Reference Designation	Module Name
A1	RF Amplifier
A2	First Mixer
A3	Second Mixer
A4	IF Filter
A5	IF Amplifier
A6A1	Serial Asynchronous Interface
A6A2	Microcomputer
A7A1	Front Panel Display
A7A2	Front Panel Switch
A8	Latch
A11A1	Lower Loop (Synthesizer)
A11A2	Upper Loop (Synthesizer)
A13	Transfer Loop (Synthesizer)
A14	HF Loop (Synthesizer)
A15	Frequency Standard
A16	34 MHz Generator
A18	Power Supply
A23A1	BFO Lower Loop (Synthesizer)
A23A2	BFO Upper Loop (Synthesizer)
A25	IF Converter

A certain amount of dismantling is necessary to gain access to certain areas of the receiver. Details for dismantling and re-assembly are contained in paragraph 1.3.1. After alignment, ensure that all dismantled assemblies are correctly reassembled and that all shielding covers are replaced using all the screws provided or their exact equivalents.

Table 1-2 lists the test equipment required. Those listed in the example column are recommended only. Any instruments with equal or better characteristics may be substituted.

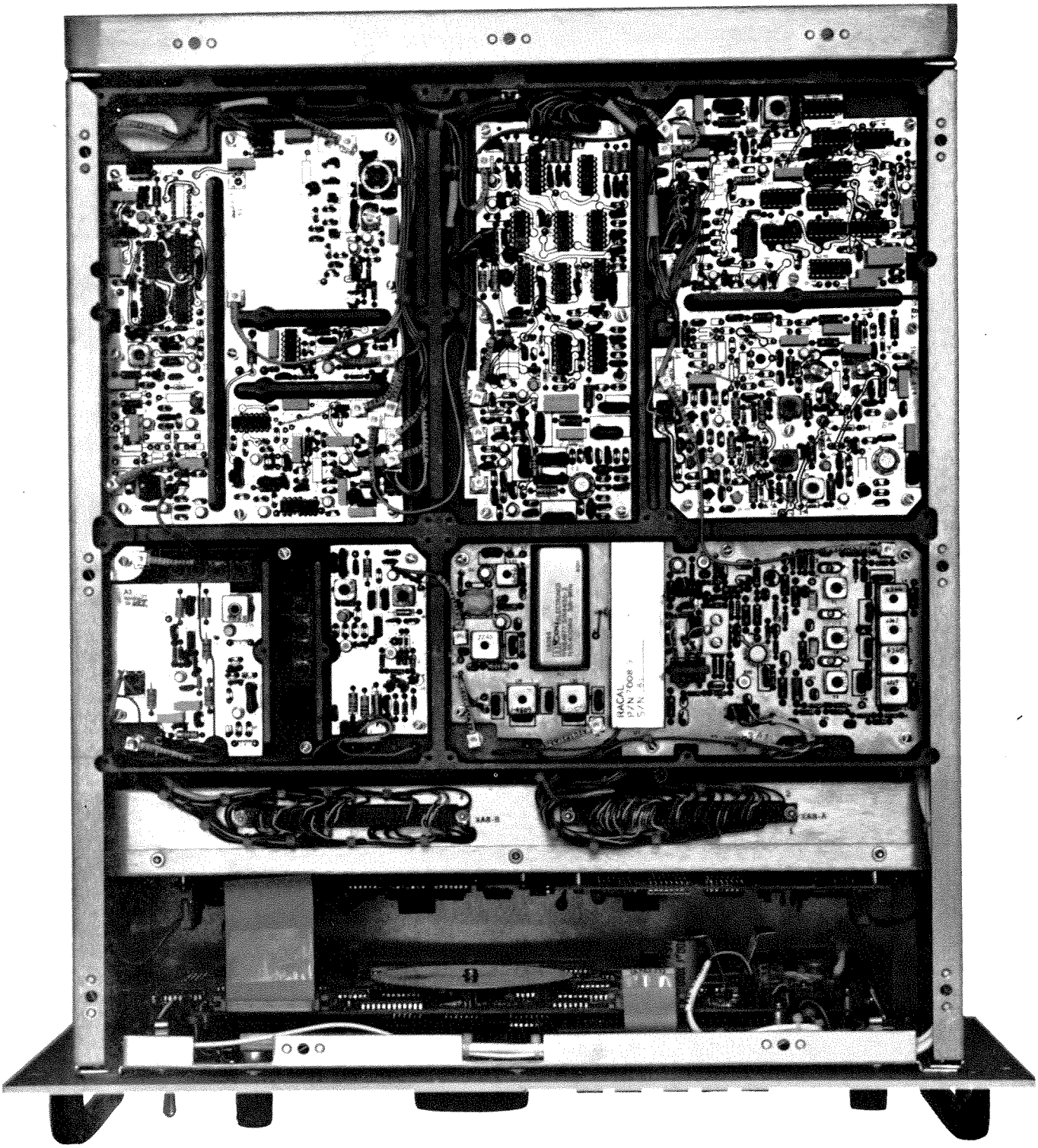


Figure 1-3. Bottom View, RA6778C Receiver

TABLE 1-2. TEST EQUIPMENT

Item	Instrument	Specifications	Recommended Instrument or Equal
1	Digital Multimeter	Range: 0 to 150 Vac and dc 0 to 1A ac and dc Display: 3½ digits Accuracy: ±2 L.S. digit	Fluke 8000A
2	Oscilloscope, Dual Trace	Sensitivity: 5 mV/div. Frequency: dc to 2 MHz	Tektronix 465
3	HF Voltmeter	Range: 300 mV to 3 Vrms Frequency: 100 kHz to 70 MHz Input Impedance: > 1 M ohm with 50 ohm adapter Accuracy: ±1% of full scale	Boonton 91H
4	Distortion Analyzer	Distortion Levels: 0.1 to 100% Frequency: 5 Hz to 600 kHz Voltage Range: 300 uV to 300 Vrms Voltmeter Accuracy: ±2% up to 300 kHz	Hewlett-Packard 331A
5	Spectrum Analyzer/ Tracking Generator	Frequency Range: 1 kHz to 100 MHz Frequency Bandwidth: 10 Hz	Hewlett-Packard 8552B/8553B/8443A/141T Marconi TR2370
6	High Impedance Probe (for item 5)	Frequency Response: ±0.5 dB from 0.1 to 110 MHz ±3 dB from 1 kHz to > 500 MHz Input Impedance: 100K ohms shunt capacity of 3 pF @ 100 MHz with 10:1 or 100:1 divider, 1M ohm with 1 pF @ 100 MHz	Hewlett-Packard 1121A Marconi TK2374
7	Digital Frequency Meter	Frequency Range: 0 to 50 MHz Sensitivity: 0.1 Vrms, 0.3 V pulse @ 8 ns min. p.w. Impedance: 1M ohm Accuracy: 1 part in 10^6 ±1 count	Hewlett-Packard 5327C
8	Signal Generator	Frequency Range: 500 kHz to 100 MHz Accuracy: ±0.5% of dial setting Stability: < 10 parts in 10^6 Output Level Range: −140 dBm to +10 dBm Modulation: AM – 0 to 100% FM ±150 kHz @ 30 MHz Output Impedance: 50 ohms	Hewlett-Packard 8640A
9	Variable Voltage Stabilized Power Supply	Voltage Output: 0 to 10 Vdc @ 1A Load Regulation: ±4 mVdc Line Regulation: ±4 mVdc	Hewlett-Packard 6213A
10	Terminating Coupler	50-ohm BNC	

1.3.1 Receiver Disassembly and Reassembly

Figures 1-2 and 1-3 show the location of the modules in the receiver.

To disassemble the receiver proceed as follows:

(a) Remove the receiver from rack or cabinet. It is held by 4 screws on the front panel.

(b) Remove top cover plate by loosening six quarter-turn fasteners.

(c) The A1, A4, A5, A11, A15, A23 and A25 modules may now be removed from the chassis by loosening their respective mounting screws. Modules may be placed on their side, supported by remaining modules, and the module shield covers removed for access to test points, adjustment points, etc. Unplug coaxial and multipin connectors as necessary to completely remove modules. The Power Supply module (A18) may be removed by loosening 4 captive screws holding the module to the chassis and 7 screws holding the module to the rear panel. The A8 module can be lifted upward after removing 4 screws and disconnecting two ribbon cables, W6 and W7.

Modules A6A1, A6A2, A7 (A7A1, A7A2) require dropping the front panel. This is achieved by removing six (6) front panel screws which hold it to the side frame. Modules A6A1, A6A2 are now accessible. Four (4) and six (6) screws respectively hold the modules to the chassis. Each module has one cable and one connector for removal. Removal of the A7 requires dropping the front panel as above, disconnecting ribbon cable W6, and unfastening the power switch, the two phone jacks, and the three potentiometers. Remove the tuning knob. This reveals one front panel screw which holds the A7 to the front panel.

(d) Figure 1-3 shows a bottom view of the chassis. To gain access to any of the 5 boards contained in this section, remove the shielding cover from the appropriate compartment. A printed circuit board may be removed by disconnecting the cables and loosening the captive screws. To reassemble the receiver follow the reverse procedure.

1.3.2 Alignment Procedure, Power Supply A18

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2 and Oscilloscope, item 2.

Procedure

(a) Disconnect the cable located on the top of the power supply.

(b) Connect the digital voltmeter, item 1, between chassis (0V) and each of the following pins of the power supply, A18, in turn. Use the oscilloscope, item 2, to measure the ac ripple.

A18 Board Pin No.	Voltage	AC Ripple (p-p)
J1 – J17	−12V ±0.5V	5 mV
J1 – 14	−7V ±0.5V	5 mV
J1 – 4	+20V ±1V	5 mV
J1 – 7	+12V ±0.5V	5 mV
J1 – 11	+5V +0.5 −0.2V	5 mV

(c) Disconnect all test equipment and reconnect the cable to the power supply.

NOTE

Throughout the receiver, the following cable color code is used for DC power distribution:

+20V	RED
+12V	ORANGE
+5V	BROWN
−7V	VIOLET
−12V	WHITE/VIOLET
0V	BLACK

1.3.3 Alignment Procedure, Frequency Standard Board, A15

Test Equipment Required: Digital Frequency Meter, item 7 of Table 1-2.

Procedure

Disconnect the cable from connector J4 on module A15. Connect the digital frequency meter to connector J4 and adjust the crystal oscillator (through the access hole in the top of the crystal) to obtain a reading on the digital frequency meter of 5,000,000 Hz ±0.1 Hz.

1.3.4 Alignment Procedure, Lower Loop Board, A11A1 and BFO Lower Loop Board, A23 A1

Test Equipment required: Digital Multimeter, item 1 of Table 1-2; Oscilloscope, item 2; and HF Voltmeter, item 3.

Procedure

(a) Connect the HF voltmeter (high impedance probe) between the junction of R1 and CR2, and chassis (0V). Adjust the core of transformer T1 (1 MHz input) to a maximum indication on the HF voltmeter. The level should be approximately 1 V rms.

(b) Set the kHz portion of the receiver frequency to 000.00. (For A23, set the BFO frequency to 000 Hz).

(c) Connect the multimeter, set to the 50 Vdc range, between TP1 (positive) and chassis (negative).

(d) Adjust L1 (6 - 7 MHz VCO) for a reading of +14V on the multimeter; +6V for A11A1.

(e) Measure the output signal level from the 6 - 7 MHz VCO at TP2 using the HF voltmeter (high impedance probe). The level should be approximately 1 V rms.

(f) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate those indicated.

TP3: 1 MHz square wave; approximatelv 1:1 on/off ratio, 3.5V p-p.
TP4: 1 kpps, positive going, 3.5V p-p; 10 kpps on A23A1.
TP5: 1 kpps, positive going, 3.5V p-p; 10 kpps on A23A1.
TP6: 1 kpps, negative going strobe pulse, 3.5V p-p; 10 kpps on A23A1.
TP7: 13 to 20 kHz, square wave, 3.5V p-p.
TP8: 13 to 20 kpps, negative going strobe pulse, 3.5V p-p.

(g) Disconnect all test equipment.

1.3.5 Alignment Procedure, Upper Loop Board, A11A2, and BFO Upper Loop Board, A23A2

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2; Oscilloscope, item 2; and HF Voltmeter, item 3.

Procedure

(a) Set the kHz portion only of the receiver frequency to 990.00. (For A23, set the BFO frequency to +8000 Hz.)

(b) Connect the multimeter, set to the 50 Vdc range, between board pin E7 (positive) and chassis (negative).

(c) Adjust L4 for a reading of +14V on the multimeter.

(d) Set the kHz portion of the receiver frequency to 000.00. (For A23A2, set the BFO frequency to – 8000 Hz.)

(e) Connect the multimeter, set to the 50 Vdc range, between TP7 (positive) and chassis (negative).

(f) Adjust L1 for a reading of +16V on the multimeter (for A23A2 +8V).

(g) Connect the HF voltmeter, 50 ohms input impedance, between board pin E1 and chassis (0V). Check that the level indicated is 225 mV rms plus or minus 2 dB, at kHz settings of 000.00, 500.00 and 990.00. (For A23A2, use 3 BFO settings of –8.00, ±0.00, and +8.00.)

(h) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate those indicated.

TP1: 1.013 to 1.020 MHz square wave, 3.5V p-p.
TP2: 4.6 to 3.6 MHz square wave, 3.5V p-p; 4 MHz ±80 kHz for A23.
TP3: 10.13 to 10.20 kpps, positive-going, 3.5V p-p.
TP4: 10.13 to 10.20 kpps strobe pulse, negative-going, 3.5V p-p.
TP5 & TP6: Phase comparator output pulse, positive-going and in phase, 3.5V p-p.

(i) Disconnect all test equipment.

1.3.6 Alignment Procedure, Transfer Loop Board, A13

Test Equipment Required: Oscilloscope, item 2 of Table 1-2.

There are no adjustments for this board. Use the oscilloscope, item 2 of Table 1-2, to monitor the test points listed below. Check that the signal levels displayed approximate those indicated.

TP1:	4.5 to 3.6 MHz square wave, 5V p-p.
TP2:	115 to 52 kHz square wave, 3.5V p-p.
TP3:	115 to 52 kpps, negative-going, 3.5V p-p.
TP4 and TP5:	115 to 52 kpps, 1.5 μs negative-going, and in phase 3.5V p-p.
TP6:	115 to 52 kpps strobe pulse, negative-going, 3.5V p-p.

1.3.7 Alignment Procedure, HF Loop Board, A14

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2; Oscilloscope, item 2; HP Voltmeter, item 3; and Digital Frequency Meter, item 7.

Procedure

(a) Set the receiver frequency to 29.99999 MHz.

(b) Connect the multimeter, set to the 50 Vdc range, between TP14 (positive) and chassis (negative).

(c) Connect the digital frequency meter between J5 and chassis (0V).

(d) Adjust L20 for a reading of 8V on the multimeter. Check that the digital frequency meter indicates 947.826 kHz plus or minus 10 Hz. Disconnect the digital frequency meter.

(e) Connect the multimeter, set to the 50 Vdc range, between TP3 (positive) and chassis (0V). Check that the multimeter indicates approximately 14V.

(f) Set the receiver frequency to 17.99999 MHz. Transfer the positive lead of the multimeter to TP2. Check that the multimeter indicates approximately 14V.

(g) Set the receiver frequency to 7.99999 MHz. Transfer the positive lead of the multimeter to TP1. Check that the multimeter indicates approximately 14V.

(h) Set the receiver frequency to 29.99999 MHz.

(i) Connect the HF voltmeter, high impedance input, between TP4 and chassis (0V).

(j) Adjust R38 for a reading of 1 V rms on the HF voltmeter.

(k) Rotate the frequency control across the full receiver range and check that the HF voltmeter indication is 1 V rms plus or minus 2.5 dB.

(l) Connect the HF voltmeter, high impedance input, between TP5 and chassis (0V). Check that the HF voltmeter indicates approximately 1 V rms.

(m) Connect the HF voltmeter, high impedance input, between J3 and chassis (0V).

(n) Adjust R44 for a reading of 310 mV rms plus or minus 0.5 dB on the HF voltmeter.

(o) Connect the 50 ohm termination to the LO output, (J3).

(p) Connect the multimeter, set to the 50 Vdc range, between TP13 and chassis (0V). Set the frequency to 7 MHz.

(q) Adjust L4 for a reading of 14V on the multimeter.

(r) Set the frequency to 17.99999 MHz.

(s) Adjust L5 for a reading of 14V on the multimeter.

(t) Set the frequency to 29.99999 MHz.

(u) Adjust L6 for a reading of 14V on the multimeter. Disconnect the multimeter.

(v) Connect the multimeter, set to the 10 Vdc range, between TP10 (positive) and chassis (0V). Check that the multimeter indicates approximately 3.5V. Disconnect the multimeter.

(w) Use the oscilloscope to monitor the test points listed below. Check that the signal levels displayed approximate those indicated below.

TP6:	442 to 474 kpps strobe pulses, negative-going, 3.5V p-p.
TP7 & TP8:	442 to 474 kpps phase comparator output pulses, negative-going and in phase, 3.5V p-p.
TP12:	885 to 948 kHz, approximate square wave, 2.8V p-p.

1.3.8 Alignment Procedure, 34 MHz Generator Board, A16

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2; Oscilloscope, item 2; HF Voltmeter, item 3; and Digital Frequency Meter, item 7.

Procedure

(a) Connect the oscilloscope to TP3. Check that a 1 MHz square wave is displayed, 2:3 on to off ratio, at a level of not less than 2V p-p.

(b) Connect the oscilloscope to J9. Check that the amplitude of the 1 MHz waveform displayed is approximately 0.5V p-p.

(c) Connect the oscilloscope to coaxial connector J14. Check that the amplitude to the 1 MHz waveform displayed is approximately 0.5V p-p.

(d) Connect the oscilloscope to TP9. Check that the amplitude of the 1 MHz square wave displayed exceeds 2V p-p.

(e) Set the receiver front panel MODE switch to USB.

(f) Connect the oscilloscope to coaxial connector J12.

(g) Adjust R65 to set the amplitude of the displayed 1.40185 MHz waveform to 0.8V p-p.

(h) Connect the digital frequency meter to coaxial connector J12. Check that the digital frequency meter indicates 1 401 850 Hz plus or minus 1 Hz. Disconnect the digital frequency meter.

(i) Connect the oscilloscope to coaxial connector J11. Check that the amplitude of the 1.4 MHz waveform displayed is 0.8V p-p.

(j) Connect the digital frequency meter to coaxial connector J11.

(k) On the receiver, set the MODE switch to CW.

(l) Connect the oscilloscope to TP15. Check that the amplitude of the waveform displayed is approximately 400 mV p-p.

(m) Connect the oscilloscope to coaxial connector J12. Check that the amplitude of the waveform displayed exceeds 0.5V p-p.

(n) Connect the oscilloscope to coaxial connector J11. Check that the amplitude of the Waveform displayed exceeds 0.5V p-p.

(o) Connect the digital frequency meter to J13.

(p) Connect the multimeter, set to the 10 Vdc range, to TP1 (positive) and chassis (0V).

(q) Adjust L2 for a multimeter indication of + 6V. Check that the digital frequency meter indicates 34 000 000 Hz. Disconnect the digital frequency meter.

(r) Disconnect all test equipment.

1.3.9 Typical Signal Levels, 34 MHz Generator Board, A16

Test Equipment Required: Oscilloscope, item 2 of Table 1-2; and HF Voltmeter, item 3.

Typical signal levels at the test points not already covered are listed below:

Test Points	Freq. MHz	Volts	Remarks
TP2	5.0	3.0 p-p	Measured with oscilloscope
TP4	34.0	.75 rms	Measured with HF VM
TP5	34.0	.4 rms	Measured with HF VM
TP6	34.0	1.4 rms	Measured with HF VM
TP8	4.0	3.0 p-p	Square wave, unsymmetrical
TP11	1.0	3.5 p-p	Square wave, .6 duty cycle
TP12	1.0	3.5 p-p	Square wave, .6 duty cycle
TP14	1.0	3.5 p-p	Negative-going pulses

1.3.10 100 kHz IF Converter, A25

No adjustments are required on the 100 kHz IF converter. However, the following test should be performed to insure proper operation.

Test Equipment Required: Spectrum Analyzer, Item 4 of Table 1-2, Digital Frequency Meter, Item 7, and Signal Generator Item 8.

Procedure

(a) Disconnect IF output from the IF module, A5 (P7A2).

(b) By means of a suitable adapter, connect a cable from the output of the signal generator, item 8, to the cable disconnect at step a.

(c) Connect the analyzer to the 100 kHz IF output on the rear panel of the receiver.

(d) Set the signal generator frequency to 1.4 MHz and the output level to −10 dBm.

(e) Tune the signal generator for maximum output as indicated on the analyzer. Ensure that the output level is greater than −6 dBm on the analyzer.

(f) Set the signal generator frequency to exactly 1 400 000 Hz.

(g) Connect the frequency meter to measure the IF output frequency. Ensure that this is 100 kHz ±1 Hz, and that the output level is still greater than −6 dBm.

1.3.11 Alignment Procedure, IF Board, A5

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2; HF Voltmeter, item 3; Distortion Analyzer, item 4; Spectrum Analyzer/Tracking Generator, item 5; High Impedance Probe, item 6; Digital Frequency Meter, item 7; Signal Generator, item 8; and 50-ohm terminating coupler, item 10.

Procedure

(a) Disconnect the output plug from the A4 module at A4J1-A3. Connect the tracking generator output to coaxial connector A4J1-A3 using BNC adapter and 50-ohm coupler.

(b) Connect the spectrum analyzer RF input to P29A1 on A25 module.

(c) Set the tracking generator/spectrum analyzer controls as follows:

Center Frequency	1.4000 MHz
Sweep Width	20 kHz/div.
Bandwidth	3 kHz/div.
Output Level	−70 dBm
Input Attenuation	10 dB
Log Ref. Level	− 0 dBm

(d) Set R3, R7 and R95 fully counterclockwise.

(e) Set the AGC to SHORT (SH).

(f) Observe the analyzer trace. Adjust L1 and L2 to obtain the bandpass waveform defined below, adjusting the manual gain control as required.

(g) Set the spectrum analyzer tracking generator for zero scan width at 1.4000 MHz with an output level of −68 dBm.

(h) Connect the HF voltmeter, using the high impedance probe, to A5TP3.

(i) Adjust R3 on the A5 board for an indicated output of 200 +20/−0 mV.

(j) Connect the digital multimeter between A5TP6 and ground.

(k) Adjust R7 for a multimeter reading of 1.40 ±.05V. Ensure that the HF voltmeter still indicates 200 +20/−0 mV.

(l) Increase the tracking generator output by 6 dB (−62 dBm). Adjust R95 for a multimeter reading of 1.56 ±0.01V.

(m) Decrease the tracking generator output by 6 dB to –68 dBm. Ensure that multimeter reading falls back to 1.40 ±0.05V.

(n) Increase the tracking generator output level by 50 dB to –18 dBm. Ensure that output at the HF voltmeter does not increase by more than 3 dB.

(o) Ensure that the digital multimeter reading stays within limits of 2 to 3 volts.

(p) Disconnect all test equipment.

(q) Connect the distortion analyzer, with the FUNCTION control set to VOLTMETER, across the rear panel AF Line terminal on TB1, with a 600-ohm resistive load.

(r) Set the receiver AGC to SHORT (SH) and MODE to USB.

(s) Connect the signal generator to the A5 IF input using the BNC adapter and 50-ohm coupler.

(t) Set the signal generator to 1.4000 MHz CW output at a level of –48 dBm.

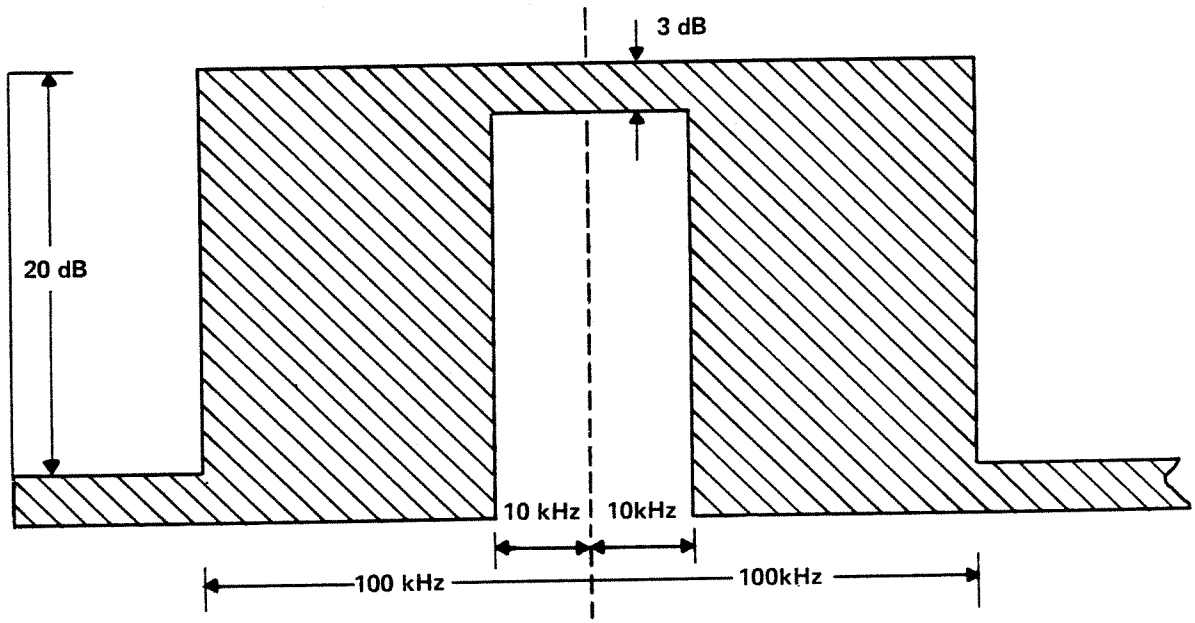
(u) Adjust AF LEVEL preset control for 1 mW output. (780 mV in 600 ohms.)

(v) Set receiver FILTER switch to 8 and MODE to AM.

(w) Set signal generator to 30% AM. Adjust R56 for an AF output of 1 mW.

(x) Connect distortion analyzer to PHONES output at receiver front panel.

(y) Set AF GAIN control on front panel to maximum. Ensure that output indicated by the analyzer is at least 20 mW.



1.3.12 Typical Signal Levels, IF Module, A5

Test Equipment Required: HF Voltmeter, item 3 of Table 1-2; Distortion Analyzer, item 4; and Signal Generator, item 8.

Procedure

(a) Signal generator output level –68 dBm connected to A5 IF input, using BNC adapter and 50 ohm terminating coupler.

(b) Set receiver MODE to USB.

(c) Measure at the following test points using HF voltmeter with high impedance probe. TP5: 1.4mV; TP2: 90mV; TP3: 200mV; TP4: between 90mV and 130mV.

(d) Measure the following using distortion analyzer as voltmeter, high input impedance. TP7; between 50 and 90mV; Pins 8 and 9 (Ground on 9): not less than 150mV.

1.3.13 Alignment Procedure, Filter Assembly, A4

There are no adjustments to be made to the filter board. However, the procedures which follow provide checks upon the filter characteristics. Since the filters are sealed units, any filter that fails to meet performance figures should be replaced. Six crystal filters are included on the board, as shown in the following table:

FL1	150 Hz
FL2	250 Hz
FL3	400 Hz
FL4	750 Hz
FL5	1.25 kHz
FL6	3.2 kHz

Test Equipment Required: HF Voltmeter, item 3 of Table 1-2; digital Frequency Meter, item 7; and Signal, item 8.

Procedure

Symmetrical Filters

(a) Remove the coaxial connector from the chassis-mounted second mixer output connector (right-hand front, see Figure 6-1 and 6-4.)

(b) Connect the output of the signal generator to the filter board input via the coaxial connector disconnected at step (a).

(c) Connect the digital frequency meter to the UNCAL output connector on the signal generator.

(d) Connect the HF voltmeter, 50 ohm input impedance, to the IF OUT jack on the rear panel.

(e) Set the receiver front panel controls as follows:

MODE	AM	AGC	OFF
FILTER	Widest (8 kHz)		

(f) Set the signal generator frequency to 1.4 MHz and the output level to 150 μV rms.

(g) From the following paragraphs, perform the tests that are applicable to the symmetrical filters, setting the FILTER switch to the appropriate bandwidth in each case.

150 Hz Symmetrical Filter

(a) Tune the signal generator for maximum output, as indicated on the HF voltmeter. Ensure that the output level is greater than 50 mV rms.

(b) Set the RF GAIN control for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1 399 925 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 400 075 Hz.

250 Hz Symmetrical Filter

(a) Tune the signal generator for maximum output, as indicated on the HF voltmeter. Ensure that the output level is greater than 50 mV rms with the RF GAIN control on the receiver fully clockwise.

(b) Set the RF GAIN control on the receiver for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1 399 875 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 400 125 Hz.

425 Symmetrical Filter

(a) Tune the signal generator for maximum output, as indicated on the HF voltmeter. Ensure that the output level is greater than 50 mV rms with the IF GAIN control on the receiver fully clockwise.

(b) Set the RF GAIN control for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1 399 787 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 400 213 Hz.

750 kHz Filter

(a) Tune the signal generator for a maximum output, as indicated on the HF voltmeter. Ensure that the output level is greater than 50mV rms.

(b) Set the RF GAIN control for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1 399 625 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 400 375 Hz.

1.25 kHz Symmetrical Filter

(a) Tune the signal generator for maximum output, as indicated on the HF voltmeter.

(b) Set the RF GAIN control for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1 399 375 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below the 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1 400 625 Hz.

3.2 kHz Symmetrical

(a) Tune the signal generator for a maximum output, as indicated on the HF voltmeter. Ensure that the output level is greater than 50 mV rms.

(b) Set the RF GAIN control for an indication of 50 mV on the HF voltmeter.

(c) Decrease the signal generator frequency until the output falls 3 dB below 50 mV level. Ensure that the frequency indicated on the digital frequency meter is less than 1.398400 Hz.

(d) Increase the signal generator frequency until the output falls 3 dB below 50 mV level. Ensure that the frequency indicated on the digital frequency meter is greater than 1.401600 Hz.

1.3.14 Alignment Procedure, Second Mixer Board, A3

Test Equipment Required: Digital Multimeter, item 1 of Table 1-2; Spectrum Analyzer/ Tracking Generator, item 5; High Impedance Probe, item 6; Signal Generator, item 8..

Procedure

(a) Set R9 fully counter clockwise.

(b) Disconnect P5 from J11 (Main Chassis Top Side).

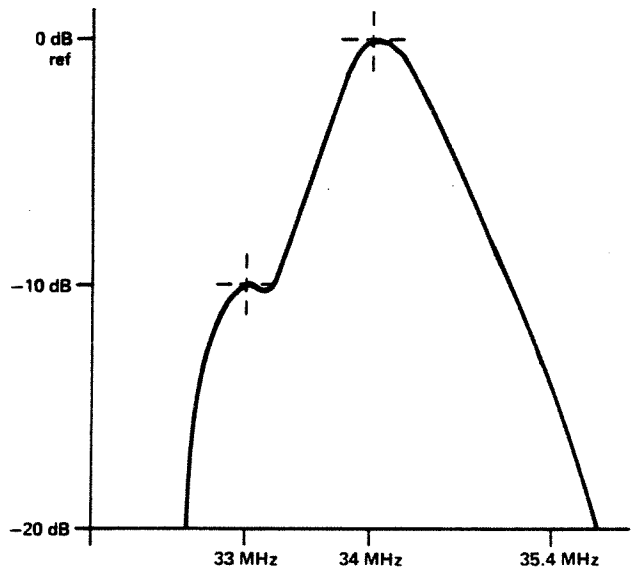
(c) Connect the output of the tracking generator to A3J2.

(d) Connect the high impedance probe between LINK 2 and TP2. (Note: TP2 is low potential terminal for 34 MHz drive, but is NOT receiver ground.)

(e) Set tracking generator/spectrum analyzer as follows:

Center Frequency	34.00000 MHz
Output Level	+10 dBm
Sweep Width	0.5 MHz/div.
Bandwidth	30 kHz
Input Attenuation	10 dB
Log Ref. Level	0 dBm
Scale	10 dB/div

(f) Observe trace and adjust L10, L12, L13, L14 to obtain the response characteristic shown below.



NOTE

The response may have two peaks – the upper frequency peak should be set at 34.000 MHz, the lower at about 33 MHz.

(g) Disconnect test equipment. Reconnect the 34 MHz input from A16 (P1 to A3J2).

(h) Connect HF voltmeter using its high impedance probe to LINK 2 and TP 2 (Low Potential). Ensure that the level indicated is greater than 0.3 volts. Remove HF voltmeter.

(i) Connect the digital multimeter between ground and TP4. Adjust R8 for an indication of 1.0 ±.01 volts. Remove multimeter.

(j) Connect the high impedance probe, item 14, to LINK 1 and TP2 (Low Potential).

(k) Connect the tracking generator output to 35.4 MHz input of A3, (A3W1P1).

(l) Set the tracking generator/spectrum analyzer as follows:

Output Level	−10 dBm
Center Frequency	35.4000 MHz
Sweep Width	0.5 MHz/div.
Bandwidth	30 kHz
Input Attenuation	10 dB
Log Ref. Level	0 dBm
Scale	10 dB/div.

(m) Observe trace and adjust L1, L6, L7, L8, L9, L11 to obtain the maximum response at 35.4 MHz with good symmetry at ±1 MHz. Ensure that output level indicated by the analyzer is greater than −4 dBm.

(n) Disconnect the tracking generator, and replace with the signal generator set to 35.400000 MHz CW and output level −63 dBm.

(o) Set the analyzer to zero sweep width at 1.4000 MHz.

(p) Connect the analyzer high impedance probe to E3 and ground.

(q) Adjust L15 for maximum output.

(r) Ensure that the level indicated by the analyzer is greater than −12 dBm.

(s) Adjust R9 so that the level indicated by the analyzer is −25 dBm.

(t) Remove all test equipment.

1.3.15 Typical Signal Levels, Second Mixer Module, A3

Test Equipment Required: Same as paragraph 1.3.14

For an input level of –60 dBm, the levels indicated below should be present. Due to the high levels of local oscillation present it is necessary to use a selective voltmeter. The spectrum analyzer with the high impedance probe makes an excellent measuring device, but indications will have to be converted from the dBm 50-ohm reading to true voltage.

Input	–63 dBm
TP5	–45 dBm
TP1	–44 dBm
LINK 1	–51 dBm
TP3	–25 dBm
Output	–25 dBm

1.3.16 Alignment Procedure, First Mixer Module, A2

Test Equipment Required: HF Voltmeter, item 3 on Table 1-2; Spectrum Analyzer/Tracking Generator, item 5; High Impedance Probe, item 6; and Signal Generator, item 8.

Procedure

(a) Remove the local oscillator input to J1 of A2.

(b) Connect the tracking generator to the LO input.

(c) Connect the spectrum analyzer via the high impedance probe to TP5 of A2. Set analyzer controls as listed below:

Center; Past Center	Auto
Vertical Scale Range	10 dB/Div
Vertical Scale	-30 dBm
Horizontal Range	MHz/Div
Horizontal Scale	2 MHz/Div
Filter B.W.	1 or 2
Counter Readout	29.8

(d) Turn POWER to ON.

(e) Set the receiver front panel controls as follows:

Frequency	15.0000 MHz
MODE	CW
AGC	SHORT

(f) Adjust coil L4 of A2 to provide a notch (minimum amplitude) to 20.2 MHz while observing the spectrum analyzer output response trace.

(g) Adjust coil L7 to provide a notch at 30.7 MHz

(h) Adjust coil L5 to provide a notch at 34.3 MHz.

(i) Adjust coil L6 to provide a notch at 35.4 MHz.

(j) Check the output passband for less than 2 dB ripple between 37 and 67 MHz.

(k) Check for not less than 40 dB attenuation below passband for frequencies lower than 35.4 MHz.

(l) Set receiver to 1.5 MHz.

(m) Tune analyzer to 35.4 MHz.

(n) Tune T1, L8, and T2 for a response similar to that shown in Figure 3-6 of Test Fixture Alignment Procedure.

(o) Disconnect the tracking generator from the LO input, and reconnect the normal input from the local oscillator.

(p) Remove P1 from the chassis.

(q) Connect the tracking generator to P1.

(r) Connect the analyzer, using a suitable adapter to the J4 socket, having disconnected the mixer.

(s) Set the tracking generator/analyzer controls as follows:

Output Level	0 dBm
Bandwidth	100 kHz
Scan Width	2 MHz/div.
Input Attenuator	−10 dB
Scan Tune	10 ms
Log Ref. Level	+10 dBm

(t) Set tracking generator to SCAN HOLD and adjust the analyzer center frequency to 56.710 ±0.05 MHz. Adjust L20 for minimum level.

(u) Set tracking generator to MARKER and ensure that a notch is shown on the display.

(v) Set tracking generator to SCAN HOLD and set center frequency to 86.68 ±0.05 MHz. Adjust L19 for minimum level as shown on the analyzer display.

(w) Reset analyzer center frequency to 56.710 ±0.05 MHz and readjust as necessary. Set tracking generator to Marker.

(x) Set analyzer to sweep 0-100 MHz. Check that all frequencies above 56 MHz are better than 37 dB down, from a reference level at 30 MHz.

(y) Set analyzer to 2 dB Log response and adjust the analyzer to display the passband response. Ensure that peak-to-peak ripple from 1 MHz to 30 MHz is less than 1 dB.

(z) Reconnect P1 cable to chassis.

(aa) Connect tracking generator to A2U1P1.

(ab) Connect HI impedance probe to E7.

(ac) Observe trace and adjust L21 for best flat response over middle 3.2 kHz. Ensure that ripple is less than 1 dB for ±1.5 kHz.

(ad) Adjust T5 for maximum output at 35.4 MHz. Ensure that the 3 dB bandwidth is greater than 8 kHz.

(ae) Reconnect A2U1P1 to J4.

(af) Set the receiver frequency to 2.00000 MHz.

(ag) Connect the output of the signal generator to the chassis-mounted first mixer input J10 BNC connector. Set the signal generator frequency to 2.000 MHz and output level to 1 mV rms.

(ah) Connect the HF voltmeter with the 50 ohms input impedance adapter, to the IF OUT connector, J5, on the rear panel.

(ai) Tune the signal generator for maximum output, as indicated on the HF voltmeter. Ensure that the output level is not less than 50 mV rms.

(aj) Set the receiver frequency to 3.99900 MHz.

(ak) Set the signal generator frequency to 4 MHz.

(al) Tune the signal generator for maximum output, as indicated on the HF voltmeter. Ensure that the output level is not less than 50 mV rms.

(am) Set the receiver frequency to 4.00000 MHz.

(an) Tune the signal generator for maximum output. Ensure that the output level is not less than 50 mV rms.

(ao) Set the receiver frequency to 29.9 MHz.

(ap) Set the signal generator frequency to 29.9 MHz.

(aq) Tune the signal generator for maximum output. Ensure that the output level is not less than 50 mV rms.

(ar) Set the receiver POWER switch to off.

1.3.17 Alignment Procedure, RF Amplifier, A1

Test Equipment Required: Spectrum Analyzer and Tracking Generator, item 6 of Table 1-2.

Procedure

Refer to procedure for A1 test fixture, page 2-2.

1.4 PARTS LIST

Table 1-3 lists all modules and replaceable electrical parts contained on the main chassis of the RA6778C Receiver. The modules and parts are listed in order of reference designation. Where Table references are included under the description column refer to the chapter of the prefixed Table number for further breakdown of the module or circuit card. That is, Table 6-2 would be found in Chapter 6 and will provide a complete parts list for that particular circuit card. Illustrations are also included in each chapter showing location of parts.

1.5 CHASSIS WIRING DIAGRAM

Figure 1-4 is the receiver chassis wiring diagram showing all interconnections between the modules and connectors. Figure 1-5 is the logic wiring diagram.

TABLE 1-3. PARTS LIST, RA6778C RECEIVER, MAIN CHASSIS COMPONENTS

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A1	RF Amplifier Module Assembly (See Table 2-2 for further breakdown)	06894-3	
A2	First Mixer Circuit Card Assembly (See Table 3-2 for further breakdown)	07215-4	
A3	Second Mixer Circuit Card Assembly (See Table 4-2 for further breakdown)	06896-2	
A4	IF Filter Module Assembly (See Table 5-3 for further breakdown)	08337	
A5	IF Amplifier Module Assembly (See Table 6-2 for further breakdown)	08339	
A6	Microcomputer Module Assembly (See Table 7-5 for further breakdown)	08686	
A6A1	Asynchronous Interface Circuit Card Assembly (See Table 7-6 for further breakdown)	08373	
A6A2	Microprocessor Circuit Card Assembly (See Table 7-7 for further breakdown)	09042	
A7	Panel Board Module Assembly (See Table 8-3 for further breakdown)	08698-1	
A7A1	Front Panel Circuit Card Assembly (See Table 8-4 for further breakdown)	08343-1	
A7A2	Front Panel Switch Circuit Card Assembly (See Table 8-5 for further breakdown)	08681-1	
A8	Receiver Latch Circuit Card Assembly (See Table 9-3 for further breakdown)	08356-1	
A11	Upper/Lower Loop Synthesizer Module Assembly (See Table 10-3 for further breakdown)	06903-1	
A13	Transfer Loop Circuit Card Assembly (See Table 11-5 for further breakdown)	06904	
A14	HF Loop Circuit Card Assembly (See Table 12-6 for further breakdown)	06905	
A15	Frequency Standard Module Assembly (See Table 13-2 for further breakdown)	06906-4	
A16	34 MHz Generator Circuit Card Assembly (See Table 14-2 for further breakdown)	08744-1	
A18	Power Supply Module Assembly (See Table 15-3 for further breakdown)	06909-2	

TABLE 1-3. PARTS LIST, RA6778C RECEIVER, MAIN CHASSIS COMPONENTS (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A23	BFO Synthesizer Module Assembly (See Table 16-3 for further breakdown)	06913	
A25	100 kHz IF Converter Module Assembly (See Table 17-2 for further breakdown)	08344	
C1-6, 11	Not Used		
C7-10, 12-17	Capacitor, Feed-through, 1000 pF, +20% (AVX)	26406	BSF-1BBGP102M
J1	Connector, Coaxial BNC	60056	UG492A/U
J2	Connector, Digital I/O	61279	MS83723-O1R-1419N
J3	Connector, Antenna Select	61094	MS83723-01R-1210-N
J4	Connector, Auxilliary Select	61277	MS83723-01R-1006N
J5, 6	Connector, BNC, IF Output	60046	KC19-110
J7, 8	Connector, BNC, 1 MHz Reference	60002	051-075-0000
J9	Not Used		
J10, 11	Connector, SMB-SMB Bulkhead	60057	
J12	Connector, MA-9P Plug	61165	DEMA-9P
J13	Connector	61300	DC 37 Pin
J14, 15	Connector, Phone Jack	61502	JJ-034
LS1	Loudspeaker, 16 ohms, 1.5 watts (Quom)	42759	25A07Z16
P6	Connector, P/0 Main Harness (Cannon)	61172	DBM-13W3S
P28	Connector, P/0 Main Harness (Cannon)	61166	DEMA-9S
Q1, 2	Transistor, Darlington, PNP	32520	MJE-700-PNP
Q3	Transistor, Darlington, NPN	32519	MJE-800-NPN
R1	Potentiometer, Variable, 1K ohms, 1/3W	08764	
R2	Potentiometer, Variable, 10K ohms, 1/3W	08763	
R3	Potentiometer, Variable, 10K ohms, 1/3W	08765	
S1	Switch, DPDT, Continental slide	52425	GF326
S2	Switch, DPDT (Alco)	50019	MSTG225N

TABLE 1-3. PARTS LIST, RA6778C RECEIVER, MAIN CHASSIS COMPONENTS (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
TB1	Terminal, AF line out (Cinch)	70337	8-164-Y
W1	Cable, 1st L.O. A2-A14	07042-1	
W2	Cable, Transfer Oscillator, A13-A14	07042-2	
W3	Cable, Varactor, A13-A14	07042-3	
W4	Cable, 1 MHz, A13-A16	07042-4	
W5	Cable, 34 MHz, A16-A3	07042-5	
W6	Cable, Ribbon, Front Panel Latch	08620	
W7	Cable, Ribbon, Latch-Microcomputer	08622	
W8	Cable, Ribbon, A6-Connector Mounting	08619	
W9	Cable, Power Cable In, Mates A18J1	57023	17258-B
W10	Cable, Power Cable, Mates A18J2	07130	

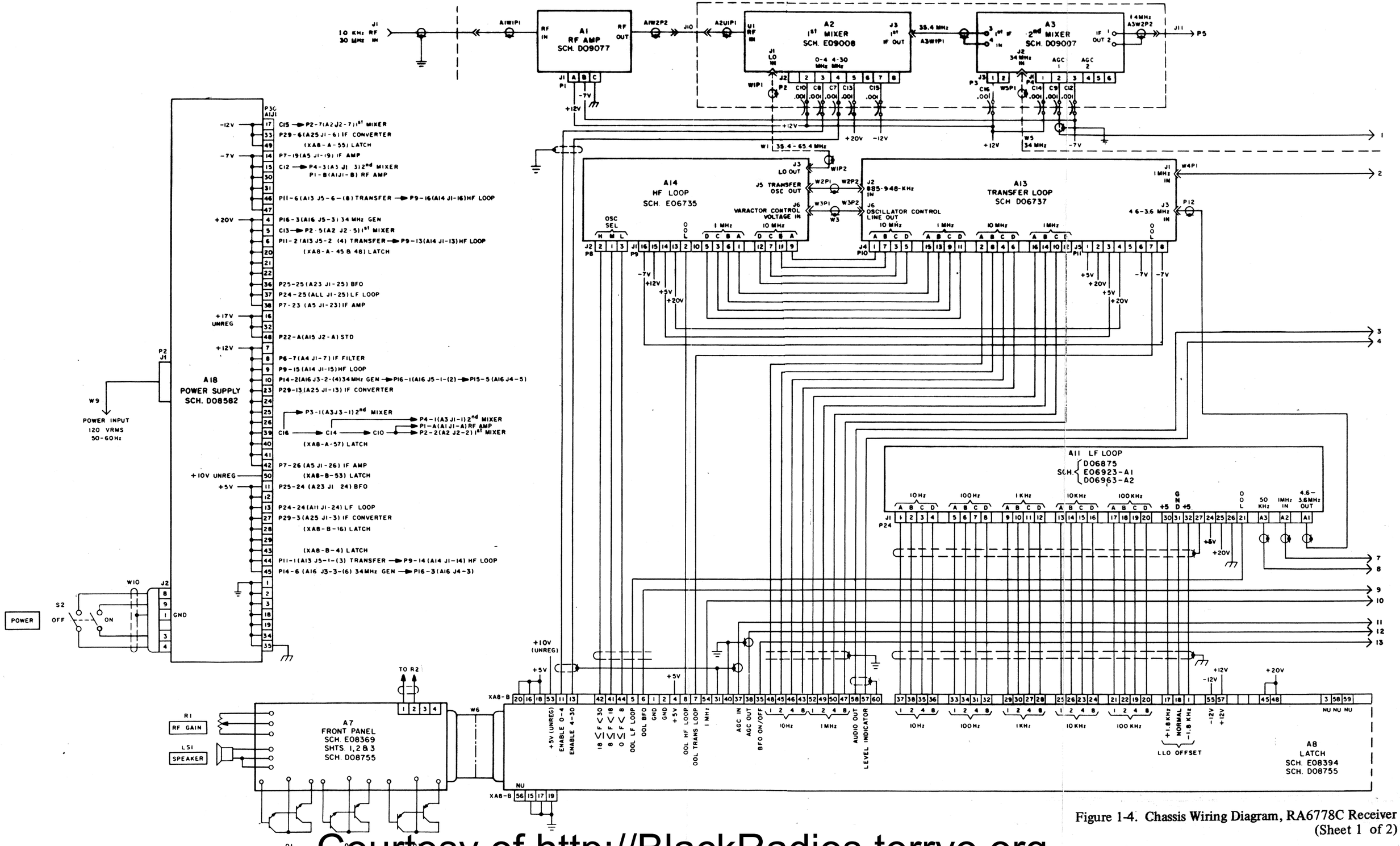


Figure 1-4. Chassis Wiring Diagram, RA6778C Receiver (Sheet 1 of 2)

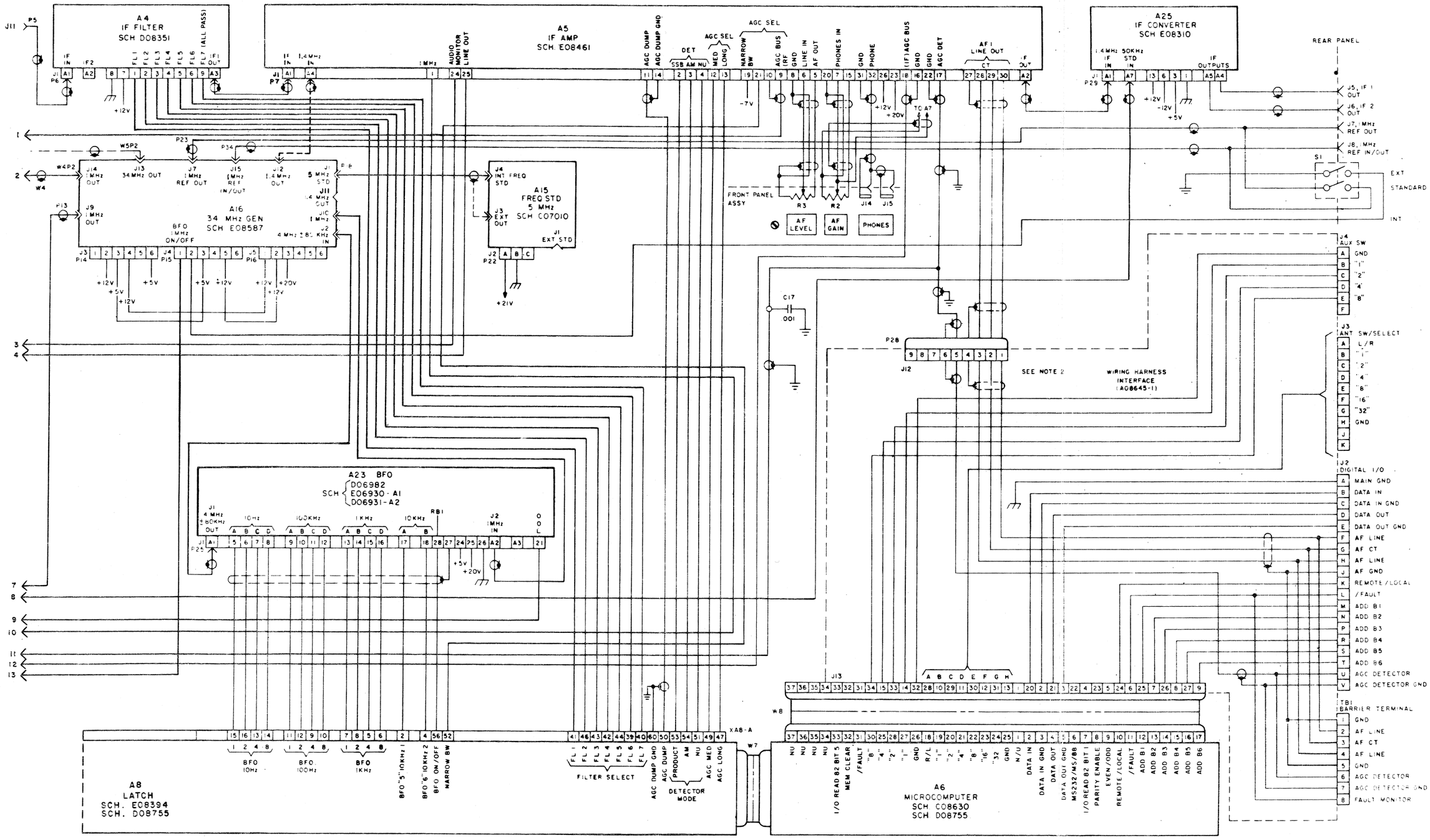


Figure 1-4. Chassis Wiring Diagram, RA6778C Receiver (Sheet 2 of 2)

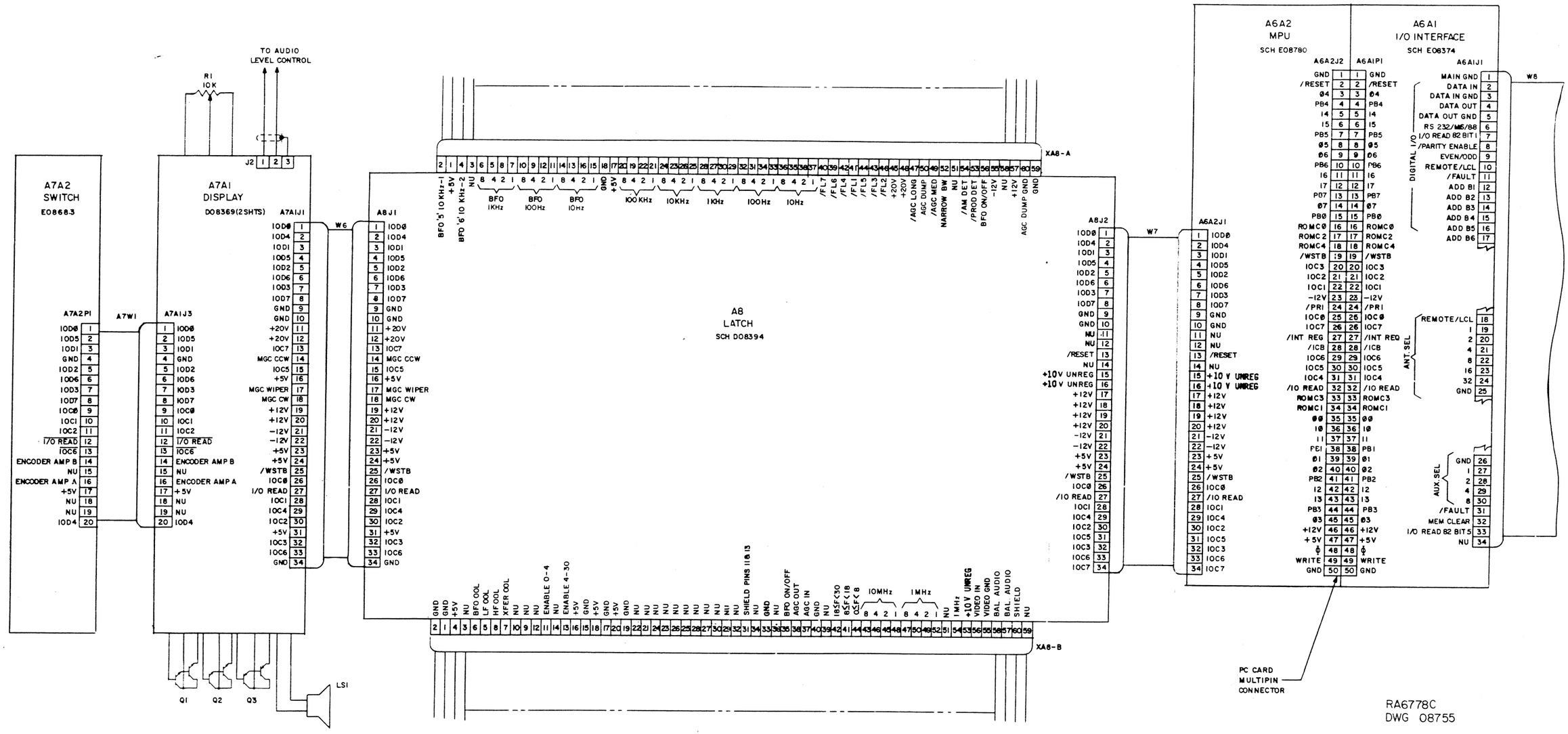


Figure 1-5. Logic Wiring Diagram, RA6778C Receiver

CHAPTER 2
RF AMPLIFIER, A1

2.1 THEORY OF OPERATION

The RF amplifier module, A1, receives the RF input signal to the receiver through the rear panel RF IN connector J1. This module contains an input filter, an RF amplifier and an output filter. Figure 2-1 is a schematic diagram of the RF Amplifier A1.

The input, through terminal E1, to the module is first applied to a two-section elliptical low-pass filter which has a cut-off frequency of 35 MHz and characteristic impedance of 50 ohms. The two inductors (L1-L2) are adjustable by means of a threaded core. The filtered output is then applied to a wideband amplifier consisting of two transistors, Q1 and Q2, connected in a circuit where both current and voltage feedback are used to closely control terminal impedance at 50 ohms, gain at 10 dB, and distortion. Protection of the transistors is provided by biased back-to-back diodes CR1 and CR2. The output of the amplifier is applied to a 3 dB pad which serves to define the impedance of the following 5 section elliptical low-pass filter. This filter has a cut off frequency of 32 MHz and is designed to reject signals at 35.4 MHz which would otherwise pass through the first mixer to the first IF. It also rejects signals at image frequencies (receiver tuned frequency +2 x 35.4 MHz) and eliminates first local oscillator conductance back to the antenna. The five inductors (L9-L13) are also adjustable.

2.2 RF AMPLIFIER, A1, TEST FIXTURE

Troubleshooting and alignment of the RF amplifier module, A1, is accomplished through the use of the RACAL RF amplifier (A1) test fixture and associated test equipment. The test fixture provides a base for holding the module and applies power to the module via a plug on the test fixture. The test equipment connects to the module under test via BNC adapters located on the test fixture. The RF amplifier module input is swept from 1.6 MHz through approximately 35 MHz to test and, if required, align the module for proper output waveform.

Figure 2-2 shows the RACAL RF amplifier A1 test fixture. Figure 2-3A shows the RF amplifier module A1 overall assembly. Figure 2-3B shows the module circuit card assembly and illustrates the location of the components.

2.3 TEST EQUIPMENT AND ACCESSORIES

Table 2-1 lists the test equipment and accessories required.

Table 2-1. List of Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	Spectrum Analyzer	Marconi Type TF2370
2	Power Supply	Racal
3	Test Fixture (A1)	Racal TF330/333/346
4	Zero Loss High Impedance Probe	Marconi TK2374
5	Adapter	Coaxial BNC to probe/clip head
6	Tuning Tool	Micrometals (RCI82007)

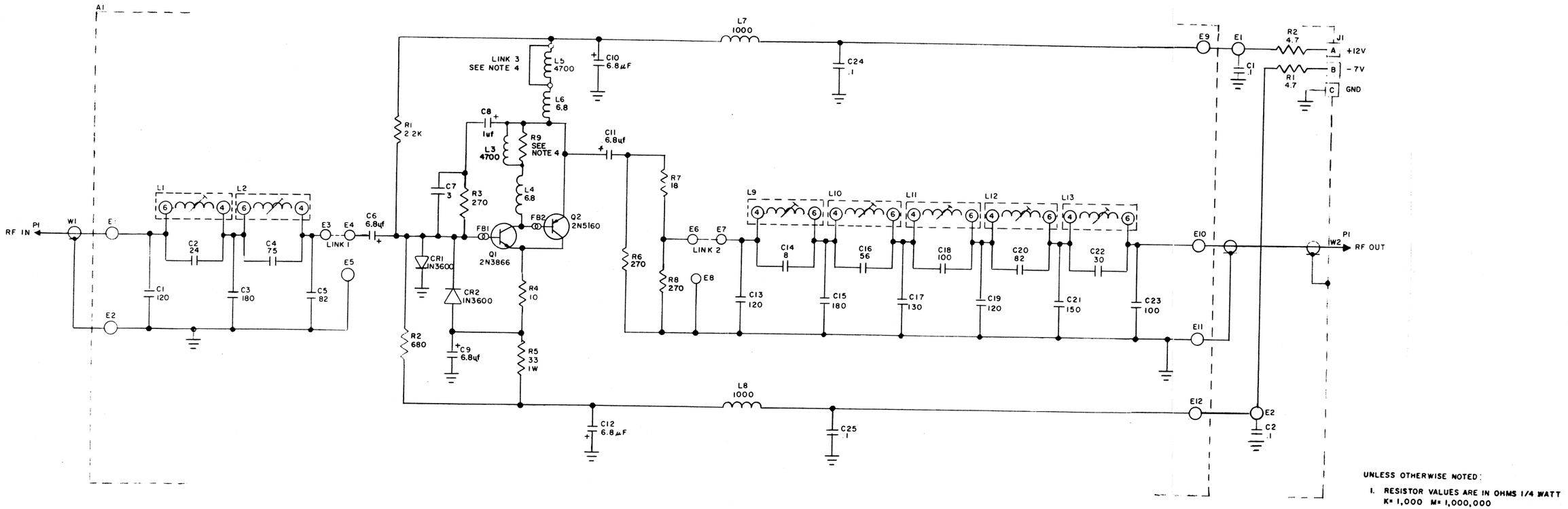
2.4 TEST AND ALIGNMENT

Tests should be conducted at room temperature. Record test results on test data sheet, Page 2-12.

The following procedures are to be used to verify satisfactory performance of the RF amplifier, A1 module.

2.4.1 Preliminary Set-Up Process

1. Install the RF amplifier board under test (B.U.T.) on the A1 test fixture.
2. Connect the power supply to the test fixture via the octal plug located on the rear apron of the test fixture. Make all required connections between test fixture and B.U.T.
3. Turn power on to the test fixture.
4. Connect the Zero Loss Hi Impedance probe with the special adapter (item 5 of Table 2-1) to pin E3 on the B.U.T. It has been found in practice that a long ground lead for the HI Z probe raises the 'grass' level to a point where the notch becomes masked. It may be necessary to remove the special adapter (item 5 in Table 2-1) and ground the probe directly to some convenient point such as a coil can.
5. Connect the TRACKING GEN OUT of the Spectrum Analyzer to the RF IN port on the test fixture. It is <u>essential</u> to use short 50 ohm coaxial cables.



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K= 1,000 M= 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.
4. R9, LINK 3 NOT FITTED.

Figure 2-1. Schematic Diagram, RF Amplifier, A1

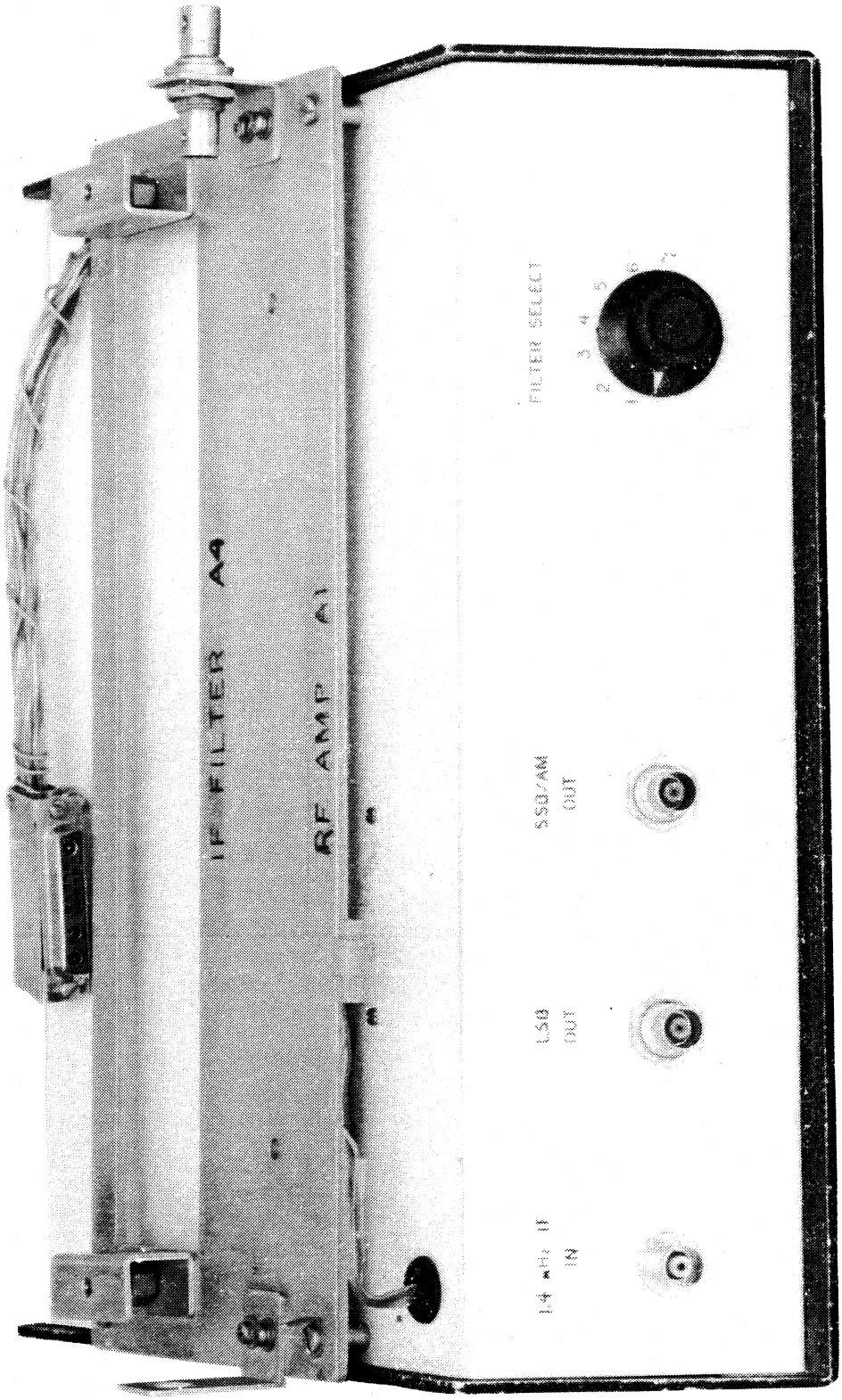


Figure 2-2. RF Amplifier A1, Test Fixture

6. Set the controls on the Spectrum Analyzer as follows:

Reference Frequency	Center
Counter Frequency	Past Center
Sweep Mode	Auto
Counter On	On
Supply On	On
Vertical Scale Range	1 dB/div
Graticle (red lights)	Out
Store	Refresh A
Display	A
Peak Mem	Not selected
Verticle Scale	−20 dBm
Add	0 dB(yellow lamp out)
Horizontal Scale	2
Horizontal Range	MHz/div
Filter Bandwidth	2 (normal)
Sweep Speed	None selected

Note 1: When adjusting the coil slugs (if required) in the next sections exercise EXTREME CAUTION as these slugs are easily damaged by excessive torque during rotation. NOTE 2: Refer to Figure 2-3B for parts location on the RF Amplifier Module.

2.4.2 Input Filter Test and Alignment Process

1. Adjust the REFERENCE FREQUENCY controls on the spectrum analyzer to obtain 46.43 ±0.1 MHz displayed on the counter.

2. Carefully adjust coil L2 (upper-right corner) on the RF Amplifier B.U.T. to obtain a minimum display on the analyzer screen. It will be necessary to change the Vertical Scale setting from −20 dBm to −90 dBm in increments as the null is reached. Record the level on test data sheet.

3. Adjust the REFERENCE FREQUENCY controls on the spectrum analyzer to obtain 66.67 ± 0.1 MHz on the counter display. Readjust, if necessary, vertical scales of spectrum analyzer to observe waveform.

4. Adjust coil L1 (lower-right corner) on B.U.T. to obtain a null on the spectrum analyzer as before. Proceed in the same manner as step 2 above. Record the null level in dB on test data sheet.

5. Once L1 and L2 are aligned it is preferable not to adjust these coils further for the remainder of this procedure.

2.4.3 30 MHz Low Pass Filter Alignment Process (1.5 MHz - 30 MHz)

1. Remove the Zero Loss Hi Impedance probe and the special adapter from both the spectrum analyzer and the test fixture.

2. Connect a BNC-BNC coaxial cable from the RF OUT port on the test fixture to the 50 ohms INPUT port on the spectrum analyzer. It is essential to use short 50 ohms coaxial cables.

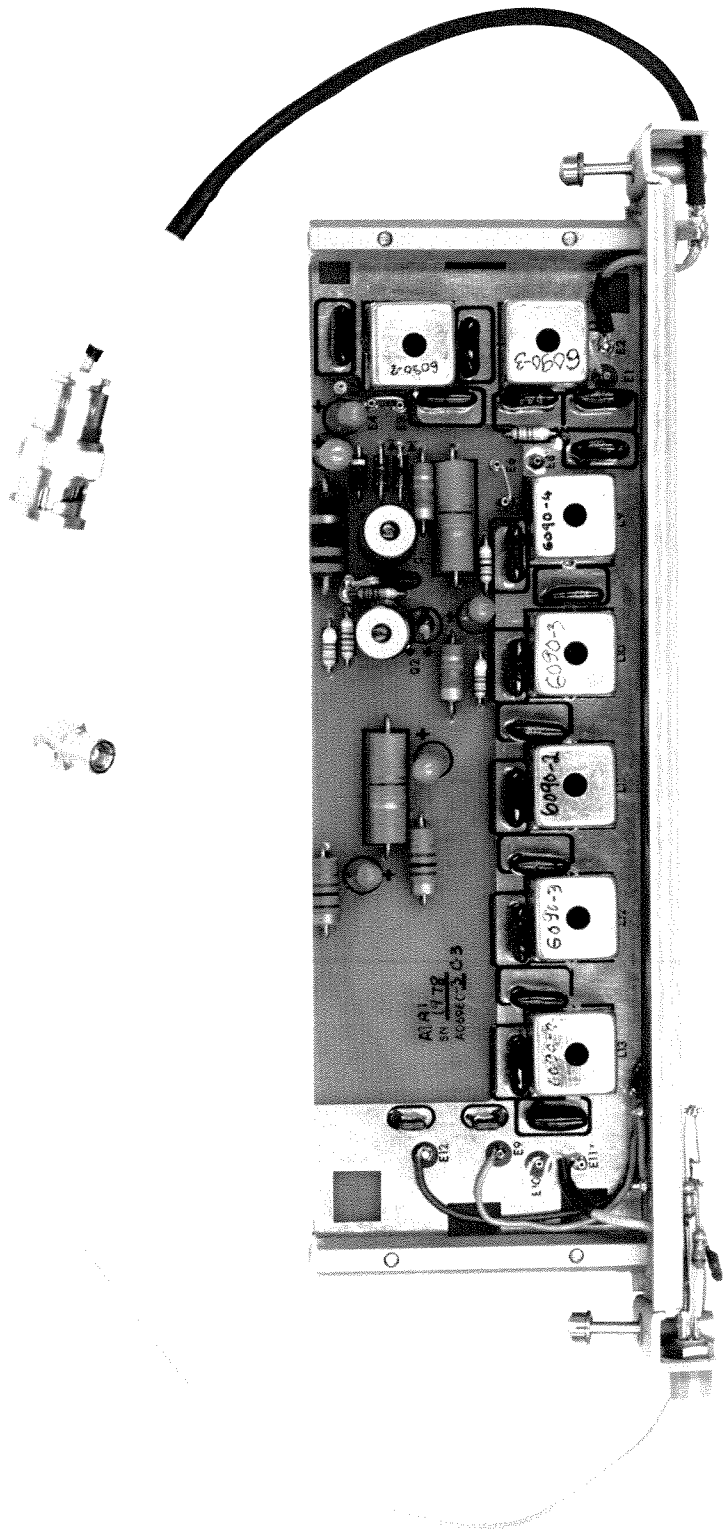


Figure 2-3A. RF Amplifier A1, Overall Assembly

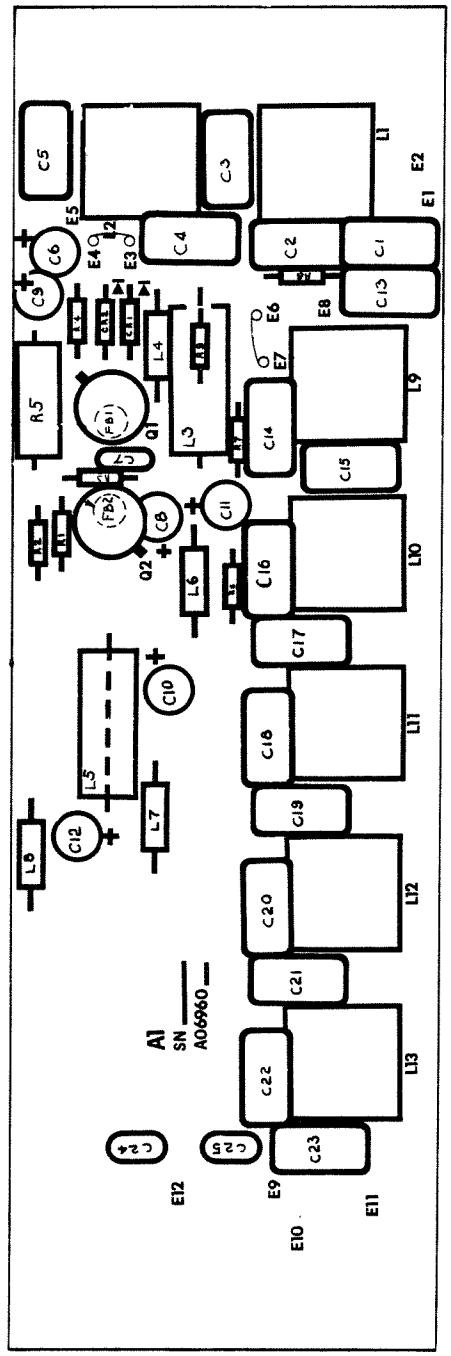


Figure 2-3B RF Amplifier A1, Circuit Card Assembly

3. Set the controls of the spectrum analyzer as follows:

Vertical Scale Range	1 dB/div
Vertical Scale	0 dBm (ref. blue light)
Reference Frequency	L H
Horizontal Scale	5
Horizontal Range	MHz/div
Reference Frequency	25.7 MHz ±0.1 MHz

4. The spectrum analyzer screen should have a 'marker' exactly one (1) division in from the left hand side of the screen. This is the 0 'marker' or 0 MHz. Therefore, every consecutive division to the right of this line is 5 MHz greater than the previous division.

5. You are now ready to test and to align (if required) the filter for optimum performance. Read the following subsections carefully first before attempting alignment. If difficulty is experienced in achieving the rejection at 35.4 MHz while maintaining the response at 30 MHz, it may be necessary to make small adjustments to L1 and L2.

   5.1 Disconnect BNC coaxial cable from RF OUT port of test fixture and connect it to OUTPUT 50 ohms of TRACKING GEN of Spectrum Analyzer. You should have connection between INPUT 50 ohms and OUTPUT 50 ohms of Spectrum Analyzer.

   5.2 Observe the ground level of signal on the spectrum analyzer. Adjust vertical scales (ADD), if necessary, to place the level at bottom of screen. Note the level in dB. This is the reference ground level.

   5.3 Re-make the connections between; INPUT 50 ohm of spectrum analyzer and RF OUT port of test fixture, and OUTPUT TRACKING GEN of spectrum analyzer and RF IN of test fixture.

   5.4 If required carefully adjust coils L9, L10, L11, L12 and L13 on B.U.T. to obtain waveform similar to that shown in Figure 2-4 (disregard the waveform higher than 30 MHz.) The spectrum analyzer is presently set to display the "ripple" from 1.5 MHz through 30 MHz.

   5.5 If similar waveform is obtained change the spectrum analyzer setting as follows:

Vertical Scale Range	1 dB/div
Vertical Scale	–60 dBm (blue lighted scale)
Horizontal Scale	10
Horizontal Range	kHz/div
Reference Frequency	35.4 MHz

   5.6 Adjust L11, L12, if necessary, to bring down the signal level 5 divisions or more from the top reference line for total of at least –70 dB. Caution should be taken not to lower signal level too much over –70 dB as this may degrade the response at 30 MHz.

   5.7 Repeat steps 3 and 5.4 thru 5.6 until no improvement can be obtained. Record the level observed in step 5.6 on test data sheet.

6. Return to step 3. Make additional settings on spectrum analyzer as follows:

Counter Frequency	Bright line
Sweep Mode	Single

7. Move BRIGHT LINE POSITION of Spectrum Analyzer to left until counter frequency reads 1.5 MHz. The level at this point should be at least +5.5 dB from the ground level noted in step 5.2. Record this level.

8. Move BRIGHT LINE POSITION to right until counter frequency reads 2.0 MHz. The "ripple" should stay in –2 dB and +1 dB of 7.5 dB. Check on test data sheet.

9. Move BRIGHT LINE to right until counter reads 30 MHz. Between 2.0 to 30 MHz, the "ripple" should be between -1 dB and +1 dB of +8.5 dB. Record. Before proceeding, the stop band should be examined to ensure that no response rises above the –90 dB line between 40 and 100 MHz. This can be done by setting the analyzer to 10 dB/div and sweeping 0 - 100 MHz.

2.4.4 Corrective Action

If the above procedures fail to produce the predicted or desired results, trace signals through to the fault; first through the input filter, then the amplifier and then the output filter. Refer to the circuit schematic diagram, Figure 2-1. Figures 2-3A and 2-3B show locations of circuits and components on the module. If required, use the oscilloscope (item 2 of Table 1-2) to trace signals to fault.

Repair fault and/or replace faulty components. Care must be taken to avoid overheating of semiconductor and sensitive components when soldering or unsoldering. Use a clip-on heat sink or a pair of pliers on the device leads before applying heat.

After repair, repeat the procedures, as required, to assure a correctly aligned and operating module.

2.5 PARTS LIST, RF AMPLIFIER, A1

Table 2-2 lists the major components contained on the RF Amplifier module, A1. Table 2-3 lists the electrical components contained on the Circuit Card Assembly.

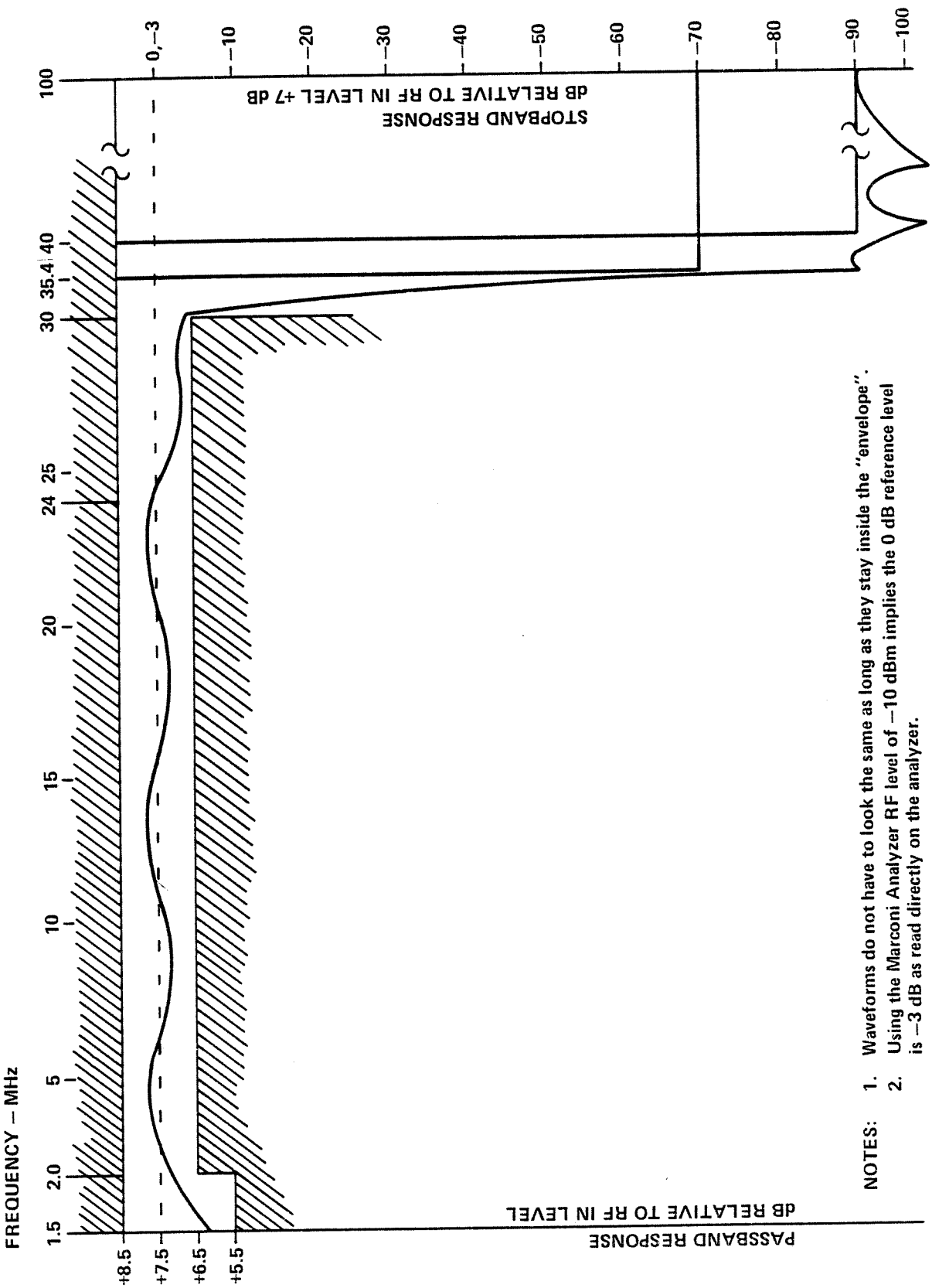


Figure 2-4. Gain/Frequency Characteristics Curve

DATE _____
CKD BY _____

MODULE A1
USED ON _____

TEST DATA SHEET

PART NAME: A1 RF Amplifier
PART NUMBER: _____
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
2.4.2.2	Null level at 46.43 MHz				dB
2.4.2.4	Null level at 66.67 MHz				dB
2.4.3.5(7)	Signal level at 35.4 MHz			-65	dB
2.4.3.7	Response at 1.5 MHz		+5.5		dB
2.4.3.8	Ripple level 1.5 – 2.0 MHz		-2	+1	dB
2.4.3.9	Ripple level 2.0 – 30 MHz		-1	+1	dB

TABLE 2-2. PARTS LIST, RF AMPLIFIER ASSEMBLY (A1) 06894

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A1	Circuit Card Assembly (See Table 2-3 for further breakdown)	06960-3	
C1, C2	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
J1	Connector, 3-pin (Winchester)	61163	SM3PN
R1, R2	Resistor, Composition, 4.7 ohms, ±5%, 1/4W	10607	RC07GF4R7J
W1	Input Cable Assembly	08685	
W2	Output Cable Assembly	06999	
–	Base Assembly	06623	
–	RF Shield	70950	
–	Cover	09264	

TABLE 2-3. PARTS LIST, RF AMPLIFIER CIRCUIT CARD ASSEMBLY (A1A1) 06960-3

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 13, 19	Capacitor, Mica, 120 pF, ±2%	22113	CM05FD121G03
C2	Capacitor, Mica, 24 pF, ±2%	22164	CM05CD240G03
C3, 15	Capacitor, Mica, 180 pF, ±2%	22118	CM05FD181G03
C4	Capacitor, Mica, 75 pF, ±2%	22125	CM05ED750G03
C5, 20	Capacitor, Mica, 82 pF, ±2%	22108	CM05ED820G03
C6, 9, 10, 11, 12	Capacitor, Tantalum, 6.8 uF, ±20%	25032	T368B685M035AS
C7	Capacitor, Mica 3 pF (Cornell-Dubilier)	22300	CD6C030K500
C8	Capacitor, Tantalum, 1 uF, ±20% (Union Carbide)	25033	T368A105M035AS
C14	Capacitor, Mica, 8.0 pF, ±½ pF	22149	CM05CD080D03
C16	Capacitor, Mica, 56 pF, ±2%	22111	CM05ED560G03
C17	Capacitor, Mica, 130 pF, ±2%	22140	CM05FD131G03
C18, 23	Capacitor, Mica, 100 pF, ±2%	22109	CM05FD101G03
C21	Capacitor, Mica, 150 pF, ±2%	22101	CM05FD151G03
C22	Capacitor, Mica, 30 pF, ±2%	22160	CM05ED300G03
C24, 25	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
CR1, 2	Diode	35555	1N3600
FB1, 2	Ferrite Bead (Mullard)	45051	FX1242
L1, 10, 12	Coil, Variable	06090-3	
L2, 11	Coil, Variable	06090-2	
L3, 5	Choke, 4.7 mH	43039	MS90541-3
L4, 6	Choke, 6.8 uH	43028	MS14046-2
L7, 8	Choke, 1000 uH	43038	MS90539-15
L9, L13	Coil, Variable	06090-4	
Q1	Transistor	32019	2N3866
Q2	Transistor	32027	2N5160
R1	Resistor, Composition, 2.2K Ohms, ±5%, ¼W	10671	RC07GF222J

TABLE 2-3. PARTS LIST, RF AMPLIFIER CIRCUIT CARD ASSEMBLY (A1A1) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R2	Resistor, Composition, 680 Ohms, ±5%, ¼W	10659	RC07GF681J
R3, 6, 8	Resistor, Composition, 270 Ohms, ±5%, ¼W	10649	RC07GF271J
R4	Resistor, Film, 10 Ohms, ±2%, ¼W	12152	RL07S100G
R5	Resistor, Composition, 33 Ohms, ±5%, 1W	11227	RC32GF330J
R7	Resistor, Composition, 18 Ohms, ±2%, ¼W	10621	RC07GF180J
–	Printed Wiring Board	06621	

CHAPTER 3
FIRST MIXER A2

3.1 THEORY OF OPERATION

The First Mixer, A2 provides for mixing the RF input from module A1 with the first local oscillator signal from module A14. The resultant difference frequency from this mixing is filtered and amplified, to provide a selected first IF signal with transmitted modulation. Selection is accomplished through the first local oscillator on module A14 which tracks 35.4 MHz above the RF frequency selected. This 35.4 MHz difference frequency occurring in the mixer, from the RF and the local oscillator, then provides for the first IF signal. The functions, on the A2 module, that condition, mix and form the first IF are; an oscillator filter network, an oscillator amplifier and driver, an RF filter network, a mixer, a bandpass filter and an IF amplifier. Also contained on the board is a meter drive circuit for output to the front panel. Figure 3-1 shows a functional block diagram of the first mixer module A2 while Figure 3-2 shows the schematic diagram.

3.1.1 RF Filter, Mixer and Bandpass Filter

The RF output of the A1 module is connected to the first mixer through a two section elliptical lowpass filter. This filter has a cut-off frequency of 35 MHz and serves to present a defined impedance to the mixer, U1, RF input port. The filter consists of a double tuned tank circuit, in series with the incoming signal. It offers a very low impedance to the wanted RF signals but an increasingly higher impedance to frequencies above 30 MHz. The mixer U1, is an integrated circuit for mixing both the incoming RF signal (0.01 to 29.99999 MHz) and the first local oscillator signal (35.4 to 65.4 MHz). The mixer output is connected directly to crystal roofing filter FL1 which passes only the difference frequency of 35.4 MHz with an 8 kHz bandwidth. This then provides the first IF signal for Receiver operation.

3.1.2 First Local Oscillator Filter Network

The filter network for the incoming first local oscillator signal is comprised of two separate filters which are selectable through Receiver control. The first filter provides filtering to the signal between 35.4 and 39.4 MHz while the second filter provides the 39.4 to 65.4 MHz filtering. The appropriate filter is selected automatically, through the Receiver Control, as the RF frequency is selected. The filter for the 35.4 to 39.4 MHz signal consists of a three section tunable tank circuit with each tank consisting of a crystal and tunable coil. This filter is tuned to reject spurious unwanted signals generated in the oscillator synthesizer circuits. The filter for the 39.4 to 65.4 MHz signal is comprised of four sections of series resonant circuits with each section containing a capacitor and tunable coil connected in series with each other but parallel to signal flow. A second capacitor connected in series with signal flow provides isolation to each resonant circuit. Each circuit is tuned to reject the spurious unwanted signals. The input and output signals for both filters are connected to diode switches which are reverse biased, only when Receiver control provides the bias signal; thus, the appropriate filter is selected automatically as the desired RF frequency is selected.

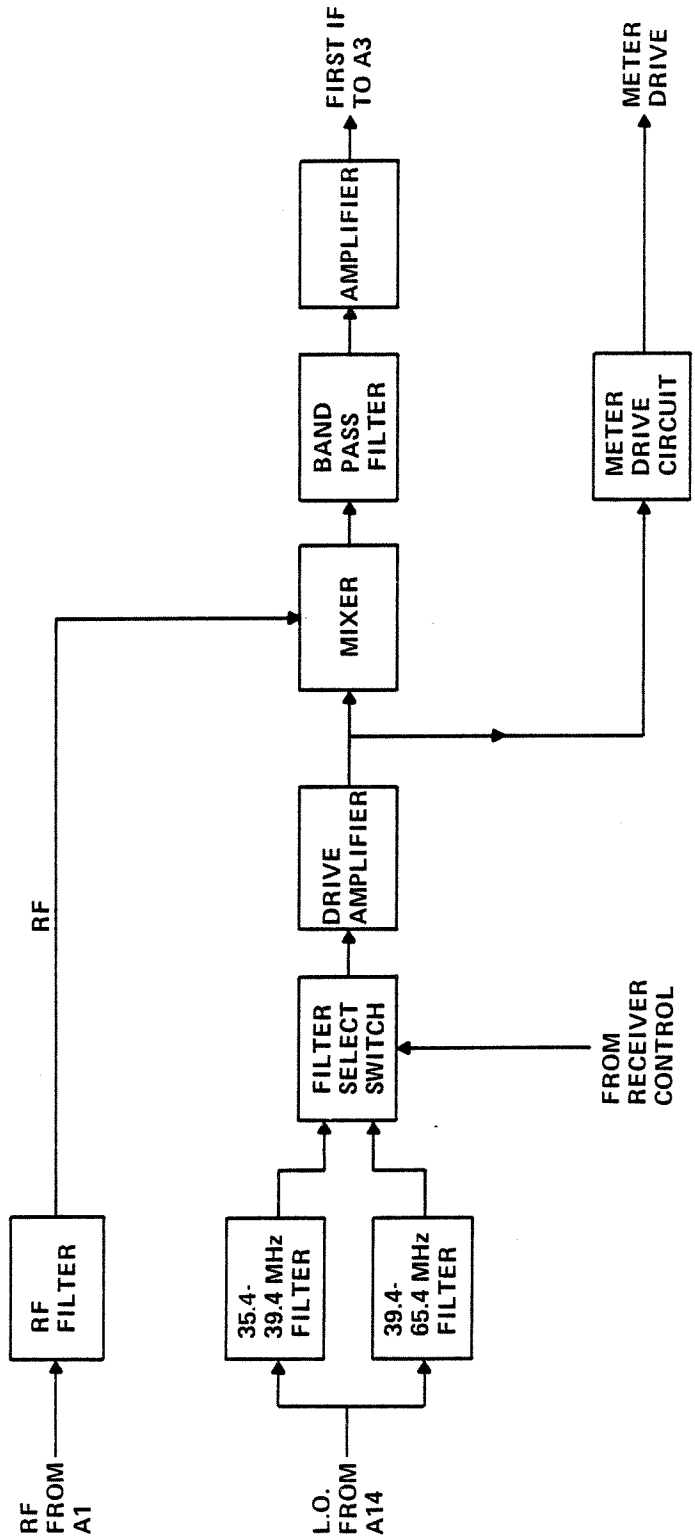
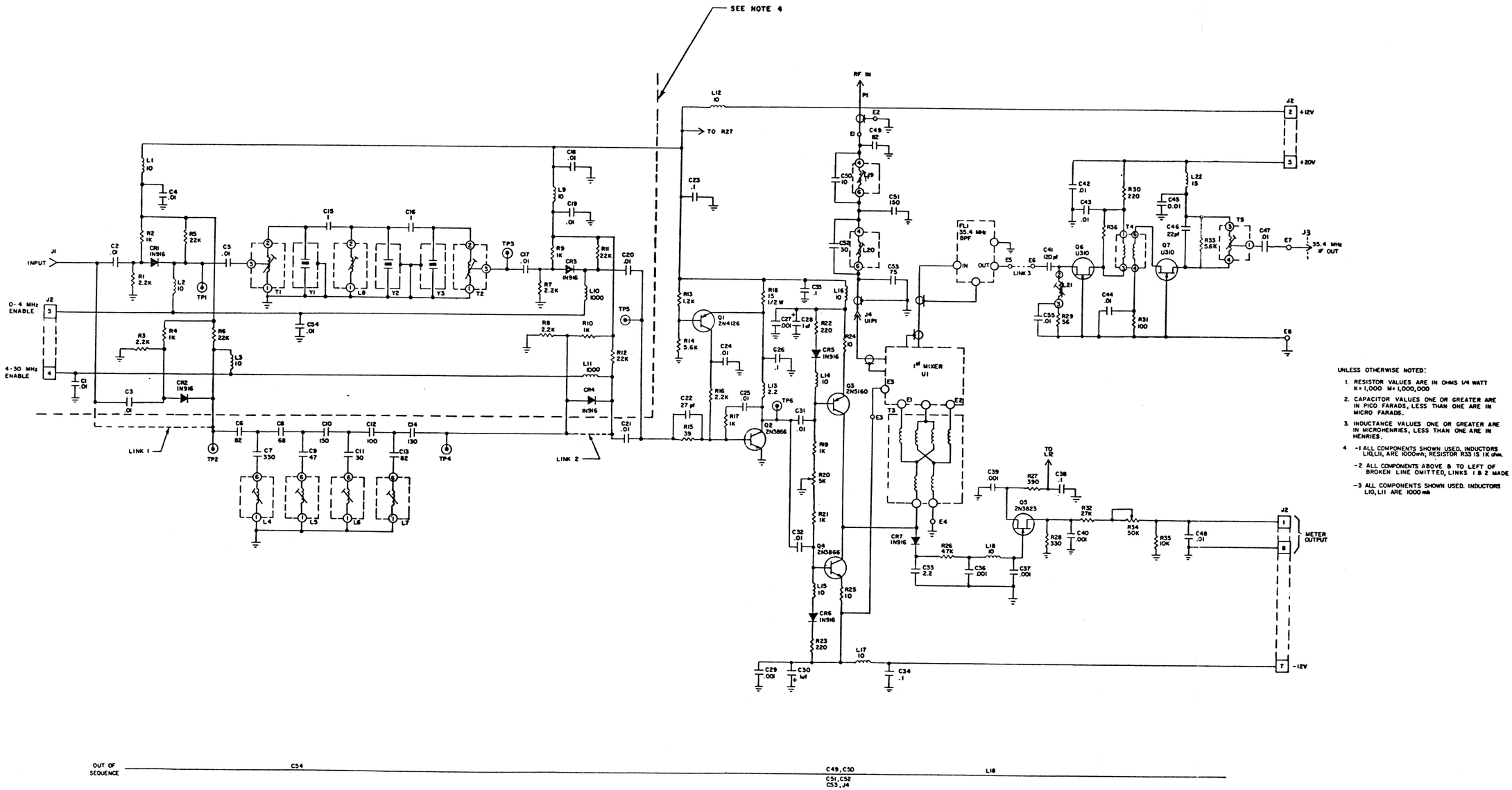


Figure 3-1. Functional Block Diagram, First Mixer Module A2



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT K = 1,000 M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICRO FARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN HENRIES.
4. -1 ALL COMPONENTS SHOWN USED. INDUCTORS L10,L11, ARE 1000mh; RESISTOR R33 IS 1K ohm.
   -2 ALL COMPONENTS ABOVE B TO LEFT OF BROKEN LINE OMITTED, LINKS 1 & 2 MADE
   -3 ALL COMPONENTS SHOWN USED. INDUCTORS L10, L11 ARE 1000 mh

Figure 3-2. Schematic Diagram, First Mixer, A2

3.1.3 Oscillator Amplifier and Driver

The output of the diode filter select switch, described in paragraph 3.1.2 is coupled to a transistor amplifier consisting of transistors Q1 and Q2. The signal is applied to the base of Q2 with Q1 regulating the gain of the stage. The output of this amplifier is coupled to a driver amplifier consisting of transistors Q3 and Q4. This stage is a complimentary amplifier with a balanced input applied to the base of each transistor. Potentiometer R20 provides an adjustment to maintain this balance between the two inputs. The output of the driver amplifier is coupled directly to driver transformer T3, which couples the oscillator signal to the input port of mixer U1.

3.1.4 IF Amplifier

The IF signal derived from bandpass filter FL1, and described in paragraph 3.1.1, is further filtered through C41, L21, C55 and R29. This filtered IF signal is coupled to a two stage field effect transistor amplifier, consisting of Q6 and Q7. The first stage is transformer coupled through T4 to the second stage. This high linear amplifier is coupled through transformer T5 which is tapped to provide the first IF signal output from module A2.

3.1.5 Meter Circuit (Not Used)

A meter drive circuit is contained on module board A2 that can be used to monitor the output of the oscillator drive amplifier. The same drive output that is coupled to the drive transformer is routed, through a diode, to a filter consisting of capacitors C35, C36, and C37, resistor R26 and coil L18. The filtered signal is then coupled to the gate of a field effect transistor, Q5. Amplifier Q5 provides drive for the meter through resistors R32 and R34. Resistor R34, a potentiometer, provides adjustment for the meter output level.

3.2 FIRST MIXER A2, TEST FIXTURE

Troubleshooting and alignment of the first mixer A2 is accomplished through the use of the RACAL first mixer (A2) test fixture and associated test equipment. The test fixture provides a convenient base to mount the A2 module for testing, while at the same time providing easy access to all areas of the PC board. All input and output ports are located on the rear apron of the test fixture, with all controls and a meter located on the front apron.

Contained within the test fixture is a second mixer board, that provides the necessary isolation and filtering action for elimination of the 35.4 MHz output of the first mixer (See Figure 3-5). The mixer also provides the proper load for the first mixer under test. A 1.4 MHz filter is also included in the test fixture along with a 23 MHz temperature controlled crystal oscillator. The crystal oscillator eliminates the need for an external RF source. The meter, located on the front apron, allows an operator to align the first mixer for proper output levels. All associated test equipment is interfaced to the test fixture through BNC chassis connectors. Figure 3-3 shows the first mixer module A2 test fixture. Figure 3-4A shows the overall assembly of the A2 module, while Figure 3-4B shows the circuit card assembly.

3.3 TEST EQUIPMENT AND ACCESSORIES

Table 3-1 lists the test equipment and accessories required to satisfactorily test the A2 module.

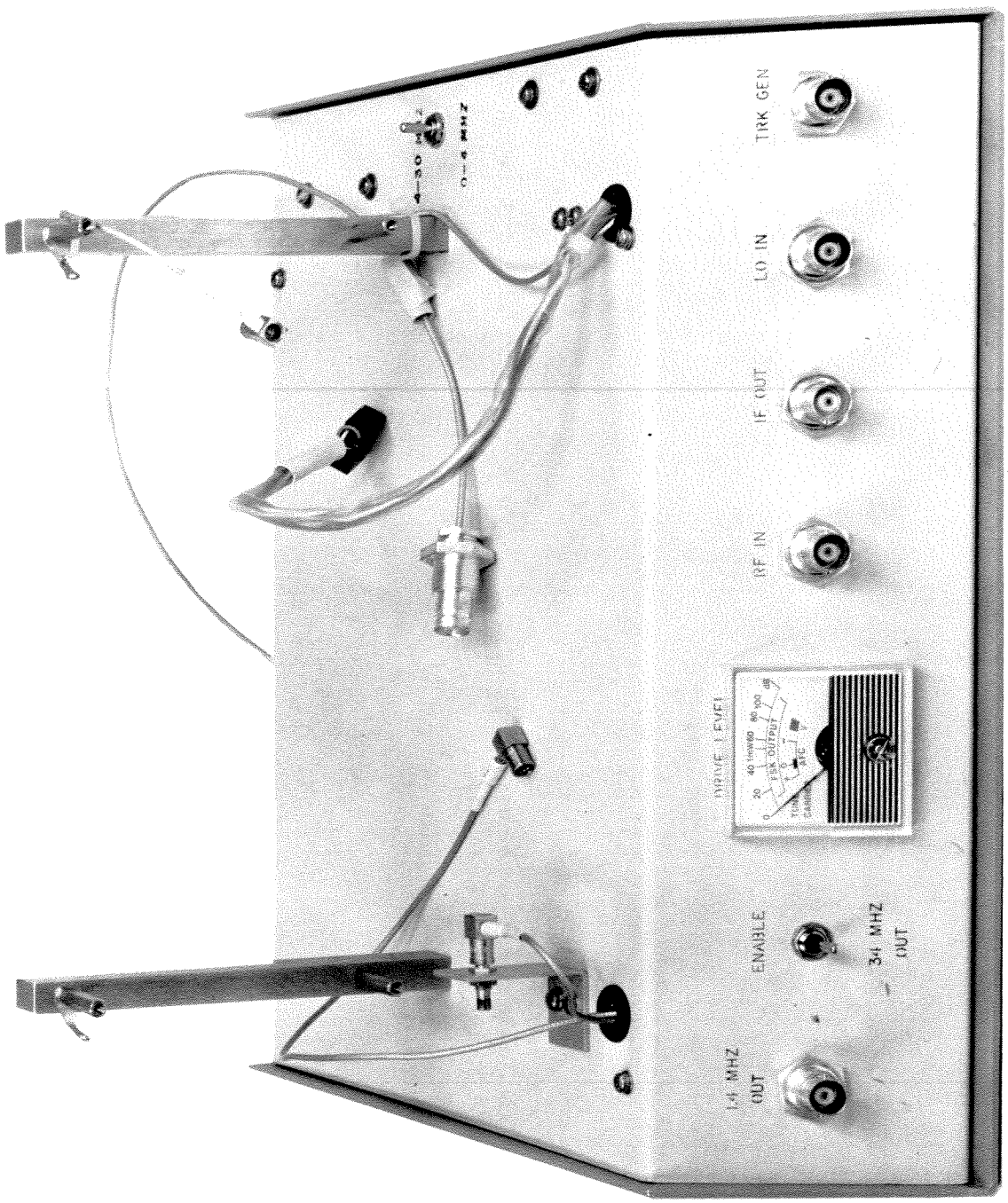


Figure 3-3. First Mixer A2, Test Fixture

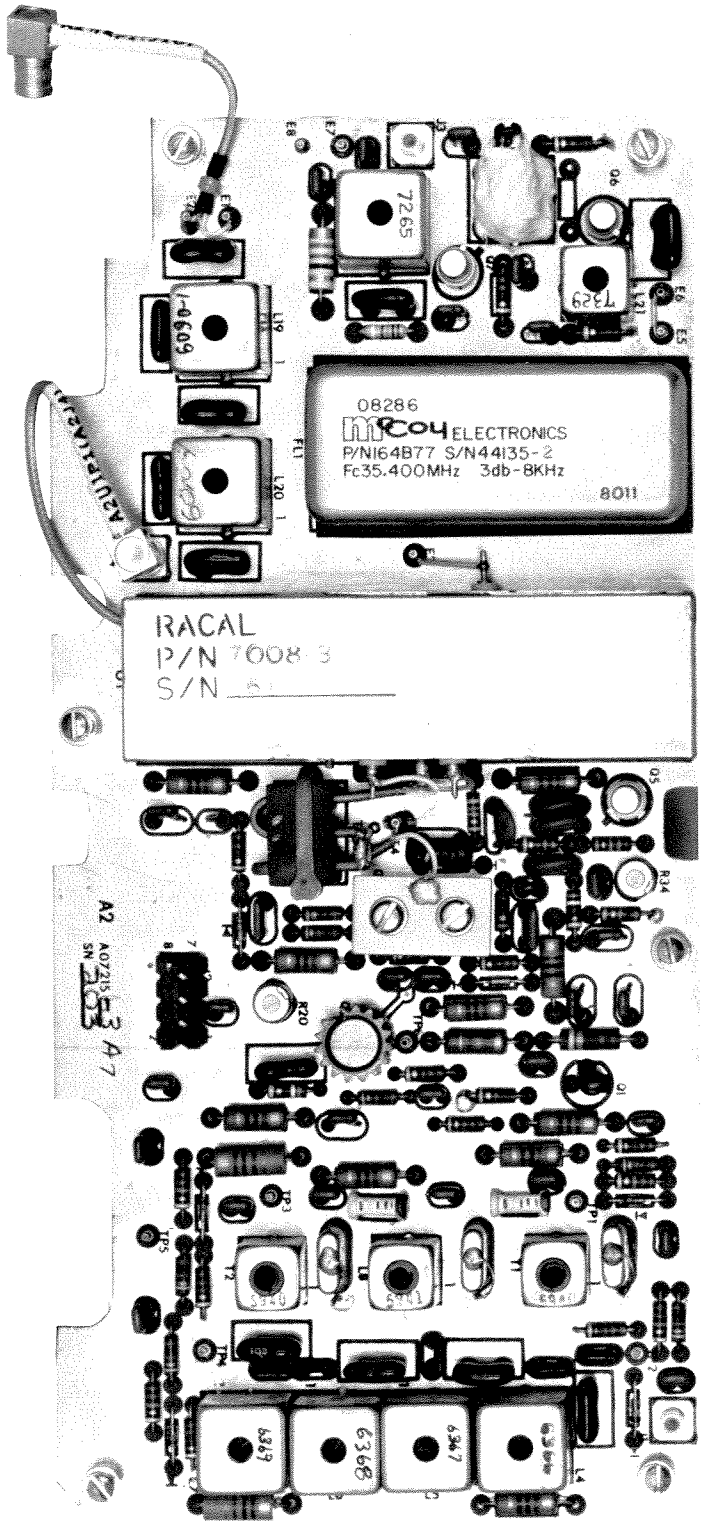


Figure 3-4A. First Mixer A2, Overall Assembly

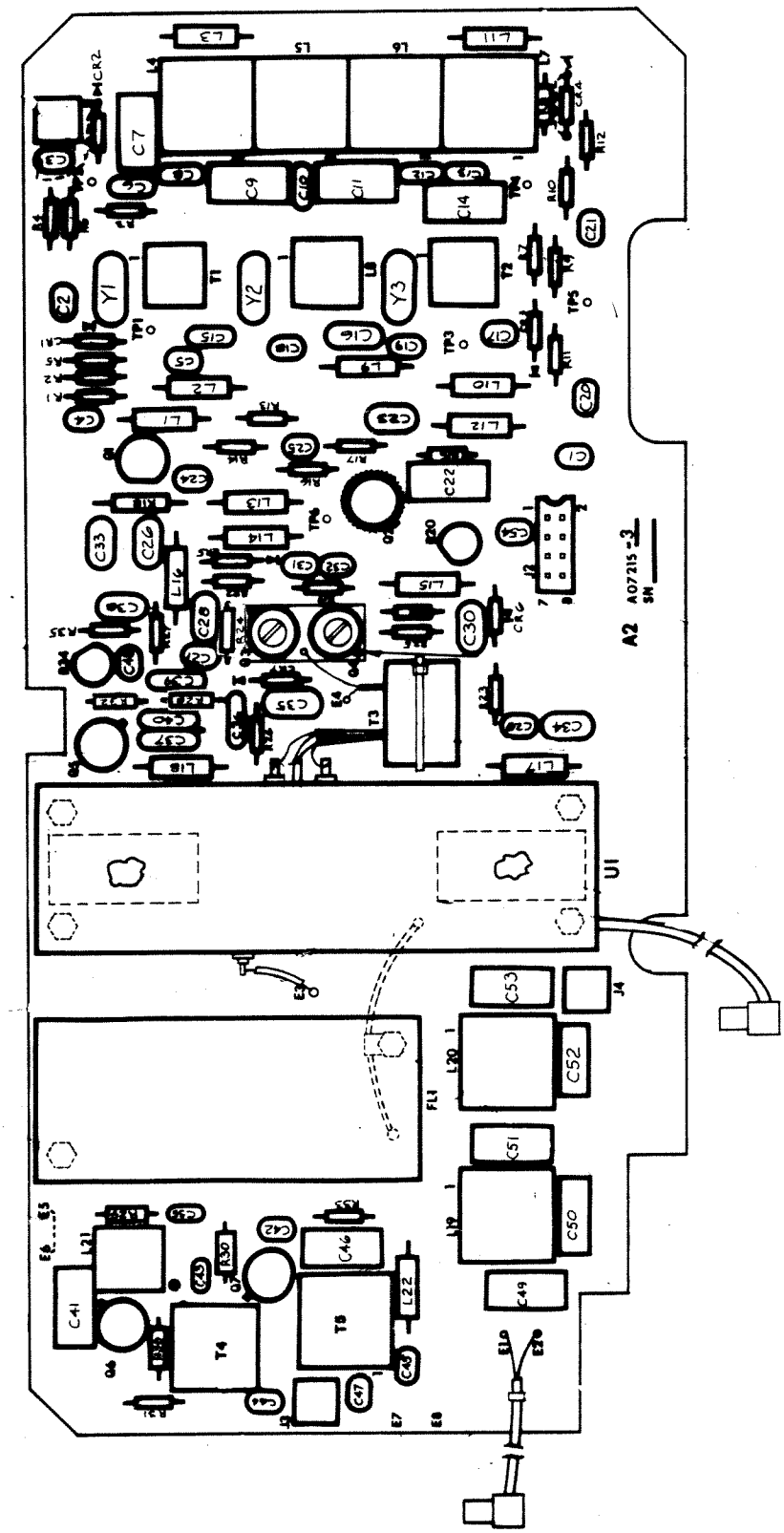


Figure 3-4B. First Mixer A2, Circuit Card Assembly

Table 3-1. Test Equipment and Accessories

Item	Description	Equipment Recommended or Equal
1	Spectrum Analyzer	HP 141T, 8552B, or 8553B
2	Tracking Generator	HP 8443A
3	High Z Probe	HP 1121A
4	RF Generator	HP 606, or Logimetrics 921A
5	RF Multivoltmeter	Boonton 91H
6	RF Millivoltmeter Adapter	50 ohm – 100:1 Hi Z
7	Mixing Unit	Racal (See Figure 3-5)
8	Noise Generator	SKTU 4151/2/50
9	Test Fixture	Racal
10	100 ohm Load	Racal
11	Power Supplies	Racal
12	Analog DC Voltmeter	RCA WV-98C

3.4 TEST AND ALIGNMENT

The following procedures are to be used to verify satisfactory performance of the First Mixer module, A2. Tests should be conducted at room temperature. Record test data results on test data sheet, page 3-19.

3.4.1 Driver Amplifier DC Bias Test

1. Place the A2 Board under test (B.U.T.) on the test fixture.
2. Connect the Power Supply plug to the test fixture.
3. Connect the Power Supply plug from the fixture to the board under test. Do not connect any other jacks.
4. Connect a digital multimeter between the collectors of Q3 and Q4 and ground set to DC volts.
5. Switch on the supply and adjust R20 so that the multimeter reads Zero volts. Record results.
6. Disconnect Digital Multimeter and connect all the other jacks to the board.

3.4.2 Highpass Filter Alignment

1. Connect the Tracking Generator to LO IN connector on test fixture.
2. Connect the Analyzer to TP4 on B.U.T. using the HI-Z probe.
3. On the test fixture, set the filter select switch to the 4 to 30 MHz position.
4. Set the Tracking Generator Analyzer controls as follows:

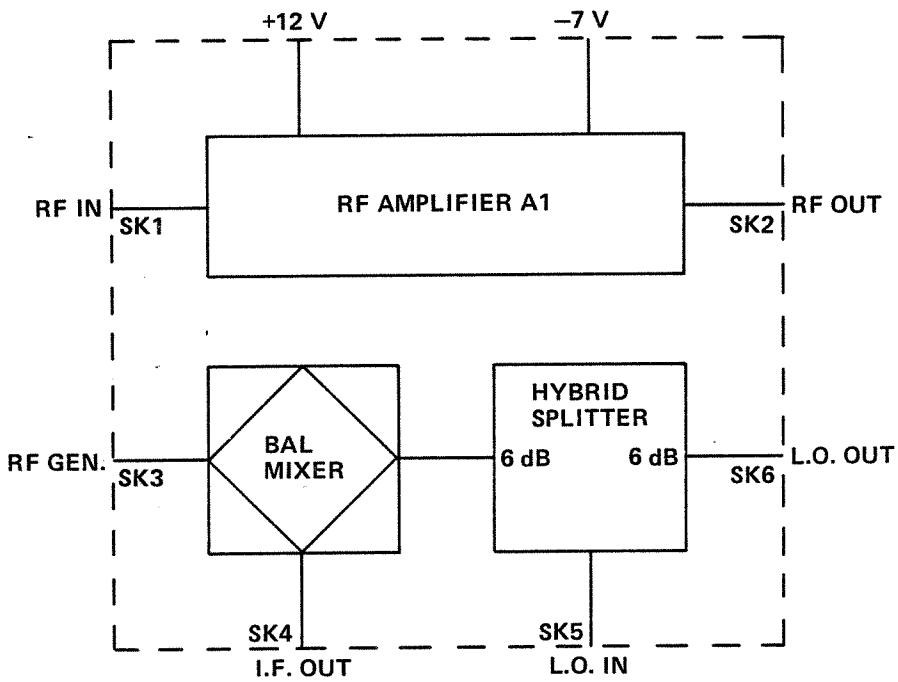


Figure 3-5. Block Diagram of Mixing Unit

Output Level	0 dBm
Bandwidth	300 kHz
Scan Width	10 MHz/div.
Input Attenuator	–30 dBm
Scan Time	10 mSec
Log Ref. Level	+10 dBm
Video Filter	10 kHz

5. Adjust analyzer frequency so that 0 MHz response is at left-hand end of display.

6. Set the marker to the following frequencies, adjusting the corresponding coils to align the notches.

20.2 ±0.2 MHz	L4
30.7 ±0.2 MHz	L7
34.3 ±0.1 MHz	L5
35.4 ±0.05 MHz	L6

7. Set the analyzer to sweep 0-100 MHz.

8. Set marker to 35.40 MHz. Ensure that all frequencies below markers are at least –40 dB relative to peak bandpass response. Record on test data sheet.

9. Set marker to 36.90 MHz. Ensure that all frequencies above marker are within 5 dB of peak passband response. Record on test data sheet.

10. Set Tracking Generator to SCAN HOLD.

11. Connect the RF Millivoltmeter via 100:1 divider to each side of the mixer drive input. Ensure that voltage is greater than +5 volts at each side. Record results.

12. Adjust Tracking Generator frequency to 65 MHz. Ensure that voltage at mixer drive points is greater than 5 volts. Record results.

13. Adjust R34 so that meter reads in center of greenband.

14. On the test fixture set the filter select switch to the 0 to 4 MHz position. Connect the Analyzer to TP3. Tune to 35.4 MHz center frequency and set to SCAN.

15. Tune T1, L6, and T2 to obtain an output response similar to that shown in Figure 3-6. Be certain to align the notch to 35.4 MHz.

3.4.3 RF Input Lowpass Filter Alignment

1. Connect the Tracking Generator to the RF IN on B.U.T. A2W1P1(J10).

2. Connect the Analyzer, using a suitable adapter to the J4 socket on the B.U.T.

3. Set the Tracking Generator/Analyzer controls as follows:

Output Level	0 dBm
Bandwidth	100 kHz
Scan Width	2 MHz/div.
Input Attenuator	–10 dB
Scan Tune	10 mS
Log Ref. Level	+10 dBm

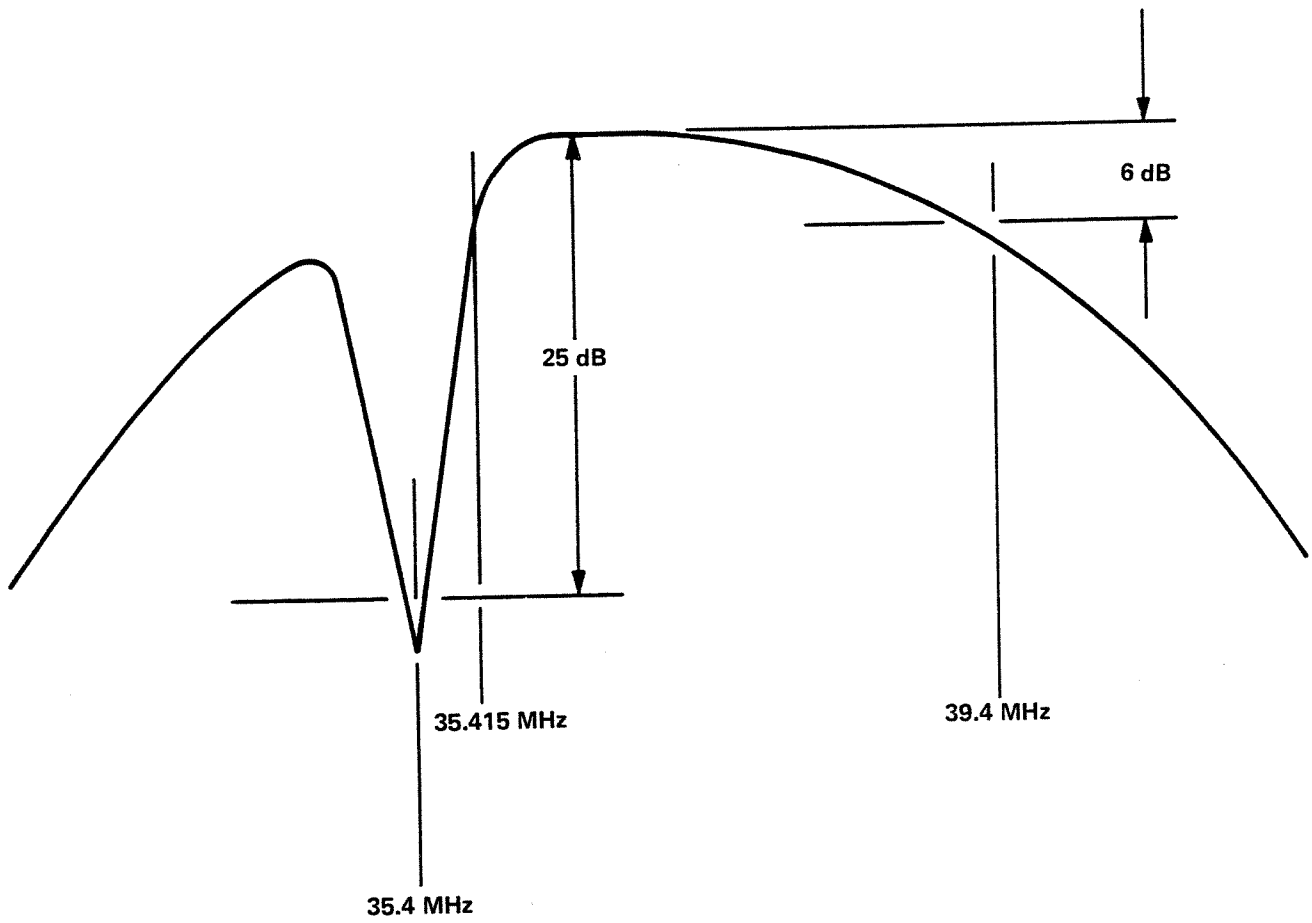


Figure 3-6. Typical Output Characteristics, 0 to 4 MHz Filter.

4. Set Tracking Generator to SCAN HOLD and adjust the Analyzer center frequency to 56.710 ±0.05 MHz. Adjust L20 for minimum level.

5. Set Tracking Generator to MARKER and ensure that a notch is shown on the display.

6. Set Tracking Generator to SCAN HOLD and set center frequency to 86.68 ±0.05 MHz. Adjust L19 for minimum level as shown on the analyzer display.

7. Reset Analyzer center frequency to 56.710 ±0.05 MHz and readjust as necessary. Set Tracking Generator to Marker.

8. Set Analyzer to sweep 0-100 MHz. Check that all frequencies above 56 MHz are better than 37 dB down, from a reference level at 30 MHz. **Record results.**

9. Set Analyzer to 2 dB log response and adjust the Analyzer to display the passband response. Ensure that peak to peak ripple from 1 MHz to 30 MHz is less than 1 dB. **Record.**

10. Reconnect input cable to mixer on B.U.T. to J4 on B.U.T. Reconnect A2W1P1(J10).

3.4.4 Overall Board Response

1. Connect the test equipment as shown in Figure 3-7.

2. Set the Tracking Generator/Analyzer controls as follows:

Output Level	−10 dBm
Frequency	35.400 MHz
Bandwidth	3 kHz
Scanwidth	2 kHz/div.
Input Attenuator	−10 dB
Scan Time	50 mSec/div.
Log Ref Level	0 dBm
Scale	2 dB Log

3. Set RF Generator for +6 dBm, 44 MHz, CW.

4. Observe trace and adjust L21 for best flat response over middle 3.2 kHz. (Refer to Figure 3-8.) Ensure that ripple is less than 1 dB for ±1.5 kHz. **Record results.**

5. Adjust T5 for Max. output at 35.4 MHz and ensure that peak response is greater than 0 dBm. **Record on test data sheet.**

6. Ensure that −3 dB bandwidth is greater than 8 kHz. **Record on test data sheet.**

7. Set Scanwidth to 10 kHz/div. Set scale to 10 dB Log. Ensure that −60 dB bandwidth is less than 20 kHz. **Record result on test data sheet.**

3.4.5 Noise Figure Measurement

1. Connect test equipment as shown in Figure 3-9.

2. Set Spectrum Analyzer controls as follows:

Scanwidth	Zero
Frequency	1.4 MHz

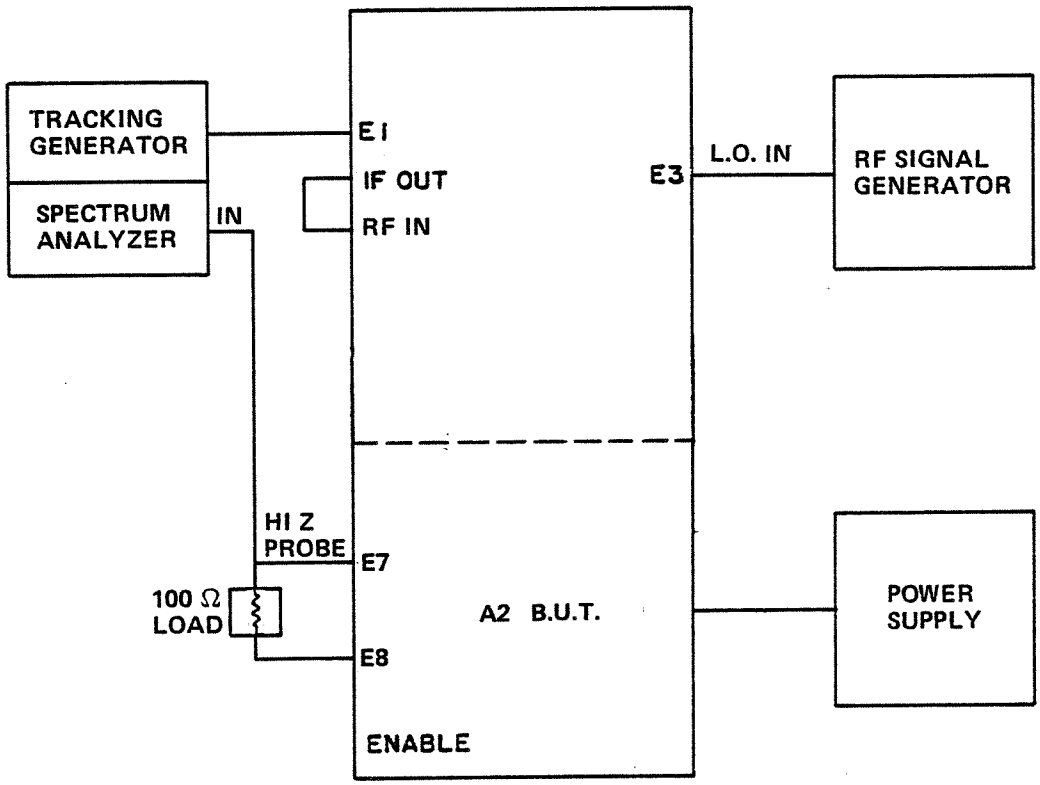


Figure 3-7. Overall Board Response, Test Set-Up

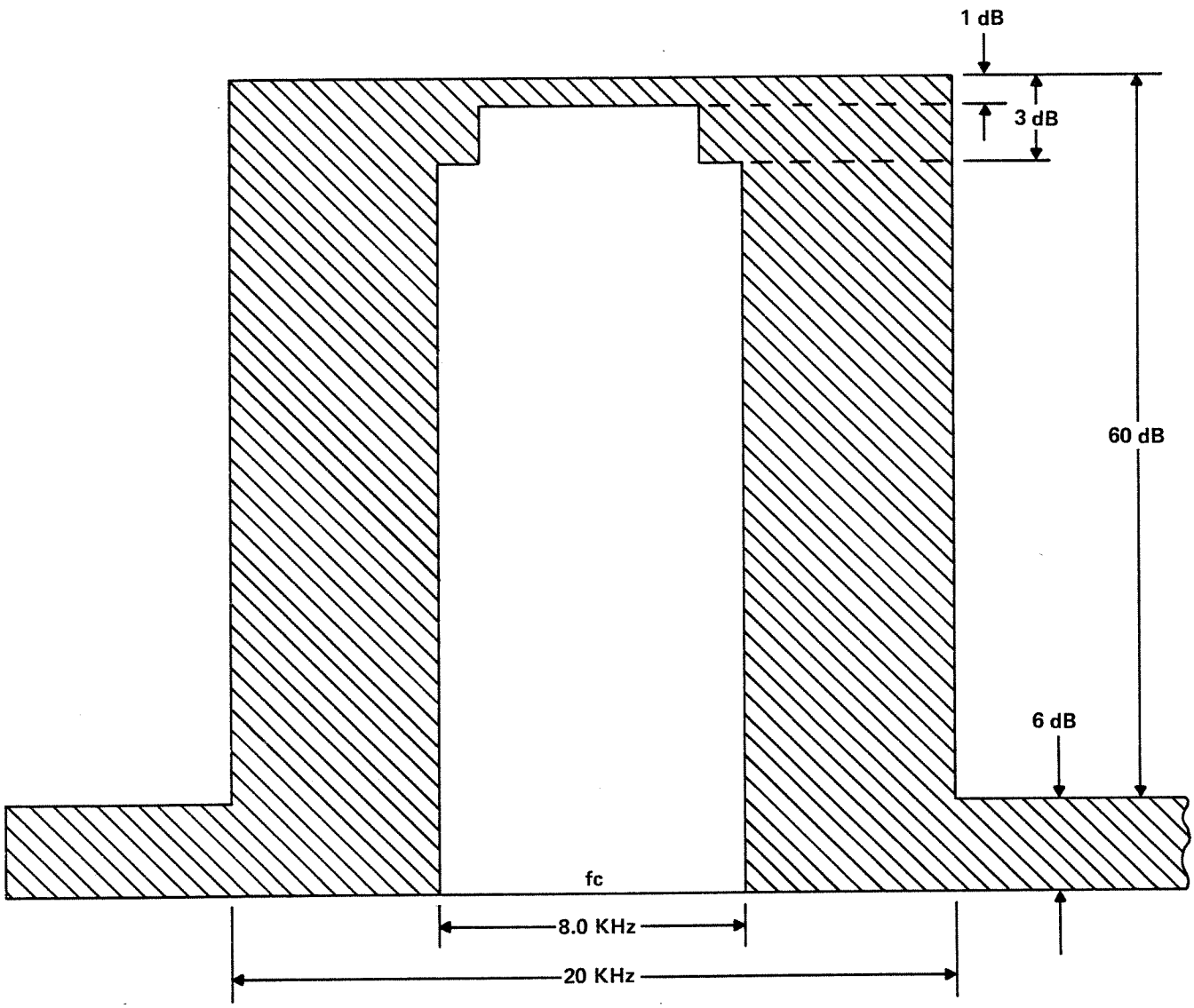


Figure 3-8. Overall Filter Response

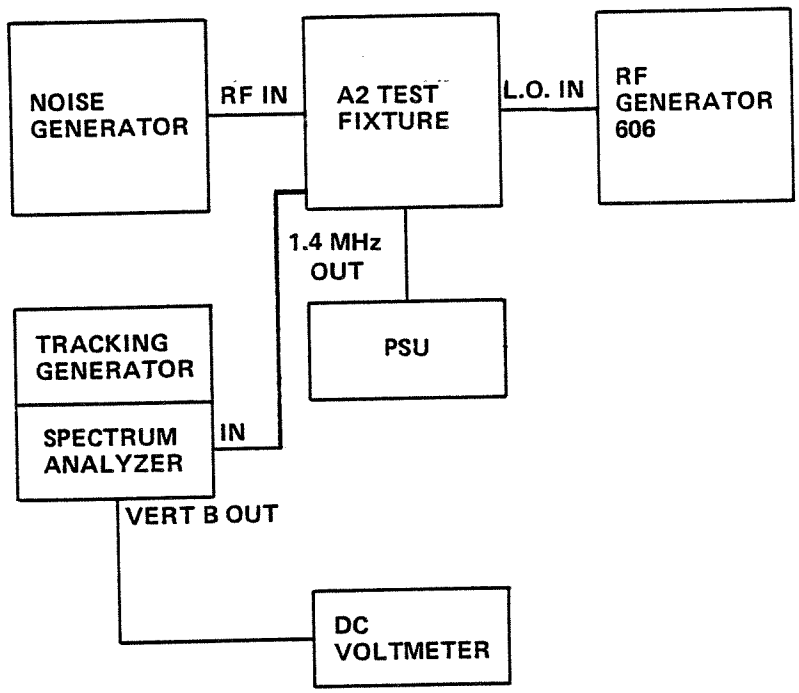


Figure 3-9. Noise Figure Measurement, Test Set-Up

Bandwidth	1 kHz
Input Attenuator	0
Scan Time	50 mS
Log Ref Level	–50 dB/10 dB Log
Video Filter	10 Hz

3. Connect the High Z probe to the 1.4 MHz Output on test fixture.

4. Set RF Generator to 37 MHz with an Output of 0 dBm.

5. Connect DC voltmeter to vertical output skt. on Spectrum Analyzer IF section, and set to indicate negative voltage at 0 to 0.5V. Ensure the 34 MHz switch on the test fixture is set to ENABLE.

6. Ensure Noise Generator level is reduced to minimum.

7. Change position of trace on Spectrum Analyzer by 3 dB, using the REF level control and note the change in voltage on the DC voltmeter. Return the REF level control to its previous position.

8. Increase the level out of the Noise Generator until the noise level as shown on the DC Voltmeter increases by 3 dB.

9. Note the reading in dB on the Noise Generator and ensure that it is less than 11 dB. Record on test data sheet.

10. Repeat steps 7, 8 and 9, but with the LO input frequency set to 65 MHz. Record the level on test data sheet.

11. Turn power off, and remove the board under test from test fixture.

3.4.6 Overall Gain Check

1. Connect the Signal Generator using 50 ohm coaxial cable to the RF Input A2P1. Set the Signal Generator frequency to 29.9 MHz and the Signal Generator output to -10 dBm. Set the LO Signal Generator to 65.3 MHz at a level of 0 dBm and connect to J1 on A2. Ensure switch on test fixture is in 4-30 MHz position.

2. Set Analyzer as follows:

CTR. Freq.	35.400 MHz
Input Attenuation	20 dB
Log Ref. Level	0 dBm (2 dB Log)
Bandwidth	30 kHz
Scan Width	5 kHz

3. Connect Analyzer input using HI-Z probe across 100 ohm load connected to A2J3 (IF Output). Ensure level displayed is no less than the minimum called out on the test data sheet.

4. Set Signal Generator and test fixture frequencies to 5.5 MHz. Ensure level displayed is no less than the minimum called out on test data sheet.

3.4.7 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (Drive Amplifier, Oscillator, filter, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, steps 11 and 12 in paragraph 3.4.2 could isolate a fault in the oscillator signal to the voltage divider circuit of the drive amplifier and associated component. Further signal tracing may then be accomplished, using the oscilloscope or voltmeters, to trace the fault to a single component. Maximum use should also be made of the test points provided on the A2 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductors and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as required.

3.5 PARTS LIST, FIRST MIXER, A2

The parts list for the A2 module is contained in Table 3-2.

DATE _____
CKD BY _____

MODULE A2
USED ON _____

TEST DATA SHEET

PART NAME: A2 First Mixer Board
PART NUMBER: 07215-4
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
3.4.1(5)	Drive Amplifier DC Bias				
3.4.2(8)	Pass Filter Rejection		–	-40	dB
3.4.2(9)	High Pass Filter Passband Ripple		–	5	dB
3.4.2(11)	Drive Volts LO Amplifier 36.9 MHz		5	–	volts
3.4.2(12)	Drive Volts LO Amplifier 65 MHz		5	–	volts
3.4.3(8)	Low Pass Filter Rejection >56 MHz		–	-37	dB
3.4.3(9)	Low Pass Filter Passband Ripple		–	1	dB
3.4.4(4)	Crystal Filter Passband Ripple ±3 kHz		–	1	dB
3.4.4(5)	Crystal Filter Peak Response Level		0	+4	dBm
3.4.4(6)	Crystal Filter 3 dB Points		8	–	kHz
3.4.4(7)	Crystal Filter 60 dB Points		–	20	kHz
3.4.5(9)	Overall Noise Figure @ 1.6 MHz			11	dB
3.4.5(10)	Overall Noise Figure @ 29.6 MHz			11	dB
3.4.6(3)	Overall Gain Check at 29.9 MHz		6	9	dB
3.4.6(4)	Overall Gain Check at 5.5 MHz		6	9	dB

TABLE 3-2. PARTS LIST, FIRST MIXER CIRCUIT CARD ASSEMBLY (A2) 07215-4

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-5, 17-21, 24, 25, 31, 32, 42-45, 47, 48, 54, 55	Capacitor, Ceramic, 0.01 uF, ±20%	21733	8121-050-651-103M
C6, 13	Capacitor, Mica, 82 pF, ±5%	22320	CD6F820J300
C7	Capacitor, Mica, 330 pF, ±2%	22117	CM05FD331G03
C8	Capacitor, Mica, 68 pF, ±5%	22318	CD6C680J500
C9	Capacitor, Mica, 47 pF, ±2%	22112	CM05ED470G03
C10	Capacitor, Mica, 150 pF, ±5%	22326	CD7F151J500
C11, 52	Capacitor, Mica, 30 pF, ±2%	22160	CM05ED300G03
C12	Capacitor, Mica, 100 pF, ±5%	22322	CD6F101J300
C14	Capacitor, Mica, 130 pF, ±5%	22026	CM05FD131JN3
C15, 16	Capacitor, Ceramic, 1 pF, ±10%	21342	301-000-M7G-109K
C22	Capacitor, Mica, 27 pF, ±5%	22008	CM05E270JN3
C23, 26, 33, 34, 38	Capacitor, Ceramic, 0.1 uF, ±20%	21732	8131-050-651-104M
C27, 29	Capacitor, Ceramic, 0.001 uF, ±20%	21718	8121-050-W5R-102K
C28, 30	Capacitor, Ceramic, 1 uF, ±20%	21748	8121-050-651-105M
C35	Capacitor, Ceramic, 2.2 pF, ±½ pF	21339	331-000-M7G-229D
C36, 37, 39, 40	Capacitor, Ceramic, 0.001 uF	21703	DD102G
C41	Capacitor, Mica, 120 pF, ±5%	22025	CM05FD121JN3
C46	Capacitor, Mica, 22 pF, ±5%	22006	CM05ED220JN3
C49	Capacitor, Mica, 82 pF, ±5%	22021	CM05ED820JN3
C50	Capacitor, Mica, 10 pF, ±5%	22001	CM05CD100JN3
C51	Capacitor, Mica, 150 pF, ±5%	22027	CM05FD151JN3
C53	Capacitor, Mica, 75 pF, ±5%	22020	CM05ED750JN3
CR1-7	Diode	35514	1N916
FL1	Filter Assy, 35.4 MHz (Non-Repairable)	08286	
J1, 3, 4	Connector, SMB	60044	700209-002

TABLE 3-2. PARTS LIST, FIRST MIXER CIRCUIT CARD ASSEMBLY (A2) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
J2	Connector, Control	06846-4	
L1-3, 9, 12, 14-18	Choke, Fixed, 10 uH	43029	MS14046-4
L4	Coil, Variable	06366	
L5	Coil, Variable	06367	
L6	Coil, Variable	06368	
L7	Coil, Variable	06369	
L8	Coil, Variable	05941	
L10, 11	Choke, Fixed, 1000 uH	43038	MS90539-15
L13	Choke, Fixed, 2.2 uH	43025	MS18130-12
L19	Coil, Assy, RF Variable	06090-1	
L20	Coil, Assy, RF Variable	06090-4	
L21	Coil, Assy, RF Variable	07329	
L22	Choke, Fixed, 15 uH	43030	MS14046-6
Q1	Transistor	31508	2N4126
Q2, 4	Transistor	32019	2N3866
Q3	Transistor	32027	2N5160
Q5	Transistor	32511	2N3823
Q6, 7	Transistor	32507	U310
R1, 3, 7, 8, 16	Resistor, Composition, 2.2K Ohms, ±5%, ¼W	10671	RC07GF222J
R2, 4, 9, 10, 17, 19, 21	Resistor, Composition, 1K Ohms, ±5%, ¼W	10663	RC07GF102J
R5, 6, 11, 12	Resistor, Composition, 22K Ohms, ±5%, ¼W	10695	RC07GF223J
R13	Resistor, Composition, 1.2K Ohms, ±5%, ¼W	10665	RC07GF122J
R14	Resistor, Composition, 5.6K Ohms, ±5%, ¼W	10681	RC07GF562J
R15	Resistor, Composition, 39 Ohms, ±5%, ¼W	10629	RC07GF390J
R18	Resistor, Composition, 15 Ohms, ±5%, ½W	10919	RC20GF150J
R20	Resistor, Variable, 5K Ohms	16016	Beckman 62PR5K

TABLE 3-2. PARTS LIST, FIRST MIXER CIRCUIT CARD ASSEMBLY (A2) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R22, 23, 30	Resistor, Composition, 220 Ohms, ±5%, ¼W	10647	RC07GF221J
R24, 25	Resistor, Composition, 10 Ohms, ±5%, ¼W	10615	RC07GF100J
R26	Resistor, Composition, 47K Ohms, ±5%, ¼W	10703	RC07GF473J
R27	Resistor, Composition, 390 Ohms, ±5%, ¼W	10653	RC07GF391J
R28	Resistor, Composition, 330 Ohms, ±5%, ¼W	10651	RC07GF331J
R29	Resistor, Composition, 56 Ohms, ±5%, ¼W	10633	RC07GF560J
R31	Resistor, Composition, 100 Ohms, ±5%, ¼W	10639	RC07GF101J
R32	Resistor, Composition, 27K Ohms, ±5%, ¼W	10697	RC07GF273J
R33	Resistor, Composition, 5.6K Ohms, ±2%, ¼W	12161-562	RL075562G
R34	Resistor, Variable, 50K Ohms	16014	Beckman 62P-R50K
R35	Resistor, Composition, 10K Ohms, ±5%, ¼W	10687	RC07GF103J
T1, 2	Transformer, Variable	05940	
T3	Transformer, Wide Band	06158	
T4	Transformer, Wide Band	06467-1	
T5	Transformer, Variable	07265	
U1	Mixer Box Assembly	07008-3	
W1	Cable, RF Input	07041-5	
Y1	Crystal, 35.398 MHz	46260-1	046260-1
Y2	Crystal, 35.400 MHz	46260-2	046260-2
Y3	Crystal, 35.402 MHz	46260-3	046260-3
–	Printed Wiring Board	07216	
–	Pad, Transistor for Q2, 3, 4	70750	69011-1058
–	Pad, Transistor for Q5, 6, 7	70752	7717-7N White

CHAPTER 4
SECOND MIXER, A3

4.1 THEORY OF OPERATION

The Second Mixer, A3, contains an amplifier stage, attenuator, and a mixer. The schematic is shown in Figure 4-2.

Figure 4-1. is a simplified block diagram of the second mixer. The 35.4 MHz first IF output from the first mixer is amplified and applied to a 35.4 MHz bandpass filter to a balanced mixer where it is mixed with the filtered 34 MHz output from the 34 MHz generator board. The second IF is produced by selecting the 1.4 MHz difference frequency at the output of the mixer.

The output signal level from the first stage of IF amplification is controlled by the AGC input from the main IF amplifier A5. The output from the second stage of IF amplification is applied to the balanced mixer through a 35.4 MHz bandpass filter.

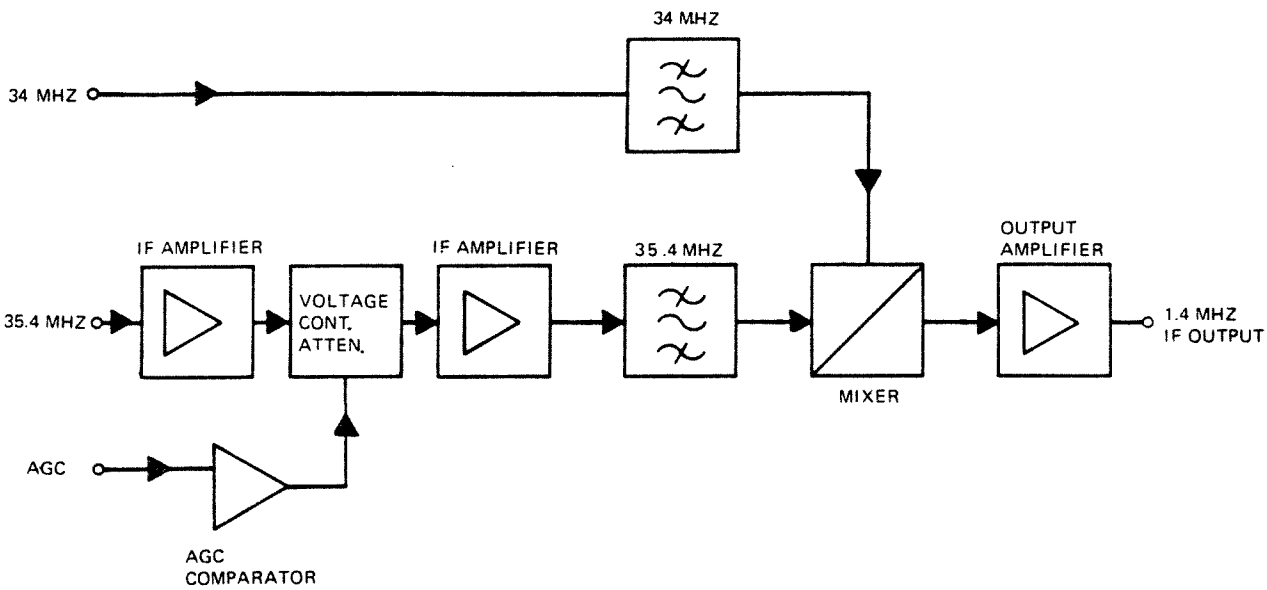


Figure 4-1. Simplified Block Diagram, Second Mixer, A3

The 34 MHz second mixer injection frequency, received from the 34 MHz generator board of the frequency synthesizer section, is applied to the mixer through a 4 section 34 MHz synchronously-tuned bandpass filter. The 1.4 MHz difference frequency IF output from the mixer is amplified before being applied to the IF filter board.

4.1.1 Amplifier Stage

The 35.4 MHz first IF output from the first mixer is applied to an amplifier stage, Q1, via board pin E1 and C1. The amplified output is applied via C8 to a further amplifier stage, Q5, and is also applied via C7 to a voltage controlled attenuator. This utilizes two PIN diodes, CR1 and CR2, and is controlled by the AGC input at pin J1-2 from the IF Amplifier board, A5.

4.1.2 PIN Diode Attenuator

The impedance presented to the 35.4 MHz IF signal by the PIN diodes is a function of the forward direct current passing through the diodes. When no forward current is allowed to flow the impedance is extremely high and this impedance is progressively reduced as the forward current is increased.

The differential AGC voltage output from the emitter followers, Q7 is applied to the base of Q6. This stage controls the current flow through the two PIN diodes, CR1 and CR2. Thus, an increase in the AGC voltage causes an increased current to flow through the PIN diodes. The output from the tuned circuit of Q1 is, therefore reduced by the shunt effect.

4.1.3 Mixer

A cross-coupled balanced mixer circuit, Q9 and Q10, produces the 1.4 MHz second intermediate frequency, which is the difference frequency between the 35.4 MHz first IF and the second mixer injection signal from the 34 MHz generator board. The 35.4 MHz output signal from Q5 is applied via a bandpass filter to the base of Q9, and the 34 MHz signal at J2 is applied via a bandpass filter to the base of Q10. The output from the mixer is applied to a 1.4 MHz IF amplifier stage, Q11, which has a stage gain of approximately 10 dB. The final output is applied to the IF filter board via board pin E3.

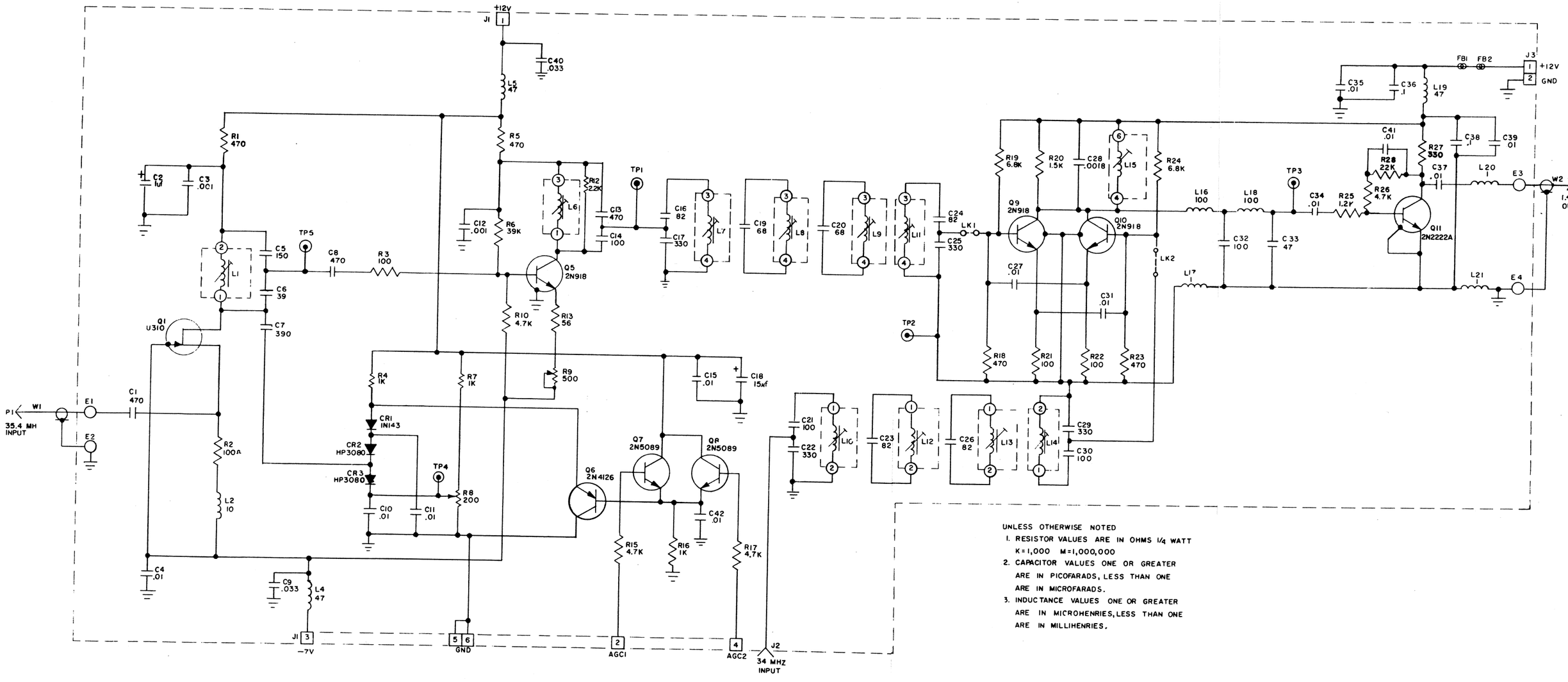
4.2 SECOND MIXER, A3, TEST FIXTURE

Testing, trouble shooting and alignment of the Second Mixer Module, A3, is accomplished through the use of the Second Mixer, A3, test fixture and associated test equipment. The Second Mixer Module plugs into the test fixture with the test equipment connection being made via the test fixture. The test fixture contains a 34 MHz TCXO, a control for the AGC range and a 1.4 MHz crystal filter for proper matching of the output stage.

Figure 4-3 shows the RACAL 2nd Mixer (A3) test fixture. Figure 4-4A shows the 2nd Mixer module, A3, overall assembly while Figure 4-4B shows the module circuit card assembly.

4.3 TEST EQUIPMENT AND ACCESSORIES

Table 4-1 lists the test equipment and accessories required.



UNLESS OTHERWISE NOTED

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN MILLIHENRIES.

Figure 4-2. Schematic Diagram, Second Mixer, A

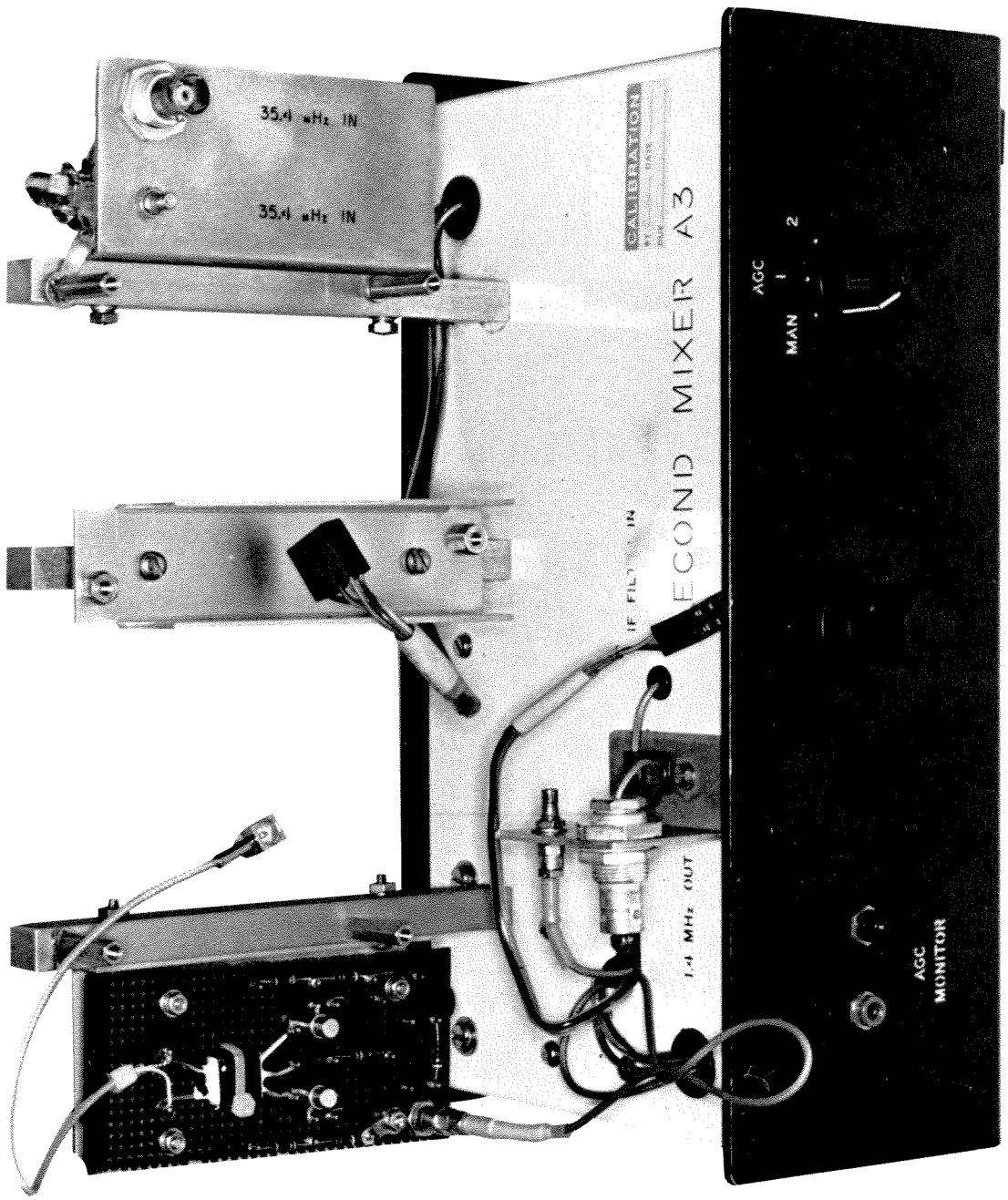


Figure 4-3. Second Mixer A3, Text Fixture

Table 4-1. List of Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	RF Generator	Logimetrics 921-A
2	Spectrum Analyzer	Marconi 2370 or HP141T, 8552B, 8553B
3	Tracking Generator	HP8443A
4	Hi-Z Probe	Marconi
5	Digital Multimeter	Data Precision Model 248
6	DC Power Supply	RACAL
7	Test Fixture	RACAL TF332
8	50 Ω Stepped Attenuator	KAY
9	Oscilloscope	Tektronics 465

4.4 TEST AND ALIGNMENT

The following procedures provide all the information necessary to verify that the A3 module meets all the specifications set forth. Tests should be conducted at room temperature. Record data on test data sheet, page 4-13.

4.4.1 Preliminary

1. Check that all R.F. varible coils have sufficient locking material to ensure that the adjustable cores will not be disturbed by vibration or shock.

2. Ensure that DC power to the test fixture is switched OFF.

3. Mount the A3 board under test into the test fixture and make the necessary DC and coaxial connections.

   NOTE: The RED face of J-1 and J-3 must be upwards.

4.4.2 34 MHz Filter Alignment

1. Remove A3J2 from 34 MHz input on left hand side of test fixture. In its place connect the Tracking Generator to the 34 MHz input connector on the test fixture.

2. Connect the spectrum Analyzer, using the Hi-Z probe to LK-2 connecting the ground clip to TP-2.

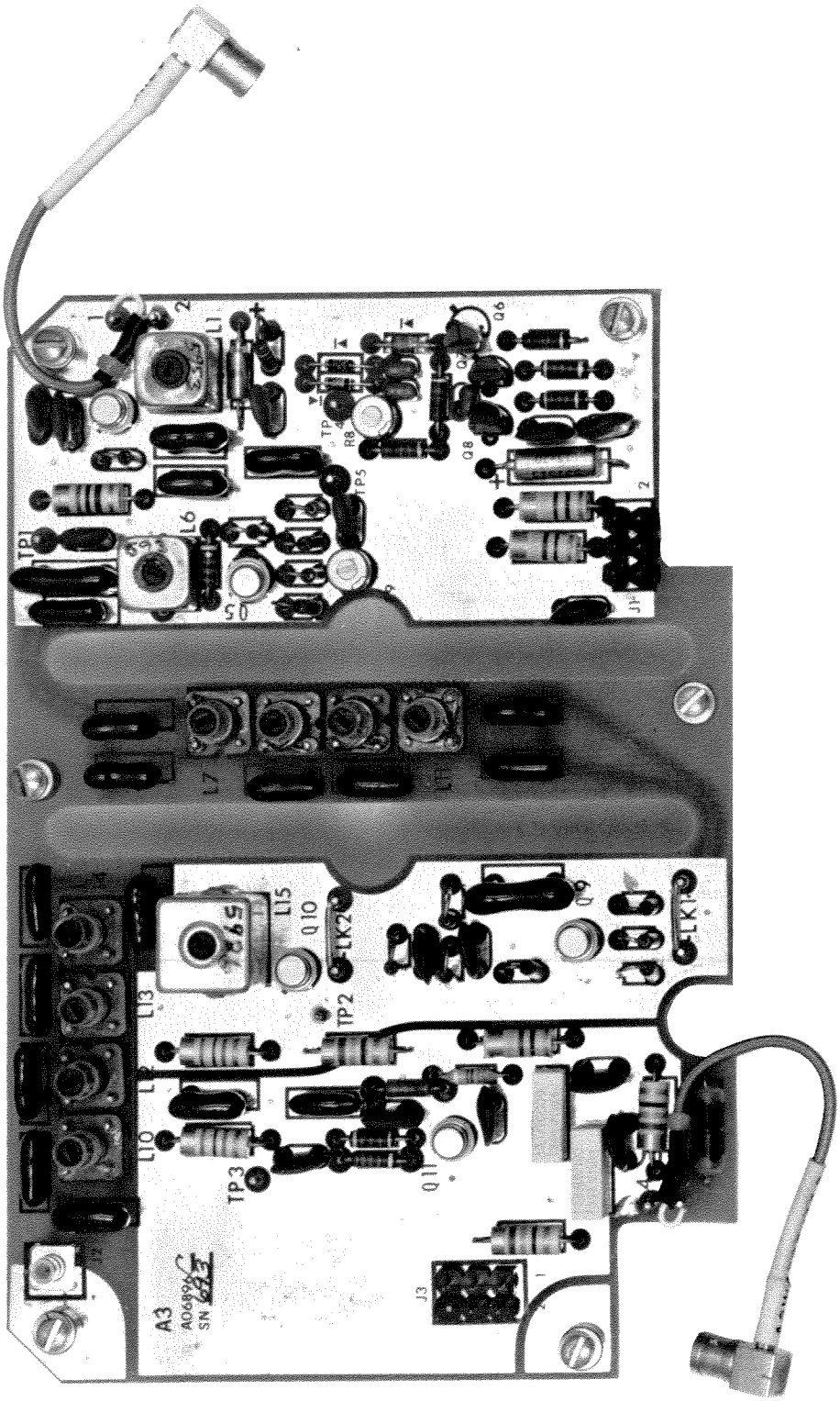


Figure 4-4A. Second Mixer A3, Overall Assembly

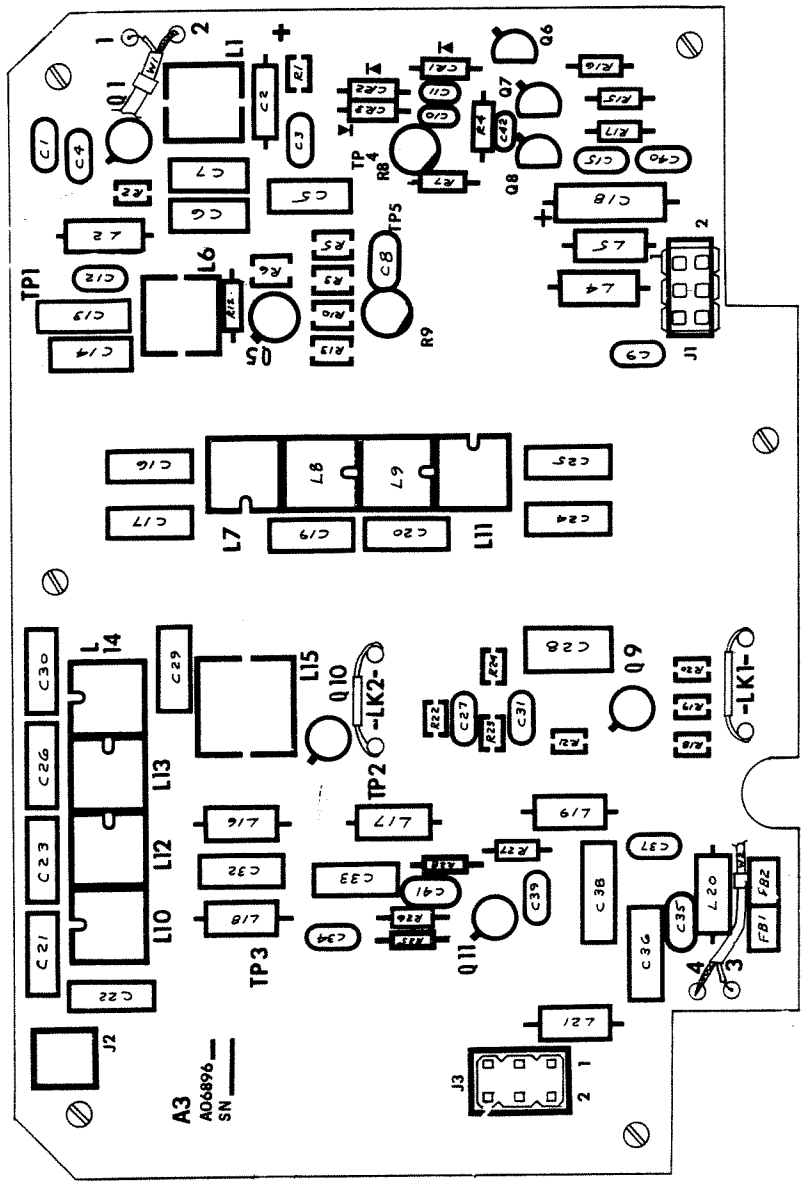


Figure 4-4B. Second Mixer, A3 Circuit Card Assembly

3. Set the analyzer control as follows:

Center Frequency	34 MHz
Horizontal Scale	1 MHz/div
Vertical Scale	10 dB/div
Vertical Range	10 dB/div
Filter BW	50 kHz

4. Set the tracking generator output to −10 dBm.

5. Align the coils L10, L12, L13 and L14 for maximum response at 34.000 MHz. starting with L12.

   NOTE: It is not likely that a smooth single peaked response will be obtained. A double peaked response should be aligned so that HF peak is at 34.000 MHz with the frequency of the lower peak between 33 and 33.8 MHz.

6. Ensure that the response of the filter conforms to Figure 4-5.

7. Disconnect the tracking generator and connect the 34.000 MHz source from the test fixture.

8. Carefully adjust L10 only for peak output displayed on the analyzer.

9. Ensure that the peak output level is not less then +2 dBm. Record this level.

4.4.3 35.4 MHz Amplifier Alignment

1. Check for 1.1 ±0.01 Volts measured at TP-4. If not at this value set R-8 to obtain this value.

2. Set R-9 fully counterclockwise.

3. Connect the tracking generator to the input connector via a 20 dB 50 Ω attenuator.

4. Connect the analyzer to LK 1 using the Hi-Z probe and ground clip to TP2.

5. Set the analyzer controls as follows:

Center Frequency	35.4 MHz
Horizontal Scale	1 MHz/div
Vertical Scale	10 dB/div
Vertical Range	10 dB/div
Filter BW	50 kHz

6. Align L1 and L6 for maximum response at 35.4 MHz.

7. Align L7, L8, L9 and L11 for maximum response at 35.4 MHz adjusting the tracking generator output level as necessary.

8. Repeat steps (6) and (7) adjusting for maximum response at 35.4 MHz with best symmetry at ±1 MHz. Ignore the response at 34 MHz due to the 34 MHz second mixer drive signal.

9. Ensure that for a maximum output at 35.4 MHz of −30 dBm, the output level of the tracking generator does not exceed −38 dBm, use the stepped attenuator to decrease the output of the tracking generator to −38 dBm. Record results.

4.4.4 1.4 MHz Amplifier Alignment

1. Disconnect the tracking generator from the test fixture and replace it with a stable 35.4 MHz signal generator.

2. Set the signal generator to 35.4000 MHz for CW output at a level of −63 dBm.

3. Set the analyzer controls as follows:

Center Frequency	1.4 MHz
Horizontal Scale	0.2 MHz/div
Vertical Scale	0 dB/div
Vertical Range	10 dB/div
Filter BW	50 kHz

NOTE: The analyzer is now set so that the graticule is calibrated directly in dBm.

4. Connect the analyzer using the Hi-Z probe to the output of the A3 board under test pin E-3.

5. Adjust L15 for maximum output indicated by the analyzer trace.

6. Ensure that the indicated level at the analyzer is greater than -12 dBm. Record results.

7. Adjust R-9 for a level indicated by the analyzer of -15 dBm.

8. Transfer the Hi-Z probe to the TP-3. Ensure that the level indicated is -25 dBm ±1dB. Record this level on the test data sheet.

9. Set analyzer center frequency to 35.4 MHz.

10. Measure the signal level at E-1 (35.4 MHz input). Ensure that this is -60 dBm ±1 dB. Check on test data sheet.

11. Transfer the probe to TP5. Record level indicated by the analyzer on test data sheet.

12. Transfer the probe to TP1. Record level indicated by the analyzer on test data sheet.

13. Transfer the probe to LK1. Record level indicated by the analyzer on test data sheet.

4.4.5 AGC Check

1. Set the analyzer center frequency to 1.4000 MHz.
2. Connect the Hi-Z probe to E-3 on the A3 board.
3. Switch the AGC control to position 1.
4. Connect the digital multimeter to the AGC MONITOR terminals.
5. Adjust the AGC control for a voltage reading of 1.70 Volts. Ensure that the output indicated by the analyzer is −20 dBm ±1 dB. **Record results.**
6. Adjust the AGC control for a voltage of 2.40 Volts. Ensure that the output indicated by the analyzer is −50 dB ±5 dB. **Record results.**
7. Switch AGC control to position 2 and ensure output is again −50 dB ±5 db.

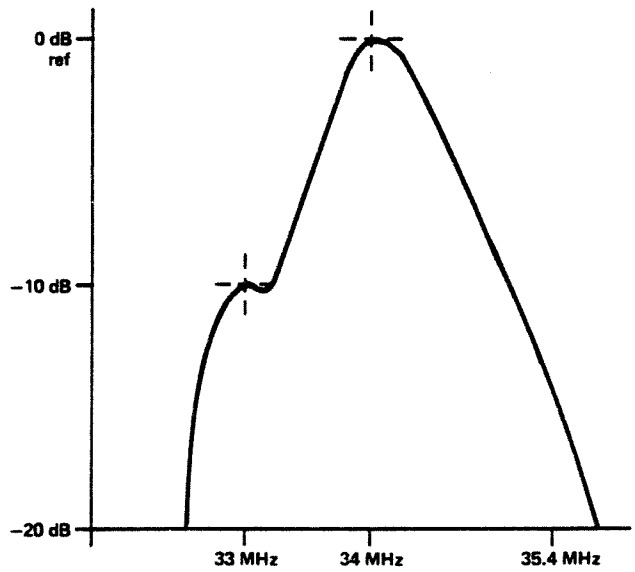


Figure 4-5. 34 MHz Filter Response Curve

Note: This diagram is for guidance and shows only the approximate position of the response at 33 MHz.

4.4.6 CORRECTIVE ACTION

If the above procedures have failed to produce predicted or desired results trace signals to the fault. As indicated by the fault symptoms, trace through the 34 MHz filter, the 34.5 MHz IF stages, the AGC stages, the 35.4 MHz filter, the mixer stages and/or the output stage. Refer to the module schematic diagram, Figure 4-2, and Figures 4-4A and 4-4B for location of circuitry and components. Use the oscilloscope, as required, to trace signals.

Repair circuitry and/or replace faulty components. Care must be taken to avoid overheating semiconductor and sensitive components when soldering or unsoldering. Use a clip-on heatsink or a pair of pliers on the device leads before applying heat.

After repair, repeat the procedures in sections 4.4, as required, to assure that the module is aligned and operating correctly.

4.5 PARTS LIST, SECOND MIXER, A3

The parts list for the A3 circuit card is contained in Table 4-2.

DATE _____ MODULE A3

CKD BY _____ USED ON _____

TEST DATA SHEET

PART NAME: A3 Second Mixer Board JOB NO: _____

PART NUMBER: 06896 SERIAL NO: _____

USED ON: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
4.4.2.9	34 MHz Drive Level (Output LK2)		+2		dBm
4.4.3.9	35.4 MHz Gain (Input for -30 dBm Out)		-50	-38	dBm
4.4.4.6	Overall Gain (Max)		-12	-5	dBm
4.4.4.8	Level at TP3		-26	-24	dBm
4.4.4.10	Input Voltage (E1)		-61	-59	dBm
4.4.4.11	Level at TP5				dBm
4.4.4.12	Level at TP1				dBm
4.4.4.13	Level at LK1				dBm
4.4.5.5	Level at 1.4 MHz OUT (1.70 Volts)		-21	-19	dBm
4.4.5.6	Level at 1.4 MHz OUT (2.40 Volts)		-55	-45	dBm

TABLE 4-2. PARTS LIST, SECOND MIXER ASSEMBLY (A3) 06896

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 8	Capacitor, Ceramic 470 pF, ±10%	21737	831-000-X5F0-471K
C2	Capacitor, Tantalum, 1 uF, ±20%, 35V	25034	CS13BF105M
C3, 12	Capacitor, Ceramic, 0.001 uF, ±20%	21747	832-000-X5T-102M
C4, 15, 27, 31, 34, 35, 37, 39, 41	Capacitor, Ceramic, 0.01 uF, +80% −20%	21740	805-000-Z5V0-103Z
C5	Capacitor, Mica, 150 pF, ±2%	22101	CM05FD151G03
C6	Capacitor, Mica, 39 pF, ±2%	22100	CM05ED390G03
C7	Capacitor, Mica, 390 pF, ±2%	22105	CM05FD391G03
C9, 40	Capacitor, Ceramic, 0.033 uF, +80% −20%	21744	5705-000-X5F-333M
C10, 11, 42	Capacitor, Ceramic, 0.01 uF, ±20%	21733	8121-050-651-103M
C13	Capacitor, Mica, 470 pF, ±2%	22114	CM06FD471G03
C14, 21, 30, 32	Capacitor, Mica, 100 pF, ±2%	22109	CM05FD101G03
C16, 23, 24, 26	Capacitor, Mica, 82 pF, ±2%	22108	CM05ED820G03
C17, 22, 25, 29	Capacitor, Mica, 330 pF, ±2%	22117	CM05FD331G03
C18	Capacitor, Tantalum, 15 uF, ±20%, 20V	25035	CS13BE156M
C19, 20	Capacitor, Mica, 68 pF, ±2%	22107	CM05ED680G03
C28	Capacitor, Mica, 1800 pF, ±2%	22148	CM06FD182G03
C33	Capacitor, Mica, 47 pF, ±2%	22112	CM05ED470G03
C36, 38	Capacitor, Polycarbonate, 0.1 uF, ±20%, 10V	26871	C280MCF/A100K
CR1	Diode	35530	1N143
CR2, 3	Diode	35537	HP 5082-3080
FB1, 2	Ferrite Bead	45051	Mullard FX1242
J1, 3	Connector, Control	06846-3	
J2	Connector, Coaxial, 34 MHz input	60044	700209-002
L1	Coil Variable	05953	
L2	Choke, Fixed, 10 uH	43029	MS14046-4
L4, 5, 19	Choke, Fixed, 47 uH	43032	MS90538-4

TABLE 4-2. PARTS LIST, SECOND MIXER ASSEMBLY (A3) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
L6	Coil, Variable	05931	
L7, 8, 9, 11	Coil, Variable	05948	
L10, 12-14	Coil, Variable	05949	
L15	Coil, Variable	05926	
L16, 18	Choke, Fixed, 100 uH	43033	MS90538-12
L17, 20, 21	Choke, Fixed, 1 uH	43024	MS18130-8
Q1	Transistor	32507	U310
Q2, 3, 4	Not Used		
Q5, 9, 10	Transistor	31500	2N918
Q6	Transistor	31508	2N4126
Q7, 8	Transistor	32021	2N5089
Q11	Transistor	31511	2N2222A
R1, 5, 18, 23	Resistor, Composition, 470 Ohms, ±5%	10655	RC07GF471J
R2, 3, 21, 22	Resistor, Composition, 100 Ohms, ±5%	10639	RC07GF101J
R4, 7, 16	Resistor, Metal Glaze, 1K Ohms, ±2%	12061	RL07S102G
R6	Resistor, Composition, 39K Ohms, ±5%	10701	RC07GF393J
R8	Resistor, Variable, 200 Ohms, ½W	16077	62P-R200
R9	Resistor, Variable, 500 Ohms, ½W	16025	62P-R500
R10	Resistor, Composition, 4.7K Ohms, ±5%	10679	RC07GF472J
R11, R14	Not Used		
R12	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R13	Resistor, Composition, 56 Ohms, ±5%	10633	RC07GF560J
R15, 17	Resistor, Metal Glaze, 4.7K Ohms, ±2%	12067	RL07S472G
R19, 24	Resistor, Composition, 6.8K Ohms, ±5%	10683	RL07GF682J
R20	Resistor, Composition, 1.5K Ohms, ±5%	10667	RC07GF152J
R25	Resistor, Metal Glaze, 1.2K Ohms, ±5%	12085	RL07S122G
R26	Resistor, Metal Glaze, 4.7K Ohms, ±5%	12020	RL07S472G
R27	Resistor, Film, 330 Ohms, ±2%, 1/4W	12161-331	RL07S331G
R28	Resistor, Film, 22K Ohms, ±2%, 1/4W	12161-223	RL07S223G

CHAPTER 5
IF FILTER, A4

5.1 THEORY OF OPERATION

The IF Filter module, A4, contains the crystal filters (and attenuator) which are used in the control of the received signal selectivity. A schematic diagram of the A4 module is shown in Figure 5-1. Six crystal filters and an attenuator are used for selecting one of the seven bands. Signal selection is effected by applying a ground to the appropriate selection line, J1 pins 1-5, 6 and 9. The seventh position, selected through J1 pin 9, makes use of a broadband, 5 dB, 5-pad attenuator, R1, R9, and R10, to simulate the insertion loss of the filter. In this position, the receiver selectivity is defined by the 8 kHz roofing filter (FL1) in the A2 module.

Since the selection circuit for each filter and the attenuator is the same, only one example is given, that of filter FL1.

A ground applied to pin J1-1 through E-11) is inverted by stage U2D. The output of U2D, through R23, applies +12 volts to the cathode of CR13. The +12 volts at "A" through R22 thus biases CR14 on and CR13 off. This allows the input signal into J1-A1, filtered through FL1, on through CR14 to drive output emitter follower stage Q1.

Since all other selection lines are at +12 volts, the corresponding diodes CR2, CR4, CR6, CR8, CR10 and CR12 are all biased off. This prevents the signals from the remaining filters FL2-6 and the attenuator from going through to drive Q1. Q1 output, through J1-A3, goes on to drive the following IF Amp. stage A5. Q1 stage provides a low output impedance for this drive.

5.2 IF FILTER, A4, TEST FIXTURE

Testing and troubleshooting of the IF Filter, A4, module is accomplished through the use of the RACAL If Filter (A4) Test Fixture and associated test equipment. The fixture connects to the module and provides for the selection of each of the six filters and the attenuator. Supply voltage to inputs to and outputs from the A4 module are supplied through the test fixture. A swept frequency, about 1.4 MHz (the IF frequency) is utilized to verify correct operation of each individual filter.

Figure 5-2 shows the RACAL IF Filter (A4) Test Fixture. Figure 5-3A shows the IF Filter module, A4, overall assembly while Figure 5-3B shows the module circuit card assembly.

5.3 TEST EQUIPMENT AND ACCESSORIES

Table 5-1 lists the test equipment required.

Table 5-1. List of Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	Spectrum Analyzer and Tracking Generator	Marconi TF2370 or HP141T Storage Display 8553B RF Section 8443A Tracking Generator
2	DC Power Supply	RACAL
3	Test Fixture	RACAL TF333
4	Oscilloscope	Tektronics 465

5.4 TESTING

Tests should be conducted at room temperature. Record data on test data sheet, page 5-10.

5.4.1 Preliminary Set-Up

1. Place the A4 Filter Module under test into the test fixture.

2. Connect the input plug from the test fixture to the module under test.

3. Preset the Spectrum Analyzer as follows:

Reference Frequency	Center
Counter Frequency	Past Center
Sweep Mode	Auto
Vertical Scale Range	1 or 2 dB/div
Store	High Defn (Medium Presistance on H-P)
Peak Mem	Off
Reference Frequency	1.4000 MHz
Vertical Scale	0 dBm
Horizontal Scale	Adjust range according to
Range	B.W. of filter being checked
Filter Bandwidth	Normal (2)
Sweep Speed	None selected

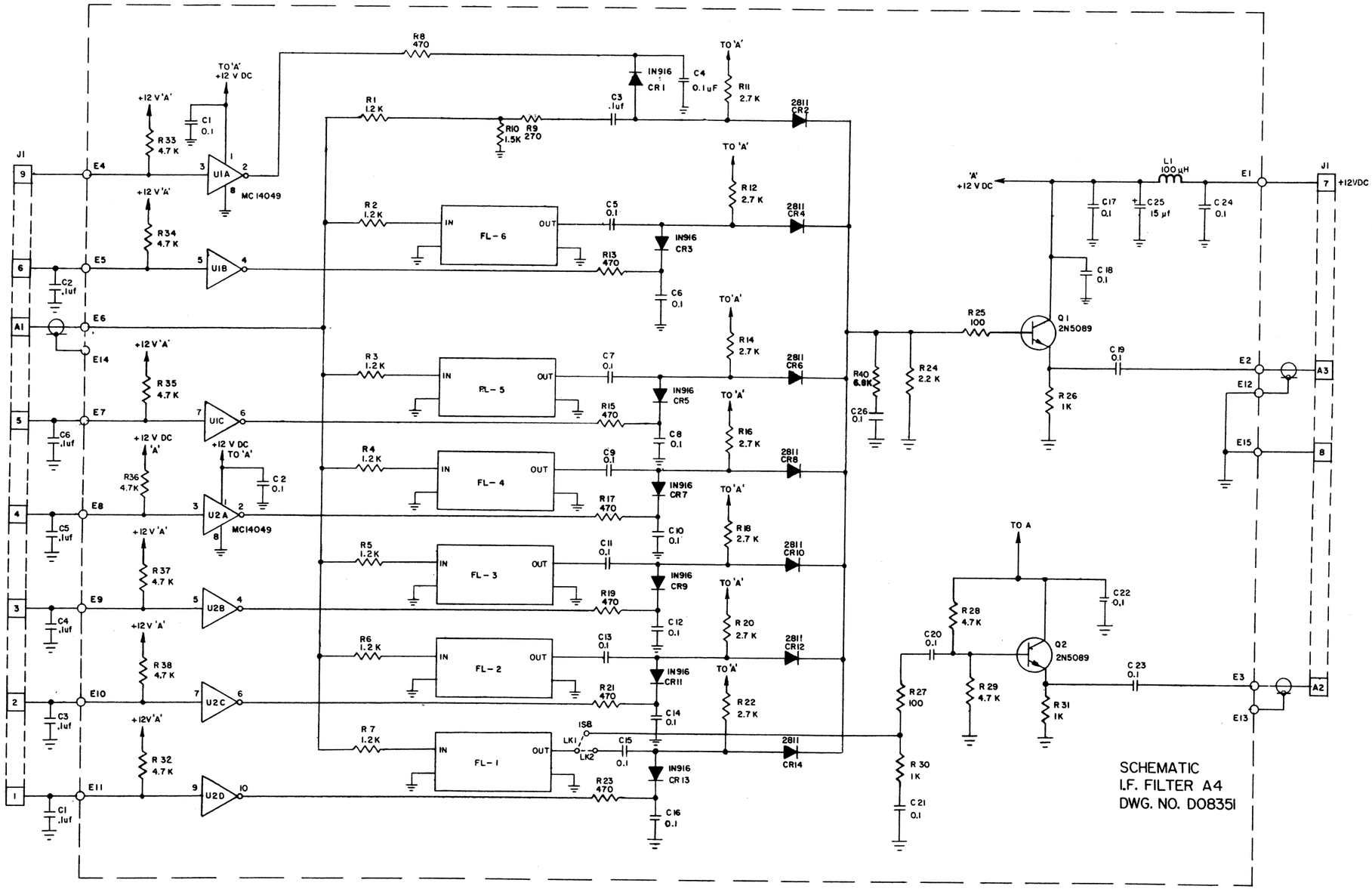
4. Connect the spectrum analyzer Tracking Generator output to the 1.4 MHz IN on the front of the test fixture via a coaxial T-connector at the test fixture port.

5. Connect a 50 ohm Coax Cable to the Spectrum Analyzer input and the Coaxial T-connector on the 1.4 MHz port on the test fixture.

6. Connect the power supply to the test fixture. Do not apply D.C. power to the test fixture at this time.

7. Set the FILTER SELECT switch to position 7.

8. Observe the reference level shown on the spectrum analyzer, and record on test data sheet.



UNLESS OTHERWISE NOTED
1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K = 1,000 M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MIROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN HENRIES.

Figure 5-1. Schematic Diagram, IF Filter, A4

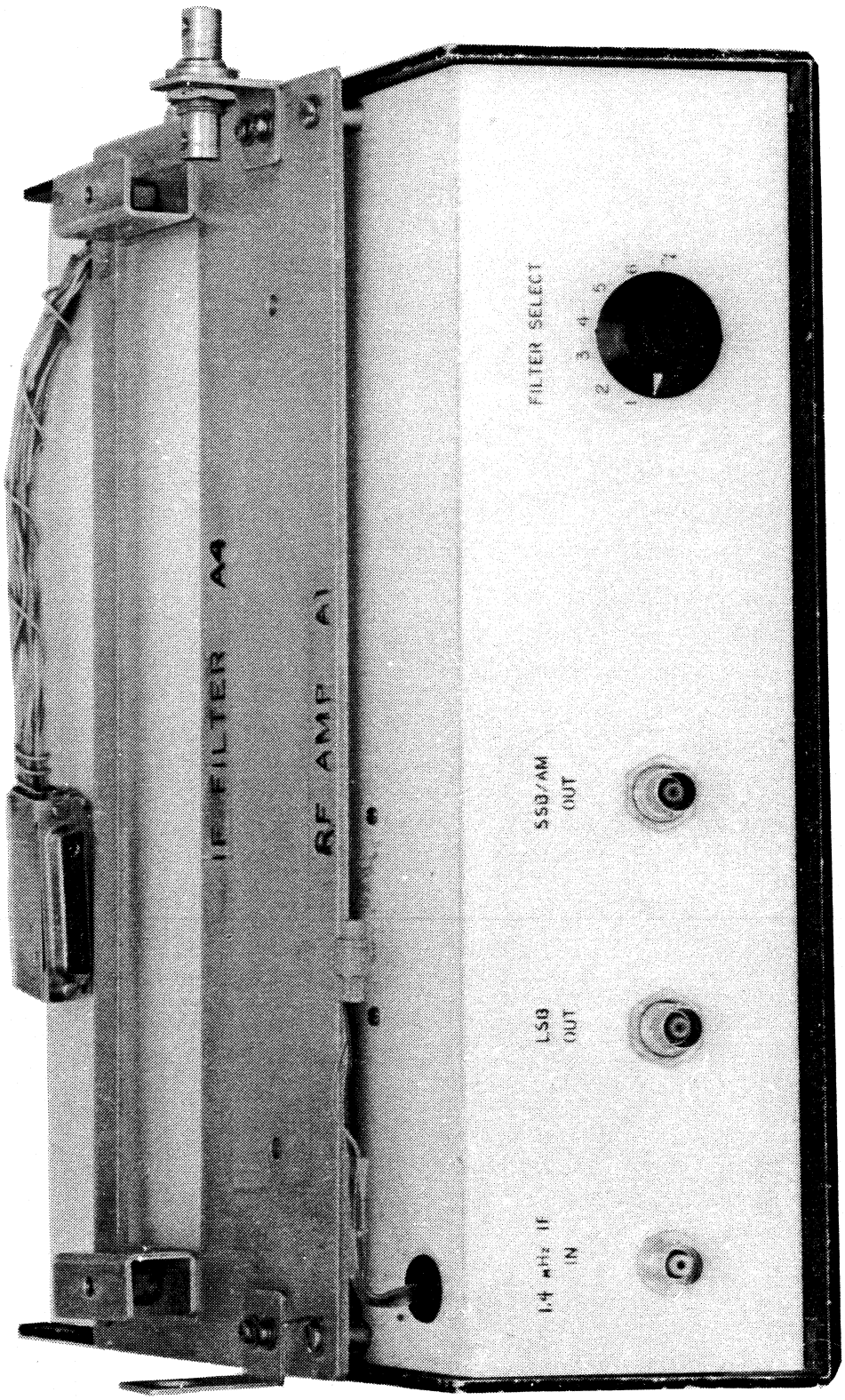


Figure 5-2. IF Filter A4, Test Fixture

5.4.2 IF Filter Response Check

1. Apply DC power to the test fixture.

2. Disconnect the 50 ohm Coax Cable on the Spectrum Analyzer input from the coaxial T-connector and reconnect this cable to the SSB/AM OUT port.

3. Observe and record the level shown on the spectrum analyzer. Ensure that this level is MORE than 6.5 dB and not LESS than 8.5 dB below the reference level noted in step 5.4.1(8) and record on test data sheet.

4. Set the spectrum analyzer as follows:

   Press store A and then Display A and Display B. This sets the reference to determine the insertion loss. For the H-P Analyzer, set the IF Gain Vernier for 0 dB (top of screen), indication.

5. Verify the requirements in Table 5-2 by the following steps:

   5.1 Filter 1 response test.

   5.1.1 Set FILTER SELECT Switch on test fixture to 1 position.

   5.1.2 Note the difference between the top of the response waveform and the insertion loss reference level as noted in step 3 above. Record.

   5.1.3 Change Spectrum Analyzer setting as follows:

Counter Frequency	Bright Line (Marker mode on H-P)
Vertical Scale Range	1 or 2 dB per division
Sweep Mode	Man

   5.1.4 Move bright line to the left and right for 3 dB point bandwidth in the similar mode. Note the 3 dB bandwidth on test data sheet.

   5.1.5 Measure the peak to peak ripple between the two 3 dB points. Record.

   5.1.6 To measure the 60 dB point bandwidth, change the Spectrum Analyzer settings as follows:

Counter Frequency	Past Center
Sweep Mode	Auto
Vertical Scale Range	10 dB/div
Vertical Scale	–45 dBm

   5.1.7 Adopting the BRIGHT LINE and MAN sweep mode, place the bright line at 60 dB points (6 cm from the top of waveform).

   5.1.8 Calculate the bandwidth and record on test data sheet.

   5.1.9 Ensure that the level outside the bandwidth is less than 60 dBm maximum. Record results.

   5.2 The response test of the rest of filters are done in exactly the same manner. Follow Table 5-2 for proper settings. Record all results.

6. Temporarily connect the Tracking Generator OUT from the spectrum analyzer to pin 11 of Link 2 in the A4 module under test.

7. Connect the spectrum analyzer input to the LSB OUT port on the front of the test fixture.

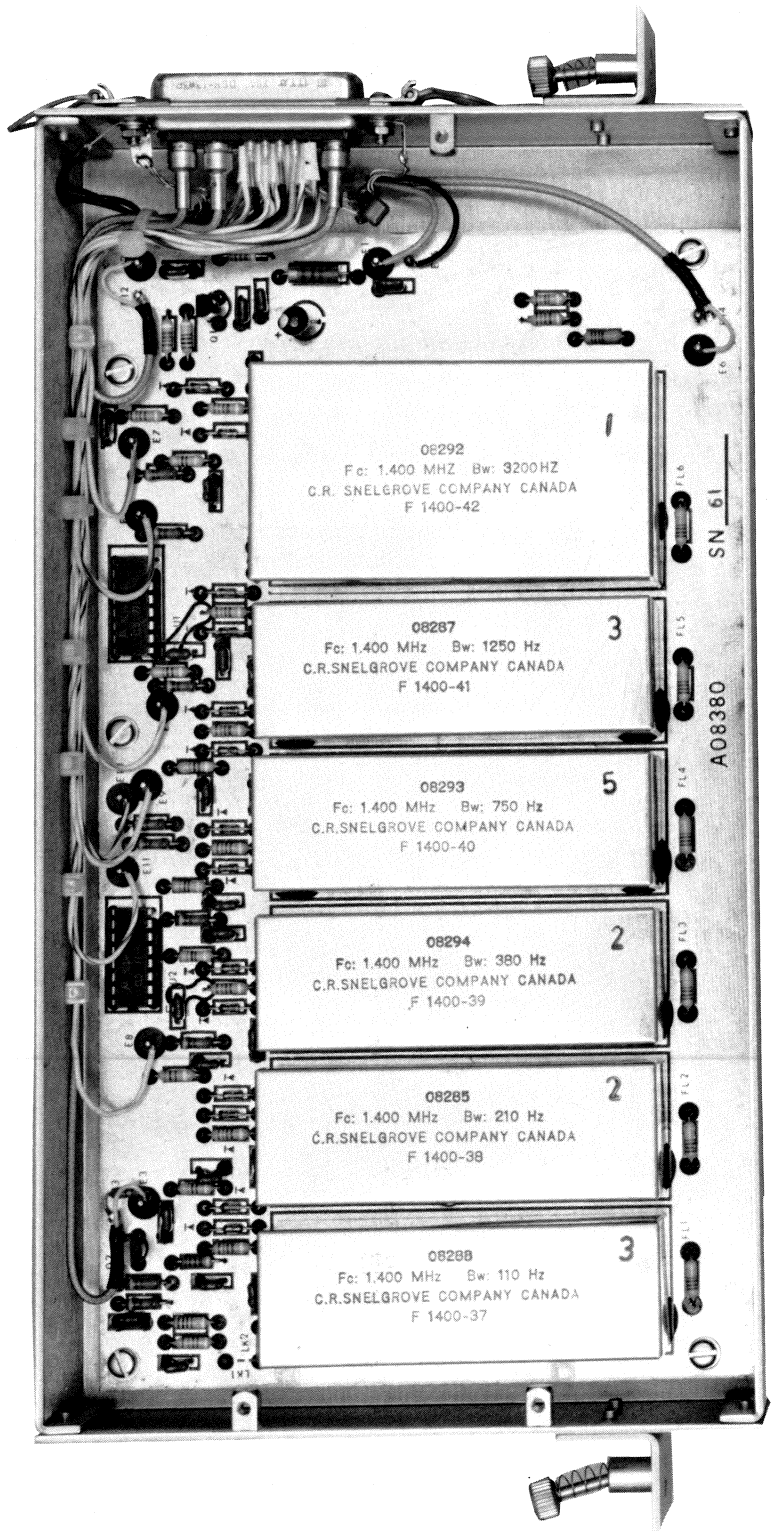


Figure 5-3A. IF Filter A4, Overall Assembly

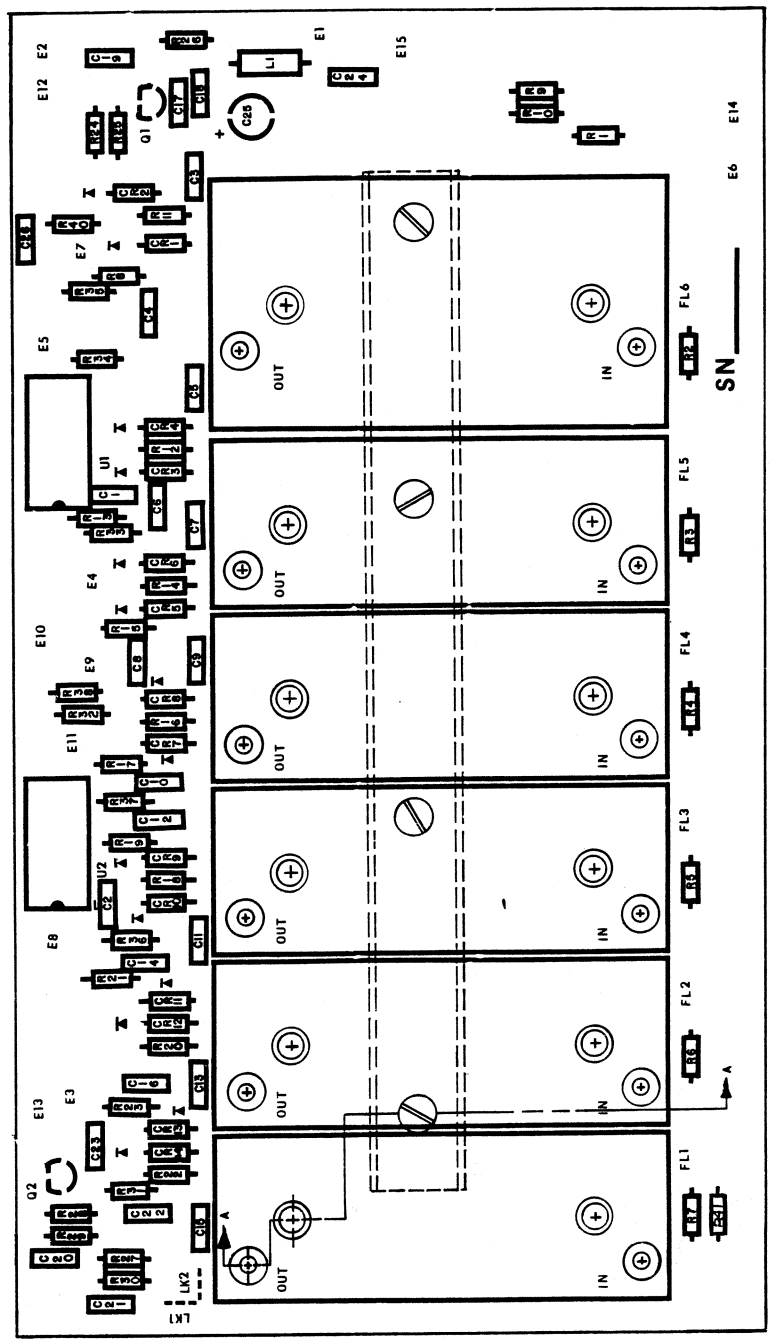


Figure 5-3B. IF Filter A4, Circuit Card Assembly

8. Observe the level on the spectrum analyzer. It should be within the limits of –4 dBm to –7 dBm. Record on test data sheet.

9. Turn off the DC power supply to the test fixture and remove the A4 module under test.

Table 5-2. RA6778C Filter Response Characteristics

Filter Select No.	Insertion Loss dB	3 dB (min.) Bandwidth	60 dB (max.) Bandwidth	Filter Response Characteristics
1	±2	110 Hz	420 Hz	Peak to peak ripple, 3 dB within 3 dB bandwidth. Differential delay 4000 secs. from -50 Hz to +50 Hz.
2	±2	210 Hz	670 Hz	Peak to peak ripple, 3 dB within 3 dB bandwidth. Differential delay 2000 secs. from -88 Hz to +88 Hz.
3	±2	380 Hz	1090 Hz	Peak to peak ripple, 3 dB within 3 dB bandwidth. Differential delay 1750 secs. from -150 Hz to +150 Hz.
4	±2	750 Hz	1880 Hz	Peak to peak ripple 3 dB, within 3 dB bandwidth. Differential delay 1000 secs. from -263 Hz to +263 Hz.
5	±2	1250 Hz	3120 Hz	Peak to peak ripple, 3 dB within 3 dB bandwidth. Differential delay 500 secs. from -438 Hz to +438 Hz.
6	±	3.2 Hz	4.6 kHz	Peak to peak ripple, 3 dB within 3 dB bandwidth. Differential delay 150 secs. from -1200 Hz to +1200 Hz.
7	0 Reference for insertion loss.	ALL	PASS	Resistive Pad on circuit card.

5.4.3 CORRECTIVE ACTION

If the above procedures have failed to produce predicted or desired results, a fault may be suspected. If faulty operation occurs only when one filter is switched in, then this filter is probably at fault and should be replaced. Otherwise trace signals to the fault. As indicated by the fault symptoms, trace through the filter selection circuitry and the output circuitry. Refer to the module schematic diagram, Figure 5-1, and Figures 5-3A and 5-3B for location of circuitry and components. Use the oscilloscope (item 4 of Table 5-1) as required, to trace signals.

Repair circuitry and/or replace faulty components. Care must be taken to avoid unsoldering. Use a clip-on heat sink or pair of pliers on the device leads before applying heat.

After repair, repeat the procedures in Section 5.4, as required, to assure that the module is operating correctly.

5.5 PARTS LIST, IF FILTER, A4

The parts list for the A4 module is contained in Table 5-3 while Table 5-4 contains the parts list for circuit card A4A1.

DATE _____
CKD BY _____

MODULE A4
USED ON _____

TEST DATA SHEET

PART NAME: A4 IF Filter Module
PART NUMBER: 08337
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS MIN	LIMITS MAX	UNITS
5.4.1.8	Reference Level		REFERENCE		dBm
5.4.2.3	Insertion Loss Reference Level		-8.5	-6.5	dB
5.4.2.5	Filter 150 Hz BW (C08288)	(LOW/HIGH)			
	Insertion Loss		-1	+1	dB
	3 dB Point BW	/	±55	–	Hz
	Peak to Peak Ripple within 3 dB BW		–	3.0	dB
	60 dB Point BW	/	–	+210	Hz
	Rejection outside 60 dB Points		60	–	dB
	Filter 250 Hz BW (C08285)				
	Insertion Loss		-1	+1	dB
	3 dB Point BW	/	±105	–	Hz
	Peak to Peak Ripple within 3 dB BW		–	3.0	dB
	60 dB Point BW	/	–	±335	Hz
	Rejection outside 60 dB Points		60	–	dB
	Filter 425 Hz BW (C08294)				
	Insertion Loss		-1	+1	dB
	Peak to Peak Ripple over 3 dB BW		–	3	dB
	3 dB Point BW	/	+190		Hz
	60 dB Point BW	/	–	±545	Hz
	Rejection outside 60 dB Points		60	–	dB
	Filter 750 Hz BW (C08293)				
	Insertion Loss		-1	+1	dB
	3 dB Point BW	/	+375	–	Hz
	Peak to Peak Ripple over 3 dB BW			3	dB
	60 dB Point BW	/		±940	Hz
	Rejection outside dB Points		60	–	dB

DATE _____
CKD BY _____

MODULE A4
USED ON _____

TEST DATA SHEET

PART NAME: A4 IF Filter Module (Continued)
PART NUMBER: _____
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
5.4.2.5	Filter 1.25 kHz BW (C08287)	(LOW/HIGH)			
(Cont.)	Insertion Loss		-1	+1	dB
	3 dB Point BQ	/	±625	–	Hz
	Peak to Peak ripple over 3 dB BW		–	3	dB
	60 dB Point BW	/	–	+1.56	kHz
	Rejection outside 60 dB points		60	–	dB
	Filter 3.2 kHz BW (C08292)				
	Insertion Loss		-1	+1	dB
	3 dB Point BW	/	±1.6	–	kHz
	Peak to Peak ripple over 3 dB BW		–	3	dB
	60 dB Point BW	/	–	±2.3	kHz
	Rejection outside 60 dB points		60	–	dB
	Output Level		-8	-4	dBm

TABLE 5-3. PARTS LIST, IF FILTER MODULE, A4

08337

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A4A1	IF Filter, Circuit Card Assembly (See Table 5-4 for further breakdown)	08380	
–	Module Case, Marking	08728	
–	Spring Latch Assembly	61188	
–	Cover, Module	06724-2	
J1	Connector, DBM-13W3P	61171	
J1A1	Cable Assembly, IF In	07149-4	
–	Connector, J1A1, J1A3	60021	
J1A2	Not Used		
J1A3	Cable Assembly, IF Out	07149-6	
W1	Cable Assembly	08939	

TABLE 5-4. PARTS LIST, IF FILTER CIRCUIT CARD ASSEMBLY, A4A1 08380

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-24, 26	Capacitor, Ceramic, 0.1 uF, ±20%, 50V	21732	8131-050-651-104M
C25	Capacitor, Electrolytic, 15 uF, ±20%, 20V	25062-156	
~~CR1-3,5,7,9,11,13~~	Diode	35514	1N916
CR2,4,6,8,10,12,14	Diode	36002	HP5082-2811
FL1	Filter, IF	08288	
FL2	Filter, IF	08285	
FL3	Filter, IF	08294	
FL4	Filter, IF	08293	
FL5	Filter, IF	08287	
FL6	Filter, IF	08292	
L1	Inductor, RF, 100 uH, ±5%	43033	
Q1, 2	Transistor, NPN	32021	2N5089
–	Pad Transistor, Q1, Q2	70752	7717-7NWHT
R1-7	Resistor, Film, 1.2K Ohms, ±2%, ¼W	12161-122	RL07S122G
R8, 13, 15, 17, 19, 21, 23	Resistor, Film, 470 Ohms, ±2%, ¼W	12161-471	RL07S471G
R9	Resistor, Film, 270 Ohms, ±2%, ¼W	12161-271	RL07S271G
R10	Resistor, Film, 1.5K Ohms, ±2%, ¼W	12161-152	RL07S152G
R11, 12, 14, 16, 18, 20, 22	Resistor, Film, 2.7K ohms, ±2%, ¼W	12161-272	RL07S272G
R24	Resistor, Film, 2.2K Ohms, ±2%, ¼W	12161-222	RL07S222G
R25, 27	Resistor, Film, 100 Ohms, ±2%, ¼W	12161-101	RL07S101G
R26, 30, 31	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R28, 29, 32-28	Resistor, Film, 4.7K Ohms, ±2%, ¼W	12161-472	RL07S472G
R40	Resistor, Film, 6.8K Ohms, ±2%, ¼W	12161-682	RL07S682G
U1, 2	Integrated Circuit, Hex Inverter Buffer	36576	MC14049
–	Printed Wiring Board	08355	

CHAPTER 6
IF/AF ASSEMBLY, A5

6.1 THEORY OF OPERATION

Figure 6-1 is a simplified block diagram of the IF/AF Assembly, A5, with the schematic diagram shown in Figure 6-2. It contains the 1.4 MHz second IF amplifier, the audio and AGC detectors and the audio amplifiers. An envelope detector is provided for AM reception, and a product detector for all other reception modes. The output from the AGC detector is used to control the gain of both the first and second IF amplifier stages. It is also available at a terminal on the rear panel. This AGC detector output is normally connected to the AGC BUS output at the rear panel connector, but may be used separately for test purposes. The audio output from the preamplifier is applied to the line amplifier and to the phone amplifier, which drives the phone jack and is also applied, through an ON/OFF switch, to the front panel loudspeaker.

6.1.1 Input Amplifier

The 1.4 MHz IF signal from the filter assembly is applied to an integrated circuit gain-controlled amplifier, U1. This device contains two amplifier sections which, in this application, are connected in cascade to provide high gain and AGC range. The input signal is applied via C1 to pin 1, and the output from the first section, at pin 12, is applied via R3 and C7 to the input of the second section at pin 10. The output, taken from pin 7, is applied via a bandpass filter and C15 to an IF output amplifier composed of Q5, Q6 and Q7. The amplifier output from emitter-follower Q7 is provided through C19 and R17 to pin J1-A2 and from there to the A25 IF converter module.

6.1.2 AGC Detector and Amplifier Stages

The IF signal from the output of amplifier stage Q5 is applied through C13 to the AGC amplifier composed of Q1, Q2 and U2. Potentiometer R7 is used to establish the AGC threshold level by adjusting the base bias of Q1. Due to the filtering action of capacitors C67 and C68, the output of U2 will be a DC level which reflects the amplitude of the IF signal. When the IF amplitude increases, the positive increase in the output of U2 will be applied through diode CR1 to charge capacitors C70 and C72 through R77 and R78. This RC network determines the AGC attack time constant. The AGC voltage established across C70 and C72 is applied to buffer amplifier U3, which drives the AGC output line through R82.

The decay rate of the AGC voltage level in response to a decrease in IF amplitude is determined by selection signals operating through a decoder circuit consisting of U5, U8 and U10. When a logic 0 is applied to the L (long) select input, all inputs to decoder U5 (pins 10, 11, 13 and 9) are disabled. The AGC voltage level which was established by U2 through CR11 can only discharge through R72 and Q3, providing a relatively long time constant; this will be true regardless of the state of the NARROW B/W input. If the M, or medium, select signal is asserted, the resulting logic 0 applied to the A1 input of U5 will cause either the S1 or the S2 input to be selected (depending on the state of the NARROW B/W signal on the A0 input). In either case, the selected input will provide an additional discharge path for the AGC voltage through a 680K resistor (R74 or R75) U5 and Q3. This discharge path provides a medium decay time constant.

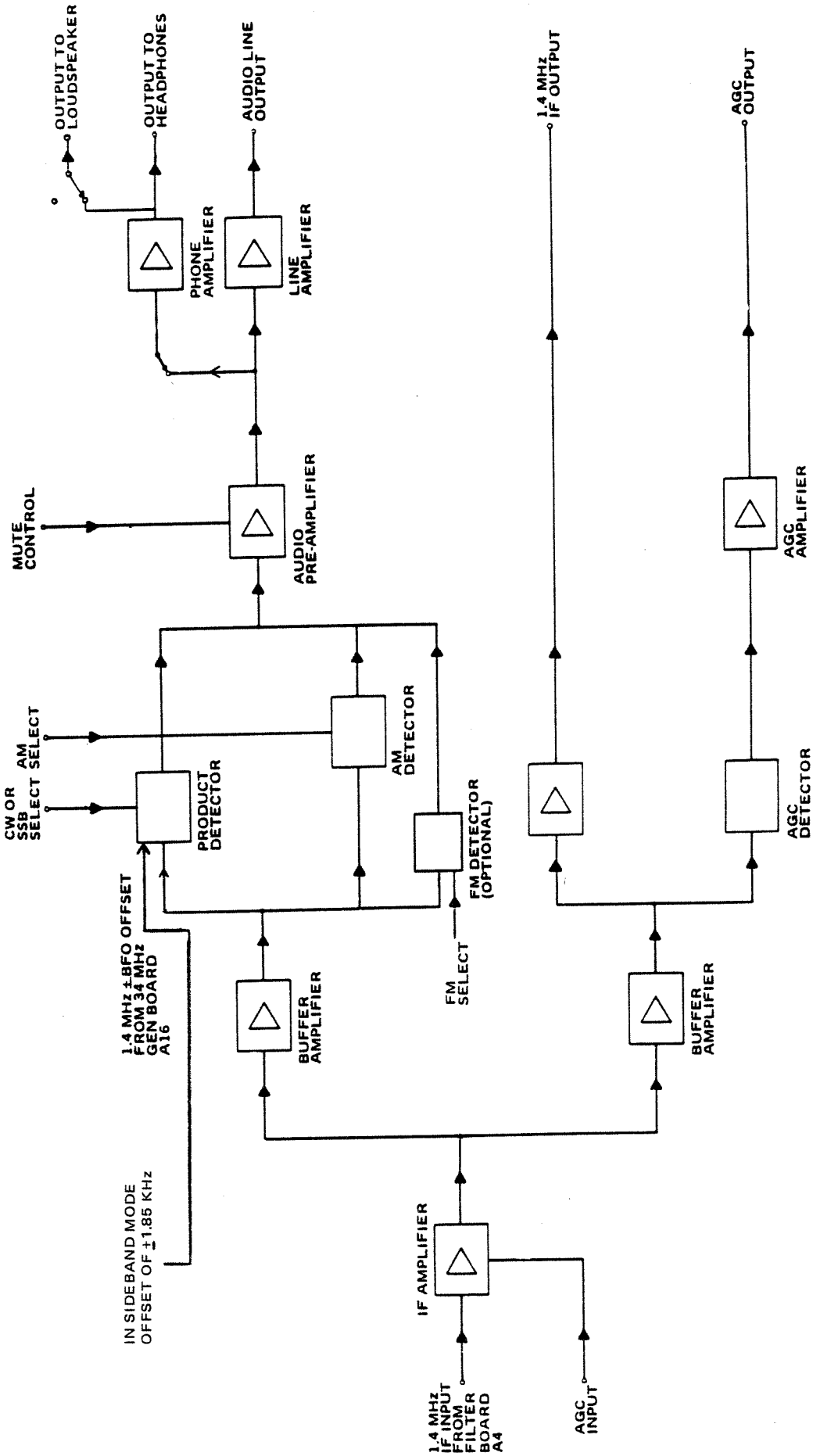


Figure 6-1. Simplified Block Diagram, IF Amplifier, A5

If neither the L nor the M time constant select inputs are asserted, a short time constant will be provided by selection of either R73 or R76 as the AGC discharge path (depending on the NARROW B/W signal) and by the action of NAND gates U10 and bilateral switch U8. The output of U10 will be low in response to high M and L inputs; this low applied to the switch control (A2) input of U8 will cause the ground path for C70 through the D2 and S2 switch connections to be opened. This removal of C70 from the AGC circuit shortens both the attack (change) and decay rates, to compensate for the time constant of the narrow filter.

Transistor Q3, with its base voltage established by divider R68/R69, supplies a negative voltage to pin 12 of U5 for the discharge of AGC voltage through the selected input path. Diode CR12 provides a bypass of R78 for discharging capacitors C70 and C72. Assertion of the DUMP input signal (low) provides an immediate discharge path for the AGC voltage through R81.

The AGC detector output on pin J1-17 is returned to pin J1-18 as the AGC BUS and after buffering by amplifier U4 is routed to the A3 module via pin J1-9. An R/C network consisting of R87 and C73 provides a delaying action in the application of AGC voltage to the A3 module when a short time constant is selected at decoder U5.

6.1.3 AM and SSB Detectors

The IF output from U1 and the bandpass filter is coupled to a buffer stage, Q8, via C14 and C15. The output from Q8, at TP4, is capacitance-coupled to both the AM detectors, via C21 and the SSB detectors, via C24.

The amplifier Q11, Q12 has a gain of about 12 dB to provide a suitable signal level for the low distortion AM detector CR1. C25 conducts components at 1.4 MHz to ground and further filtering is provided by L5, C31, C27, cut-off frequency being about 20 kHz. R56 provides for precise matching of AF output level with that of the product detector which consists of T1, CR2, CR3, CR4, CR5. A similar low-pass filter is used to remove the unwanted IF frequency.

A diode switching arrangement, controlled by the mode selection, is used to select the output from either the AM detector or the SSB detector. In the AM condition, a ground is applied to board pin J1-3. This is routed to CR7 via R40. The diode becomes forward-biased and a path is opened for the output from the AM detector to the audio preamplifier via C36. Diode CR6 remains reverse-biased and isolates the output from the SSB detector.

For SSB mode functions, the ground is transferred to board pin J1-2. Diode CR6 becomes forward biased and provides a path for the output from the SSB detector, while CR7 becomes reverse-biased and isolates the output from the AM detector.

6.1.4 FM Detector (option not fitted)

The IF signal from the output of Q8 is also applied through C1 to the base of emitter-follower Q1, and from there to integrated circuit FM detector/demodulator U1. The components associated with FM detection are located on a separate module (A1) mounted on the main board. When a ground is applied to the FM select input, the output of the FM demodulator will be enabled through CR2 and applied to the audio preamplifier, Q15.

6.1.5 Audio Pre-Amplifier

The output from the selected detector is applied to a high gain impedance-matching amplifier, Q15 and Q16. The amplifier output is applied to the preset A.F. line level control via pin J1-5 and is also passed to the A.F. Gain Control via PIN J1-15.

The base voltage of Q16 is controlled by the D3 output of bilateral switch U8, which will supply a −7V level to mute the audio output whenever the A3 input of U8 goes high. The A3 control input to U8 is supplied by the Q output of monostable multivibrator U9. U9 produces a 30 ms positive output, muting the audio output, whenever a positive or negative transition occurs at the "1 MHz" input (J1-1). The "1 MHz" signal is derived from the LSB of the 1 MHz frequency code, and transfers whenever a frequency change involving this code is made. This feature provides momentary muting of the receiver audio whenever the receiver frequency setting is changed.

6.1.6 Audio Line Amplifier

The output of the audio preamplifier is applied through the line-level control to board pin 22 and the input of audio line amplifier U7. U7 drives the audio line through transformer T2.

6.1.7 Phone/Speaker Amplifier

The output of the audio preamplifier is applied through the audio gain control to board pin 24, and to the phone amplifier, U6. The output of U6 is applied to the front panel phone jack and loudspeaker.

6.2 IF/AF ASSEMBLY, A5, TEST FIXTURE

Troubleshooting and alignment of the IF/AF assembly, A5, is accomplished through the use of the RACAL IF/AF Amplifier (A5) test fixture and associated test equipment. The test fixture provides a convenient base to mount the A5 module for testing, while also providing easy access to all areas of the PC board. All input and output ports are located on the rear apron of the test fixture, with all controls located on the front apron.

The front apron controls for the module, control the AF gain, mode, AGC time constant, MGC, and bandwidth. Enclosed within the test fixture is a spectrally clean 1.4 MHz signal source for carrier re-insertion in SSB mode. All associated test equipment is interfaced to the test fixture via BNC chassis mounted connectors. Figure 6-3 shows the IF/AF assembly A5 test fixture. Figure 6-4A shows the overall assembly of the A5 module, while Figure 6-4B shows the circuit card assembly.

6.3 TEST EQUIPMENT AND ACCESSORIES

To perform troubleshooting and alignment, using the test fixture, requires the use of additional test equipment and accessories. This additional equipment is used to inject signals, provide power, monitor signals and their levels, make connections and to signal trace. The test equipment and accessories required are listed in Table 6-1.

6-4 TEST AND ALIGNMENT

The following procedures contain all the information necessary to completely test the A5 module.

All tests should be conducted at room ambient temperature. Record results on the test data sheets, pages 6-20 and 6-21.

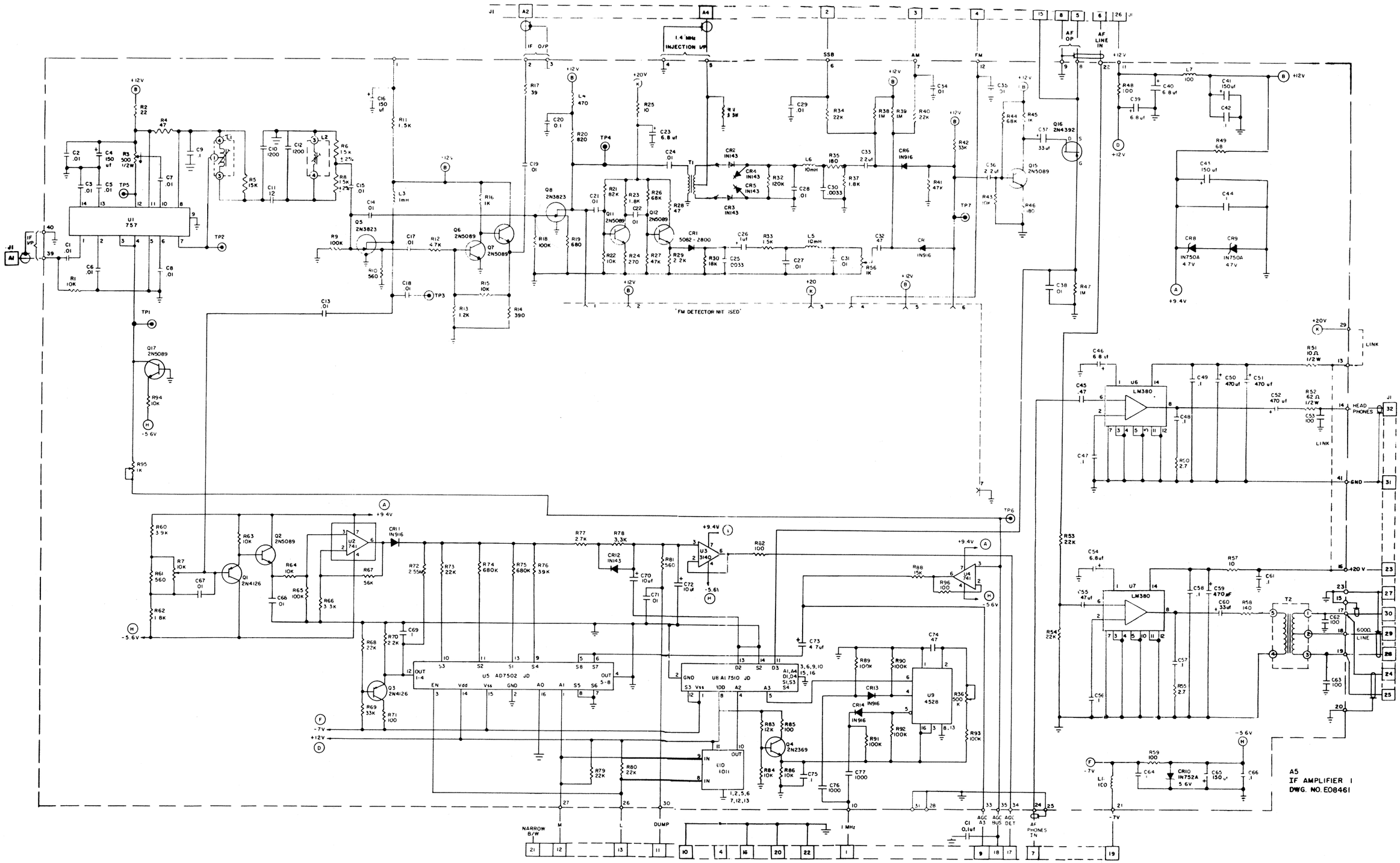


Figure 6-2. Schematic Diagram, IF/AF Assembly, A5

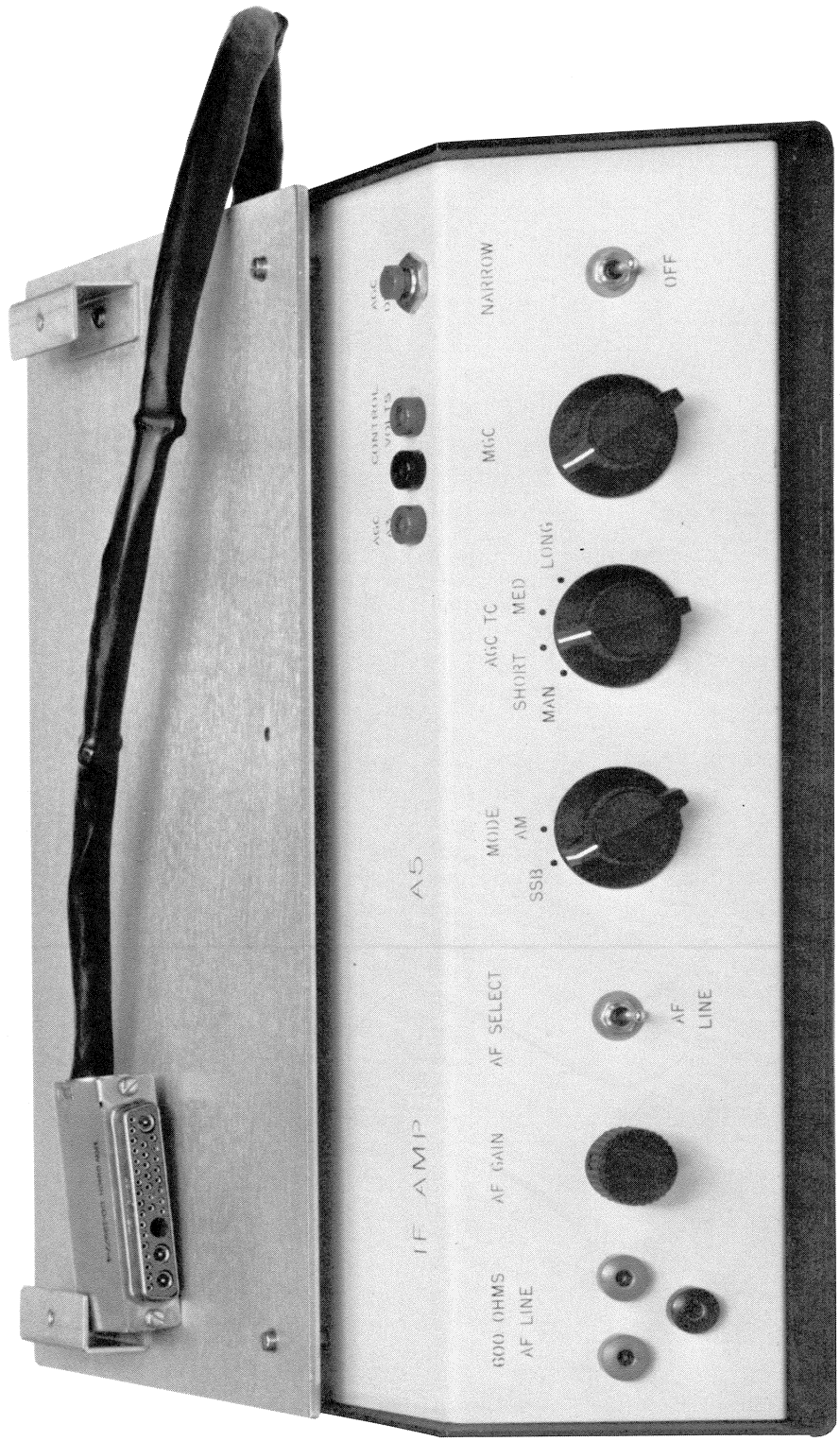


Figure 6-3. IF/AF Assembly A5, Test Fixture

Table 6-1. Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	Spectrum Analyzer	HP141T, 8552B or 8553B
2	Tracking Generator	HP8443A
3	Oscilloscope	Tektronix 465
4	RF Multivoltmeter	Boonton 91H
5	Distortion Analyzer	HP332A
6	Digital Multimeter	Data Precision 248
7	RF Generator	Logimetrics 921A
8	Coaxial Cables	RG-58 (50 ohms)
9	AGC TC Box	Racal 08863
10	AF Match Box	Racal 08046
11	DC Power Supply	Racal
12	Test Fixture	Racal TF334

6.4.1 IF Amplifier Alignment

1. Ensure the DC power supply is off.
2. Set the AF SELECT switch on the test fixture to AF LINE position.
3. Set the AGC switch on the test fixture to SHORT position.
4. Set the MODE switch on the test fixture to the AM position.
5. Install the A5 module under test into the test fixture making the necessary connections.
6. Set the following controls on the A5 module under test as follows:

R3	CCW
R7	CCW
R56	CCW
R95	CCW

7. Connect the tracking generator of the spectrum analyzer to the IF IN port located on the rear apron of the test fixture. Set the output of the tracking generator to −70 dBm.
8. Connect the spectrum analyzer to the IF OUT port on the rear apron of the test fixture. Switch the DC power on to the test fixture.
9. Adjust the spectrum analyzer controls as follows:

Center Frequency	1.4000 Hz
Bandwidth	3 kHz

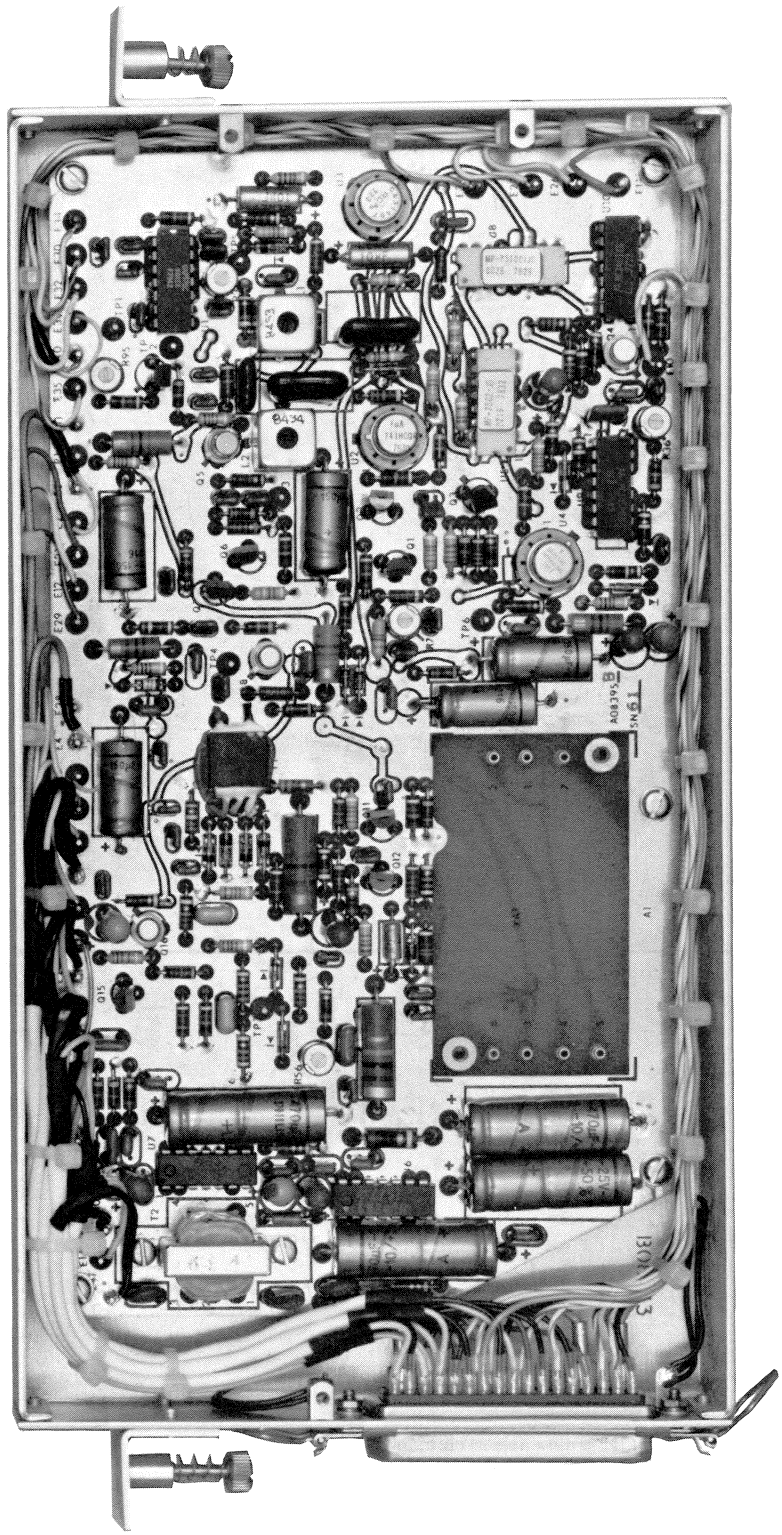


Figure 6-4A. IF/AF A5, Overall Assembly

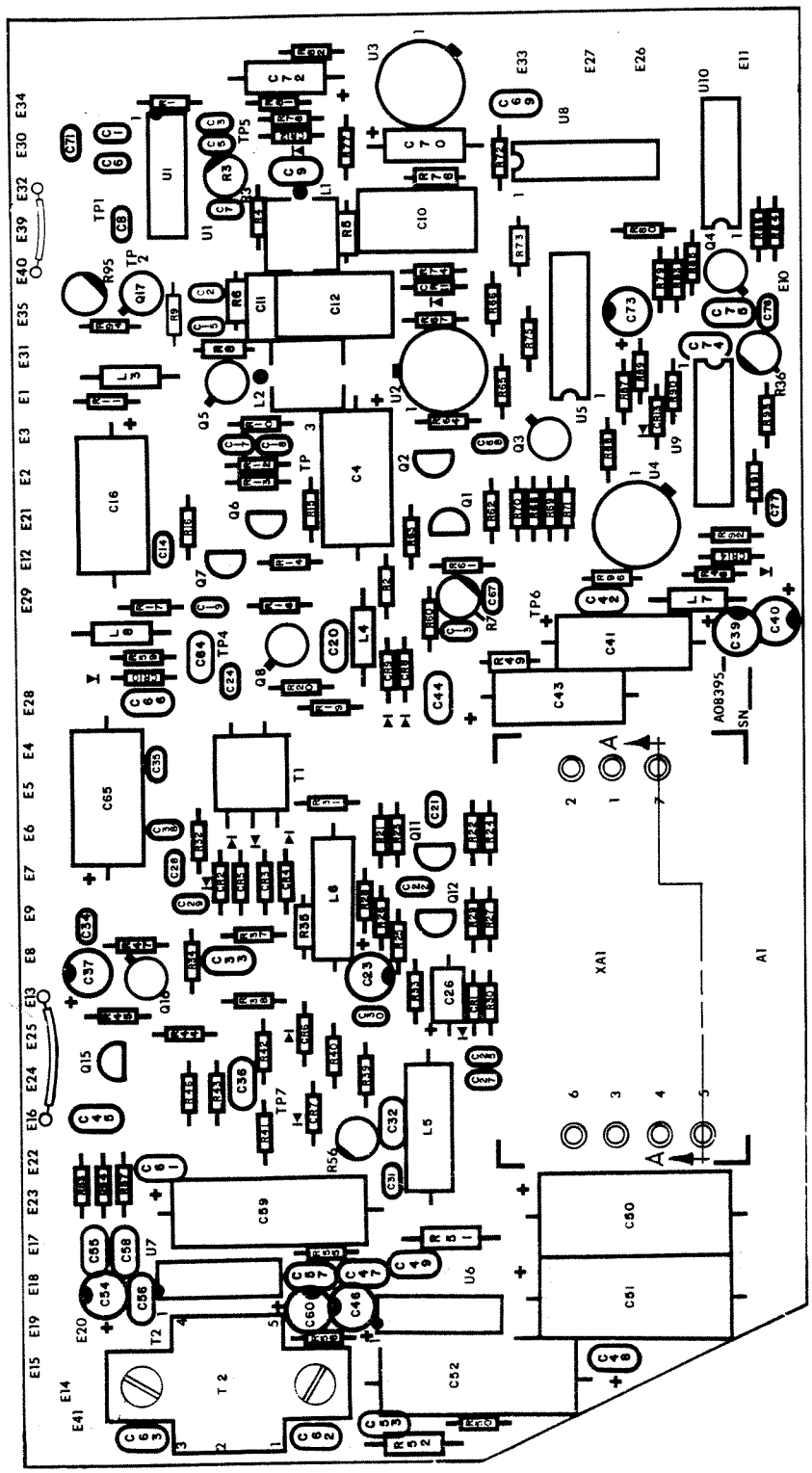


Figure 6-4B. IF/AF A5, Circuit Card Assembly

Scanwidth	10 kHz
Time	5 mSec/div
Input Attenuator	−10 dB
Log REF Level	−10 dBm
Scale	2 dB Log

10. Adjust the tracking generator of the spectrum analyzer for an output level to obtain a response on the analyzer. Adjust L1 and L2 for a peak response at 1.4 MHz. Ensure that the final shape conforms to the limits prescribed in Figure 6-5. (This is only for the −3 dB points).

11. Adjust the spectrum analyzer controls as follows:

Scanwidth	.05 MHz
Time	10 mSec/div
Input Attenuator	−10 dB
Log REF Level	0 dBm
Scale	10 dB Log

12. Check the −20 dB points on Figure 6-5. **Record on test data sheet.**

13. Adjust the output level of the tracking generator on the spectrum analyzer so the response indicated by the spectrum analyzer is at the −10 dBm level. Ensure that the tracking generator output level is less than −65 dBm. **Record on test data sheet.**

14. Set the spectrum analyzer scanwidth control to zero. Reset the frequency to 1.4000 MHz. if necessary.

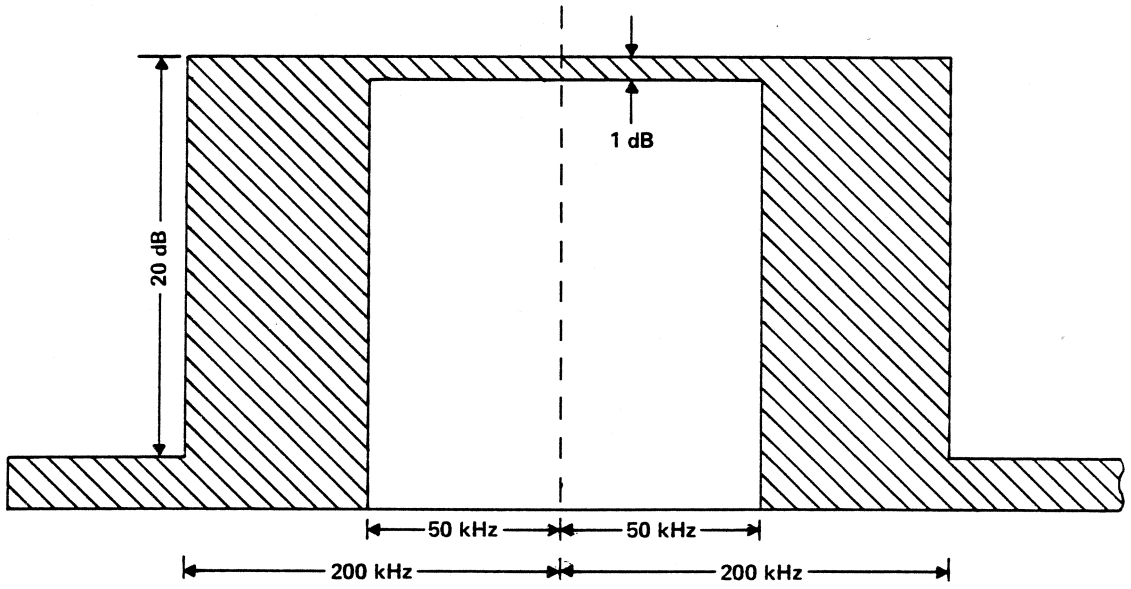


Figure 6-5. Passband Characteristics

15. Set the output level of the tracking generator to –68 dBm. Connect the RF Millivoltmeter using a Hi-Z adapter to TP3. Adjust R3 on the A5 board under test for an indicated output level of 200 mV on the RF Millivoltmeter. Record indicated level.

    Note: This adjustment is important and care must be taken to ensure an absolute accuracy within the limits specified on the test data sheet.

16. Disconnect the spectrum analyzer RF IN port.

17. Disconnect the RF Millivoltmeter from TP3 and connect it to the IF OUT port on the rear apron of the test fixture using a 50 ohms adapter. Record the level indicated on the RF Millivoltmeter and ensure that it is within the limits specified on the test data sheet.

6.4.2 AGC Adjustment

1. Connect the digital multimeter (10 VDC scale) between ground and the CONTROL VOLTS test point on the test fixture. Adjust R7 to obtain a reading of 1.40 ±0.05 Volts on the digital multimeter. Record the voltage on the test data sheet.

2. Increase the Tracking Generator output level by 6 dB to -62 dBm and adjust R95 on the A5 board under test for a reading of 1.56 Volts on the digital multimeter.

3. Return the Tracking Generator level to -68 dBm and ensure that the digital multimeter reading is within the limits of 1.40 ±0.05 Volts. Record on test data sheet.

4. Note the RF Millivoltmeter reading on the dB scale; increase the tracking generator output level by 50 dB to -18 dBm. Ensure that the new RF Millivoltmeter reading is less than 3 dB above the level noted. Record on the test data sheet.

5. Record the voltage level at the CONTROL VOLTS test point indicated by the digital multimeter. Ensure that it is between 2.000 and 3.000 Volts.

6. Record the voltage level at the AGC A3 test point indicated by the digital multimeter. Ensure that it is the same as in step 5.

7. Using the Rx 1K resistance position of the digital multimeter, connect the leads between ground and U5 pin 5 or 6. Ensure that the measured resistance is less than 500 ohms. Record results.

8. Set the AGC TC control on the test fixture to MED and ensure the resistance measured is greater than 10 megohms using the Rx 10m position. Now set the AGC TC control to LONG and ensure the resistance is still greater than 10 megohms. Record results.

9. Set the digital multimeter to 10 VDC scale. Check the DC voltage at pin 12 of U5 to ground (across R70). Ensure voltage is between –1.95 Volts and –2.1 Volts DC. Record.

10. Connect the spectrum analyzer RF IN port to the IF OUT port located on the rear apron of the test fixture.

11. Connect the AGC TC box as shown in Figure 6-6.

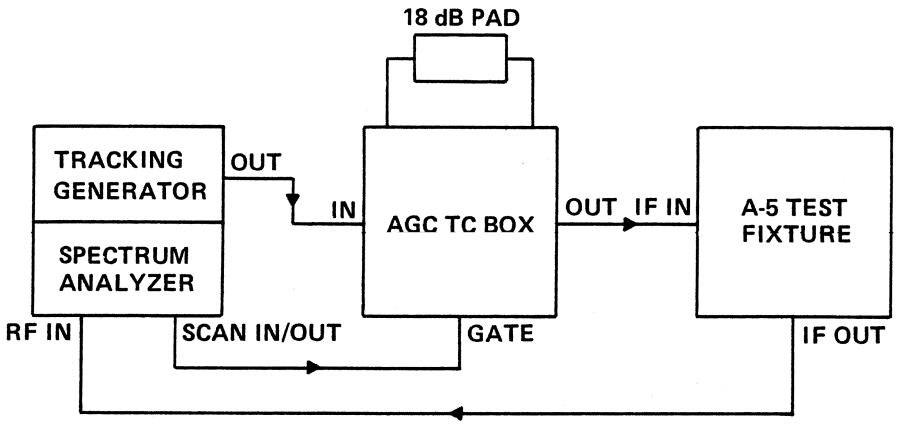


Figure 6-6. Equipment Set-Up Diagram, AGC Adjustment

12. Set the tracking generator output level to 0 dBm.

13. Set the spectrum analyzer controls as follows:

Center Frequency	1.4000 MHz
Bandwidth	300 kHz
Scanwidth	Zero
Input Attenuator	−10 dB
Log REF Level	+10 dBm
Scale	2 dB Log
Display Adjust	As Required
Video Filter	Off
Scan Time	5 mSec/div

14. Set the AGC TC box for ATTACK.

15. Set the AGC TC switch on the test fixture to SHORT position.

16. Set the NARROW switch on the test fixture to the NARROW position.

17. Observe the trace on the spectrum analyzer and set it as in Figure 6-7, using the HORIZONTAL control on the AGC TC box and the Display adjust control on the spectrum analyzer. Record the time frame (t) shown in Figure 6-7.

18. Set the spectrum analyzer for single sweep at maximum persistance. Erase the trace on the display screen if necessary.

19. Set the AGC TC switch on the test fixture to MED position and trigger one sweep of the spectrum analyzer. Record the time (t) as shown in Figure 6-7. Erase the sweep on the spectrum analyzer. (Slight adjustments may be necessary to relocate the trace properly).

20. Set the AGC TC switch on the test fixture to LONG and repeat step 19. Record.

Note: This Time Frame is the time interval between the initial rise and when the signal is within 1 dB of its final value.

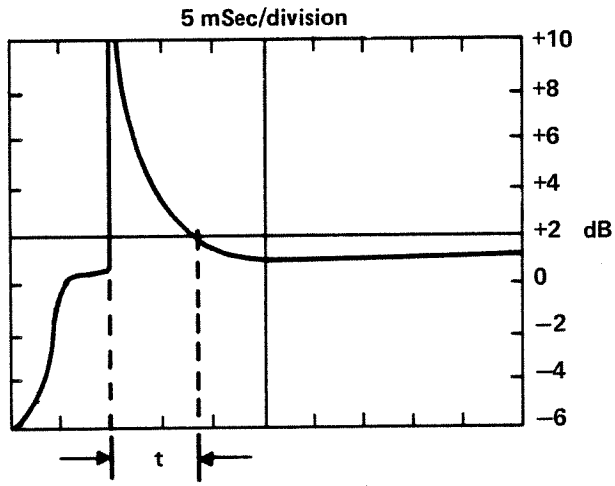


Figure 6-7. Attack Time Constant

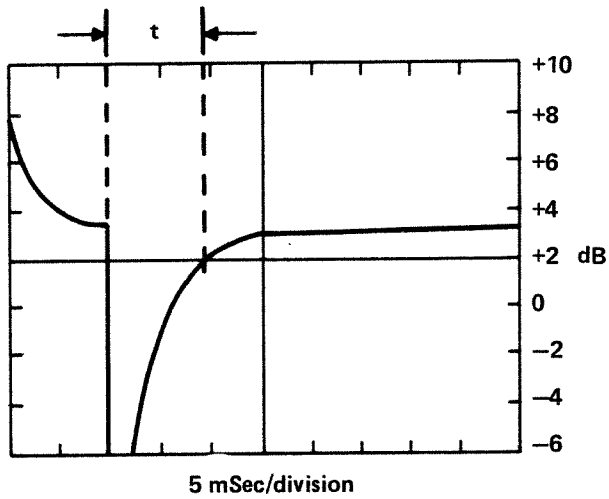


Figure 6-8. Decay Time Constant

21. Set the spectrum analyzer for a continuous sweep and medium persistance.

22. Set the AGC TC box to DECAY and the AGC TC switch on the test fixture to SHORT. Adjust the Display Adjust control on the spectrum analyzer as required to relocate the trace on the screen.

23. Repeat step 19, utilizing Figure 6-8. **Record on test data sheet.**

24. Set the NARROW switch on the test fixture to the OFF position.

25. Repeat step 19, utilizing Figure 6-8. **Record results.**

26. Set the NARROW switch on the test fixture to the NARROW position.

27. Set the AGC TC switch on the test fixture to the MED position.

28. Set the spectrum analyzer scan time to 50 mSec/div.

29. Observe the trace and record the time for the signal to return to within 1 dB of its final value. See Figure 6-8. **Record on the test data sheet.**

30. Set the NARROW switch on the test fixture to the OFF position. **Repeat step 29. Record.**

31. Set the spectrum analyzer scan time to 1 sec/div.

32. Set the AGC TC switch on the test fixture to LONG position. Repeat step 29. Adjust the persistance and Display as necessary.

33. Disconnect the AGC TC box and reconnect the tracking generator output to the IF IN port located on the rear apron of the test fixture.

34. Set the tracking generator output level to −14 dBm. Set the spectrum analyzer Display Adjust to zero, scan mode to INT and scan time to 5 mSec/div.

35. Set the AGC TC switch on the test fixture to MAN position. Set the Log REF switch on the spectrum analyzer to 0 dB.

36. Adjust the MGC control on the test fixture for an indicated IF output level of −10 dBm on the spectrum analyzer. See note after step 20.

37. Measure the DC voltage on the CONTROL VOLTS test point on the test fixture. Ensure that this reading is between 2.300 and 2.500 volts. **Record results.**

38. Set the AGC TC switch on the test fixture to the SHORT position and set the Log REF control on the spectrum analyzer to +10 dBm. Depress the DUMP switch on the test fixture. Ensure that the voltage measured at the CONTROL VOLTS test point falls to less than 1 volt and the output indicated by the spectrum analyzer rises to a level greater than 0 dBm. **Record on test data sheet.**

6.4.3 AF Output Level Check

1. Set the controls on the test fixture as follows:

AF Select	AF Line
Mode	SSB

2. Connect the AF Distortion Analyzer to the RED terminals on the test fixture using the AF Match Box. Use the Voltmeter position of the AF Distortion Analyzer. See Figure 6-9.

3. Set the AF Match Box to the OUT position.

4. Set the controls of the Signal Generator to 1.401 MHz with an output level of **-30 dBm.**

5. Connect the signal generator to the IF IN port on the rear apron of the test fixture.

6. Adjust the AF Gain control on the test fixture for an indication of 1.0 Volt as indicated on the AF Distortion Analyzer in the voltmeter position.

7. Set the AF Match Box switch to the IN position. Ensure the AF output level on the AF Distortion Analyzer falls to 0.5 V RMS. Confirm that the Audio Tone is approximately 1000 Hz using the oscilloscope. Record on test data sheet.

8. Reverse the BNC-Banana adapter in the AF Line terminals. Ensure that the AF output does not change by more than ±0.5 dB. Record on test data sheet.

9. Set the AF Match Box switch to the OUT position.

10. Change the connection between the test fixture and the AF Match Box so that one RED and BLACK terminal of the AF Line port on the test fixture is used. Ensure that the AF output level as indicated on the Distortion Analyzer is 0.5 ±0.02 Volt. Record.

11. Change the connection between the test fixture and the AF Match Box so that the other RED terminal and BLACK terminal is used. Ensure that the AF output level as indicated by the Distortion Analyzer is 0.5 ±0.02 Volt. Record.

12. Return the BNC-Banana adapter to the two RED terminals on the test fixture and set the AF Match Box to the IN position.

6.4.4 AF Distortion Check

1. Set the following controls:

Signal Generator	
Frequency	1.40100 MHz
Output Level	–30 dBm
Mod Select	CW
Test Fixture	
AF SELECT	AF LINE
NARROW	OFF
AGC TC switch	SHORT

2. Ensure that a 1000 Hz tone is present on the AF LINE terminals of the test fixture utilizing the oscilloscope.

3. Adjust the AF GAIN control on the test fixture for an indication of 1 mWatt on the AF Distortion Analyzer. (Note: +10 dB = 1 mWatt on HP332). Do not disturb the setting of the AF Gain control on the test fixture while measuring the AF Distortion. Measure the AF distortion of the A5 module under test. Record results.

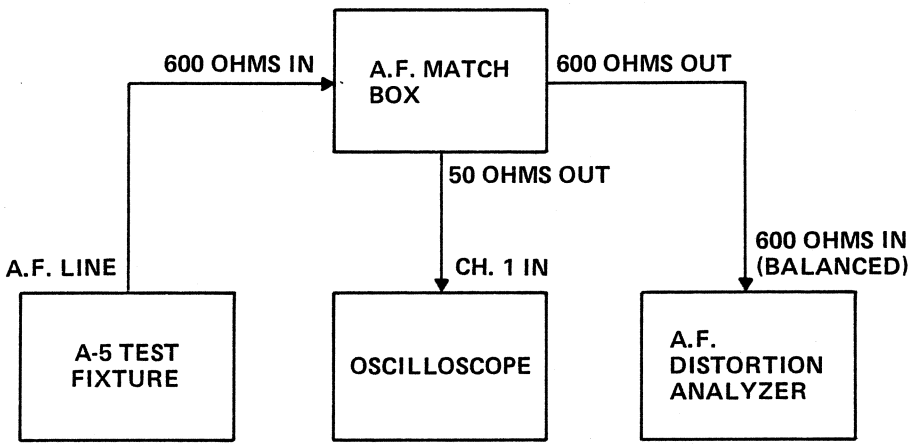


Figure 6-9. Equipment Set-Up Diagram, AF Output Level Check

4. Set the MOD SELECT switch on the signal generator to INT 1 kHz position and adjust the MOD LEVEL CONTROL to 30% at 1000 Hz. Set the MODE switch on the test fixture to the AM position.

5. Reset the signal generator to 1.4000 MHz.

6. Ensure that a 1000 Hz tone is present and set R56 for an AF output level of +11 dB on the AF voltmeter of the AF Distortion Analyzer. Record on test data sheet.

7. Increase the signal generator output level to –9 dBm. Set the % Modulation to 75% at 1000 Hz.

8. Adjust the AF GAIN control on the test fixture for a 1 mWatt level reading on the AF voltmeter of the distortion analyzer. Measure the AF distortion of the A5 module under test. Record on test data sheet.

9. Disconnect the coaxial cable from the AF LINE terminals on the front of the test fixture and reconnect it to the AF 1 port on the rear apron of the test fixture. Set the AF SELECTOR switch on the test fixture to the AF 1 position.

10. Ensure that a 1 kHz tone is present and set the AF GAIN control on the test fixture for an output level of 1 mW.

11. Using the distortion analyzer measure the distortion using the 1 mWatt as reference. Record on test data sheet.

12. Increase the AF GAIN control on the test fixture to maximum. Ensure that the AF output level is at least 2 volts as indicated by the voltmeter of the distortion analyzer. Record. Return the AF GAIN control to the 1mWatt level. (1 mWatt = +10 dB.)

6.4.5 AF Frequency Response Check

1. Set the MODE switch on the test fixture to SSB position.

2. Set the signal generator to CW. Reconnect the high stability oscillator to the 1.4 MHz IN port on the rear apron of the test fixture. Set the signal generator to 1.401 MHz.

3. Set the AF SELECT switch on the test fixture to the AF LINE position.

4. Transfer the AF Coaxial cable from the AF1 port to the AF LINE port on the test fixture.

5. Set the AGC TC switch on the test fixture to the SHORT position.

6. Adjust the AF GAIN control to read 1 mWatt on the voltmeter of the distortion analyzer and ensure that a 1000 Hz tone is present.

7. Set the AGC TC switch on the test fixture to the MAN position and adjust the MGC control on the test fixture for a reading of 1 mWatt output on the voltmeter of the distortion analyzer.

8. Tune the signal generator between 1.400 and 1.420 MHz to locate the peak AF response. Reset the AF GAIN control on the test fixture for 1 mWatt, if necessary.

9. Tune the signal generator between 1.4002 MHz and 1.418 MHz. Ensure that at no frequency the AF output level falls -3 dB below the 1 mWatt reference level. Record on test data sheet.

6.4.6 AF Blank Check

1. Connect the AF BLANK port on the rear apron of the test fixture to the A-Gate BNC terminal located on the rear apron of the oscilloscope.

2. Connect the Channel 1 input of the oscilloscope to the 50 Ohms port on the AF Match Box.

3. Set the oscilloscope time base to 5 mSec/div and the vertical sensitivity to 50 mVolts/div.

4. Set the signal generator to 1.401 MHz.

5. Observe that the AF output indicated by the oscilloscope is zero for a specific time period. Adjust R36 so the period of time is 30 mSec. **Record results.**

6.4.7 Corrective Action

If any of the above tests fail to produce the required results, isolate the fault to a function (IF, AGC or audio) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function; for instance, steps 15, 16 and 17 in paragraph 6.4.1. could isolate a fault in the IF signal to amplifiers Q6, Q7 and associated components, if the results of step 15 are correct but step 17 is not. Further signal tracing may then be accomplished, using the oscilloscope or Voltmeters, to trace the fault to a single component. Maximum use should also be made of the test points provided on the A5 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductors, and other sensitive components when soldering. Use the proper wattage soldering iron; too much heat can cause damage to the circuit card and/or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 6.4.1 through 6.4.6.

6.5 PARTS LIST, IF/AF ASSEMBLY, A5

The parts list for the A5 module is contained in Table 6-2 while the parts list for circuit card A5A1 is contained in Table 6-3.

DATE _____
CKD BY _____

MODULE A5
USED ON _____

TEST DATA SHEET

PART NAME: A5 IF/AF Amplifier Board
PART NUMBER: 08339
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS MIN	LIMITS MAX	UNITS
6.4.1(12)	1.4 MHz BPF alignment satisfactory		pass	fail	
6.4.1(13)	Input for -10 dBm at IF OUT			-65	dBm
6.4.1(15)	Gain adjustment R-3 satisfactory		200	225	mV
6.4.1(17)	Signal level at IF OUT (50 ohms)		75	–	mV
6.4.2(1)	CONTROL VOLTS (R-7 adjustment)		1.35	1.45	Volts
6.4.2(3)	CONTROL VOLTS (-68 dBm IN)		1.35	1.45	Volts
6.4.2(4)	AGC Control Range (-68 to -18 dBm IN)		–	3	dB
6.4.2(5)	AGC CONTROL VOLTS (-18 dBm IN)		2.000	3.000	Volts
6.4.2(6)	AGC A-3		2.000	3.000	Volts
6.4.2(7)	U-5 ON resistance (C-73 NEG to Gnd) SHORT		–	500	Ohms
6.4.2(8)	U-5 OFF resistance (C-73 NEG to Gnd) MED				
	& LONG position on AGC TC switch		10	–	mOhms
6.4.2(9)	U-5 pin 12 to Gnd		-2.1	-1.95	volts
6.4.2(17)	AGC Time Constant SHORT attack			15	mSec
6.4.2(19)	AGC Time Constant MED attack			15	mSec
6.4.2(20)	AGC Time Constant LONG attack			15	mSec
6.4.2(23)	AGC Time Constant SHORT decay (Narrow)		45	50	mSec
6.4.2(25)	AGC Time Constant SHORT decay		45	50	mSec
6.4.2(29)	AGC Time Constant MED decay (Narrow)		.75	1.25	Sec
6.4.2(30)	AGC Time Constant MED decay		.75	1.25	Sec
6.4.2(32)	AGC Time Constant LONG decay		4	6	Sec
6.4.2(37)	CONTROL VOLTS (MAN)		2.300	2.500	Volts
6.4.2(38)	AGC DUMP Residual voltage		–	1.00	Volt
6.4.3(7)	Audio OUT LINE LEVEL 600 Ohms		488	512	mVOLT
6.4.3(8)	Line OUT Transformer Balance		Pass	Fail	
6.4.3(10)	Line OUT Transformer 300 Ohms		480	520	mVolt
6.4.3(11)	Line OUT Transformer 300 Ohms		480	520	mVolt

DATE _____ MODULE A5

CKD BY _____ USED ON _____

TEST DATA SHEET

PART NAME: A5 IF/AF Amplifier Board (Continued) JOB NO: _____

PART NUMBER: _____ SERIAL NO: _____

USED ON: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
6.4.4(3)	Audio Output Distortion (SSB)		–	-34	dB
6.4.4(6)	AM Detector functional		Pass	Fail	
6.4.4(8)	Audio OUTPUT Distortion (AM)		–	-34	dB
6.4.4(11)	Audio OUTPUT Distortion				
	(Phones Output)		–	-34	dB
6.4.4(12)	Phone Output Level		2.0	–	Vrms
6.4.5(9)	Audio Frequency Response				
	(250 Hz – 10 kHz)		–		dB
6.4.6(5)	AF Blank functional		Pass	Fail	

TABLE 6-2. PARTS LIST, IF AMPLIFIER MODULE (A5) 08339

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A5A1	IF Amplifier Circuit Card Assembly (See Table 6-3 for further breakdown)	08395	
–	Spring Latch Assembly	61183	
–	Cover,Module	06724-1	
J1	Connector DBM-36W4P	61167	
J1A1	Connector, IF In	60021	
J1A2	Connector, IF Out	60021	
J1A4	Connector, IF Out (Not Used)	60021	
W1	Cable Assembly	08930	

TABLE 6-3. PARTS LIST, IF AMPLIFIER CIRCUIT CARD ASSEMBLY (A5A1) 08395

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 2, 3, 5-8, 13-15, 17-19, 21, 22, 24, 27-29, 31, 34, 35, 38, 67, 68, 71	Capacitor, Ceramic, .01 uF, ±20% (Erie)	21733	8121-050-651-103M
C4, 16, 41, 43, 65	Capacitor, Electrolytic, 150 uF, +20%, −10% 16V (Mepco/Electra)	24053	ET151X016A5
C9, 20, 42, 44, 47, 48, 49, 56-58, 61, 64, 66, 69, 75	Capacitor, Ceramic, .1 uF, ±20% (Erie)	21732	8131-050-651-104M
C10, 12	Capacitor, Mica, 1200 pF, ±2%	22147	CM06FD122G03
C11	Capacitor, Mica, 12 pF, ±2%	22128	CM05G120G03
C23, 39, 40, 46, 54	Capacitor, Tantalum, 6.8 uF, ±20% (35V Dipped)	25032	T368B685M035AS
C25, 30	Capacitor, Ceramic, .0033 uF, ±10% (Erie) 50V	21723	8121-050-W5RO-332K
C26	Capacitor, Tantalum, 1 uF, ±20%, 35V	25034	CS13BF105M
C32, 45, 55, 74	Capacitor, Ceramic, .47 uF, ±20% (Erie) 50V	21761	8131-050-651-474M
C33, 36	Capacitor. Ceramic, 2.2 uF, ±20%(Erie)	21766	8141-050-651-225M7
C37,60	Capacitor, Tantalum, 33 uF, ±20% (Union Carbide)	25019	T368B336K010AS
C50, 51, 52, 59	Capacitor, Electrolytic, 470 uF, +100% −10%	24058	ET471X025A01
C53, 62, 63	Capacitor, Ceramic, 100 pF, ±10% (Erie)	21763	831-000-X5FO101K
C70, 72	Capacitor, Tantalum, 10 uF, ±5%	25055	T110B106J020AS
C73	Capacitor, Tantalum, 4.7 uF, ±20% (Dipped)	25042	T3628475K035AS
C76, 77	Capacitor, Ceramic, .001 uF (Erie) ±20%	21756	8101-050-651-102M
CR1	Diode (HP)	36003	5082-2800
CR2-5, 12	Diode	35530	1N143
CR6, 7, 11, 13, 14	Diode	35514	1N916
CR8, 9	Diode	33542	1N750A
CR10	Diode	33543	1N752A
L1	Coil, RF Variable	08433	
L2	Coil, RF Variable	08434	
L3	Choke, 1 mH	43038	MS90539-15
L4	Choke, 470uH	43037	MS90539-7
L5, 6	Choke, 10 mH	43042	MS90541-11
L7, 8	Choke, 100 uH	43033	MS90538-12
Q1, 3	Transistor	31508	2N4126
Q2, 6, 7, 11, 12, 15, 17	Transistor	32021	2N5089
Q4	Transistor	32255	2N2369
Q5, 8	Transistor	32511	2N3823
Q9, 10, 13, 14	Not used		
Q16	Transistor	32505	2N4392
R1, 15, 22, 43, 63, 64, 84, 94	Resistor, Metal Glaze, 10K Ohms, ±2%, ¼W	12071	RL07S103G
R2	Resistor, Composition, 22 Ohms, ±5%, ¼W	10623	RC07GF220J
R3	Resistor, Variable, 500 Ohms, ½W (Beckman)	16025	62P-R500
R4, 28	Resistor, Composition, 47 Ohms, ±5%, ¼W	10631	RC07GF470J
R5, 6, 88	Resistor, Metal Glaze, 15K Ohms, ±2%, ¼W	12073	RL07S153G
R8, 11, 33	Resistor, Metal Glaze, 1.5K Ohms, ±2%, ¼W	12119	RL07S152G

TABLE 6-3. PARTS LIST, IF AMPLIFIER CIRCUIT CARD ASSEMBLY (A5A1) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R7	Resistor, Variable, 10K Ohms, ½W (Beckman)	16023	62P-R10K
R9, 18, 65, 93	Resistor, Metal Glaze, 100K Ohms, ±5%, ¼W	12024	RL07S104J
R10, 81	Resistor, Composition, 560 Ohms, ±5%, ¼W	10657	RC07GF561J
R12	Resistor, Metal Glaze, 4.7K Ohms, ±2%, ¼W	12067	RL07S472G
R13	Resistor, Composition, 1.2K Ohms, ±5%, ¼W	10665	RC07GF122J
R14	Resistor, Composition, 390 Ohms, ±5%, ¼W	10653	RC07GF391J
R16	Resistor, Composition, 1K Ohms, ±5%, ¼W	10663	RC07GF102J
R17	Resistor, Metal Glaze, 39 Ohms, ±2%, ¼W	12091	RL07S390G
R19	Resistor, Metal Glaze, 680 Ohms, ±2%, ¼W	12059	RL07S681G
R20	Resistor, Metal Glaze, 820 Ohms, ±2%, ¼W	12060	RL07S821G
R21	Resistor, Metal Glaze, 82K Ohms, ±2%, ¼W	12105	RL07S823G
R23, 37, 62	Resistor, Metal Glaze, 1.8K Ohms, ±2%, ¼W	12062	RL07S182G
R24	Resistor, Metal Glaze, 270 Ohms, ±2%, ¼W	12136	RL07S271G
R25, 57	Resistor, Composition, 10 Ohms, ±5%, ¼W	10615	RC07GF100J
R26, 44	Resistor, Metal Glaze, 68K Ohms, ±2%, ¼W	12080	RL07S683G
R29	Resistor, Metal Glaze, 2.2K Ohms, ±2%, ¼W	12063	RL07S222G
R30	Resistor, Metal Glaze, 18K Ohms, ±2% , ¼W	12074	RL07S183G
R31	Resistor, Composition, 3.3K Ohms, ±5%, ¼W	10675	RC07GF332J
R32	Resistor, Composition, 120K Ohms, ±5%, ¼W	10713	RC07GF124J
R34, 40, 79, 80	Resistor, Composition, 22K Ohms, ±5%, ¼W	10695	RC07GF223J
R35, 46	Resistor, Metal Glaze, 180 Ohms, ±2%, ¼W	12137	RL07S181G
R36	Resistor, Variable, 500K Ohms (Beckman)	16086	62P-R500K
R38, 39, 47	Resistor, Composition, 1M Ohms, ±5%, ¼W	10735	RC07GF105J
R41, 27	Resistor, Composition, 47K Ohms, ±5%, ¼W	10703	RC07GF473J
R42	Resistor, Composition, 33K Ohms, ±5%, ¼W	10699	RC07GF333J
R45	Resistor, Metal Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R48, 59, 82	Resistor, Metal Glaze, 100 Ohms, ±2%, ¼W	12057	RL07S101G
R49	Resistor, Metal Glaze, 68 Ohms, ±2%, ¼W	12099	RL07S680G
R50, 55	Resistor, Composition, 2.7 Ohms, ±5%, ¼W	10601	RC07GF2R7J
R51	Resistor, Composition, 10 Ohms, ±5%, ½W	10915	RC20GF100J
R52	Resistor, Composition, 62 Ohms, +5%, ½W	10934	RC20GF620J
R53, 54, 68	Resistor, Metal Glaze, 22K Ohms, ±2% , ¼W	12075	RL07S223G
R56, 95	Resistor, Variable, 1K Ohms, ½W (Beckman)	16015	62P-R1K
R58	Resistor, Metal Film, 140 Ohms, ±1%, ¼W	12138	RN55D1400F
R60	Resistor, Metal Glaze, 3.9K Ohms, ±2%, ¼W	12066	RL07S392G
R61	Resistor, Metal Glaze, 560 Ohms, ±2%, ¼W	12058	RL07S561G
R66	Resistor, Metal Glaze, 3.3K Ohms, ±2% , ¼W	12065	RL07S332G
R67	Resistor, Metal Glaze, 56K Ohms, ±2%, ¼W	12079	RL07S563G
R69	Resistor, Metal Glaze, 33K Ohms, ±2%, ¼W	12139	RL07S333G
R70	Resistor, Composition, 2.2K Ohms, ±5%, ¼W	10671	RC07GF222J
R71, 85, 96	Resistor, Composition, 100 Ohms, ±5%, ¼W	10639	RC07GF101J
R72	Resistor, Metal Film, 2.55M Ohms, ±1%, ¼W	12149	RN50D2554F
R73	Resistor, Metal Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S473G
R74, 75	Resistor, Metal Film, 680K Ohms, ±1%, ½W	12161-684	RN55D6843F

TABLE 6-3. PARTS LIST, IF AMPLIFIER CIRCUIT CARD ASSEMBLY (A5A1) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R76	Resistor, Metal Film, 39K Ohms, ±2%, ¼W	12161-393	RL07S393G
R77	Resistor, Metal Glaze, 2.7K Ohms, ±2%, ¼W	12064	RL07S272G
R78	Resistor, Film, 3.3K Ohms, ±2%, ¼W	12161-332	RL07S332G
R83	Resistor, Metal Glaze, 12K Ohms, ±2%, ¼W	12072	RL07S123G
R86	Resistor, Composition, 10K Ohms, ±5%, ¼W	10687	RC07GF103J
R87	Resistor, not used		
R89, 90, 91, 92	Resistor, Composition, 100K Ohms, ±5%, ¼W	10711	RC07GF104J
T1	Transformer	05943	
T2	Transformer, Line Output	06943	
U1	Integrated Circuit OP Amp 757	36541	757DC
U2, 4	Integrated Circuit OP Amp 741	36542	uA741HC
U3	Integrated Circuit OP Amp 3140	36629	3140T/5
U5	Integrated Circuit (Analog Devices)	36664	AD 7502JD
U6, 7	Integrated Circuit (National Semiconductor)	36517	LM380N
U8	Integrated Circuit (Analog Devices)	36665	AD 7510 D1JD
U9	Integrated Circuit (Motorola)	36611	MC14528BCL
U10	Integrated Circuit (Motorola)	36571	MC14011BCL
–	Printed Wiring Board	08396	

CHAPTER 7

SERIAL ASYNCHRONOUS INTERFACE (A6A1) AND MICROCOMPUTER (A6A2)

7.1 THEORY OF OPERATION

This chapter provides information on the Serial Asynchronous Interface Module A6A1 and the Microcomputer Module A6A2; however, these two boards are only a part of the Receiver Control circuitry. This Receiver Control circuitry provides control over the Receiver, either from the front panel or from a remote location and consists of modules: A6A1, A6A2, A7A1, A7A2 and A8. In order to show how the A6A1 and A6A2 modules function within the Receiver Control section an overall description of the complete section is presented here. Figure 7-1 shows the function of the five modules within the Receiver Control section and Figure 7-2 shows a functional block diagram.

The heart of the Receiver control circuitry is the microcomputer which is an 8 bit integrated circuit microcomputer, constructed on circuit card assembly A6A2. This unit receives all commands from either the front panel switch card A7A2 or the remote interface card A6A1, processes them into control data and routes the control signals to the appropriate control circuits of the receiver. At the same time this unit provides the readout signals displayed either on the front panel display card A7A1 or at a remote location through A6A1. The microcomputer is interfaced to the front panel cards and the various Receiver control circuits through latch circuit card assembly A8.

The A8 circuitry provides the address and data decoders, latches, analog to digital and digital to analog converters and gates to control the data flow between the microcomputer and the Receiver control circuits, and between the microcomputer and the front panel circuit cards. Information (commands to the receiver)that is entered from the Receiver keyboards are routed through data latches to the data bus, that is connected to the microcomputer. Frequency commands entered through the tuning knob are formed by a tuning encoder, then routed through a decoder to the same data bus as the keyboard information. The microcomputer processes this information against its permanently stored control program in its memory, then forms the control and readout signals, and routes them to the data bus through bilateral switches and a latch circuit. Control of the control and readout signal is accomplished through control commands, also formed in the microcomputer from the input commands, then routed, through an address decoder, to the appropriate Receiver control circuit and front panel readout.

The microcomputer receives the information, from the front panel circuit card A7A2 or from a remote location, through circuit card A6A1. Its direction is asserted by the address data direct circuitry which also controls direction of the processor bus. The incoming information is routed to the central processing unit (CPU) along with information from the memory. This memory information is selected automatically from pre-proposed address codes. After all information is received and processed, the address data then redirects the I/O bus for outgoing information. A master reset circuit provides for resetting the CPU and memory circuits to an initial condition and at the same time will cause the microcomputer to cease its current operations. Information from a remote location is routed through a rear panel connector interfaced to circuit card A6A1. This circuitry can receive commands from a controller and return information to that same controller. Commands are routed to the processor and data buses and can change any operating parameters in the same manner as control from the front panel. Circuit card A6A1 also provides the antenna and auxiliary select outputs.

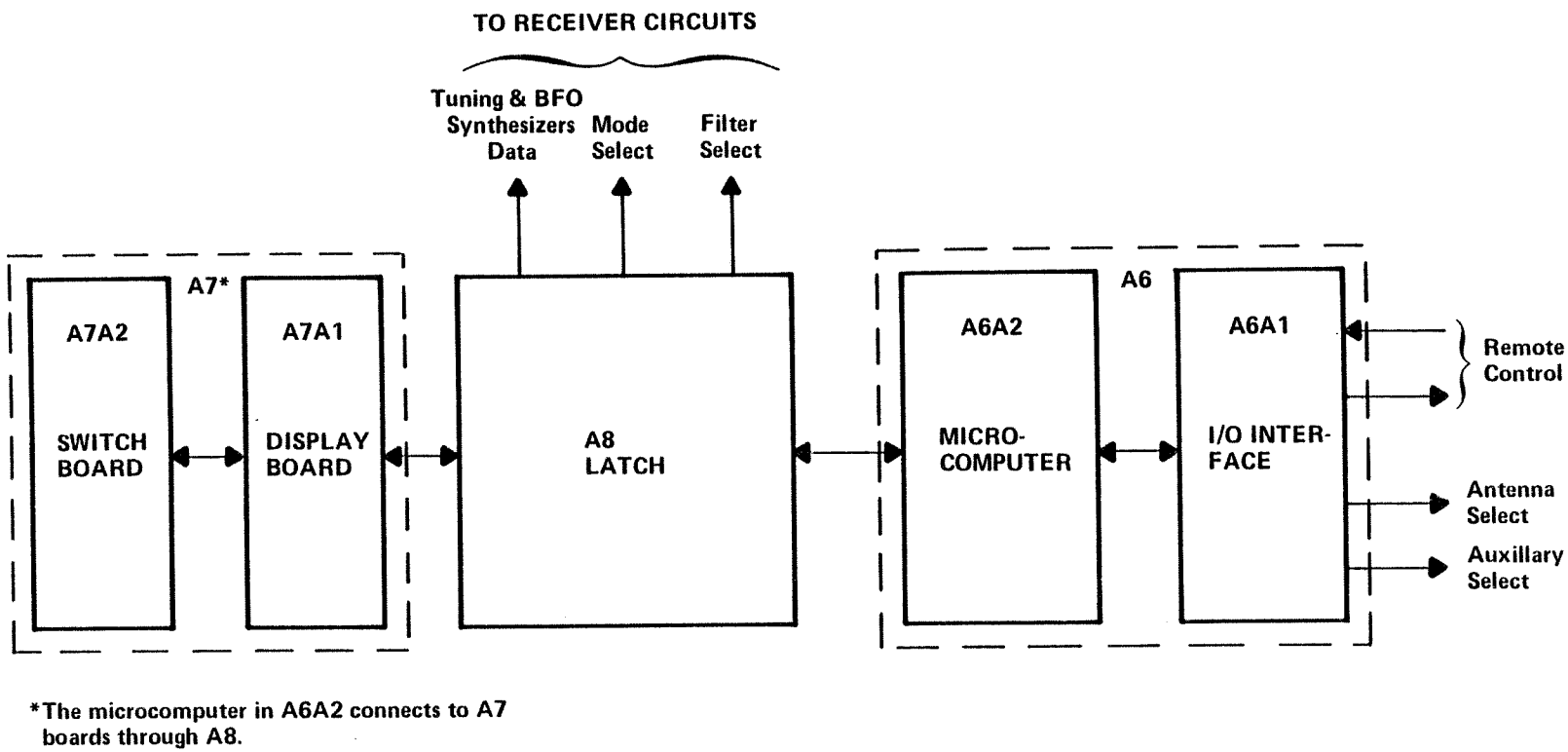


Figure 7-1. RA6778C Receiver Control Section Module Function

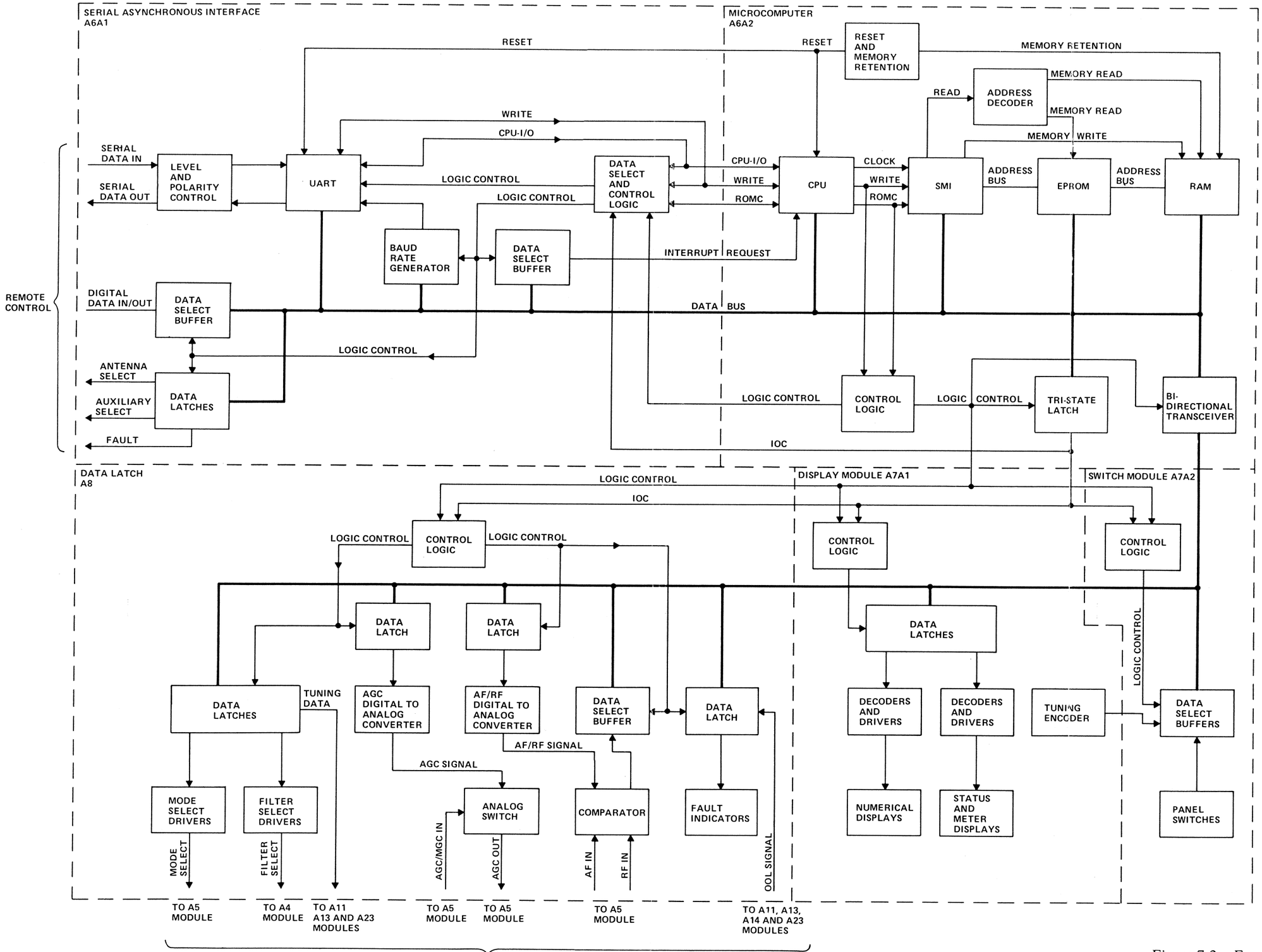


Figure 7-2. Functional Block Diagram, RA6778C Receiver Control

7.1.1 Serial Asynchronous Interface (A6A1)

The function of the A6A1 module is shown in the overall functional block diagram in Figure 7-2. An interconnect diagram between A6A1 and A6A2 is shown in Figure 7-3. A schematic diagram of A6A1 is shown in Figure 7-4. The serial asynchronous interface board, A6A1, contains the interface between the microcomputer and the remote controller. The A6A1 board contains a UART (universal asynchronous receiver transmitter) which provides an interface between the parallel bi-directional data lines on the microcomputer bus and the serial data lines from and to the remote controller. As indicated in the block diagram, Figure 7-2, separate in (receive) and out (transmit) serial data lines connect from the remote controller to the UART. The UART connects directly to the microcomputer (CPU) data bus. When the remote controller sends a command to the UART, the UART sends an interrupt request signal to the microprocessor, as described previously. UART operation is synchronized to the microprocessor by the ROMC, clock, CPU I/O, strobe logic and tri-state latched switch signals from the microprocessor.

The UART is also driven by the baud rate generator which supplies the clock frequency for the rate of data exchange (9600 baud rate) between the UART and remote controller.

Board A6A1 also contains the Antenna and Auxiliary Select Output latch and drive circuitry. The latches are latched, in programmed sequence, by the CPU data bus, controlled by the data select and strobes circuitry. This circuitry is driven by the ROMC, clock, strobe logic and tri-state latched switch signals from the microcomputer.

Board A6A1 contains the switch array, U11, used to select (for the serial data) whether parity will be used, odd or even parity (if used), MS188 or RS232 Polarity and memory dump.

The output connector from board A6A1 contains inputs for setting the address of the receiver when under remote control.

The UART (U2) provides an interface between the parallel data lines (PB0-PB7 data bus) from the microcomputer and the serial data lines to and from the remote controller. The UART contains a receive and a transmit section. The receive section converts the incoming serial stream (from the remote controller into the RR1 input of the UART) to 8-bit words and places them on the microprocessor bus (through UART outputs RBR1-RBR8) after initiating an interrupt request to the microcomputer (through output DR). The transmit section, when directed by the microcomputer (through input TBRL), takes the 8-bit words from the microprocessor bus (through UART inputs TBR1-TBR8) and serializes them for serial transmission to the remote controller (through TR0 output from the UART). The parallel inputs and outputs of the UART are tied together and onto the bi-directional data bus, since the UART receive outputs are tri-state.

7.1.1.1 Reset and Initialization

The UART is initialized by the /RESET line from the microcomputer, through pin 2 of connector P1 and inverter U9A, to its MR input. Transmit and receive clock rates, TRC and RRC inputs, are supplied by the programmable baud rate generator U4. This generator divides the crystal, Y1, frequency down to the programmed transmit and receive serial data clock rates. The division ratio to be used by U4 is obtained from the data bus, upon initialization of the program, on inputs RA-D and TA-D. This ratio is strobed into U4 by the strobing signal from the output 0 of decoder U20 which is controlled by microcomputer timing and strobing signalsIOC0-IOC2, IOC7 and /WSTB. Both the receive and transmit clock rates are set to 16 times the baud rate of 9600. Also strobed, upon initialization, from output 1 of decoder U20 is the CRL input to the UART U2. This loads the UART control register with data from the data bus through the PI, EPE, CL1, CL2, and SBS inputs. This sets whether parity is used, odd or even parity, character length and the number of stop bits.

These parameters are set by the U11 switch assembly, on the A6A1 board, as follows:

U11 Switch	Parameter
6	MS188 Polarity - ON, RS232 Polarity - OFF
5	Not used
4	Parity enabled - ON, Parity disabled - OFF
3	Odd Parity - ON, Even Parity - OFF
2	Clears memory - ON, Provides for memory loading - OFF
1	Not used

The U11 switches (with pull up resistors on U10A) feed into tri-state buffer U6 which strobes the switch status onto the data bus at the correct program time. The strobe is generated from the X2 output of decoder U22 with IOC0, IOC1, IOC7 and /IO READ inputs from the microcomputer.

7.1.1.2 Interrupt Circuitry

When the UART requires servicing from the microcomputer it will initiate an interrupt request. The UART will initiate an interrupt request to the microcomputer under the following two conditions:

a. Upon receipt of a serial stream of data from the remote controller by asserting its DR output, indicating data is available to the microcomputer from the remote controller.

b. When its transmit buffers are empty, indicating it can accept data from the microcomputer for transmission to the remote controller, by asserting its TBRE output.

Outputs DR and TBRE will go through gate U14A, if not inhibited by microcomputer outputs 00 and 01 (microcomputer busy), and then through gate U14B, at the correct time (ROMC output through U18A, U9C, U17A-C and U18B), to drive flip-flop U17D. The outputs of this flip-flop drive one of the two inputs to each of gates U13A and U13B. The other input to gate U13B is the inverted /ICB signal from the microcomputer. Gate U13A receives its other input from Q2 of U17B and Q3 of U17C through NAND gate U13D. If the CPU in the microcomputer is currently blocking, thus ignoring interrupt requests, /ICB is high. Under this condition U13 gates are blocked. When /ICB is low, the microcomputer will accept an interrupt request, and U13A-B gates yield an output. The output from U13C sends the /PRI output and the output from U13B, through switch U5, sends the /INIT. REQ. to the microprocessor to initiate an interrupt. The microprocessor will orderly stop its normal processing and start an interrupt routine to service the UART requested.

The interrupt circuitry on board A6A1 not only generates the interrupt request, but it also provides the microcomputer with the interrupt vector, the memory address at which the interrupt routine starts. A specific sequence of ROMC signals are detected by gates U18A, U9C, and flip-flop U17. When these signals are received, gates U13A and U13D enable switches U3 and U8 to output the interrupt vector on the data bus to be read by the microcomputer.

During the interrupt routine the microcomputer will assert its /ICB output, thus not accepting any further interrupts until it has completed the routine. It will be noted that the DR and TBRE outputs from the UART are sent out through connector P1, pins 37 and 36, to the microcomputer or transmit routine. /PRI is sent to the SMI in the microcomputer to inhibit its interrupt request circuitry.

7.1.1.3 Error Outputs

The error outputs from the UART; PE (parity error), OE (overrun error) and FE (framing error) are sent to the microcomputer Port 1; bits 2, 3 and 4 through connector P1 pins 5, 42 and 43.

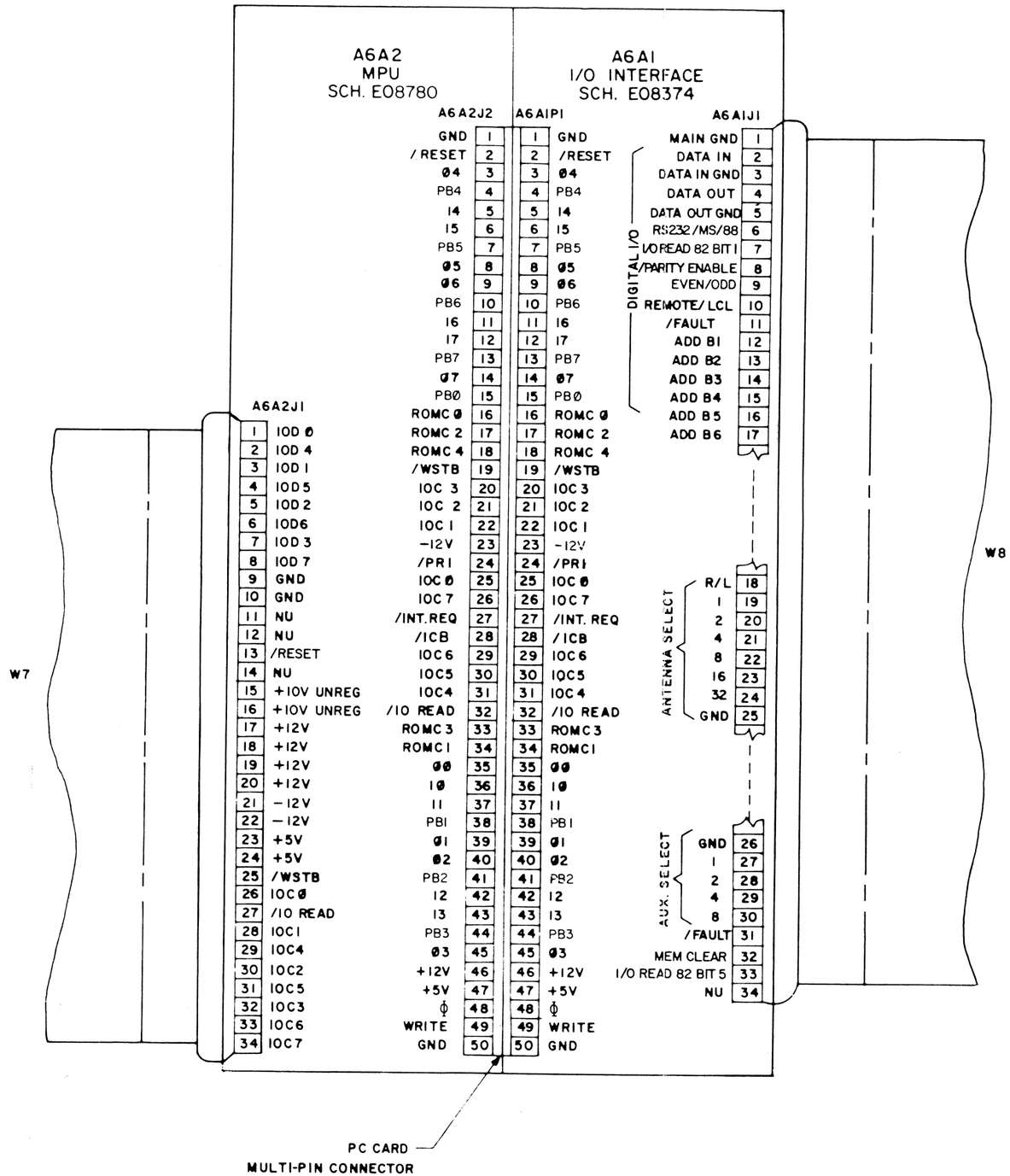


Figure 7-3. Interconnect Diagram, Microcomputer Module A6

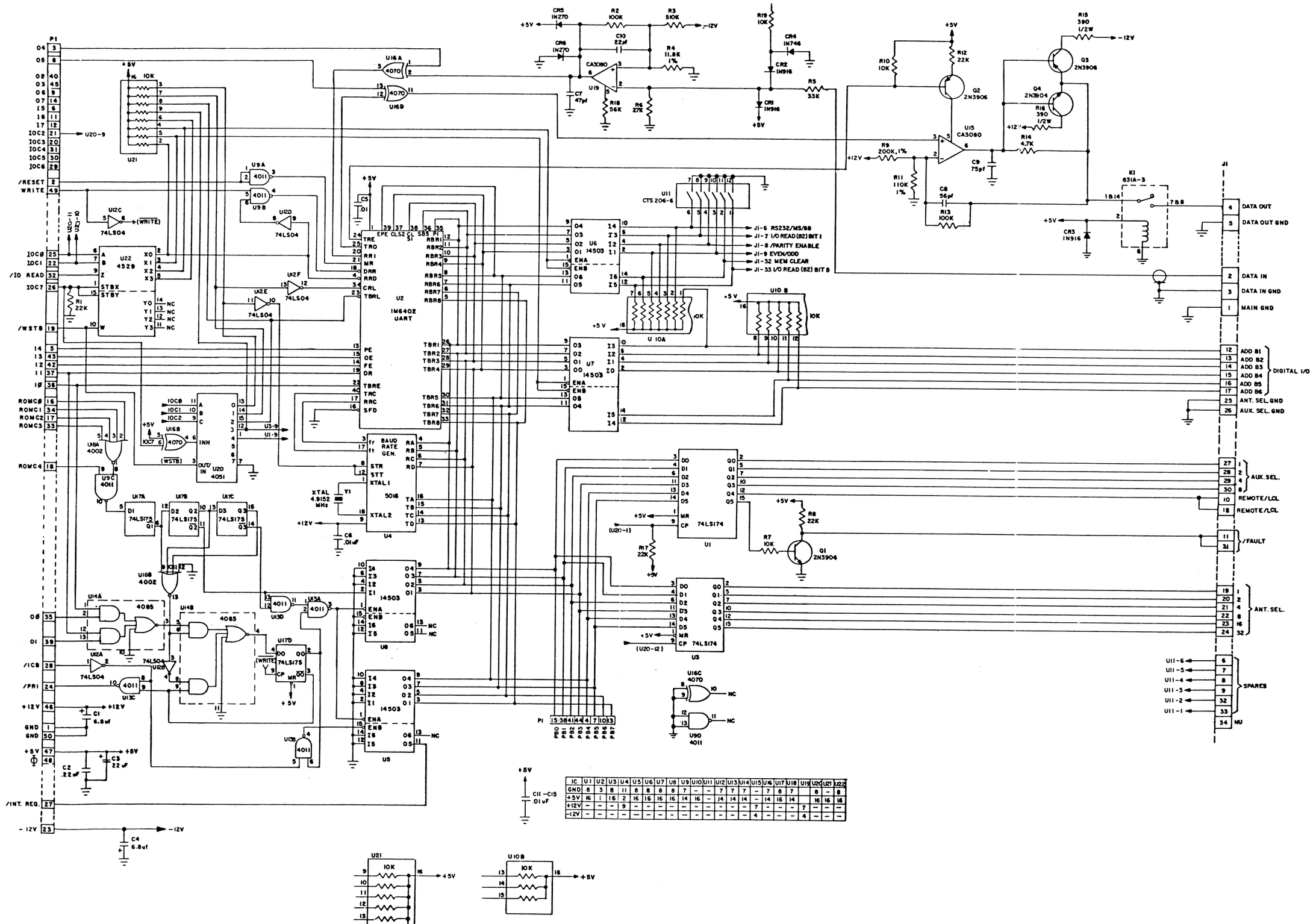


Figure 7-4. Schematic Diagram, Serial Asynchronous Interface Module, A6A1

	U1	U2	U3	U4	U5	U6	U7	U8	U9		U11	U12	U13	U14
GND	24	20	8	10	12	12	12	8	8		7	7	7	10
+5	3	40	16	20	21 24	21 24	21 24				14	14	14	20
+12	4	1												
-12														

NOTES:
1. FOLLOWING COMPONENTS NOT USED: U10, C13, C14

SCHEMATIC A6A2
MICROCOMPUTER
DRAWING 108780

Figure 7-5. Schematic Diagram, Microcomputer A6A2

7.1.1.4 Serial Inputs and Outputs

The serial input from the remote controller comes in through pin 2 of connector J1 to drive the limiting and voltage converter stage consisting of diodes CR1 and CR2 and U19. This stage converts the serial input voltage levels to the TTL logic voltage level used in the A6A1 card. The output of this stage drives one input to the exclusive OR gate U16A. The other input to this gate is the O4 output from the microcomputer CPU which serves to set the correct output polarity of this gate (U16A) to drive the RRI input to the UART (matching the serial input polarity used.)

The serial output from UART output TR0 drives one input to the exclusive OR gate U16D. The other input to this gate is the O5 output from the microprocessor CPU which serves to set the correct output polarity of the gate (U16D) to drive the following output drive stage and matches the serial output polarity used. The output drive stage consists of amplifier stage U15 and low impedance output driving transistors Q3-Q4. The output to the remote controller (at the required voltage levels) is taken from the junction of the emitters of Q3-Q4 and goes through the K1 relay contacts to come out from pin 4 of connector J1. The relay K1 opens the output circuit when power is off and, therefore, presents the required high output impedance.

7.1.1.5 Receiver Address

The receiver address for remote control is applied through the ADD B1-6 inputs (pins 12-17 of connector J1). These inputs (with pull up resistors U10B) feed into tri-state buffer U7 which strobes the data onto the data bus at the correct program time. The strobe is generated from the X1 output of decoder U22 with IOC0, IOC1, IOC7 and /IO READ inputs from the microcomputer.

7.1.1.6 Auxiliary Select, Remote/Local, Fault and Antenna Select Outputs

The four auxiliary select, Remote/Local and Fault outputs come out of connector J1 pins 27 through 30, 10 and 18, and 11 and 31, respectively. These outputs are obtained from the U1 latch (the fault through the added Q1 drive stage). The output data is latched into U1 from the data bus, at the proper program time, by the 4 output from decoder U20. U20 is driven by timing and strobing signals IOC0-IOC2, IOC7 and /WSTB from the microcomputer.

The six Antenna select outputs come out of connector J1 pins 19-24. These are obtained from U3 latch. The data from the data bus is latched into U3 by output 3 from decoder U20.

7.1.2 Microcomputer (A6A2)

The function of the A6A2 module is shown in the overall functional block diagram in Figure 7-2. A schematic diagram is shown in Figure 7-5. The microcomputer, contained on A6A2, performs the following functions:

a. Reads local controls from the front panel.

b. Drives and updates displays on the front panel.

c. Receives commands and sends data to the remote controller.

d. Computes and relays receiver tuning and operating data to the appropriate receiver circuits.

e. Initializes circuits following power application.

f. Retains memory of receiver settings at power failure or turn-off.

These functions are performed in a programmed sequence through the control of the microcomputer CPU (Central Processing Unit). As indicated in the block diagram, Figure 7-2, the CPU communicates to other components of the system primarily through its data bus (8 bi-directional data lines) and ROMC control lines.

The microcomputer makes use of the basic components in the F8 microcomputer family. A more detailed description of this microcomputer family operation, including timing and instruction set, is given in the F8 users guide available from Fairchild Camera and Instrumentation Corp., Mountain View, California.

U1 is the F8 CPU type 3850. The CPU controls operation by using other components of the microcomputer to read the program and route data throughout the receiver. The CPU 8-bit data word bi-directional ports DB0-DB7 connect to the 8 line data bus which is common to other devices in the system and is the primary means of communication between the CPU and other parts of the system. The 2.0 MHz crystal Y1, connecting across pins 38 and 39 of the CPU, is used to provide the accurate basic clock frequency. The WRITE and Φ PULSE outputs are clock outputs which provide timing drive for all devices in the microcomputer. The ROMC 0-4 outputs from the CPU connect to other devices in the system and identify operations which these devices must perform during any instruction cycle. Interrupt requests are received through the /INT REQ port. Interrupt acknowledgement is recognized through a specific sequence of ROMC states. The /ICB line tells the hardware whether the CPU is responding to interrupts. The input/output ports 00-07 and 10-17 are ports through which the CPU communicates with logic, external to the microcomputer.

7.1.2.1 Memory

The program is contained in the erasable/programmable read-only memory (EPROM). Temporary storage for receiver settings and for data computations is provided by the working random access memory (RAM), which can be written into and read by the CPU. These memories are addressed by the CPU through the memory interface. The CPU sends the ROMC and clock signals to the memory interface which recognizes the ROMC code calling for a Memory Address operation. The memory interface, in sequence, takes the memory address provided by the CPU on the data bus, addresses the ROM or RAM over the memory address bus. Then it sends a read signal to the ROM (if it is addressed) or sends a read or write signal to the RAM (if it is addressed). The CPU places the data to be read by the RAM on the data bus or reads the data placed on the data bus by the ROM or RAM, as appropriate.

The CPU receives and follows the program (sequence of instructions) which is stored in the erasable/programmable read only memory (EPROMS) contained in U5, U6 and U7. Each of these contain 2K 8-bit words for a total capacity of 6K 8-bit words of program memory. The CPU also uses the temporary random access or "scratch-pad" memory, with U8 providing 4-bits of each word and U9 providing the remaining 4-bits.

The memories are addressed by the CPU through U2, the static memory interface type 3853 (SMI). The CPU sends the ROMC 0-4, WRITE and Φ signals to the SMI (U2). The SMI, in timed sequence, recognizes the ROMC 0-4 code for a memory access operation, takes the address which the CPU has provided on the data bus, and addresses the memories over the memories address bus A0-A10. U2 address outputs A11 and A12, through decoders U3A and U3B, are also used in addressing, by enabling the appropriate memories U5-U9. The SMI determines from the ROMC 0-4 code whether the operation is a read or write and directs the memory via the CPU READ and /MEMW outputs to place data on the data bus for the CPU or accept data from the data bus from the CPU.

7.1.2.2 Reset and Memory Retention

Board A6A2 also contains the Reset and RAM memory retention circuitry. The Reset circuitry generates a reset signal when power is applied. This reset signal is applied to the CPU. When

reset comes on the CPU initializes all circuitry and causes the program to start at its initial starting or zero program address.

When power is removed, due to power turn-off or power failure, the reset signal to the CPU is removed. The CPU now causes the system to come to an orderly stop.

In addition, the memory retention circuitry (at power turn-off) connects an internal battery to the RAM so that the receiver settings in memory are retained. Thus, when power is reapplied, the receiver will be set where it was when power was interrupted. Also, at power turn off, the memory retention circuitry places the RAM in a low power drain mode which retains memory but draws a minimal amount of power from the battery. When external power is applied, the internal battery is charged by the external power supply.

Q1 and Q2 are used to generate a power on reset signal used to initialize the microprocessor and the UART in the interface board, and to provide an orderly stop when power is removed. The +5 unregulated line rises before the regulated +5 volt line upon application of power. Initially Q1 will be forward biased, as the base voltage developed by divider R2, R5 and R6 is lower than the emitter voltage of Q1. The voltage appearing across R3 and R4 causes Q2 to turn on, driving the /RESET signal on the collector low. When the voltage across CR1 is less than the base voltage of Q1, Q1 will now be reverse biased, thus turning Q2 off and allowing /RESET to go fully high by pullup R7. Zener diode CR1 serves to establish the threshold at which Q1 will cease to conduct. R5 serves to provide hysteresis, so that once Q1 is turned off the threshold moves to keep it turned off.

When power fails, this circuitry is used to bring about the cessation of processor operations, and the retention of data by the CMOS RAMs. On power failure the unregulated +5 volts drops before the regulated +5. When the threshold voltage at the base of Q1 is reached, Q1 and Q2 turn on, thus asserting /RESET. /RESET is used to stop processor operations. In addition it is fed through R10, CR4 and CR5 to the emitter of Q4. When /RESET is asserted, Q4 and Q5 cease to conduct. The gate of Q6 returns to ground as R14 discharges C15. This disables CE2 moments after /RESET has gone low. With CE2 low, the voltage on the CMOS RAM's (U8-9) is now allowed to drop to 2 volts. This voltage is supplied by the battery BT1 through R9 and CR3.

When /RESET is allowed to go high upon re-application of power, Q4 and Q5 are turned on (+5 volts applied to R10). This causes the gate of Q6 to go negative, allowing CE2 to go positive at the same time the processor is re-enabled by the removal of /RESET.

The RAM power supply consists of R8, R9, R11, CR3, CR6, BT1 and C16. This power supply serves to provide 5 volts to the RAMs when the system is in operation, and 2 volts when the unit is turned off. When power is applied, Q3 quickly charges C16 to 5 volts so that the memory has adequate power before the chip enable (CE2) goes high. When power is off, Q3 is back biased, and therefore out of the circuit. The leakage of the memories will discharge C16 until diode CR3 starts to conduct. This stops the power from dropping below about 2.1 volts even when power is removed. R8 and CR2 serve to make up the 0.5 volt base emitter voltage drop across Q3. CR6 and R9 charge BT1 when power is applied.

7.1.2.3 Read/Write – Receiver and Front Panel

The CPU, in programmed sequence, receives and sends data from and to the front panel controls and displays (Boards A7A2, A7A1) and the receiver control circuitry (through Latch Board A8) via the CPU data bus. The data is directed between the CPU data bus and the receiver control and front panel circuitry, in correct program sequence, by the bi-directional tri-state switch. This switch is controlled by the strobe logic which is driven by the ROMC and clock signals from the CPU. The addressing of the various receiver control and front panel circuitry, to accept or supply data from or to the data bus, in prescribed program sequence, is done by the strobe logic and tri-state latch switch. This switch is driven by the CPU data bus and its outputs latched to the input data at the prescribed program times by the strobe logic.

The CPU, in program sequence, writes and reads data to and from the front panel controls and displays and the receiver circuitry. The CPU data bus connects to these units through the tri-state bi-directional switch U4. The direction of data flow and timing of switch openings are controlled through pins 1 and 19 of U4. Signals to these pins are generated by the strobe logic in gates U11-13 and the Q7 output from the tri-state latched switch U14. The strobe logic inputs consist of the ROMC 0-4 and clock signals. U14 latches the data from the CPU data bus as directed by the strobe logic. Thus, at the appropriate program times, the CPU data bus connects through U4 through pins 1-8 of connector J1 to front panel (A7), and receive control circuitry (A8). The data bus from these outputs is labeled IOD0-IOD7. Also, the U14 latched outputs and the strobe logic outputs /IO READ and /WSTB come out of pins 25-34 of connector J1 and go to the front panel (A7) and receiver control circuitry (A8). The U14 latched outputs are labeled IOC0-IOC7. The strobed logic and latched outputs provide the programmed timing and codes for the various elements in the front panel and receiver control circuitry to accept or supply data from or to the data bus.

7.1.2.4 Microcomputer-Remote Control

The CPU receives and sends data from and to the remote controller via the Serial Asynchronous Interface Board, A6A1. Data to and from the CPU and Board A6A1 is sent directly through the CPU data bus. Additional control signals are exchanged between the CPU and Board A6A1 via the CPU I/O ports. When the remote controller sends commands and data to the receiver, the interface board generates an interrupt request signal. This signal requests the microcomputer to orderly stop its present program and jump to the program routine which will service the remote controller commands and data.

The microcomputer also sends the ROMC, clock, strobe logic and tri-state latch switch signals to the interface board. These are used by the interface board circuitry to synchronize its operations with the CPU, to interface the 8-bit parallel word format of the CPU data bus to the serial bit asynchronous data format of the remote controller and to generate the Antenna and Auxiliary Select Outputs.

The Reset signal from the microcomputer board, A6A2, is also sent to the interface board to initialize its circuitry at power turn-on.

The CPU receives and sends data from and to the remote controller interface board (A6A1) via the data bus. Connections between the microcomputer board and the remote controller interface board are made through connector J2. The data bus to the remote control controller interface is labeled PB0-PB7. The microcomputer receives the interrupt request (/INT REQ) signal from the remote control board. As indicated previously, this requests the microprocessor to jump to the program which will service the remote controller.

The CPU also sends the WRITE, Φ timing signals, the strobe logic output signals /IO READ and /WSTB, the tri-state latched outputs IOC0-IOC7, the ROMC 0-4 outputs, and the CPU 00-07 and 10-17 outputs, and the interrupt acknowledge signal /ICB. These signals are used by the interface board to synchronize operations between the CPU and the remote controller and to generate the Antenna and Auxiliary select outputs.

7.2 INTERFACE A6A1 AND MICROCOMPUTER A6A2, TEST FIXTURES

Testing and troubleshooting of the Serial Asynchronous Interface A6A1 and Microcomputer A6A2 is accomplished through the use of two separate test fixtures and their associated test equipment. Each test fixture provides a convenient base for mounting its respective circuit card for testing while at the same time providing easy access to the circuit card for troubleshooting.

The A6A1 Test fixture provides dynamic and static testing of the A6A1 circuit card and checks switches contained on U11. The test fixture also provides for troubleshooting when failed conditions are found. Figure 7-6 shows the A6A1 test fixture. Figure 7-7A shows the overall assembly of the A6A1 module while Figure 7-7B shows the circuit card.

The A6A2 test fixture provides the means to verify performance of the A6A2 circuit card. A functional test EPROM and three memory test EPROM's are furnished with the test fixture to provide the programs for testing the unit. Figure 7-8 shows the A6A2 test fixture. Figure 7-9A shows the overall assembly of the module while Figure 7-9B shows the circuit card.

7.3 TEST EQUIPMENT AND ACCESSORIES

To perform testing and troubleshooting, using either test fixture requires additional test equipment and accessories. This additional equipment is used to provide power, inject programming, make connections and to signal trace. The test equipment and accessories required are listed in Table 7-1.

Table 7-1. Test Equipment and Accessories

Item	Description	Recommended Equipment or Equal
1	Oscilloscope	Tektronix 465
2	DC Power Supplies: +5 VDC, +10 VDC, +12 VDC, -12 VDC	Racal
3	A6A1 Test Fixture	Racal
4	A6A2 Test Fixture	Racal

7.4 TEST AND ALIGNMENT

The following procedures contain the information necessary to completely test the A6A1 and A6A2 modules.

All tests are to be performed at ambient room temperature. Record results on the test data sheets pages 7-23 (A6A1) and 7-29 (A6A2).

7.4.1 Serial Asynchronous Interface A6A1 Test

1. Turn power supplies off and connect the power supplies to their respective terminals on the test fixture.

2. Connect the 50 pin connector on the test fixture to the board under test. Ensure correct positioning of Pin 1. Connect the 34 pin connector.

3. Set all troubleshooting switches to the OFF position.

4. Place the STATIC/DYNAMIC switch in the DYNAMIC position. Turn power supplies on.

5. Press RESET; after 2 to 3 minutes the PASS light should come on. If it does not,refer to paragraph 7.4.1.1. If BUS LOCKED light stays on, turn power off and refer to the same paragraph. Record results.

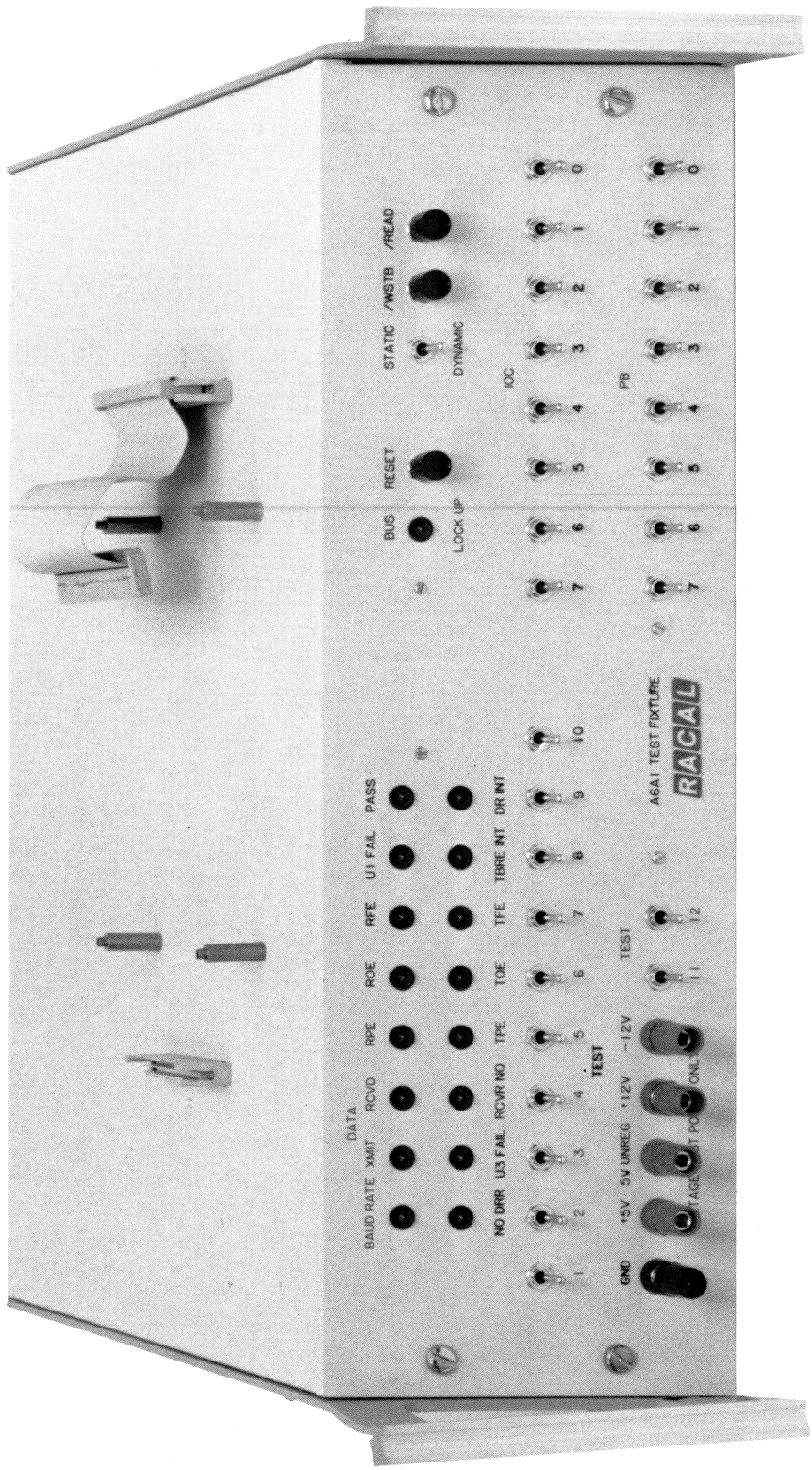


Figure 7-6. Serial Asynchronous Interface A6A1, Test Fixture

6. Set test switch number one "ON".

7. Press RESET. Turn all switches on U11 to their ON positions.

8. Referring to Table 7-2, look at the indicated front panel LED's; all should be "OFF".

Table 7-2. Front Panel LED's

U11 Switch Number	Front Panel LED
1	RFE
2	ROE
3	RPE
4	DATA RCVD
5	DATA XMIT
6	BAUD RATE

9. Turn switch #1 of U11 "OFF". Its corresponding LED should be "ON". The other 5 LED's should be "OFF".

10. Repeat step 9 for the remaining switches of U11. Record all results.

11. Turn power off. Remove unit from test fixture. All tests are now complete.

7.4.1.1 Troubleshooting

Several troubleshooting aids have been incorporated into this test fixture. These are described in the following paragraphs, and are defined in Table 7-3.

1. The Static/Dynamic switch, when set to Static, allows manual control of all address and data lines, and the read and write lines. Switches IOD Ø through IOD 7 control the data bus, and IOC Ø through IOC 7 control the address bus. Read and write functions are controlled by their corresponding switches.

2. To observe Port Operation, or character transmission, software oscilloscope loops have been provided. They operate as follows:

   a. I/O Ports - Turn the desired test number switch to the "On" position. Press "Reset." The processor will continuously strobe the selected port.

   b. Character Transmission – Depending upon which switch is turned on, the character "A" will be transmitted to or from the board under test, using the ASCII code for that letter. (Reset must be pressed to start it.)

3. LED Indicators – Numerous tests are executed during the dynamic test sequence. Any tests which fail are so indicated on the front panel indicators as described below.

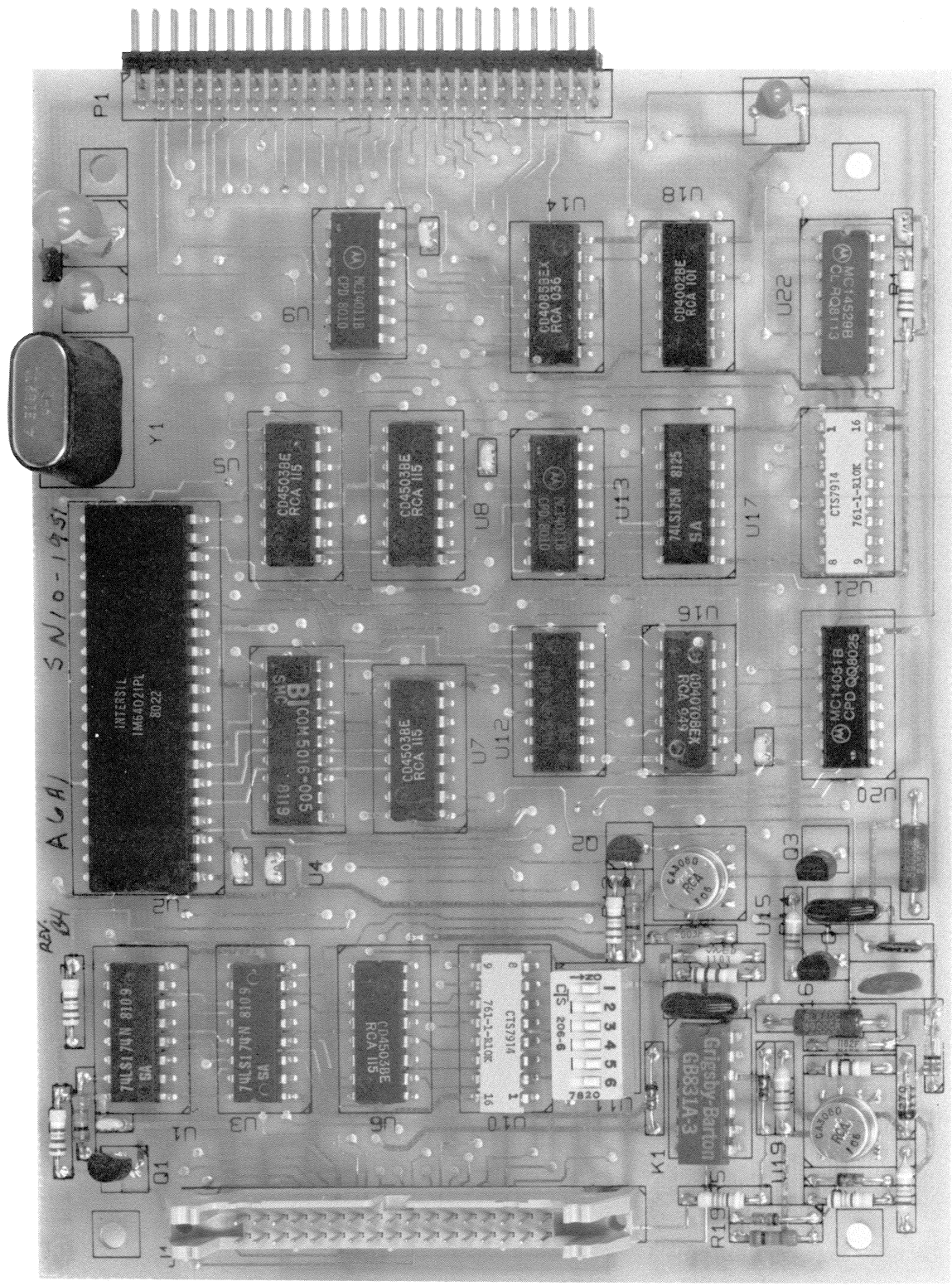


Figure 7-7A. Serial Asynchronous Interface A6A1, Overall Assembly

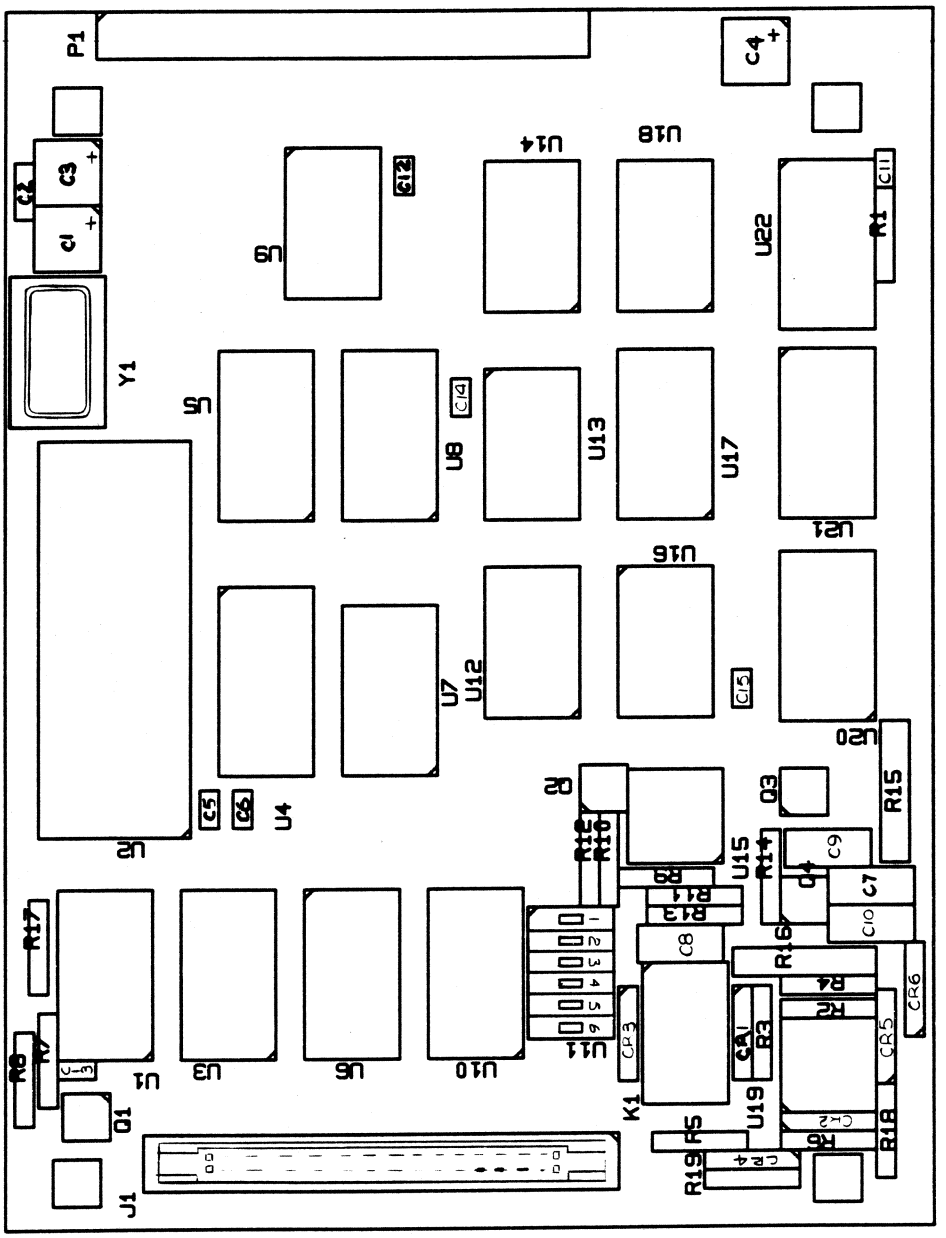


Figure 7-7B. Serial Asynchronous Interface A6A1 Circuit Card

a. Bus Locked: Indicates an overall failure of the unit. The processor was locked up and no tests were run. This is usually caused by a short circuit or solder splash.

b. RFE: A character was transmitted to the board under test and a framing error was detected.

c. ROE: Same as B, except an overrun error occurred.

d. RPE: Same as B, except a parity error occurred.

e. Data Received Error: Data was transmitted to the board under test, and it was incorrectly received.

f. Data Transmit Error: Data was sent from the board under test, but an error occurred in the process.

g. Baud Rate Error: An error occurred while attempting to program the Baud Rate generator.

h. No TBRE Interrupt: The transmitter buffer register was empty, and an interrupt was not generated.

i. No DR Interrupt: Data was sent to the board, but it did not generate an interrupt.

j. No DR Reset: The "Data Received" line on the board under test did not reset when it should have.

k. TFE: A character was transmitted from the board under test, and a framing error occurred.

l. TOE: Same as step K, except an overrun error occurred.

m. TPE: Same as step K, except a parity error occurred.

n. Received Number Buffer Error: An error occurred while testing the receiver number buffer.

o. Auxiliary Latch Failure: A failure related to the auxiliary select latch is indicated. (U1)

p. Antenna Latch Failure: A failure related to the antenna select latch is indicated. (U3)

Table 7-3. Port Tests

TEST NUMBER	PORT	TEST NUMBER	PORT
TEST 1	SWITCH TEST	TEST 7	OUT 81
TEST 2	RECEIVE 'A'	TEST 8	OUT 80
TEST 3	TRANSMIT 'A'	TEST 9	IN 82
TEST 4	OUT 84	TEST 10	IN 81
TEST 5	OUT 83	TEST 11	IN 80
TEST 6	OUT 82	TEST 12	NOT USED

DATE _____ MODULE A6A1

CKD BY _____ USED ON _____

TEST DATA SHEET

PART NAME: A6A1 Serial Asynchronous Interface JOB NO: _____

PART NUMBER: 08373 SERIAL NO: _____

USED ON: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
7.4.1(5)	Dynamic Operational Test		Pass	Fail	
7.4.1(10)	All Switches ON		Pass	Fail	
	Switch #1 OFF		Pass	Fail	
	Switch #2 OFF		Pass	Fail	
	Switch #3 OFF		Pass	Fail	
	Switch #4 OFF		Pass	Fail	
	Switch #5 OFF		Pass	Fail	
	Switch #6 OFF		Pass	Fail	

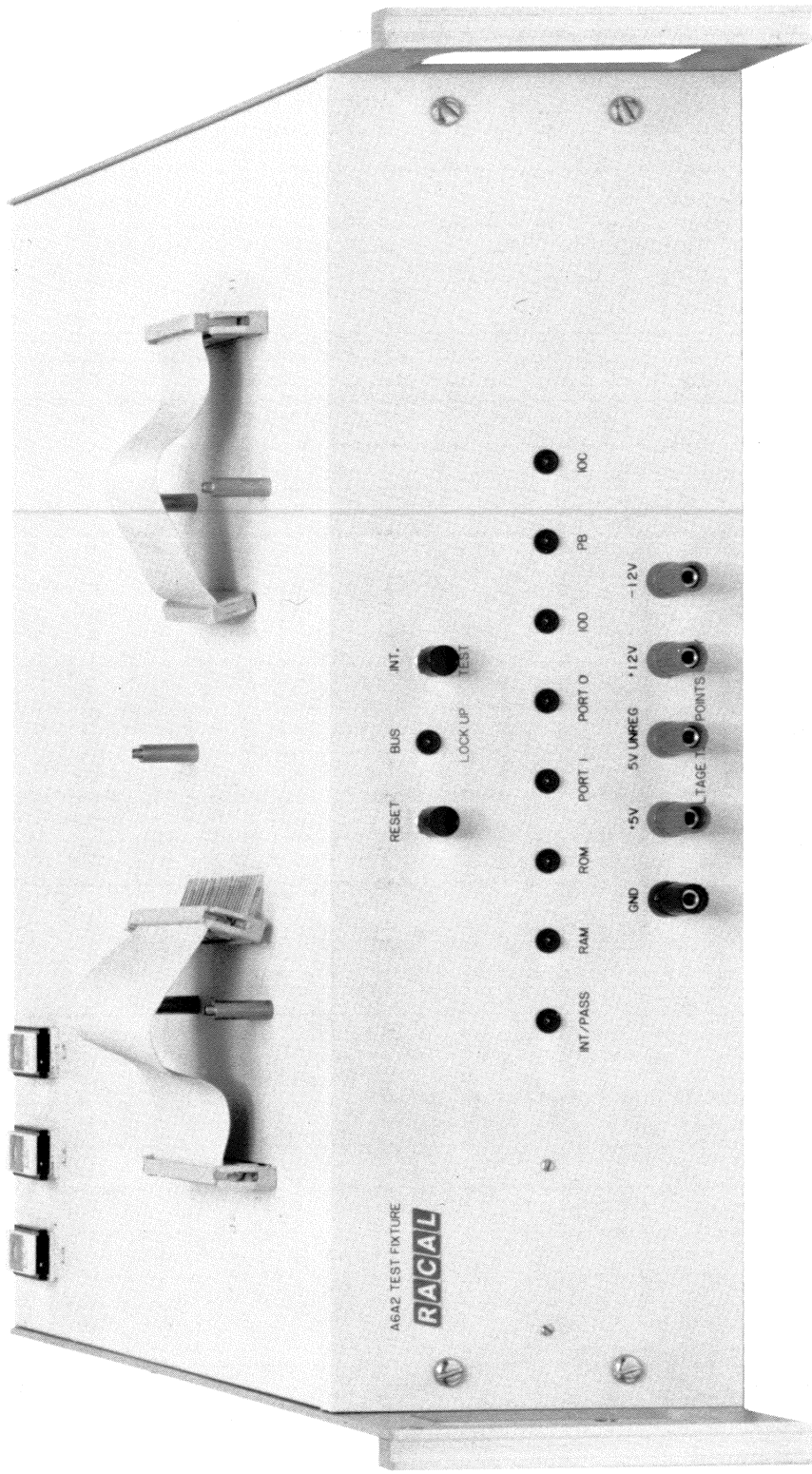


Figure 7-8. Microcomputer A6A2, Test Fixture

7.4.2 Microcomputer A6A2 Test

1. Turn power supplies off and connect the +5, +10, +12 and −12 Volt dc supplies to their respective terminals on the test fixture.

Table 7-4. Rear Panel Connectors

Pin #	Function	Pin #	Function
1	N.U.	5	GND
2	+12V	6	-12V
3	+5V	7	+5V UNREG.
4	N.U.	8	N.U.

2. Insert test EPROMS into their corresponding sockets on the board under test. Note that the EPROM marked LO goes in the U5 Socket, L2 in the U6 Socket, & L4 in the U7 Socket. Be sure to observe placement of Pin 1.
3. Attach the test connectors (2) to the A6A2 under test. Remove link LK1 from the board.
4. Turn power "ON". Measure and verify the +12V,-12V,+5V and -5V unreg. test points on the test fixture.
5. Press "RESET". "BUS LOCK" lamp will come on.
6. Release "RESET". "BUS LOCK" lamp should go out within about 1 second. If it remains lit, turn power off immediately. This indicates a serious fault (short circuit, etc.) on the board under test. All other lamps should go out.
7. PASS/INT lamp should come on. If any other lamps light, these correspond to faulty circuits on the board under test. Record results on test data sheet.
8. Press and release "INT TEST" switch on test fixture. All lights should go out. Check on test data sheet.
9. PASS/INT lamp should come on. Check on data sheet.
10. If required, re-install link LK1 in the board.
11. All tests are now complete.

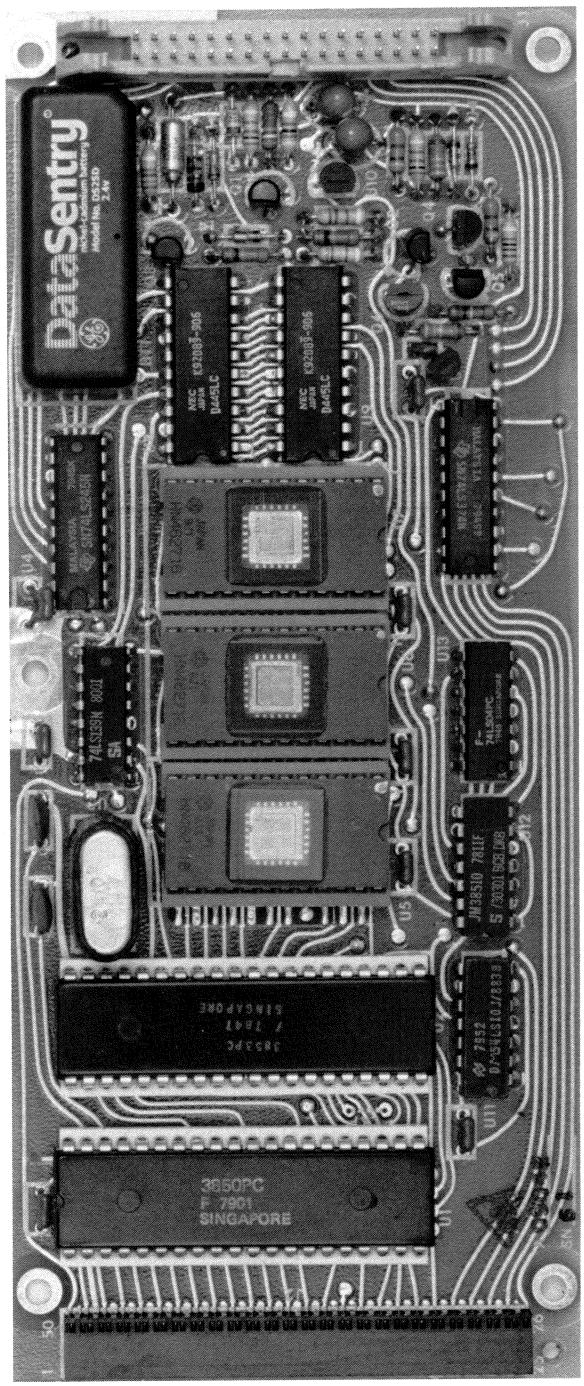


Figure 7-9A. Microcomputer A6A2, Overall Assembly

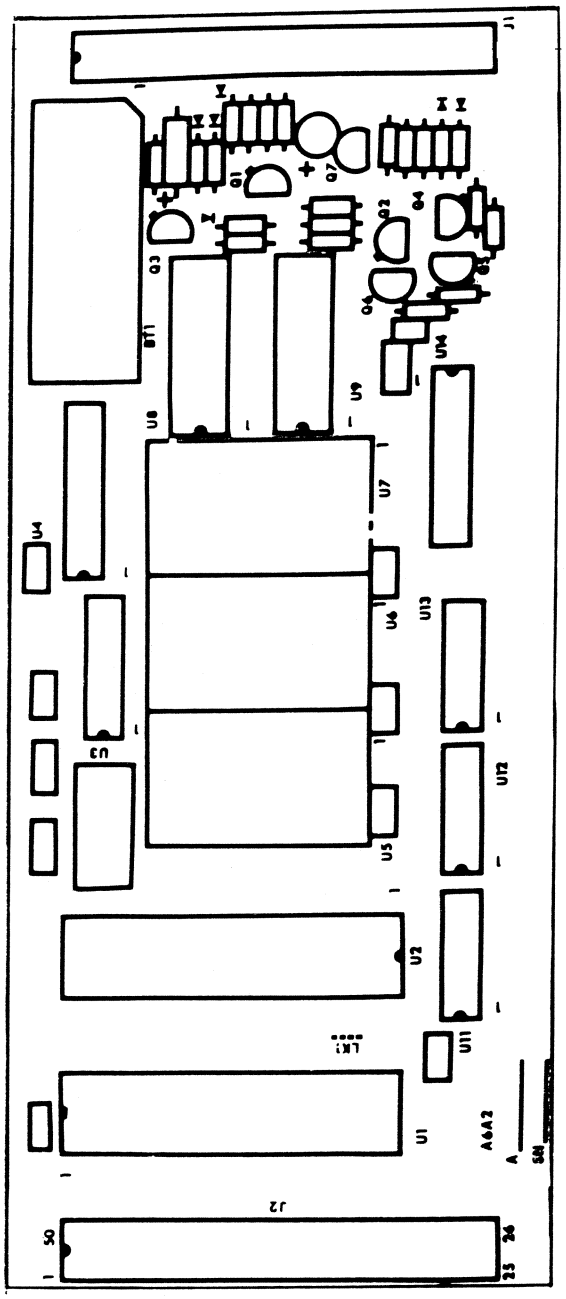


Figure 7-9B. Microcomputer A6A2 Circuit Card

7.4.3 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (static, dynamic, Interrupt, memory, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failures of memory can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope of voltmeter, to trace the fault to a single component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconducts and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, the tests for the complete circuit card should then be performed.

7.5 PARTS LIST, MICROCOMPUTER MODULE A6

The parts list for the A6 module is contained in Table 7-5. Tables 7-6 and 7-7 contain a detailed listing of the components contained on the A6A1 and A6A2 Circuit Card Assemblies.

DATE _____
CKD BY _____

MODULE A6A2
USED ON _____

TEST DATA SHEET

PART NAME: A6A2 Microcomputer Board
PART NUMBER: 09042
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
7.4.2(7)	FUNCTIONAL TEST		Pass	Fail	
7.4.2(8)	All test lamps go out when "INT TEST"				
	pressed		Pass	Fail	
7.4.2(9)	Interrupt Test		Pass	Fail	

TABLE 7-5. PARTS LIST, MICROCOMPUTER ASSEMBLY, A6

08686-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A6A1	Serial Asynchronous Interface Circuit Card Assembly, A6A1 (See Table 7-6 for further breakdown)	08373	
A6A2	Microprocessor, Circuit Card Assembly, A6A2 (See Table 7-7 for further breakdown)	09042	
–	ROM Set for A6A2	08731	

TABLE 7-6. PARTS LIST, SERIAL ASYNCHRONOUS INTERFACE CIRCUIT CARD ASSEMBLY, A6A1 08373

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 4	Capacitor, Tantalum, 6.8 uF, ±20%, 35V	25060-685	T362A685M035AS
C2	Capacitor, Ceramic, 0.22 uF, ±20% (Erie)	21742	8131-050-651-224M
C3	Capacitor, Tantalum, 22 uF, ±20%, 35V	25060-226	T362A226M035AS
C5, 6, 11-15	Capacitor, Ceramic, 0.01 uF, ±20% (Erie),50V	21733	8121-050-651-103M
C7	Capacitor, Mica, 47 pF, ±5% , 500 WVDC	22314	CD6C470J500
C8	Capacitor, Mica, 56 pF, ±5% ,500V	22017	CM05E560JN3
C9	Capacitor, Mica, 75 pF, ±2% ,500V	22125	CM05E750G03
C10	Capacitor, Ceramic, 22 pF, ±5% (Erie)	21353	801-000-C0G0-220J
CR1-3	Diode, Silicon, Pin	35514	1N916
CR4	Diode, Zener, 3.3 Volts	33557	1N746
CR5-6	Diode, Geranium	35538	1N270
J1	Connector, PCB, 34 Contact	61200	3431-2002
K1	Relay, 5 Volts, Dip 1, Form A	51811	GB-8311A-3
P1	Connector, PCB, 50 Contact	07881	
Q1, 4	Transistor, NPN, low power	32036	2N3904
Q2, 3	Transistor, PNP, low power	32037	2N3906
R1, 8, 12, 17	Resistor, Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S223G
R2, 13	Resistor, Film, 100K Ohms, ±1%, ¼W	12161-104	RL07S104G
R3	Resistor, Film, 510K Ohms, ±2%, ¼W	12161-514	RL07S514G
R4	Resistor, Film, 11.8K Ohms, ±1%, ¼W	12163	RN55D1182F
R5	Resistor, Film, 33K Ohms, ±2%, ¼W	12161-333	RL07S333G
R6	Resistor, Film, 27K Ohms, ±2%, ¼W	12161-273	RL07S273G
R7, 10, 19	Resistor, Film, 10K Ohms, ±2%, ¼W	12161-103	RL07S103G
R9	Resistor, Film, 200K Ohms, ±1%, ¼W	12130	RN55D2003F
R11	Resistor, Film, 110K Ohms, ±1%, ¼W	12129	RN55D1103F
R14	Resistor, Film, 4.7K Ohms, ±2%, ¼W	12161-472	RL07S472G

TABLE 7-6. PARTS LIST, SERIAL ASYNCHRONOUS INTERFACE CIRCUIT CARD ASSEMBLY, A6A1 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R15, 16	Resistor, Film, 390 Ohms, ±2%, ¼W	12162-391	RL20S391G
R18	Resistor, Film, 56K Ohms, ±2%, ¼W	12161-563	RL07S563G
U1, 3	Integrated Circuit, 6 Bit D flip-flop	36715	74LS174J
U2	Integrated Circuit, UART	36667	1M6402 CPL
U4	Integrated Circuit, Baud Rate Generator	36719	COM-5016-6
U5-8	Integrated Circuit, Hex 3 state buffer	36694	MC14503-BCL
U9, 13	Integrated Circuit, Quad 2 input NAND gate	36571	MC14011-BCL
U10, 21	Integrated Circuit, 15 Resistor network, 16 pin, 10K Ohms, ±2%, ¼W	19326-103	4116R-002-103
U11	Integrated Circuit, Switch Array, 6-SPST	52433	CTS206-6
U12	Integrated Circuit, Hex Inverter	36676	74LS04J
U14	Integrated Circuit, Dual 2 input AND/OR gate	36781	4085B
U15, 19	Integrated Circuit, Operational Transconductor Amplifier	36656	CA3080S/5
U16	Integrated Circuit, Quad exclusive OR gate	36653	MC14070BCL
U17	Integrated Circuit, Quad D flip-flop	36675	74LS175J
U18	Integrated Circuit, Dual 4 input NOR gate	36587	MC14002BCP
U20	Integrated Circuit, 8 channel analog multiplexer	36687	MC14051BCL
U22	Integrated Circuit, Dual Monostable Multivibrator	36650	MC14529BCL
Y1	Crystal Oscillator, 4.9152 MHz	07622	
–	Printed Wiring Board	08375	

TABLE 7-7. PARTS LIST, MICROPROCESSOR CIRCUIT CARD ASSEMBLY, A6A2 09042

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
BT1	Battery, Ni-Cad 2.4 VDC (CAUTION: Protect leads from conductive materials.)	42517	GED525D
C1, 2	Capacitor, Ceramic, 15 pF, ±5% (Erie)	21351	801-000-C0G0-150J
C3-10	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
C13-14	Capacitor, Not Used		
C15	Capacitor, Ceramic, 0.001 uF,±20% (Erie)	21756	8101-050-651-102M
C16	Capacitor, Tantalum, 4.7 uF, ±2% (Kemet)	25059	T210A475M010MS
C17	Capacitor, Tantalum, 15 uF, ±20%, 15V	25063-156	T362B156M015AS
CR1	Diode (Zener)	33543	1N752A
CR2, 4-6	Diode	35514	1N916
CR3	Diode	35538	1N270
J1	Connector, 34 Pin, 3M	61200	3M3431-2002
J2	Connector, 50 Pin, Berg	61225	65000-036
Q1, 4	Transistor, PNP	32037	2N3906
Q2, 3, 5	Transistor, NPN	32036	2N3904
Q6, 7	Transistor, FET	32518	TIS-74
R1, 7	Resistor, MF, 1K, ±2%, ¼W	12161-102	GPR5053XM102G
R2, 10, 15	Resistor, MF, 33K, ±2%, ¼W	12161-333	GPR5053XM333G
R3, 8	Resistor, MF, 10K, ±2%, ¼W	12161-103	GPR5053XM103G
R4, 12	Resistor, MF, 47K, ±2%, ¼W	12161-473	GPR5053XM473G
R5	Resistor, MF, 120K, ±2%, ¼W	12161-124	GPR5053XM124G
R6	Resistor, MF, 150K,±2%,¼W	12161-154	RL07S154G
R9	Resistor, MF, 270 Ohms, ±2%, ¼W	12161-271	GPR5053XM271G
R11	Resistor, MF, 47 Ohms, ±2%, ¼W	12161-470	GPR5053XM470G
R13	Resistor, MF, 10 Ohms, ±2%, ¼W	12161-100	GPR5053XM100G
R14	Resistor, MF, 100K Ohms, ±2%, ¼W	12161-104	GPR5053XM104G
U1	Integrated Circuit, CPU	36710	3850PC
U2	Integrated Circuit, SMI	36712	3853PC
U3	Integrated Circuit, Dual 1 of 4 Decoder	36671	74LS139J
U4	Integrated Circuit, Octal 3-State Transceiver	36741	74LS245J
U5-7	Integrated Circuit (RACAL Program)	(see Table 7-5)	
U8, 9	Integrated Circuit, 1K x 4-bit RAM	36789	NEC445L
U10	Not Used		
U11	Integrated Circuit, Triple 3 Input NAND (National)	36633	74LS10
U12	Integrated Circuit, Quad 2-Input NOR gate	36660	74LS02
U13	Integrated Circuit, Hex Inverter	36676	74LS04
U14	Integrated Circuit, Octal D Tri-State F/F	36703	74LS374
Y1	Crystal, 2 MHz	A07621	
XU5-7	I.C. Socket, 24 Pin DIP (Jermyn)	70620	A23-2023Z
–	Printed Wiring Board	09043	

CHAPTER 8

FRONT PANEL DISPLAYS (A7A1) AND FRONT PANEL SWITCHES (A7A2)

8.1 THEORY OF OPERATION

This chapter provides information on the Front Panel Display Module A7A1 and the Front Panel Switch Module A7A2; however, these two boards are only a part of the Receiver Control circuitry. This Receiver Control circuitry provides control over the Receiver, either from the front panel or from a remote location and consists of modules: A6A1, A6A2, A7A1, A7A2 and A8. In order to show how the A7A1 and A7A2 modules function within the Receiver control section an overall description of the complete section is presented in Chapter 7. Figure 7-1 shows the function of the five modules within the Receiver Control section, Figure 7-2 shows a functional block diagram and Figure 8-1 shows an Interconnect diagram between A7A1 and A7A2.

8.1.1 Front Panel Display (A7A1)

The function of the A7A1 module is shown in the overall functional block diagram in Figure 7-2 of Chapter 7. A schematic diagram is shown in Figure 8-2. The front panel displays are contained on Display Board A7A1. These displays are continually updated and driven, in programmed sequence, by the microprocessor CPU through the data bus. The displays include the numerical indicators of the tuned and BFO frequencies, the memory and the Antenna and Auxiliary selections, the receiver status LED indicators and the AF and RF meter level LED readouts. As indicated in the Block Diagram, Figure 7-2, in Chapter 7 the numerical displays are driven from the data bus through decoders and latches. The decoders convert the digital data on the bus to the code required to drive the seven segment numerical displays. Each of the digits in the numerical displays are driven, in programmed sequence, by the enabling signals from the data select and strobes circuitry (directed by the strobe logic and tri-state latched switch outputs from the microcomputer board). The receiver status and meter level LED's are each driven, in programmed sequence, from the data bus through demultiplexers controlled by the data select and strobes circuitry.

The Front Panel Displays are contained on Board A7A1. These displays are continually driven and updated, in programmed sequence, by the microcomputer. Sheet 1 of Figure 8-2 shows that the signals from the microcomputer come into the A7A1 board through J1 connector. The data bus inputs IOD0-IOD7 are fed into the latch U99. The data on the data bus is latched to the outputs of U99, through inverter stage Q1, by the short /WSTB signal pulse from the microprocessor. This latched output data (FPD0-FPD7) from U99 will be held until the next read in from the microprocessor. This data will be fed to the appropriate display by the strobes generated by the output latch U95.

U95 is fed by the IOC0-IOC3 select and the /WSTB strobe, signals from the microprocessor. One of the 16 DVS outputs of U95 is latched on at a time and will direct the FPD0-FPD7 data to the appropriate LED display. One shots U85A and U85B supply a delayed INHIBIT pulse to assure appropriate timing so that the data is correctly latched.

8.1.1.1 Meter Display

For example, when DVS0 strobe is generated, it strobes FPD0-FPD3 into latch U98. U98 is a one of 16 output which, through drivers U66 and U80 drives the AF-RF meter LED U1-13 displays. Here one of the LED's U3-13 is activated, indicating the metered level. Resistors R5-8 limit the current through the LED's. Either the AF(U2) or RF (U1) LED is activated by inputs to pins 1 and 2 of U66 which in turn are fed by decoder U83A and latch U89.

8.1.1.2 Status Displays

The status display LED's U51-56, are activated (in the proper program sequence) by the DVS1 strobe. This strobe clocks data FPD0-FPD5 into flip-flop U92. The U92 outputs, through the driver U84, then drive the appropriate displays.

8.1.1.3 Mode and AGC Displays

The Mode and AGC display LED's U26-29 and U15-18 are activated (in the proper program sequence) by the DVS2 strobe. This strobe clocks data FPD0-FPD5 into flip-flop U90. The U90 outputs, through the decoder U82 and drivers U68 and U84, then drive the appropriate displays.

8.1.1.4 Tune and MEM SCAN Displays

The tune display LED's, U62-65, are also activated (in the proper program sequence) by the DVS2 strobe. The outputs from pins 2 and 5 of U91 flip-flop, through decoder U83B and driver U70, drive the appropriate displays.

The MEM SCAN display LED, U50, is activated (in the proper program sequence) by the DVS3 strobe. This strobe clocks data FPD0-FPD4 into flip-flop U89. The U89 output from pin 10, through driver U70, drives the MEM SCAN LED U50.

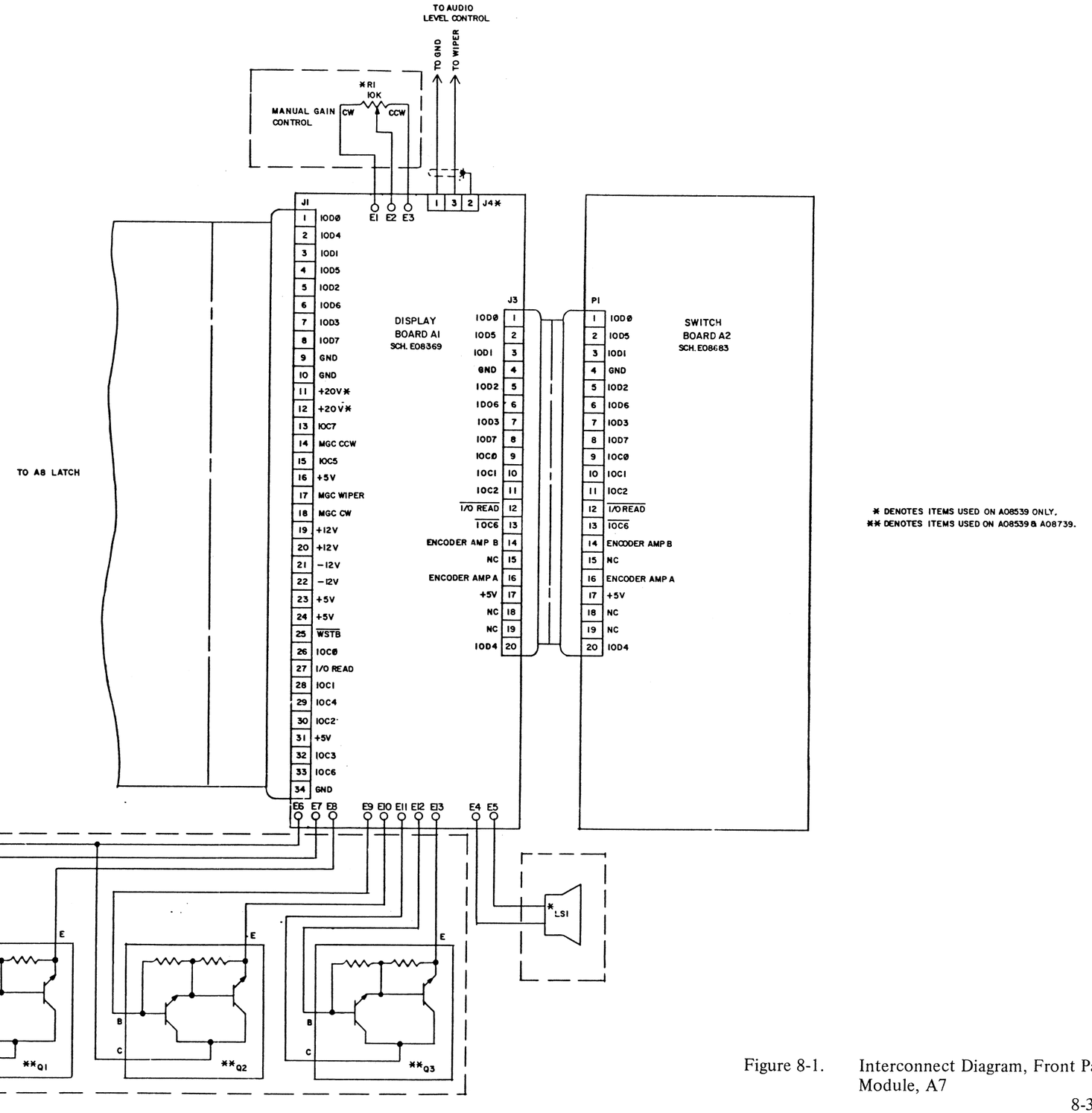
It should be noted that the output from pin 2 of U89 goes through decoder U83 and driver U66 to come out of pins 15 and 16 of U66 as the AF and RF meter inputs, described previously. Also the output from pin 12 of U89 goes on to switch the front panel speaker in or out through Q6 and Q7.

8.1.1.5 Filter Display

The filter display LED's U19-25, are activated (in the proper program sequence) by the DVS4 strobe. This strobe clocks data FPD0-FPD5 into U69 flip-flop. The U69 outputs, through the decoder U81 and driver U67, drive the appropriate displays.

8.1.1.6 Speaker Amplifier

Amplifier stage U103 supplies drive for the audio signal going to the front panel speaker. The output of this stage connects to the speaker mounted on the sub-panel assembly. The input to the amplifier is controlled by transistors Q6 and Q7. This analog switch will connect either ground or the audio signal input (from the audio level control on the front panel) to the amplifier input. The analog switch is controlled by the input from U89-12, as described earlier.



* DENOTES ITEMS USED ON A08539 ONLY.
** DENOTES ITEMS USED ON A08539 & A08739.

Figure 8-1. Interconnect Diagram, Front Panel Module, A7

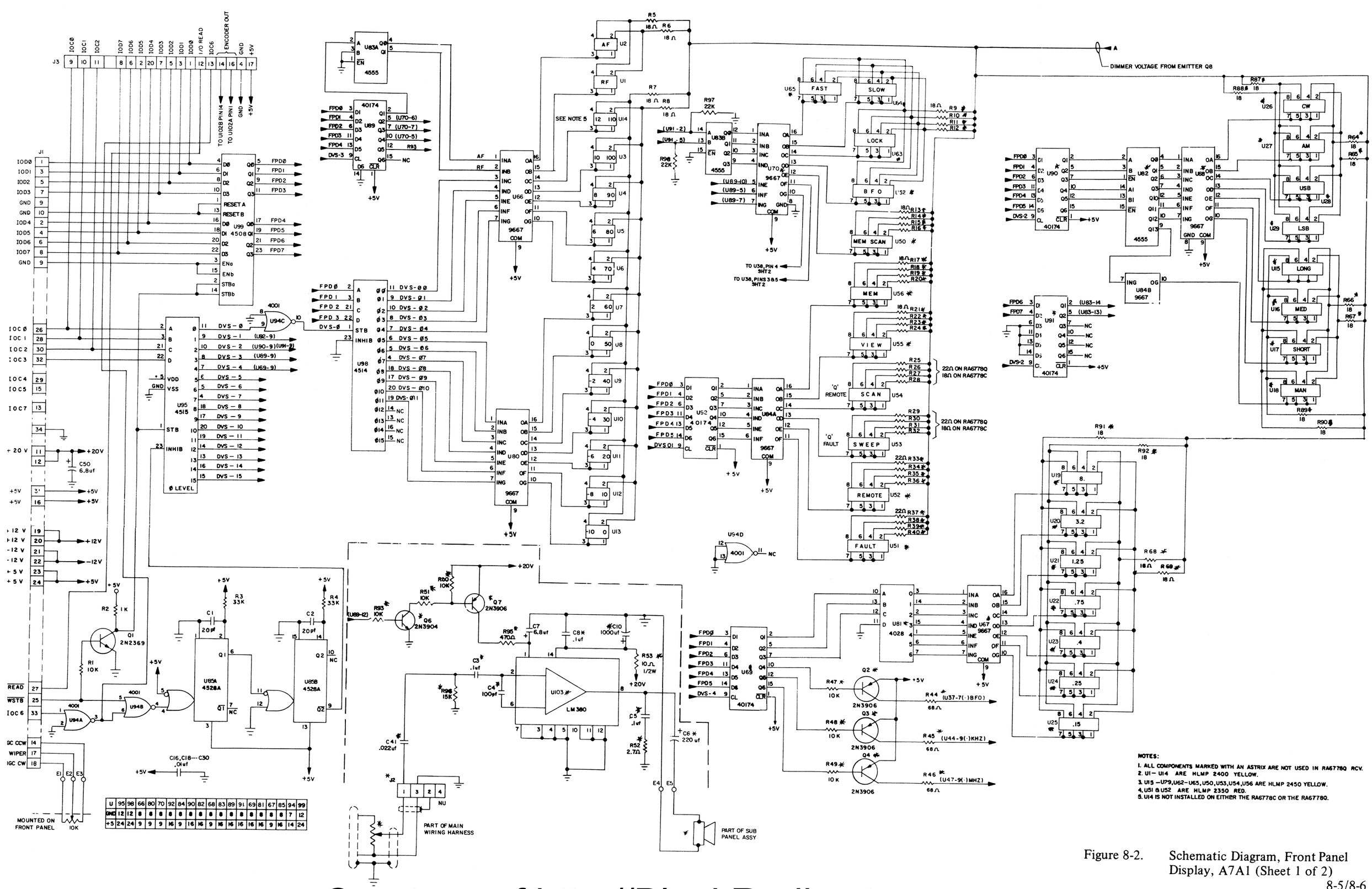
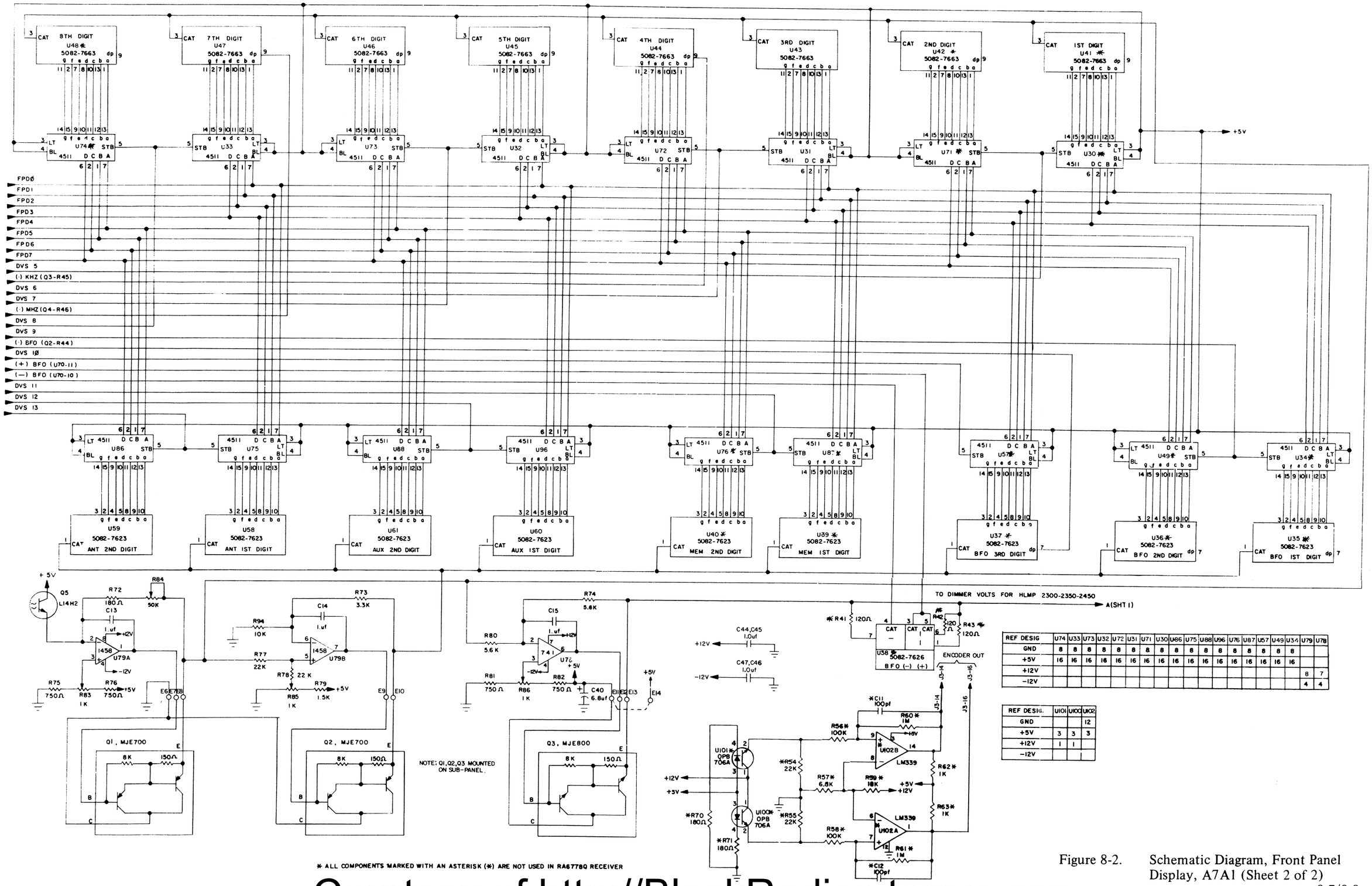


Figure 8-2. Schematic Diagram, Front Panel Display, A7A1 (Sheet 1 of 2)

8-5/8-6



REF DESIG	U74	U33	U73	U32	U72	U31	U71	U30	U86	U75	U88	U96	U76	U87	U57	U49	U34	U79	U78
GND	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8		
+5V	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16	16		
+12V																		8	7
-12V																		4	4

REF DESIG.	U101	U100	U102
GND			12
+5V	3	3	3
+12V	1	1	
-12V			

Figure 8-2. Schematic Diagram, Front Panel Display, A7A1 (Sheet 2 of 2)

8.1.1.7 Numerical Displays

Sheet 2 of Figure 8-2 is the schematic diagram of the numeric displays and their associated strobing, latch and driving circuitry. The numeric displays include the tuned frequency in kHz, the BFO frequency in kHz with sign (offset above or below center frequency), the memory channel selected and the antenna and auxiliary selections. Each numeric digit of the display is a seven segment LED display.

As indicated, each of the seven digits for the tuned frequency display (U41-47) is a type 5082-7663 display. Each of the 9 numeric digits for the BFO frequency, memory channel and antenna and auxiliary selections is a type 5082-7623 display. Each display digit is driven from its associated BCD-to-7-segment latch decoder driver type 4511 (U30-34, U49, U57, U71-73, U75-76, U86-88 and U96). The BCD input to each Latch Decoder Driver is supplied, in programmed sequence, by the FPD0-FPD7 bus (data from the microprocessor data bus, obtained as described previously). The data is latched, in the appropriate time sequence, two digits at a time, by the strobing signals DVS5-13 obtained from the microprocessor as described previously. The type 4511 then decodes the latched BCD data into the code required to drive the displays.

The + or – display for the BFO frequency indication is obtained from the type 5082-7626 LED display (U38). This display is driven by the + BFO and – BFO signals obtained from pins 10 and 11 of U70 (sheet 1), as described previously.

Also, the decimal points for the tuned frequency display and the BFO frequency display are obtained from displays U44 and U37, respectively. These are driven by the (·) BFO signals obtained from Q3-R45 and Q2-R44 (Sheet 1), as described previously.

Stages Q5, U78, U79A and U79B provide the dimmer inputs for the LED displays. Q5 is mounted on the front panel and is exposed to ambient light conditions. Its output (proportional to ambient light intensity) drives stage U79A (with output drive Q1). The output of stage U79A provides the dimmer drive to the tuned frequency displays through the CAT (pin 3) input. This sets the display light output to be compatible with ambient light conditions.

U79A output also drives the similar U79B and U78 stages. U79B provides the dimmer output for the BFO, MEMORY, Auxiliary and Antenna numerical displays. U78 provides the dimmer output for the BFO sign display (U38) and all the other front panel individual LED displays.

8.1.1.8 Tuning Encoder

As indicated on sheet 2 of Figure 8-2, the A7A1 board also contains the tuning encoder electronic circuitry (U100-102). The Tuning encoder is an optical displacement transducer of the incremental type. A metal coding disc enscribed with mirrored and black strips is attached to the encoder spindle, and rotates over two sets of LED/phototransistor detectors (U100 and U101). As the disc rotates, the detectors produce amplified pulse waveforms at the encoder outputs, pins 16 and 14 of J3. The detectors are physically displaced so that the two outputs are 90^{o} out-of-phase. Clockwise rotation of the tuning knob (from the front) causes output No. 2, at pin 14 of J3, to lead as shown in Figure 8-3. Counterclockwise rotation causes output No. 1 at pin 16 to lead.

The outputs of the two phototransistors, which are close to sinusoidal, are squared by the divider comparators U102A and B. Each transistor output is compared to a dc voltage set up by R57-R59 which controls the comparator zero crossings.

8.1.2 Front Panel Switches (A7A2)

The function of the A7A2 module is shown in the overall functional block diagram in Figure 7-2 of Chapter 7. A schematic diagram is shown in Figure 8-4. The front panel control switches are

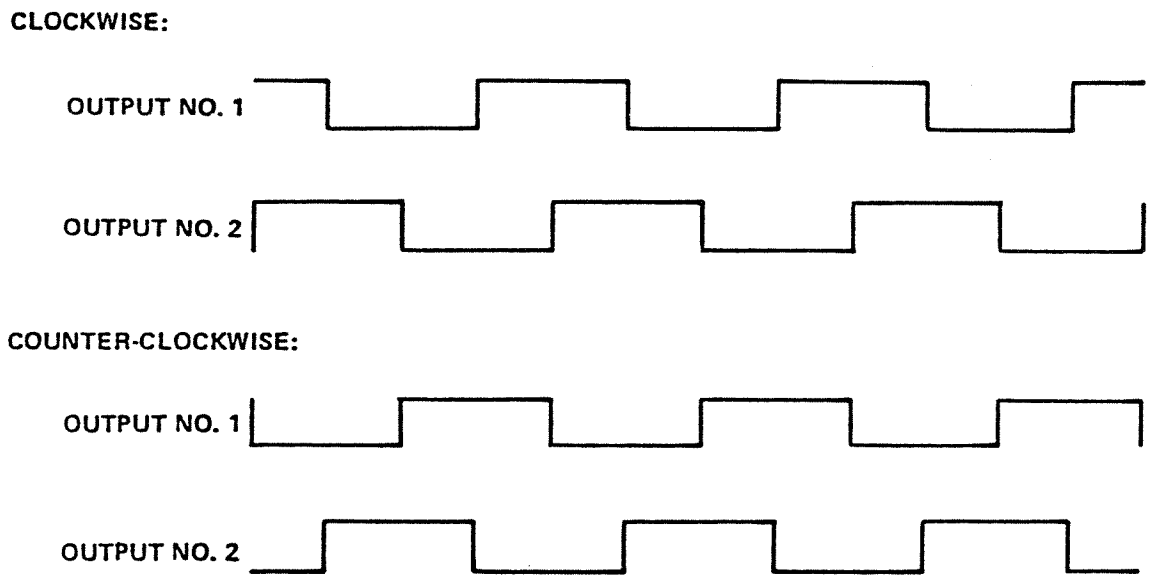


Figure 8-3. Encoder Outputs

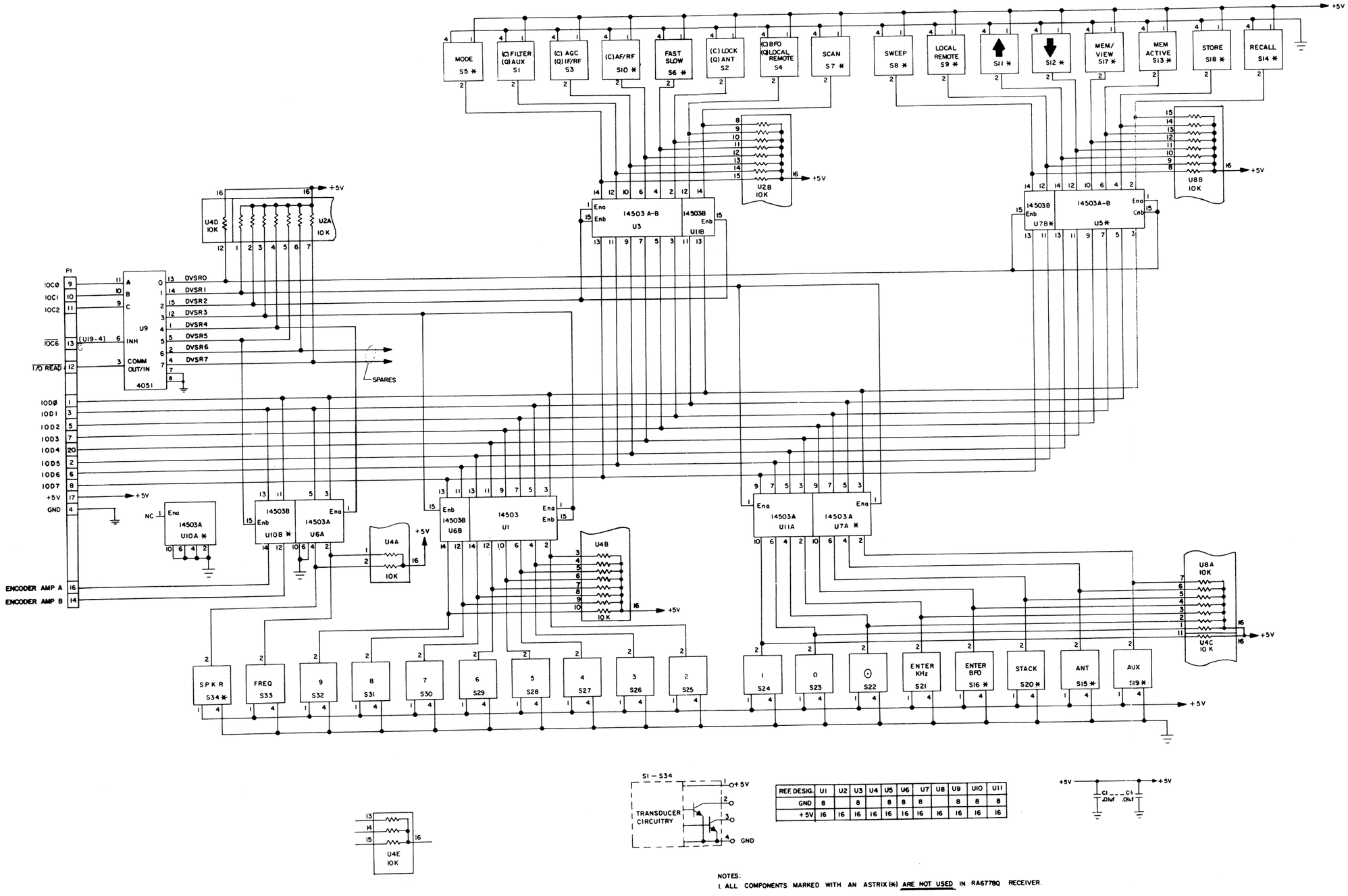
contained on switch Board A7A2. These switches are continually read, in programmed sequence, by the microcomputer CPU through the data bus. As indicated in the Block Diagram, Figure 7-2 in Chapter 7, the panel switches are read through the tri-state data select buffers onto the data bus. The switches are read in groups, with the groups being selected by enabling their associated buffer. The data select and strobe circuitry selects the buffers, in the programmed sequence, as directed by the strobe logic and tri-state latched switch outputs from the microcomputer board. It should be noted that the two digital outputs from the tuning knob encoder (in Board A7A1) are read out here as if they were two additional switches.

The ON or OFF state of the control switches on the Front Panel Switch Board A7A2 are continually read, in programmed sequence, by the microcomputer. The 34 switches are arranged in four separate groups of 8 and one group of 2. Each group, in programmed sequence, is strobed onto the data bus (IOD0-IOD7) through the associated tri-state buffers U1, 3, 5, 6, 7 and 11. Each set of buffers is enabled at the correct program times by the output from the demultiplexer U9. The timing and outputs of this demultiplexer are controlled by the /IO READ, IOC0-IOC2 and /IOC6 inputs from the microcomputer. For example, the DVSR3 output from the multiplexer (at /IO READ) enables tri-state buffers U1-U6B which place switches S25-32 on the data bus to be read by the microcomputer.

It should be noted that the tuning knob encoder outputs from board A7A1 come in through pins 14 and 16 of P1. These inputs are enabled through tri-state buffer U10B and are read out by the microcomputer in a manner similar to that described above for the front panel switches.

8.2 FRONT PANEL ASSEMBLY, A7, TEST FIXTURE

Testing and troubleshooting of the front panel display circuit card A7A1 and the front panel switches circuit card A7A2 is accomplished with the two units connected together and on the same test fixture. The test fixture provides a convenient base for mounting the circuit cards for testing



REF. DESIG.	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11
GND	8		8		8	8	8		8	8	8
+5V	16	16	16	16	16	16	16	16	16	16	16

NOTES:
1. ALL COMPONENTS MARKED WITH AN ASTRIX (*) ARE NOT USED IN RA6778Q RECEIVER.

Figure 8-4. Schematic Diagram, Front Panel Switches, A7A2

while at the same time providing easy access to the card under test for troubleshooting.

The A7 test fixture contains a programmed A6A2 circuit with type C test ROM's along with controls and indicating LED's which permits testing the A7 assembly for performance. The test fixture also contains an encoder wheel for testing the infrared sensors on the A7 assembly. Figure 8-5 shows the A7 test fixture. Figure 8-6A shows the A7A1 overall assembly while Figure 8-6B shows the circuit card and Figure 8-7A shows the A7A2 overall assembly while Figure 8-7B shows the circuit card.

8.3 TEST EQUIPMENT AND ACCESSORIES

Table 8-1 lists the test equipment and accessories required to completely test the A7 module.

Table 8-1. Test Equipment and Accessories

Item	Description	Recommended Equipment or Equal
1	Oscilloscope	Tektronix 465
2	Digital Voltmeter	Fluke 8000A
3	Power Supplies: +5 VDC @ 4 amp, +10 VDC, +12 VDC, -12 VDC, -20 VDC.	Racal
4	A7 Test Fixture	Racal

8.4 TEST AND ALIGNMENT

The following procedures provide the information necessary to completely test the A7 module.

All tests should be performed at ambient room temperature. Record results on test data sheets, pages 8-22 (A7A1) and 8-23 (A7A2).

8.4.1 Front Panel Display A7A1 and Front Panel Switches A7A2 Test

1. Turn the power supplies off. Connect the power supplies to connector on rear panel, according to Table 8-2.

Table 8-2. Power Connections

Pin #	Function	Pin #	Function
1	+20V	5	GND
2	+12V	6	-12V
3	+ 5V	7	+5V UNREG.
4	N.U.	8	N.U.

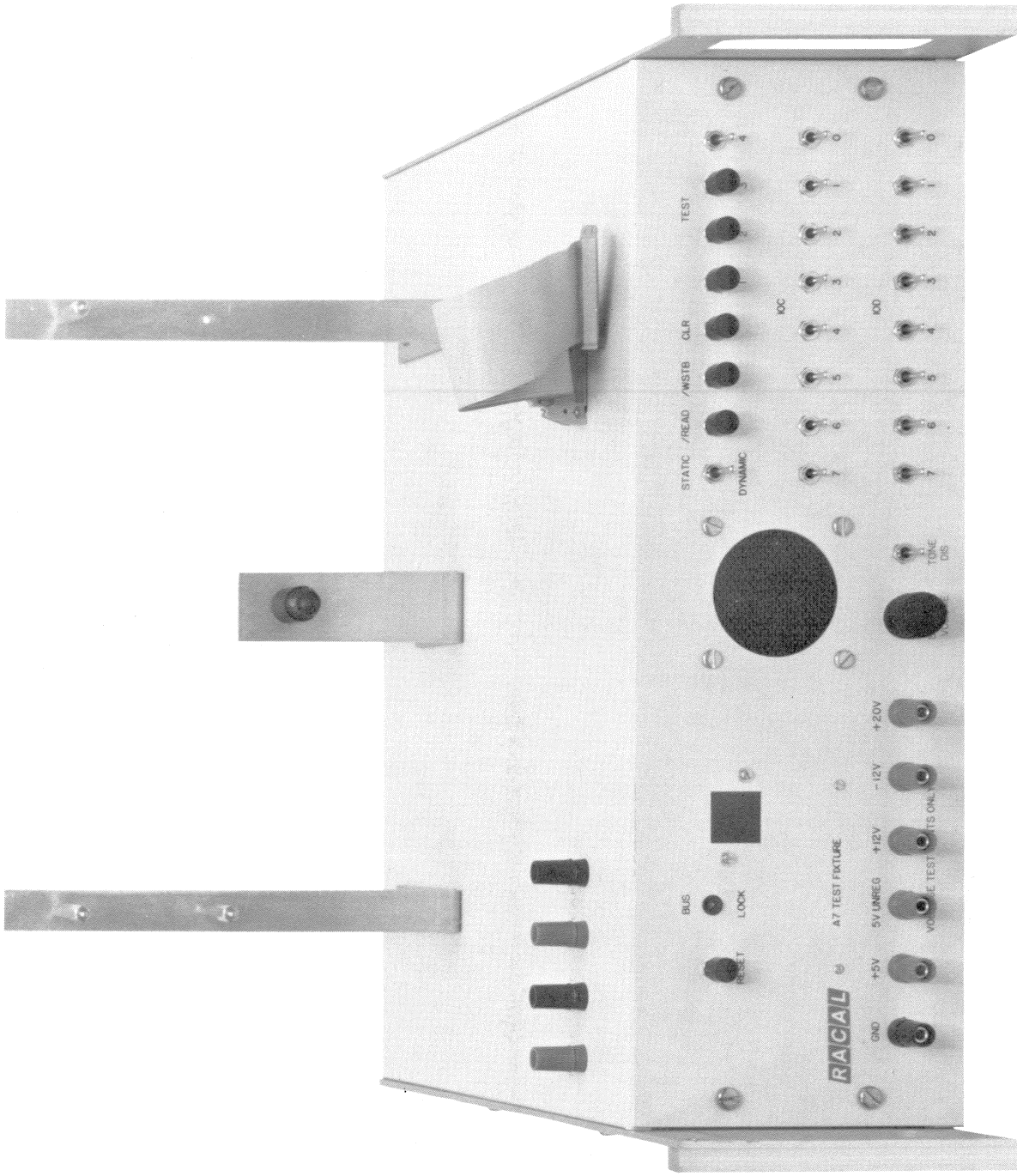


Figure 8-5. Front Panel Module A7, Test Fixture

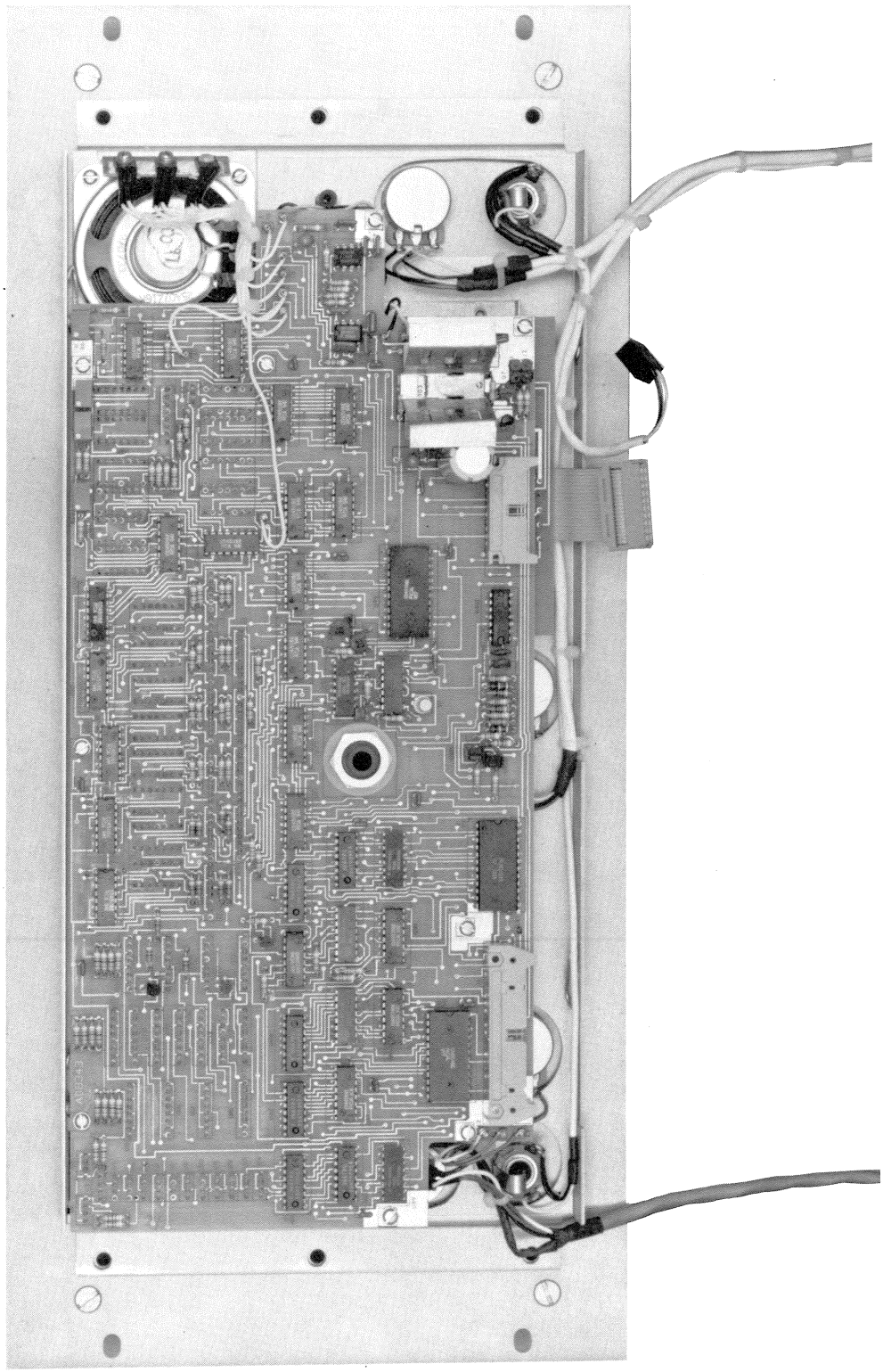


Figure 8-6A. Front Panel Display A7A1, Overall Assembly

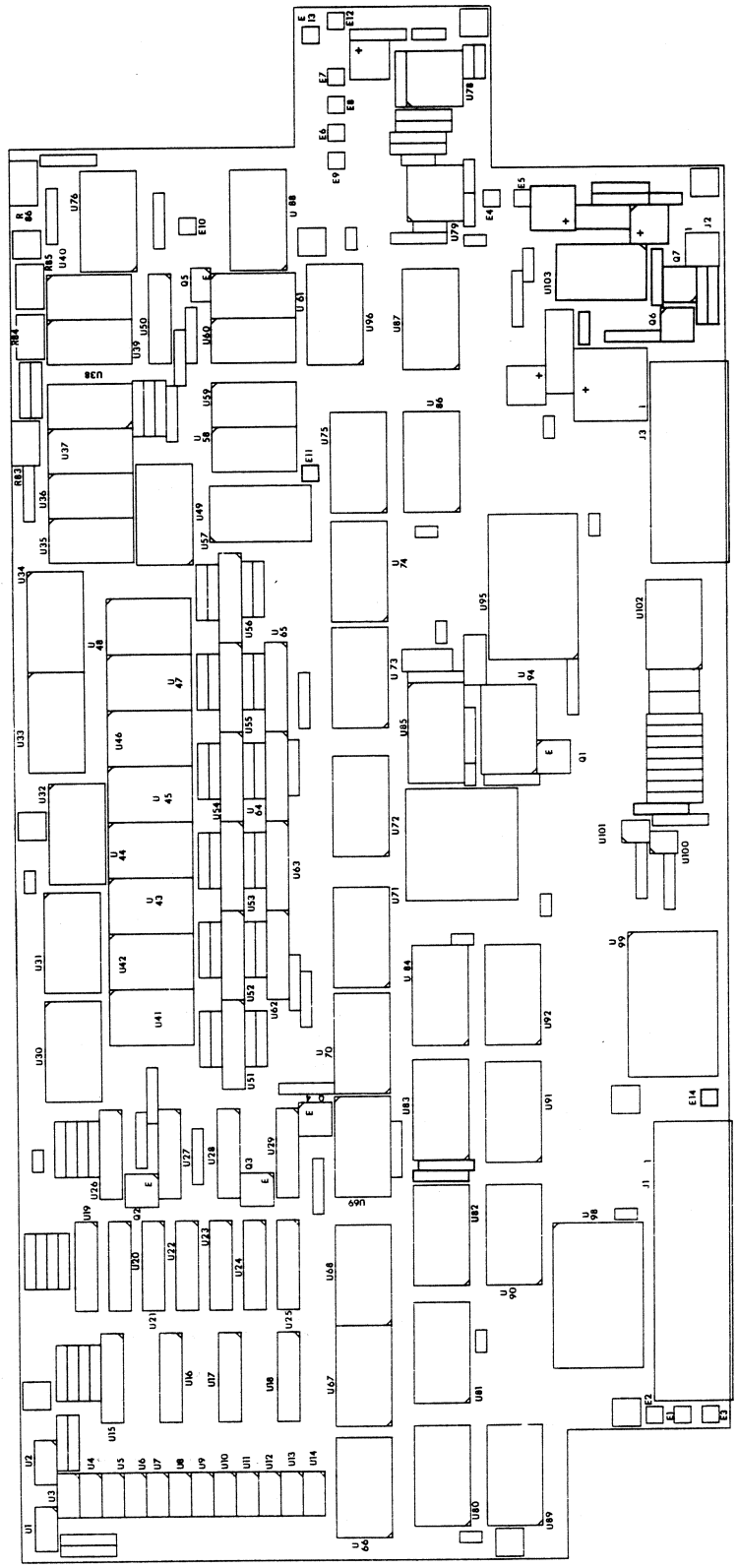


Figure 8-6B. Front Panel Display A7A1, Circuit Card

2. Connect the 34 Pin connector from test fixture to the A7 assembly. Connect the 3 pin connector from test fixture to the A7 assembly.

3. Connect black "Speaker" binding post on test fixture to point E4 on A7A1 board. Connect red "Speaker" binding post on test fixture to point E5 on A7A1 board.

4. Place "C-Q" switch on test fixture to "C" position. (Test Switch #4 up.)

5. Turn the power supplies on. Press the CLEAR then the RESET pushbuttons.

6. "BUS LOCK" light on test fixture should go out within one second after releasing "RESET" (on test fixture). If it remains on, switch power off immediately, as this indicates a serious fault on the board. Usually, the cause is a short circuit or solder splash and leaving the power on can result in damage to the board under test, the test fixture or both.

7. Set up test area which will produce 100 ft. candles of light. This light is produced by cool white florescent lamps and is to be measured with a standard light meter. (This level is to be present at the location of the photodetector on the Front Panel.)

8. Turn pot. R84 full clockwise as seen from rear of receiver to produce minimum gain of amp U79A.

9. Adjust R83 to read 2.45 volts at test point E8.

10. Adjust R85 so the intensity of the small digits match the intensity of the large digits.

11. Adjust R86 so the intensity of the bar LEDs match the intensity of both the large and small digits.

12. Adjust R84 for minimum satisfactory brightness/of Freq. Display, but voltage at E8 on A7 is not to exceed 2.5 volts.

13. Vary the amount of light allowed to fall on the photo detector. The overall brightness of the Front Panel indicators should vary in proportion to the amount of light striking the photo detector. Check on test data sheet.

8.4.2 Keyswitch Test (A7A2 Only)

1. Set static/dynamic switch to "Dynamic".

2. Press Test Switch #1.

3. Exercise each keyswitch on A7 assembly. A number should be displayed on test fixture display digits which corresponds to Figure 8-8. Record results on data sheet.

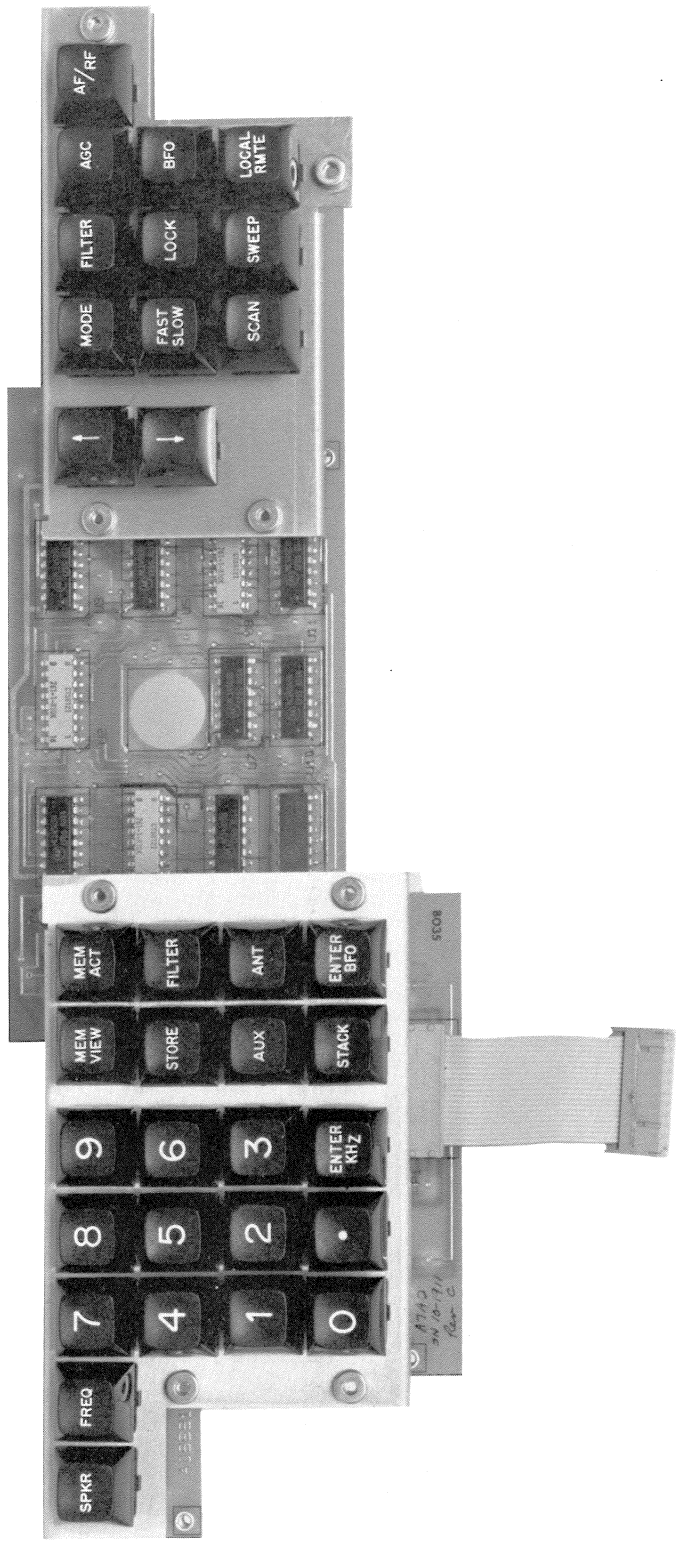


Figure 8-7A. Front Panel Switches A7A2, Overall Assembly

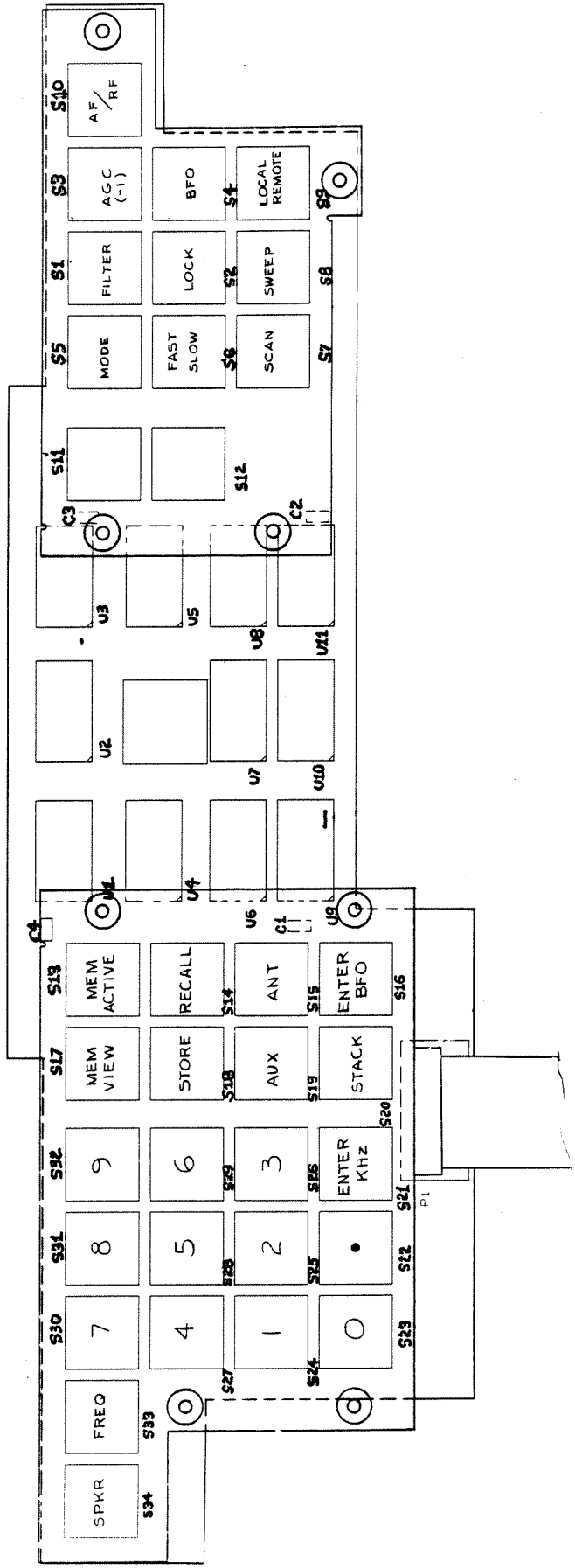


Figure 8-7B. Front Panel Switches A7A2, Circuit Card

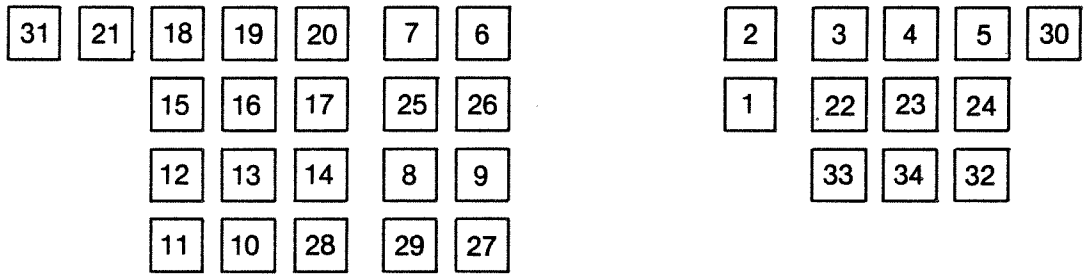


Figure 8-8. Keyswitch Test Display Numbers

4. Press "CLEAR" button on test fixture.

5. Press "RESET" button on test fixture.

8.4.3 Tuning Encoder Test

1. Place A7 assembly on test fixture so the encoder wheel of test fixture is behind infrared sensors of A7 assembly.

2. Press the "FAST/SLOW" switch on the A7A2 board so that the slow tuning function is enabled. Check that the main frequency display tunes at a rate of 1 kHz per revolution. Record on test data sheet.

3. Use the "FAST/SLOW" switch to enable fast tuning. Ensure that the tuning rate of the main frequency display corresponds to 10 kHz per revolution. Record on test data sheet.

8.4.4 Front Panel LED Segment Tests

1. Press Test Switch #2.

2. Meter segments should light successively. Record on test data sheet.

3. Press "CLEAR" button on test fixture.

4. Press "RESET" button on test fixture.

5. Test all Front Panel LED's by exercising Front Panel switches, as in normal receiver operation. The "FAULT" lamp should blink continuously throughout this procedure. Record on data sheet.

8.4.5 Audio Amplifier Test

1. Turn the test fixture internal generator to ON.

2. Press RESET and listen for a tone.

3. If no sound is heard, press the speaker switch on the A7 board. If there is still no sound, a problem exists within the amplifier system. Record on test data sheet.

4. Connect the scope probe to the active speaker terminal.

5. A 3.5 Volt peak sine wave should be seen on the scope. Be sure there are no oscillations or excessive distortion present. Record results.

6. Press "SPEAKER" switch on A7A2 board. The tone should switch on and off with successive depressions of this switch. Record on data sheet.

7. Note that the "SPEAKER VOLUME" control on the test fixture is for operator convenience only and has no effect on the above test parameters.

8. All tests are now complete.

8.4.6 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (front panel displays, switches, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failures of specific frequency counts can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope or voltmeter, to trace the fault to a single component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconducts and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, the tests for the complete module should then be performed.

8.5 PARTS LIST, FRONT PANEL MODULE A7

The parts list for the A7 module is contained in Table 8-3. Tables 8-4 and 8-5 contain a detailed listing of the components contained on the A7A1 and A7A2 Circuit Card Assemblies.

DATE _____
CKD BY _____

MODULE A7A1
USED ON _____

TEST DATA SHEET

PART NAME: A7A1 Front Panel Assembly
PART NUMBER: 08343-1
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
8.4.1(13)	Uniform LED Intensity				
	(LED's Dim Uniformly)		Pass	Fail	
8.4.3(2)	Tuning Encoder Test – SLOW		Pass	Fail	
8.4.3(3)	Tuning Encoder Test – FAST		Pass	Fail	
8.4.4(2)	Meter Segments Light Successively		Pass	Fail	
8.4.4(5)	All LED's Function Correctly		Pass	Fail	
8.4.5(3)	Tone heard from Speaker		Pass	Fail	
8.4.5(5)	3.5V P-P Sine Wave present		Pass	Fail	
	Sine Wave is Stable and Free of				
	Excessive Distortion				
8.4.5(6)	Speaker Switch Test		Pass	Fail	

DATE ____________ MODULE A7A2

CKD BY ____________ USED ON ____________

TEST DATA SHEET

PART NAME: A7A2 Front Panel Assembly JOB NO: ____________

PART NUMBER: 08681-1 SERIAL NO: ____________

USED ON: ____________

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
8.4.2(3)	All Keyswitches Respond to Panel		Pass	Fail	
	Commands				

TABLE 8-3. PARTS LIST, PANEL BOARD ASSEMBLY, A7 08698-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A7A1	LED Display Card Assembly (See Table 8-4 for further breakdown)	08343-1	
A7A2	Pushbutton Switch Card Assembly (See Table 8-5 for further breakdown)	08681-1	
	Sub Panel	08608	
	Retainer Ring	75116	
	Bushing, Encoder Spacer	08736	
	Shaft, Encoder	08735	
	Disc, Encoder	08229	
	A7A1 Support Bracket	09367	

TABLE 8-4. PARTS LIST, LED DISPLAY CIRCUIT CARD ASSEMBLY, A7A1 08343-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 2	Capacitor, Ceramic, 20pF, ± 5% (Erie)	21352	801-000-C0G0200J
C3, 5, 8	Capacitor, Ceramic, 0.1 uF, ±20% (Erie), 50V	21732	8131-050-651-104M
C4	Capacitor, Mica, 100 pF, ±5%	22109	CM05E101G03
C6	Capacitor, Electrolytic, 220 uF,-10% +75%,16VDC	24072	T362A685M035AS
C7, 40, 50	Capacitor, Tantalum, 6.8 uF, ±20%	25060-685	T362A685M035AS
C10	Capacitor. Electrolytic, 1000 uF, -10% +75%, 25 VDCW	24073	100N25
C11, 12	Capacitor, Ceramic, 100 pF, ±10%	21763	831-000-S5F0-101K
C13-15, 44-47	Capacitor, Ceramic, 1.0 uF, ±20% (Erie)	21748	8131-050-651-105M
C16, 18-30	Capacitor, Ceramic, 0.01 uF, ±20% (Erie)	21733	8121-050-651-103M
C41	Capacitor, Ceramic, 0.022 uF, ±20% (Erie)	21762	8121-050-651-223M
C9, 17, 31-39, 42, 43, 48, 49	Not Used		
J1	Connector, Ribbon, 34 Contact	61224	3431-1002
J2	Connector, 4 Pin BERG	06846-2	
J3	Connector, Ribbon, 20 Contact	61276	3492-1002
Q1	Transistor, NPN, Silicon, high speed switching	32255	2N2369
Q2-4, 7	Transistor, PNP, low power	32037	2N3906
Q5	Transistor	32521	L14H2
Q6	Transistor, NPN, low power	32036	2N3904
R1, 47-51, 93 94	Resistor, Film, 10K Ohms, ±2%, ¼W	12161-103	RL07S103G
R2, 62, 63	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R3,4	Resistor, Film, 33K Ohms, ±2%, ¼W	12161-333	RL07S333G
R5-32, 64-69, 87-92	Resistor, Film, 18 Ohms, ±2%, ¼W	12161-180	RL07S180G
R33-40	Resistor, Film, 22 Ohms, ±2%, ¼W	12161-220	RL07S220G
R41-43	Resistor, Film, 120 Ohms, ±2%, ¼W	12161-121	RL07S121G
R44-46	Resistor, Film, 68 Ohms, ±2%, ¼W	12161-680	RL07S680G
R52	Resistor, Composition, 2.7 ohms, ±5%, 1/4W	10601	
R53	Resistor, Film, 10 Ohms, ±2%, ¼W	10915	RC20GF100J
R54, 55	Resistor, Film, 22K Ohms, ±2%, ½W	12161-223	RL07S223G
R56, 58	Resistor, Film, 100K Ohms, ±2%, ¼W	12161-104	RL07S104G

TABLE 8-4. PARTS LIST, LED DISPLAY CIRCUIT CARD ASSEMBLY, A7A1 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R57	Resistor, Film, 6.8K Ohms, ±2%, ¼W	12161-682	RL07S682G
R59	Resistor, Film, 18K Ohms, ±2%, ¼W	12161-183	RL07S183G
R60, 61	Resistor, Film, 1 meg Ohms, ±2%, ¼W	12161-105	RL07S105G
R70-72	Resistor, Film, 180 Ohms, ±2%, ¼W	12161-181	RL07S181G
R73	Resistor, Film, 3.3K Ohms, ±2%, ¼W	12161-332	RL07S332G
R74, 80	Resistor, Film, 5.6K Ohms, ±2%, ¼W	12161-562	RL07S562G
R75-76, 81-82	Resistor, Film, 750 Ohms, ±2%, ¼W	12161-751	RL07S751G
R77-78, 97-98	Resistor, Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S223G
R79	Resistor, Film, 1.5K Ohms, ±2%, ¼W	12161-152	RL07S152G
R83, 85, 86	Resistor, 1K ohms, Potentiometer	16083	3299W-1-102
R84	Resistor, 50K ohms, Potentiometer	16095	
R95	Resistor, Film, 470 Ohms, ±2%, ¼W	12161-471	RL07S471G
R96	Resistor, Film, 15K Ohms, ±2%, ¼W	12161-153	RL07S153G
U1-13	Integrated Circuit, LED assembly	41022	HLMP2400
U14, 93, 97	Not Used		
U15-29, 50, 53-56, 62-65	Integrated Circuit, LED assembly	41023	HLMP2450
U30-34, 49, 57, 71-76, 86-88, 96	Integrated Circuit, Seven Segment Decoder Driver	36683	CD4511B
U35-37, 39, 40, 58-61	Integrated Circuit, LED assembly	36737	HP5082-7623
U38	Integrated Circuit, LED assembly	36738	HP5082-7626
U41-48	Integrated Circuit, LED assembly	36739	HP5082-7663
U51-52	Integrated Circuit, LED assembly	41021	HLMP-2350
U66-68, 70, 80, 84	Integrated Circuit, 7 channel LED driver	36690	UA9667DC
U69, 89-92	Integrated Circuit, Hex D flip-flop	36766	F40174BDC
U77	Not Used		
U78	Integrated Circuit, Operational Amplifier	36821	UA741TC
U79	Integrated Circuit, Dual Operational Amplifier	36673	UA1458RC
U81	Integrated Circuit, Decimal Decoder	36575	CD4028

TABLE 8-4. PARTS LIST, LED DISPLAY CIRCUIT CARD ASSEMBLY, A7A1 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U82, 83	Integrated Circuit, Binary Decoder	36579	CD4555R
U85	Integrated Circuit, One Shot Multivibrator	36611	MC14528BCL
U94	Integrated Circuit, Quad 2 input NOR gate	36569	MC14001BCL
U95	Integrated Circuit, 4 bit latch	36615	MC14515BCL
U98	Integrated Circuit, 4 bit latch	36751	MC14514BCL
U99	Integrated Circuit, Dual 4 bit latch	36810	CD4508B
U100, 101	Integrated Circuit, Optical Encoder	36754	OPB706A
U102	Integrated Circuit, Quad Voltage Comparator	36693	LM339
U103	Integrated Circuit, Audio Amplifier	36517	LM380
–	Printed Wiring Board	08370	

TABLE 8-5. PARTS LIST, FRONT PANEL SWITCH CIRCUIT CARD ASSEMBLY, A7A2 08681-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-4	Capacitor, Ceramic, 0.01 uF, ±20%	21733	8121-050-651-103M
SW1-34	Switch, Module (Microswitch)	52419	1001SD4A3A
U1, 3, 5-7, 10, 11	Integrated Circuit, Hex 3 state buffer	36694	MC4503BCL
U2, 4, 8	Integrated Circuit, 15-Resistor network, 10K Ohms	19326-103	4116R-002-103
U9	Integrated Circuit, 8 channel analog multiplexer	36687	CD4051
W1	Cable assembly, A7A1 to A7A2 Interconnect	08761	
–	Printed Wiring Board	08682	

CHAPTER 9
DATA LATCHES (A8)

9.1 THEORY OF OPERATION

This chapter provides information on the Receiver Control Data Latch, Module A8; however, this module is only a part of the Receiver Control circuitry. This Receiver Control circuitry provides control over the Receiver, either from the front panel or from a remote location and consists of modules: A6A1, A6A2, A7A1, A7A2 and A8. In order to show how the A8 module functions within the Receiver Control section, an overall description of the complete section is presented in Chapter 7. Figure 7-1 shows the function of the five modules within the Receiver Control section and Figure 7-2 shows a functional block diagram.

9.1.1 Receiver Control Data Latches (A8)

The function of the A8 module is shown in the overall functional block diagram, Figure 7-2 in Chapter 7. A schematic diagram is shown in Figure 9-1. The operating and tuning data developed by the microprocessor is relayed to the appropriate receiver circuitry through the latches in the Receiver Latch Board A8. As indicated in the Block Diagram, Figure 7-2, in Chapter 7, the receiver circuitry receives signals from latches driven from the data bus. The latches are driven, in programmed sequence. The data on the data bus is latched under control of the data select and strobes circuitry. This circuitry in turn is driven by the strobe logic and tri-state latched switches from the microcomputer board A6A2. The latches hold the data for the receiver circuitry until updated by the microcomputer.

Latch board A8 also contains the Gain Control Digital to Analog Converter. This, in programmed sequence, converts the Remote Control Gain Control digital data, relayed through the data bus, to analog form as required by the receiver circuitry. The AGC select output circuitry selects the appropriate Remote or Local AGC, under control of the microcomputer.

The hardware for the meter circuitry contains a digital to analog converter whose output is used by the software, through a successive approximation routine, to provide analog to digital conversion for front panel display.

Four separate out of lock (OOL) fault indicators are located on the A8 board. These are driven by the out of lock signals from the BFO, LF, HF and TRANSFER VCO loops in the receiver synthesizers. The fault signals are also placed on the data bus in A8, in programmed sequence, and the microprocessor includes these in generating the read out to board A7A1 of the Fault display on the Front Panel. The Latch Board, A8, receives and stores, in the programmed sequence, the microcomputer control data for application to the appropriate receiver circuitry. This includes synthesizer frequency data (main and BFO) and oscillator, filter and AGC selection data.

9.1.1.1 Receiver Control Data Latches

The data from the microcomputer bus (IOD0-IOD7) is read into latches U13, U15, U17, and U21-U24. These latches are latched flip-flops with the latching signal coming into pin 11. The latch signal is applied to each latch, in programmed sequence, by the separate outputs from the gated decoder U29. The inputs to U29 are the logic strobing signals IOC0-IOC5 and timing signal /WSTB from the microcomputer. Thus, the control data from the microcomputer, in programmed sequence, is continually updated into the latches. The latches hold this data on their respective outputs until the next update by the microprocessor. The latch outputs come out of A8 edge connectors A or B to drive the appropriate receiver circuitry. Four of the outputs from U17 go through transistor drivers Q6-10 and then come out to drive the filter selects in mixer A2 (<4 MHz or ⩾4 MHz) and the synthesizer oscillator selects (0-8, 8-18 and 18-30 MHz). The remaining outputs from latch U17 and the outputs from latches U15, U23 and U24 output data for the main synthesizer frequency. Latches U21 and U22 output data for the BFO synthesizer frequency.

Three of the U13 latch outputs drive the decoder-driver, U14, which then outputs the appropriate filter select signal, FL1-FL7, to the filter module A4. Four of the remaining outputs from latch U13 drive the decoder, U12, which then drives the transistor stages Q1-5. These in turn output the receiver mode and AGC control signals to module A5. The remaining output from latch U13 directly outputs an additional AGC (narrow) control signal.

9.1.1.2 OOL Indicators Circuitry

The out of lock signals, BFO OOL, LF OOL, HF OOL and TRANSFER OOL come into A8 through the B edge connector. These signals, through inverters U25C-U25F, drive the set inputs to their respective store flip-flops U8A-B and U16A-B. These flip-flops are clocked, in programmed sequence, by the output from decoder U20 which is controlled by the microcomputer strobe and timing signals IOC0-IOC2, IOC5 and /IO READ. The flip-flop outputs drive the OOL indicating LEDs DS1-DS4. These flip-flop outputs are also placed on the data bus IOD0-IOD3, in correct programmed sequence, through the tri-state buffer U10. U10 is driven by the same strobe signal from U20 used to clock the OOL storing flip-flops. This OOL data on the data bus is relayed, through the microcomputer, to the front panel Fault display circuitry on board A7A1, as described previously.

9.1.1.3 AGC Digital to Analog Converter and Control

The AGC signal out from edge connector B pin 38 (to the receiver circuitry) may originate from one of three inputs dependent on the AGC mode selected. These inputs are the automatic (AGC IN) input through pin 37 of edge connector B, the local manual input from the front panel RF gain control (through pin 17 of J1) and the remote control input through the digital to analog converter (DA Analog switch U27 selects the appropriate AGC signal out (from its S1-4 output to pin 38) of edge connector B. The three separate AGC inputs come in to U27 pins D1, D2 and D3 and the output from U27 is selected by the inputs to U27 pins A1, A2 and A3. These selection inputs (AGC DET, MGC ON and DAC OUT) are generated, in the proper programmed sequence, in latch U26 which is controlled by the microcomputer timing and strobe signals IOD0-IOD2 and /WSTB.

U11 is the DAC which converts the digital inputs (A1-A6) to an analog output from pin 4. This output through amplifier stage U9B is applied to the U27 analog switch, as described previously. The digital input to the DAC is obtained from the latch U18 which in turn is updated by the microcomputer data bus IOD0-IOD5. The latching strobe for the latch U18 is generated by the decoder, U29, by microcomputer strobing and timing inputs IOC0-IOC3, IOC5 and /WSTB. U4 supplies a reference voltage for the DAC and through U9A stage DC bias for output amplifier U9B.

The AGC dump signal (out of pin 50 of edge connector A) is generated by flip-flop U19A by microcomputer signals IOD0 and /WSTB and comes out through transistor stage Q11.

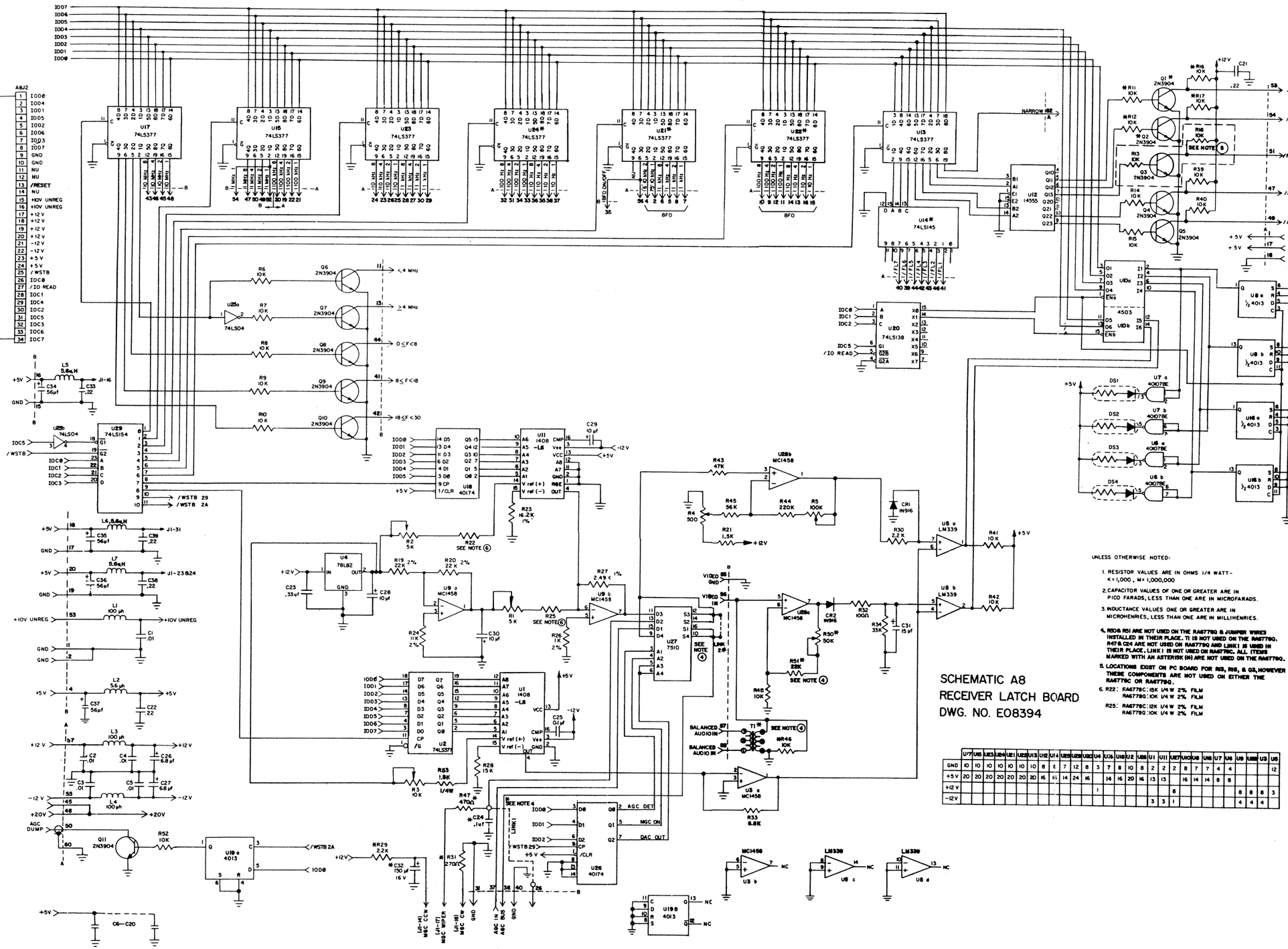


Figure 9-1. Schematic Diagram, Data Latches, A8

9.1.1.4 RF and AF Analog to Digital Converters

The AF input comes in through pins 57-58 of edge connector B and goes through the transformer T1 to drive amplifier stage U28A. In the RA6778C Receiver the Video input to U28A is not used. The rectified output of U28A (through diode CR2) then drives one input to the comparator U5B. The second input to this comparator is the output from the digital to analog converter consisting of stages U2, U1 and U3A. U1 is a DAC which converts its digital inputs (A1-A6) to an analog output from its pin 4. The digital input to this DAC is obtained from the latch U2 which in turn is updated in the correct programmed sequence, by the microcomputer data bus IOD0-IOD7. The latching strobe for the DAC (U1) is generated in decoder, U29, by microcomputer strobing and timing inputs IOC0-IOC3, IOC5 and /WSTB. The DAC output from pin 4 is fed through buffer amplifier U3A to the second input to the comparator U5B. The output of the comparator is read onto the microcomputer data bus line, IOD4, in the correct programmed sequence, through tri-state buffer U10B. This data is strobed onto the data bus by the X1 output strobe from decoder U20 which is controlled by the microcomputer strobing and timing inputs IOC0-IOC2, IOC5 and /IO READ. Thus, the microcomputer, in programmed sequence, steps the digital inputs to the DAC until the comparator output indicates the DAC output is equal to the AF generated input. The microcomputer then supplies the resulting DAC digital input to the AF front panel meter display on board A7A1, as described earlier.

In a similar manner the RF input is converted by the microprocessor for RF meter readout on the front panel. Here, comparator U5A output is read onto the microcomputer data bus through tri-state buffer U10B. The tri-state buffer is controlled by the strobe from U20. One input to the comparator is the same DAC converter output used for the AF meter conversion, as described above. The second input is the RF which is obtained from the output of analog switch U27, through buffer amplifier stage U28B. As described previously, the RF input (through AGC IN) goes through the U27 analog switch in the AGC DET mode.

9.2 DATA LATCHES A8, TEST FIXTURE

Testing and troubleshooting of the Data Latches A8 is accomplished through the A8 test fixture and its associated test equipment. The test fixture provides a convenient base for mounting the A8 circuit card while at the same time provides easy access to the card for troubleshooting.

The A8 test fixture contains a 1 kHz oscillator and front apron controls for testing AF meter circuits, analog circuits and AGC circuits of the A8 circuit card. Figure 9-2 shows the A8 test fixture. Figure 9-3A shows the overall assembly of the module while Figure 9-3B shows the circuit card.

9.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required to test the A8 module are listed in Table 9-1.

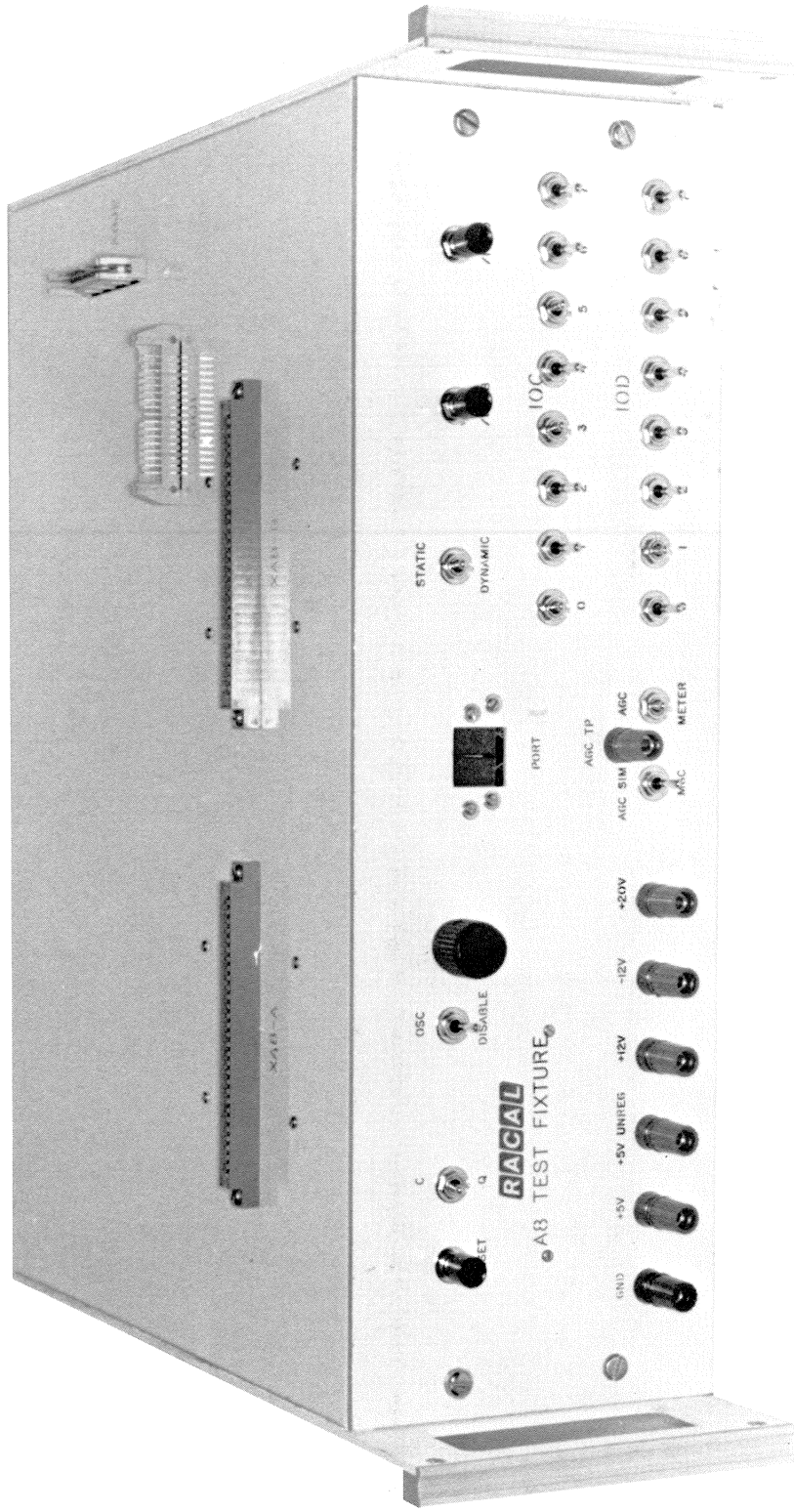


Figure 9-2. Data Latches A8, Test Fixture

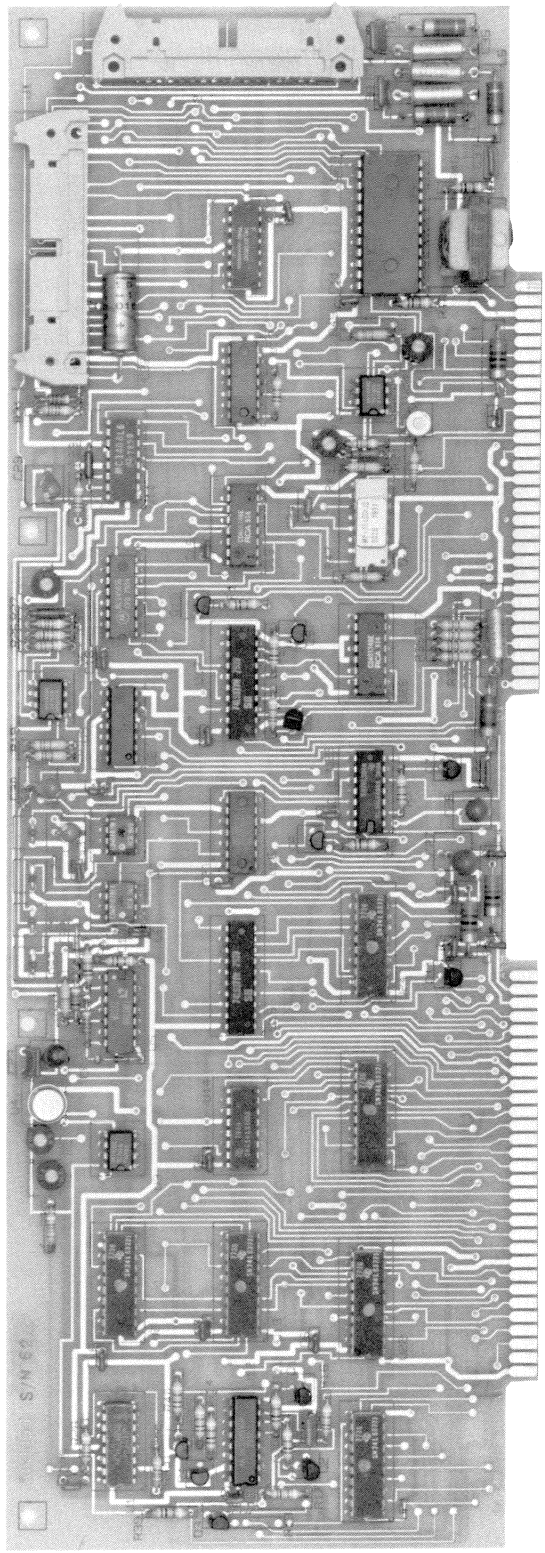


Figure 9-3A. Data Latches A8, Overall Assembly

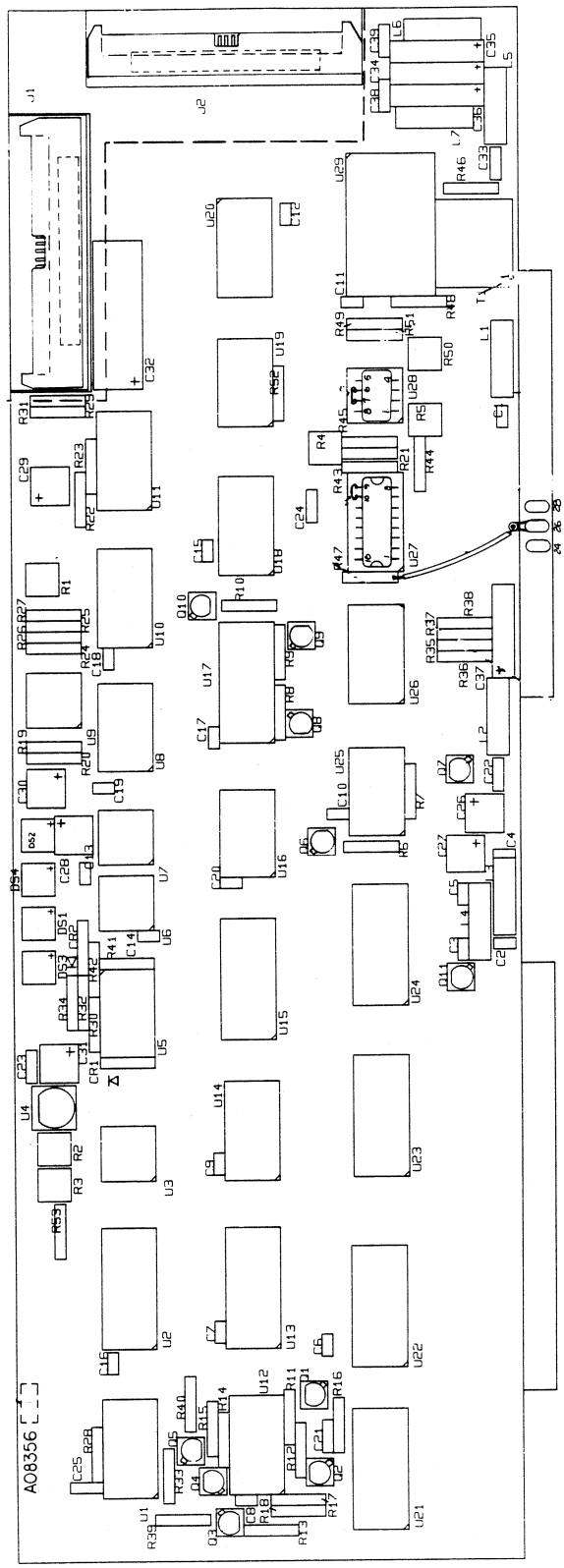


Figure 9-3B. Data Latches A8, Circuit Card

Table 9-1. Test Equipment and Accessories

Item	Description	Recommended Equipment or Equal
1	Oscilloscope	Tektronic 465
2	Digital Voltmeter	Fluke 8000A
3	Power Supplies: +12 VDC, -12 VDC, +5 VDC, +20 VDC	Racal
4	A8 Test Fixture	Racal

9.4 TEST AND ALIGNMENT

The test procedures are provided to check performance and operation of the A8 Data Latches. All tests should be performed at ambient room temperature and all test data should be recorded on test data sheet, page 9-13.

9.4.1 Preliminary Test Set-Up

1. Turn power supplies off. Connect +12, −12, +5 and +20 Volt dc supplies to their respective terminals on the test fixture.

CAUTION

REVERSAL of these connectors will cause DAMAGE to the test fixture and the board under test.

2. Plug A8 card into test fixture.

3. Connect the 34 pin connector from the test fixture to J1 on the circuit card.

4. Place the C - Q switch on the test fixture to the C position. Turn power "ON". Check supply voltages on the board under test as follows:

+5V	across	C22	+5V Unreg.	across	C1
+5V	across	C39	+12V	across	C26
+5V	across	C38	-12V	across	C27
+5V	across	C33			

Record voltages on test data sheet.

9.4.2 Digital Section Test

1. Set the DYNAMIC/STATIC switch to DYNAMIC. Turn power supplies on then press and release the RESET button.

NOTE

Upon release of the "RESET" button, the bus lock light should go out. If it remains lit, turn power "OFF" immediately. This generally indicates a serious failure, such as a short circuit or solder splash.

2. Observe the display digits on the test fixture. If zeros are indicated the digital section of the A8 board has passed all tests. Record results.

3. Ensure that all four OOL lamps light in succession. Record.

4. If numbers other than zero are indicated, these numbers correspond to faulty I/O ports, according to Table 9-2.

Table 9-2. Faulty Port Designations

Test Fixture Display	Faulty Port Number	Test Fixture Display	Faulty Port Number
20	OUT H "20"	25	OUT H "25"
21	OUT H "21"	26	OUT H "26"
22	OUT H "22"	30	OUT H "2A"
23	OUT H "23"	31	IN H "20"
24	OUT H "24"		

9.4.3 Analog Section Test

1. Ensure that jumper between pins 9 & 10 of U27 is present.

2. Set Static/Dynamic switch to "Static."

3. Set up the IOC switches so that they address port number H28.

4. Set all IOD line to logic zero.

5. Press and release the "write" button.

6. With the scope, look at pin 4 of U5. Zero volts should be indicated. Record results.

7. Set all IOD lines to logic 1. Press "write" button.

8. Adjust R3 so that pin 4 of U5 reads 10V.

9. Recheck the zero setting.

10. Check DAC half scale by setting IOD switches to H80. Press write. Pin 4 of U5 should now indicate 5 volts. Record results.

9.4.4 AF Meter Test

1. Turn on internal 1 kHz oscillator.

2. Set level control for 5 volt P-P signal at pin 5 of U28. Record results.

3. Adjust R50 for a 10 volt DC level at pin 5 of U5.

4. Turn off internal 1 kHz oscillator.

5. Voltage at pin 5 of U5 should slowly fall to zero volts. Record results.

9.4.5 RF Meter Test

1. Set up IOD lines for H01.
2. Using IOC switches, write to Port 29.
3. Observe 3, 4, 5 & 6 of U27. Pin 3 should be high, all others low. Record results.
4. Set up IOD switches for H02. Repeat step 2.
5. U27 Pin 4 should be high; 3, 5, & 6 should be low. Record on test data sheet.
6. Set up IOD switches for H04. Repeat step 2.
7. Pins 5 and 6 of U27 should be high; pins 3 &4 low. Record on test data sheet.
8. Set AGC/Meter switch to AGC.
9. Set MGC/AGC sim switch to AGC sim.
10. Write a H01 to I/O Port H29.
11. Observe AGC test point on fixture while varying MGC control of fixture. Voltage should vary from 1.0 volt to 4.4 volts. Record on test data sheet.
12. Observe Pin 14 of U27, while varying MGC control. It should vary between 1.0 volt and 4.4 volts. Record results.
13. Set AGC/MGC switch to MGC.
14. Write a H01 to I/O Port H29.
15. Vary MGC control while observing AGC test point. It should vary from 1.0 volt to 4.4 volts DC. Record results.
16. The same results should be noted at pin 14 of U27. Record on test data sheet.
17. Write a H04 to I/O Port H29.
18. Write a HFF to I/O Port H27.
19. Observe Pin 10 of U27. Adjust R1 & R2 for 2.56V ± 10 mV. Record results

NOTE

There is considerable interaction
between the settings of R1 and R2.

20. Write a H00 to Port H27. Observe Pin 10 of U27. If this point is not 1.5 volts, ±10 mV, adjust R1 and R2 until it is within this range. Record results.
21. Repeat steps 18 through 20 until no further adjustment is required.

22. Check the above voltage levels at Pin 12 of U27; and at the AGC test point on the fixture. They should be the same as those observed on Pin 10 of U27. Record results.

23. Write a H04 to Port H29.

24. Set R5 to the center of its range. In the following steps, R4 is to be used as the coarse adjustment, and R5 as the fine adjustment.

25. Write a H00 to Port H27.

26. Observe Pin 7 of U5. Adjust R4 & R5 for a reading of .68 volts.

27. Write a HFF to Port H27.

28. Observe Pin 7 of U5. Adjust R4 & R5 for a reading of 6.65 volts.

29. Repeat steps 25 through 28 until no further adjustment is required. Record results.

9.4.6 20 Volt dc Power Check

Measure the voltage at pins 11 and 12 of connector J1. 20 VDC should be present. Record results on test data sheet.

9.4.7 Potentiometer Settings

Upon completion of the above procedures, secure all potentiometer settings using a suitable sealing compound.

9.4.8 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (digital, RF section, AF section, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failures of specific addresses can be traced to specific components. Further signal tracing may then be accomplished using the oscilloscope or voltmeter, to trace the fault to a single component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductors and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, the tests for the complete module should then be performed.

9.5 PARTS LIST, DATA LATCHES MODULE A8

The parts list for the A8 module is contained in Table 9-3.

DATE _____
CKD BY _____

MODULE A8
USED ON _____

TEST DATA SHEET

PART NAME: A8 Receiver Latch Board
PART NUMBER: 08356-1
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
9.4.1(4)	+5V/C22		Pass	Fail	
	+5V/C39		Pass	Fail	
	+5V/C38		Pass	Fail	
	+5V/C33		Pass	Fail	
	+5V Unreg./C1		Pass	Fail	
	+12V/C26		Pass	Fail	
	- 12V/C27		Pass	Fail	
9.4.2(2)	Test fixture displays all zeros		Pass	Fail	
9.4.2(3)	OOL Lamps Light		Pass	Fail	
9.4.3(6)	Pin 4 of U5 – zero volts				
9.4.3(10)	Pin 4 of U5 – Five (5) volts		Pass	Fail	
9.4.4(2)	5 volt P-P Signal wave at Pin 5 of U28		Pass	Fail	
9.4.4(5)	Pin 5 of U5 – Falls to zero volts		Pass	Fail	
9.4.5(3)	U27 – Pin 3 = High Pins 4, 5 & 6 = Low		Pass	Fail	
9.4.5(5)	U27 – Pin 4 = High Pins 3, 5 & 6 = Low		Pass	Fail	
9.4.5(7)	U27 – Pins 5 & 6 = High Pins 3 & 4 = Low		Pass	Fail	
9.4.5(11)	AGC TP voltage (1.0 – 4.4 VDC)		Pass	Fail	
9.4.5(12)	Pin 14 of U27 voltage (1.0 – 4.4 VDC)		Pass	Fail	
9.4.5(15)	AGC TP voltage (1.0 – 4.4 VDC)		Pass	Fail	
9.4.5(16)	Pin 14 of U27 voltage (1.0 – 4.4. VDC)		Pass	Fail	
9.4.5(19)	Pin 10 of U27 voltage		2.55	2.57	volts
9.4.5(20)	Pin 10 of U27 voltage		1.49	1.51	volts
9.4.5(22)	Pin 12 of U27, AGC Test Point		Pass	Fail	
9.4.5(29)	Correct adjustments of R4 & R5		Pass	Fail	
9.4.6	Pin 11 of J1 20 VDC present		Pass	Fail	
	Pin 12 of J1 20 VDC present		Pass	Fail	

TABLE 9-3. PARTS LIST, RECEIVER LATCH, CIRCUIT CARD ASSEMBLY, A8 08356-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-20	Capacitor, Ceramic, 0.01 uF, ±20% (Erie)	21733	8121-050-651-103M
C21, 22, 33, 38, 39	Capacitor, Ceramic, 0.22 uF, ±20% (Erie)	21742	8131-050-651-224M
C23	Capacitor, Ceramic, 0.33 uF, ±20% (Erie)	21770	8131-050-651-334M
C24, 25	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
C26, 27	Capacitor, Tantalum, 6.8 uF, ±20% (Kement), 35V	25060-685	T362-B-685-M-035AS
C28, 29, 30	Capacitor, Tantalum, 10 uF, ±20% (Kement), 25V	25061-106	T362-B-106-M-025AS
C31	Capacitor, Tantalum, 15 uF, ±20% (Kement), 20V	25062-156	T362-B-156-M-020AS
C32	Capacitor, Electrolytic, 150 uF, 16V (Amperex)	24053	ET-151X016A5
C34-37	Capacitor, Tantalum, 56 uF, ±10%, 6 VDC	25053	M39003/01-2246
CR1, 2	Diode, Silicon, Pin	35514	1N916
DS1-4	Display, LED/Resistor Assembly	41018	HP-HLMP-6620
J1, 2	Connector, 34 Pin, right angle	61224	3M-3431-1002
L1, 3, 4	Inductor, Choke, 100 uH, ±5%	43033	MS90538-12
L2, 5, 6, 7	Inductor, Choke, 5.6 uH, ±10%	43027	MS14046-1
Q1, 2, 4-11	Transistor, NPN, low power	32036	2N3904
Q3	Not Used		
R1, 2	**Potentiometer,** 5K Ohms, ½W (Beckman)	16016	62P-R5K
R3	**Potentiometer,** 10K Ohms (Mepco)	16090-103	8014EMF103E1
R4	**Potentiometer,** 500 Ohms (Mepco)	16090-501	8014EMF501E1
R5	**Potentiometer,** 100K Ohms (Mepco)	16090-104	8014EMF104E1
R6-12, 14-17, 39-42, 46, 48, 52	Resistor, Film, 10K Ohms, ±2%, ¼W	12161-103	RL07S103G
R13,18, 49	Not Used		
R19, 20, 35-38, 51	Resistor, Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S223G
R21	Resistor, Film, 1.5K Ohms, ±2%, ¼W	12161-152	RL07S152G
R22, 28	Resistor, Film, 15K Ohms, ±2%, ¼W	12161-153	RL07S153G

TABLE 9-3. PARTS LIST, RECEIVER LATCH, CIRCUIT CARD ASSEMBLY, A8 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R23	Resistor, Film, 16.2K Ohms, ±1%, ¼W	12145	RN55D1622F
R24	Resistor, Film, 11K Ohms, ±2%, ¼W	12161-113	RL07S113G
R25	Resistor, Film, 12K Ohms, ±2%, ¼W	12161-123	RL07S123G
R26	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R27	Resistor, Film, 2.49K Ohms, ±1%, ¼W	12147	RN55D2491F
R29, 30	Resistor, Film, 2.2K Ohms, ±2%, ¼W	12161-222	RL07S222G
R31	Resistor, Film, 270 Ohms, ±2%, ¼W	12161-271	RL07S271G
R32	Resistor, Film, 100 Ohms, ±2%, ¼W	12161-101	RL07S101G
R33	Resistor, Film, 6.8K Ohms, ±2%, ¼W	12161-682	RL07S682G
R34	Resistor, Film, 33K Ohms, ±2%, ¼W	12161-333	RL07S333G
R43	Resistor, Film, 47K Ohms, ±2%, ¼W	12161-473	RL07S473G
R44	Resistor, Film, 220K Ohms, ±2%, ¼W	12161-224	RL07S224G
R45	Resistor, Film, 56K Ohms, ±2%, ¼W	12161-563	RL07S563G
R47	Resistor, Film, 470 Ohms, ± 2%, ¼W	12161-471	RL07S471G
R50	Potentiometer. 50K Ohms, ½W	16017	62P-R50K
R53	Resistor, Film, 1.8K Ohms, ±2%, ¼W	12161-182	RL07S182G
T1	Transformer, Audio (Triad), 10K	44510	TY-141P
U1	Integrated Circuit, Digital to Analog Converter	36581	1408L-8
U2, 13, 15, 17, 21-24	Integrated Circuit, Octal D type flip-flop	36669	74LS377
U3, 9, 28	Integrated Circuit, Octal D type flip-flop	36673	MC1458
U4	Integrated Circuit, Voltage Regulator	36679	74L82
U5	Integrated Circuit, Quad Voltage Comparator	36693	LM339
U6, 7	Integrated Circuit, Dual 2 input NAND gate	36795	CD40107BE
U8, 16, 19	Integrated Circuit, flip-flop	36588	MC4013BCL
U10	Integrated Circuit, Hex 3 state buffer	36694	MC4503BCL
U11	Integrated Circuit, Digital to Analog Cenverter	36758	1408L-6
U12	Integrated Circuit, Binary Decoder	36579	MC14555BCL

TABLE 9-3. PARTS LIST, RECEIVER LATCH, CIRCUIT CARD ASSEMBLY, A8 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U14	Integrated Circuit, BCD to Decimal Decoder	36698	74LS145
U18, 26	Integrated Circuit, Hex D flip-flop	36766	F40174BDC
U20	Integrated Circuit, Decoder/Demultiplexer	36714	74LS138
U25	Integrated Circuit, Hex Inverter	36676	74LS04J
U27	Integrated Circuit, Quad Switch, SPST	36665	AD7510D1JD
U29	Integrated Circuit, Decoder/Demultiplexer	36716	74LS154
–	Printed Wiring Board	08393	
–	Insulator, Mylar, 24 Pin Connector for J1, J2	A09023	

CHAPTER 10
LOWER/UPPER LOOP SYNTHESIZER, A11

10.1 THEORY OF OPERATION

This chapter provides information on the lower frequency loop board A11A1 and the upper frequency loop board A11A2; however, these two boards, combined in one module A11, are a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A11 module within the synthesizer section. Figure 10-1 shows a simplified functional block diagram of the complete section.

Three injected frequencies are supplied by the synthesizer to the mixers and detectors. The first frequency, variable in the range of 35.4 MHz to 65.4 MHz, is applied to the first mixer. The second, fixed at 34 MHz, is applied to the second mixer. The third, 1.4000 +.008 MHz is applied to the product detector for the reception of single sideband and CW signals; with the BFO Tunable in 10 Hz increments for CW reception. The indirect method of frequency synthesis is used where the required output frequencies are derived from voltage controlled oscillators which are phase locked to a common frequency source. All generated frequencies are derived from a 5 MHz internal frequency standard. The output signal from the standard is divided by five to produce a 1MHz reference frequency for the synthesizer. An external 1 MHz frequency standard may be applied in place of the internal standard via J8 on the rear panel.

To produce the 1.4 MHz output a synthesized frequency, centered at 4 MHz, is divided by 10 and mixed with 1 MHz. The frequency includes the ± BFO offset.

The 34 MHz second mixer injection frequency is derived from a 34 MHz voltage controlled oscillator (VCO) which is phase locked to the 1 MHz reference frequency. A sample of the VCO output is divided by 34, and phase-compared to the reference. Any difference in phase results in a correction dc voltage applied to the VCO.

The main output from the frequency synthesizer is the first mixer injection frequency, covering the frequency range 35.4 to 65.4 MHz in 10 Hz increments. The frequency is controlled by the frequency selections received from the front panel section. The digits of the required output are derived from five cascaded phase-locked loops where the divided output from one loop becomes the phase detector input of the next loop.

10.1.1 Lower Frequency Loop Board, A11A1

The lower frequency loop consists of a 6 to 7 MHz VCO, a programmed divider, N1 and a phase comparator; which compares the phase of the output signal from the programmed divider with that of a 1 kHz reference frequency, derived by dividing the 1 MHz reference by 1000. A phase difference produces a correction dc voltage to adjust the VCO.

In normal operation, the programmed divider, N1, has a division ratio of from 6001 to 7000, controlled by the 10 Hz, 100 Hz and 1 kHz digits. A setting for these three digits of 000 results in a division ratio of 7000, while 999 results in a ratio of 6001. The dividing factor N1 = 7000 minus the selected digits. The divider consists of a series of counters. The start of a count is determined by the frequency selection. The counter is reset when a total of 7000 has been reached.

The low frequency loop board also contains a portion of the next loop, the lower transfer loop. The output from the 6 to 7 MHz VCO is frequency-divided by the programmed divider, N2, which has a division ratio of from 354 to 453. N2 is controlled by the 100 kHz and 10 kHz digits of the selected receiver operation frequency. This is phase-compared to the output of a mixer, which has as inputs, the 1 MHz reference frequency and the output of a 1.013247 to 1.019774 MHz VCO, located in the upper loop board, A11A2.

A frequency setting of 00 for the 100 kHz and 10 kHz digits results in a division ratio of 453; and a frequency setting of 99 results in 354. The dividing factor, N2 = 453 minus the selected digits. In the USB and LSB configurations, the oscillator range is modified to allow for the SSB offset. This gives a maximum range for the VCO of from 1.012839 to 1.020297 MHz. A block diagram is given in Figure 10-2, and schematic diagram in Figure 10-7.

10.1.1.1 6-7 MHz Voltage Controlled Oscillator

The 6 to 7 MHz VCO for the low frequency loop consists of transistor Q1, a tuned circuit, L1, C1 and C2, and a varactor, CR1. Feedback is provided by the inverting gate, U1A. The square wave output signal from pin 11 is applied to the programmed divider N1, and to the programmed divider of the lower transfer loop, N2, via U1D.

10.1.1.2 Programmed Divider, N1

The programmed divider consists of four presettable decade counters, U3, U5, U6 and U10; a decode network, U22 and U23; NAND gates U9 and U1B; and a dual J-K flip-flop, U11.

The decade counters have strobed parallel-entry capability such that the starting point of a count sequence may be preset. A '1' or '0' at a data input (A, B, C, D) is transferred to the associated output when the strobe (ST) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

The division ratio of the programmed divider is controlled by the 1 kHz, 100 Hz and 10 Hz digits of the selected operating frequency as explained in paragraph 10.1.1 above.

Binary coded decimal (BCD) frequency setting information is applied to the data inputs of U3 (10 Hz data), U5 (100 Hz data) and U6 (1 kHz data). The C and D data inputs of U10 are connected to ground, while the A and B inputs are controlled by AND gate U22C and OR gate U23D, respectively.

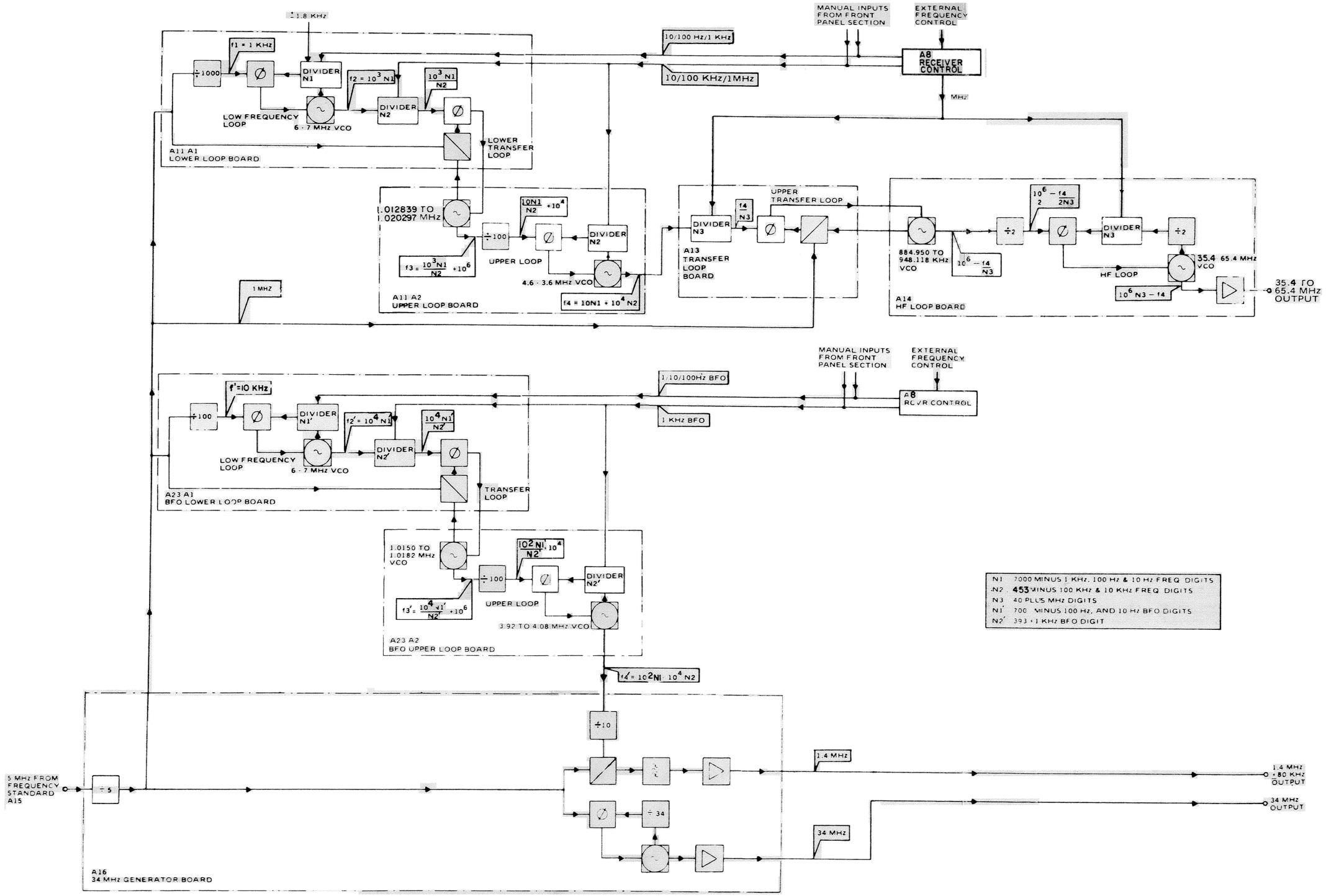


Figure 10-1. Simplified Functional Diagram, Frequency Synthesizer Section

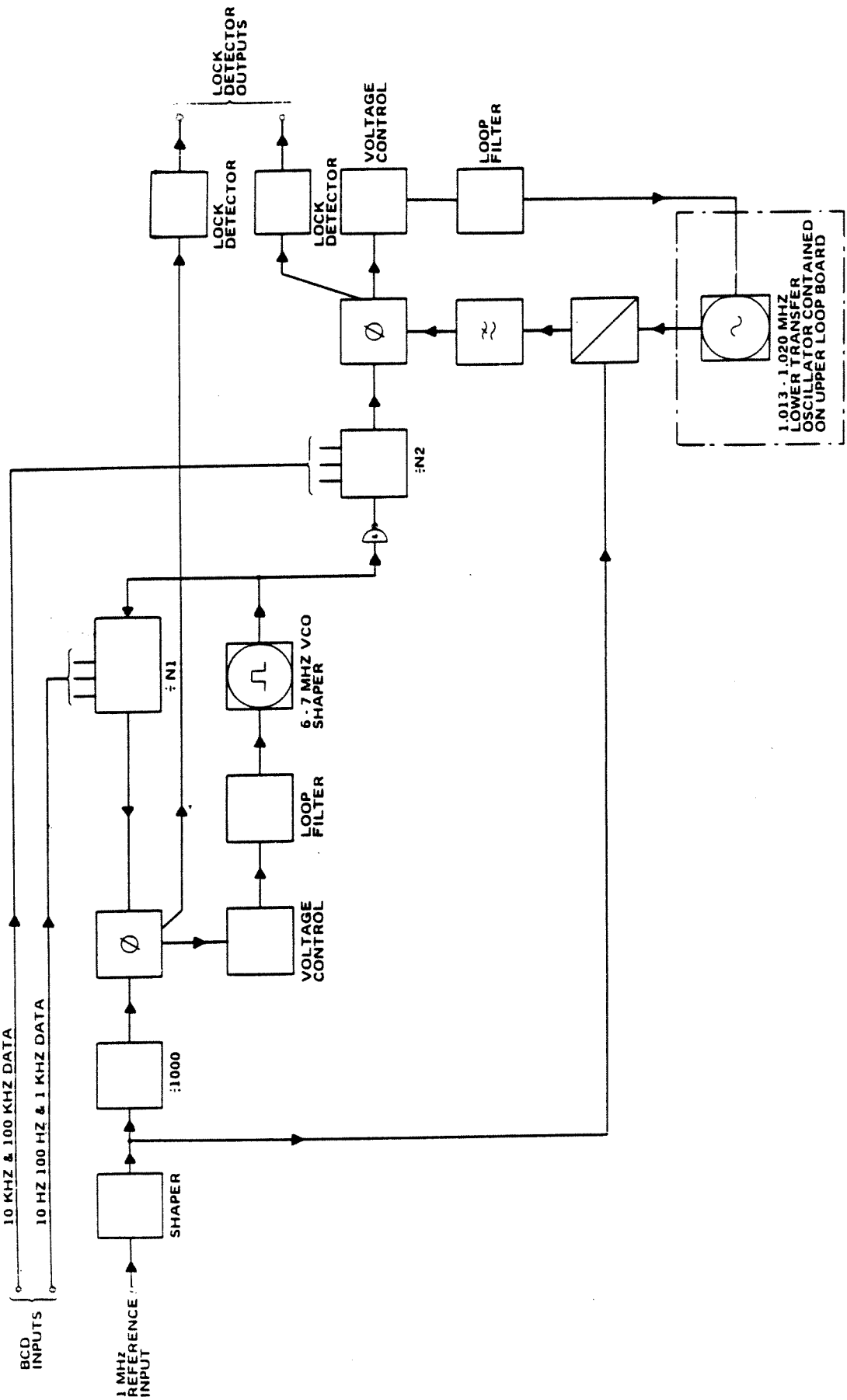


Figure 10-2. Block Diagram, Low Frequency Loop Board, A11A1

To start a counting sequence, a logic '0' strobe pulse is applied to the strobe (ST) input of each decade counter. This causes the logic level applied to each input line to be transferred to the corresponding output line. The negative-going edge of the clock pulse (from the VCO) is applied to the clock 1 input of U3and each pulse is now counted until the maximum count is decoded by network U22/U23 and NAND gate U9. The output of NAND gate U9, inverted by U1B, is applied to the K input of a dual negative-edge triggered J-K flip-flop, U11. The operation of this flip-flop, which generates the strobe pulse for the decade counters, is given in the waveform diagram, Figure 10-3. From this diagram, it can be seen that two clock pulses elapse before the start of the strobe pulse, and a further two clock pulses elapse before the end of the strobe pulse. Thus, four clock pulses are counted by U11 and must be added to the total number of counts in a cycle.

The number of counts in a cycle will vary according to: 1. the counter preload by frequency information; 2. the preload of the highest-order counter stage, U 9; and 3. the maximum count decoded by U22, U23, and U9. During normal operation, i.e., when the NORMAL control input is asserted, counter preload will be the frequency digits on U3, U5 and U6 plus the 2000 represented by the B input to U10. The maximum count decoded by U22, U23 and U9 will be 8996. If the four counts of U11 are added, the maximum count becomes 9000. The number of pulses counted to reach this count is thus 9000 minus the total counter preload (U10 preload plus frequency digits). If the frequency digits are 000, 7000 clock pulses will be counted each cycle. If the frequency input is 999, 6001 clock pulses will be counted. The counter thus divides the clock frequency by an amount varying between 6001 and 7000 in normal operation.

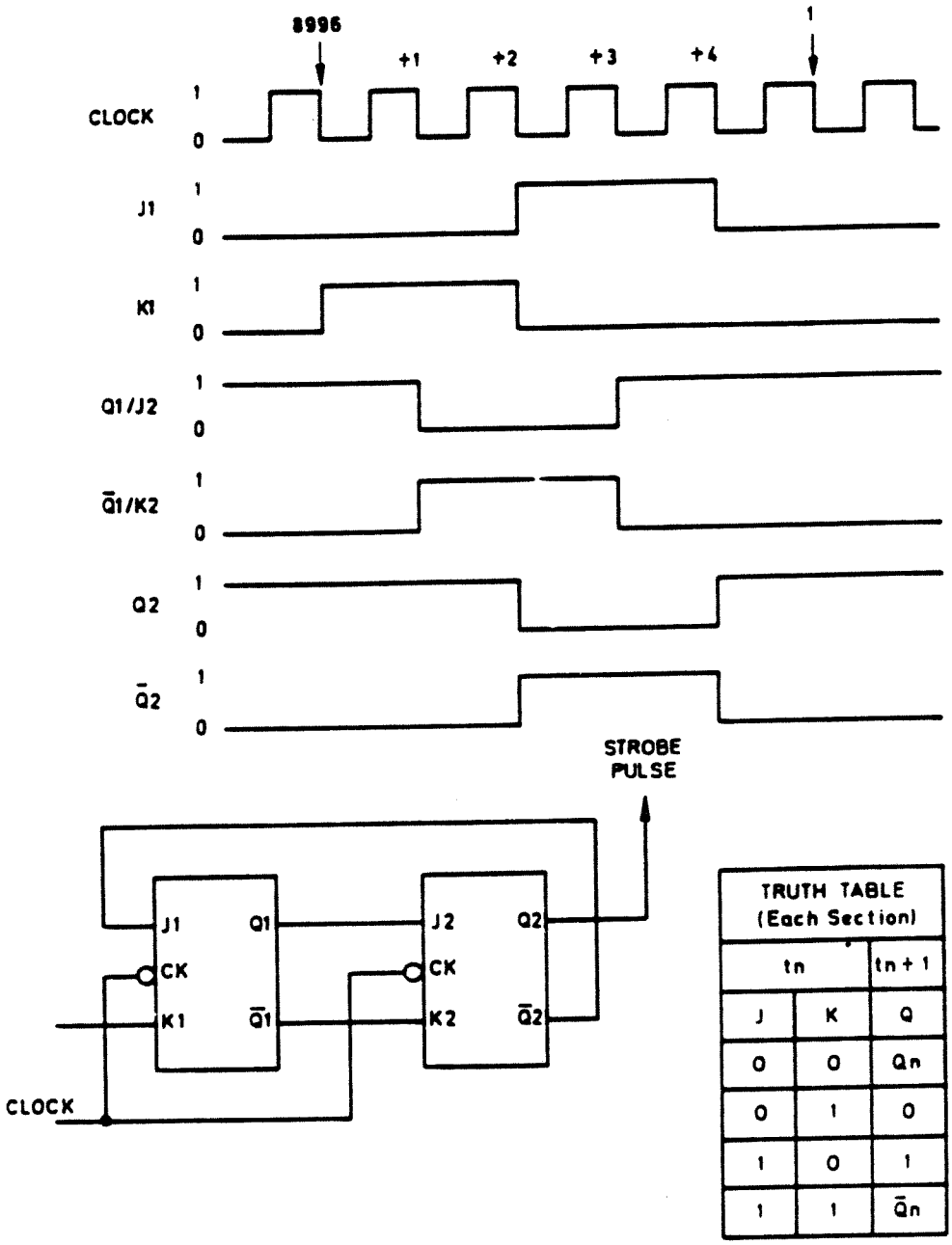
10.1.1.3 Reference Frequency Divider

The 1 MHz input signal at pin J1-A2 is coupled by transformer T1 to a shaper stage Q2. The square wave output signal from the collector of Q2 is applied to a divider consisting of three cascaded decade dividers, U2, U4 and U7. The output signal, at 1000 pps, is applied to one of the clock inputs of the LF loop phase comparator, U8.

10.1.1.4 LF Loop Phase Comparator

The phase comparator consists of a dual D-type flip-flop, U8, a two-input NAND gate, U1C, and a voltage control circuit, Q3, Q4 and Q5. It compares the output signal frequency from the programmed divider, N1, with the output signal frequency from the frequency divider. Any error between these two frequencies is used to develop a dc voltage which is applied to the 6-7 MHz VCO to eliminate the error.

The output signal from the programmed divider N1, from U10 pin 12, consists of positive-going pulses which are applied to the clock input of U8B at pin 3. The output signal from the reference divider also consists of positive-going pulses which are applied to the clock input of U8A at pin 11. The D inputs of U8, at pins 2 and 12, are both taken to the +5V line (Logic '1') via R50. Thus, when the positive edge from U10 pin 12 clocks U8B, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from the reference divider clocks U8A, the Q output at pin 9 changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1', the output from NAND gate U1C changes to '0', clearing both flip-flops of U8 via R53 to reset the Q outputs to '0' and the $\overline{Q}$ outputs to '1'.



TRUTH TABLE (Each Section)		
tn		tn + 1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Q̄n

Figure 10-3. Waveform Diagram, Strobe Pulse Generation LF Loop, A11A1

Consider the case where the 6 - 7 MHz VCO frequency is high. The positive edge from the programmed divider occurs before the positive edge from the reference divider. The resultant setting and resetting of the flip-flops causes increased conduction of Q4, due to the Q output waveform from U8B (see waveform diagram, Figure 10-4) as compared with the conduction of Q5. This causes the voltage at the collector of Q4 to become less positive, thereby reducing the voltage applied to varactor diode CR1, and reducing the VCO frequency.

If the VCO frequency is low, the programmed divider output pulse occurs after the reference pulse. The Q output waveform from U8A causes increased conduction of Q5, and the voltage at the collector of Q4 becomes more positive. The increased voltage applied to the varactor diode causes the VCO frequency to increase, correcting the error.

When the two signals are equal in frequency and phase, the two flip-slops of U8 are clocked at the same time. The two Q output waveforms are equal, and the varactor line voltage remains constant.

10.1.1.5 LF Loop Out-of-Lock Detector

The LF loop lock detector consists of a bistable latch, U12A and B and an output buffer, U12C. The $\overline{Q}$ outputs from the phase comparator, U8, are connected directly to U12A, and also to U12B via integrating components C19 and C20, and R51 and R52. Under phase-locked conditions, the in-phase negative-going $\overline{Q}$ output pulses from U8 pins 6 and 8 (Q1 and Q2 of Figure 10-4) are prevented from reaching U12B due to the time constants presented by the integrating components. Pins 1 and 2 of U12B, therefore, float up to logic '1' and the resulting logic '0' output, at U12B pin 12, forces the output of U12A to logic '1'. The inputs to the output buffer, U12C, are connected in parallel with those of U12B and the logic '0' in-lock indication output is applied to the out-of-lock gating on board A11A2 through board pin E1.

When an out-of-lock condition exists, the clock input waveforms applied to U8 are no longer in phase and the resultant longer-duration negative-going output pulses from U8 pin 6 or U8 pin 8 (dependent on whether a phase lead or a phase lag exists) are sufficient in width to overcome the time constant presented by the respective integrating components. The effect of this is to produce an alternating '0' - '1' output signal from the buffer, U12C, as shown in the waveform diagram, Figure 10-5. The output from U12C is applied to the out-of-lock gating on board A11A2 through board pin E1.

10.1.1.6 Programmed Divider, N2

This programmed divider, which forms part of the lower transfer loop, consists of three presettable decade counters, U14, U15, U19; NAND gates, U18A and B; and a dual J-K flip-flop, U20. Apart from the exceptions noted below, the operation of N2 is identical to that described from N1 in paragraph 10.1.1.2.

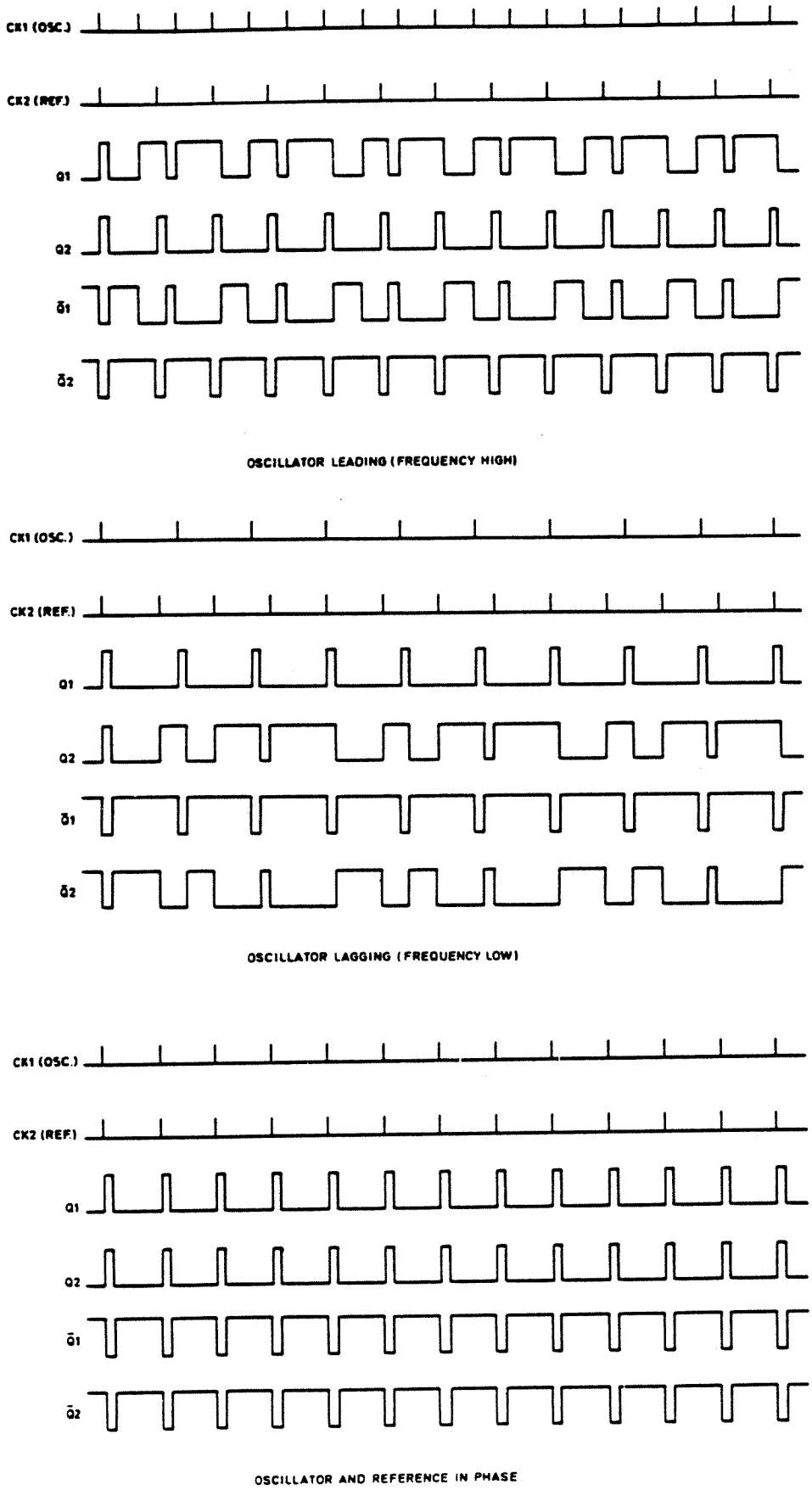


Figure 10-4. Waveform Diagram, Phase Comparator

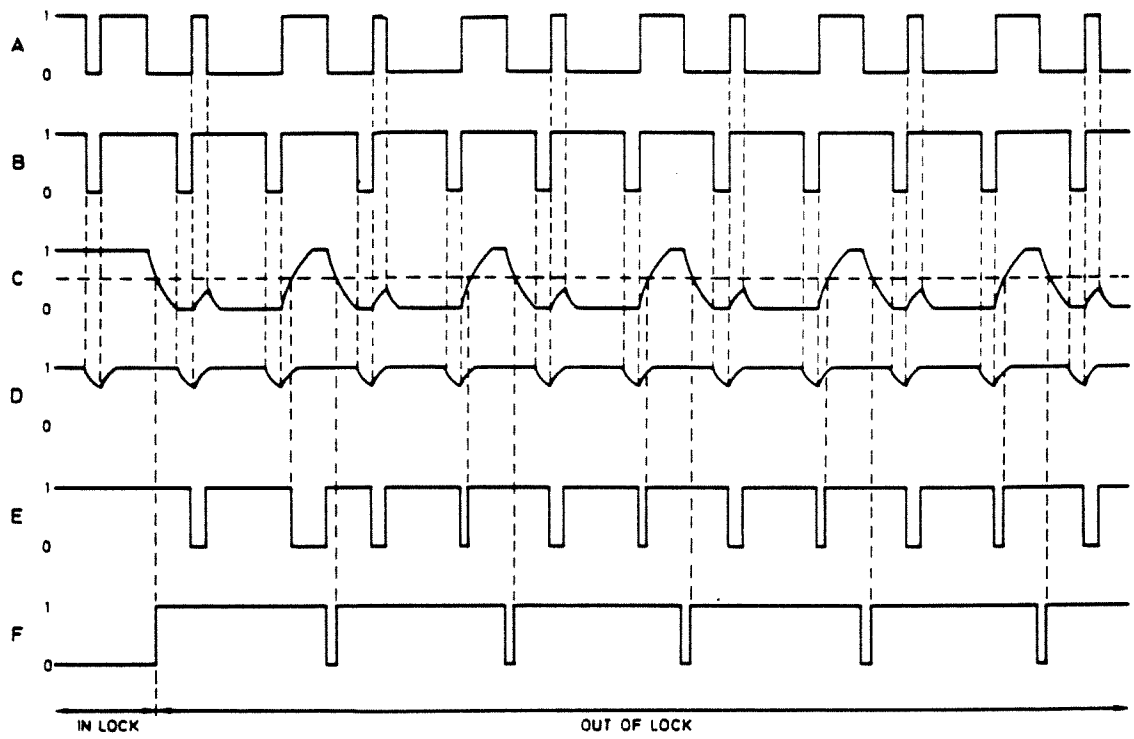
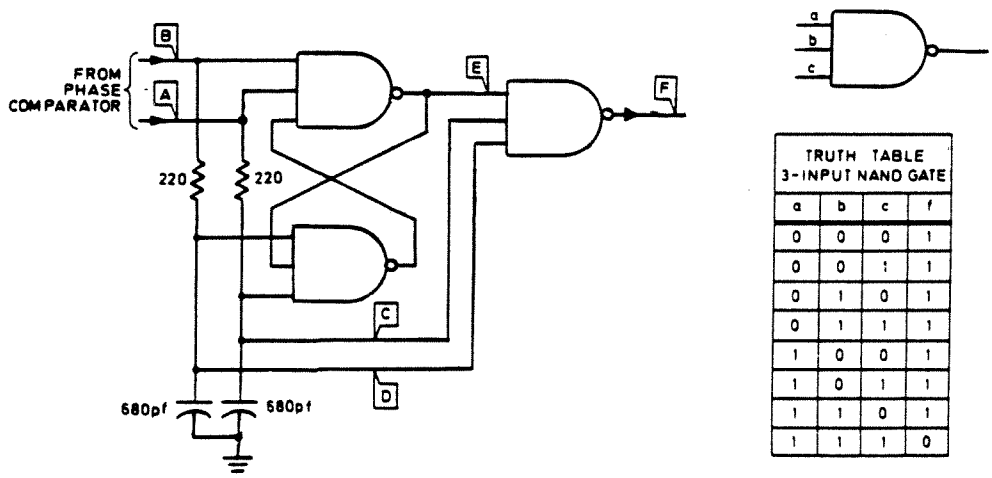


Figure 10-5A. Waveform Diagram, Lock Detector



TRUTH TABLE
3-INPUT NAND GATE

a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 10-5B. Simplified Schematic Diagram and Truth Table, Lock Detector

The division ratio of N2 is controlled by the 10 kHz and 100 kHz digits of the selected operating frequency. The division ratio is given by the expression N2 = 453 minus selected digits, i.e., the division ratio is 354 for a setting of 99.

BCD frequency setting information is applied to the data input of U14 (10 kHz data) and U15 (100 kHz data). The data inputs to U19 are all at 0 V (logic '0') so that U19 always starts counting at zero. The A and D inputs to U19 are normally grounded at the board connector.

10.1.1.7 Mixer Stage

U13 is an integrated circuit mixer where the 1 MHz square wave from Q2 is applied to the carrier input, pin 8, and the 1.013 - 1.020 MHz output from the lower transfer loop oscillator is applied to the signal input, pin 1. The output signal from the mixer, at pin 6, is applied to a low pass filter (C27, C28, L3) which selects the difference frequency. The filter is followed by a buffer stage, Q19 and an output shaper, U17A, which is fed from a voltage regulator consisting of Q20 and a 5.6 V zener diode, VR1. The square-wave output from U17A is applied to the lower transfer loop phase comparator.

10.1.1.8 Lower Transfer Loop Phase Comparator

The phase comparator consists of a dual D-type flip-flop, U16; NAND gate, U17B; and a voltage control circuit, Q21, Q22, Q23. It compares the output signal frequency from the mixer with the output signal frequency from the programmed divider, N2. Any error between these two frequencies is used to develop a dc voltage which is applied to the lower transfer loop oscillator to eliminate the error. The action of the circuit is identical to that of the LF loop phase comparator, described in paragraph 10.1.1.4.

10.1.1.9 Lower Transfer Loop Out-of-Lock Detector

This consists of a bistable latch, U21A and B, and an output buffer, U21C. It is fed from the $\overline{Q}$ outputs of the phase comparator flip-flop, U16, and produces a steady logic '0' in-lock signal or an alternating '0' - '1' out-of-lock signal at board pin E42. The action of the circuit is identical to that of the LF loop lock detector described in paragraph 10.1.1.5. The output of the U21C is applied to the out-of-lock gating on board A11A2 through board pin E42.

10.1.2 Upper Loop Board, A11A2

This board contains the VCO for the lower transfer loop and the upper loop. The output from the VCO, covering a maximum range of from 1.012839 to 1.020297, is divided by 100 and applied to one input of a phase comparator. The other input is from a programmed divider, N2, dividing the output of the upper loop VCO. The VCO covers the range of 3.6 to 4.6 MHz. N2 is the same division ratio already described for the lower transfer loop. Figure 10-6 is a block diagram of A11A2 and Figure 10-8 is the schematic diagram.

10.1.2.1 Lower Transfer Loop VCO

This voltage controlled oscillator/shaper stage Q5 and Q6 produces a square-wave output signal in the frequency range 1.013 to 1.020 MHz. The tuned circuit comprises L4, capacitors C10, C11 and C13, and a varactor diode, CR2. Positive feedback is applied to the tuned circuit through R14. Q4 and a 5.6 V zener diode, VR2, provide supply voltage stabilization.

The oscillator output signal to the mixer stage of the lower transfer loop, A11A1, is taken from the emitter of Q5 and is fed to board pin E9 via C12. The varactor line input from A11A1 is applied to CR2 via board pin E7 and inductor L5.

The lower transfer loop VCO output signal is taken from the collector of Q6 and may be monitored at TP1. It is applied to the lower loop phase comparator via a fixed divider stage, U4 and U6.

10.1.2.2 Upper Loop VCO/Shaper

This VCO/Shaper stage comprises emitter followers Q19 and Q2, NAND gate U1A, a tuned circuit L1, C2 and C3, and a varactor diode CR1. Supply voltage stabilization is provided by Q1 and a 5.6 V zener diode, VR1. The oscillator output signal, in the frequency range of 3.6 to 4.6 MHz, is applied to the following:

a. The upper transfer board, A13, via NAND gate U1C, a filter comprising R4, L2 and C5, a tuned circuit T1 and C1, and pin J1-A1.

b. The programmed divider, N2, of the upper loop via a NAND gate, U1B.

c. U8A (Pin 11), which forms part of the strobe pulse generator for the programmed divider N2.

10.1.2.3 Programmed Divider, N2

The upper loop programmed divider, which has the same division ratio as that of the lower transfer loop, consists of three presettable decade counters, U2, U3 and U5; NAND gate, U7; and a D-type flip-flop, U8A. Operation is identical to that described for the lower loop divider in paragraph 10.1.1.6.

10.1.2.4 Fixed Divider

The fixed divider consists of two decade counters, U4 and U6, connected in cascade. The lower transfer VCO output signal is applied to the A input of U4, and the divide-by-100 output is taken from U6, pin 11. This is applied as the clock input to the phase comparator (U9B, pin 3) and may be monitored at TP3.

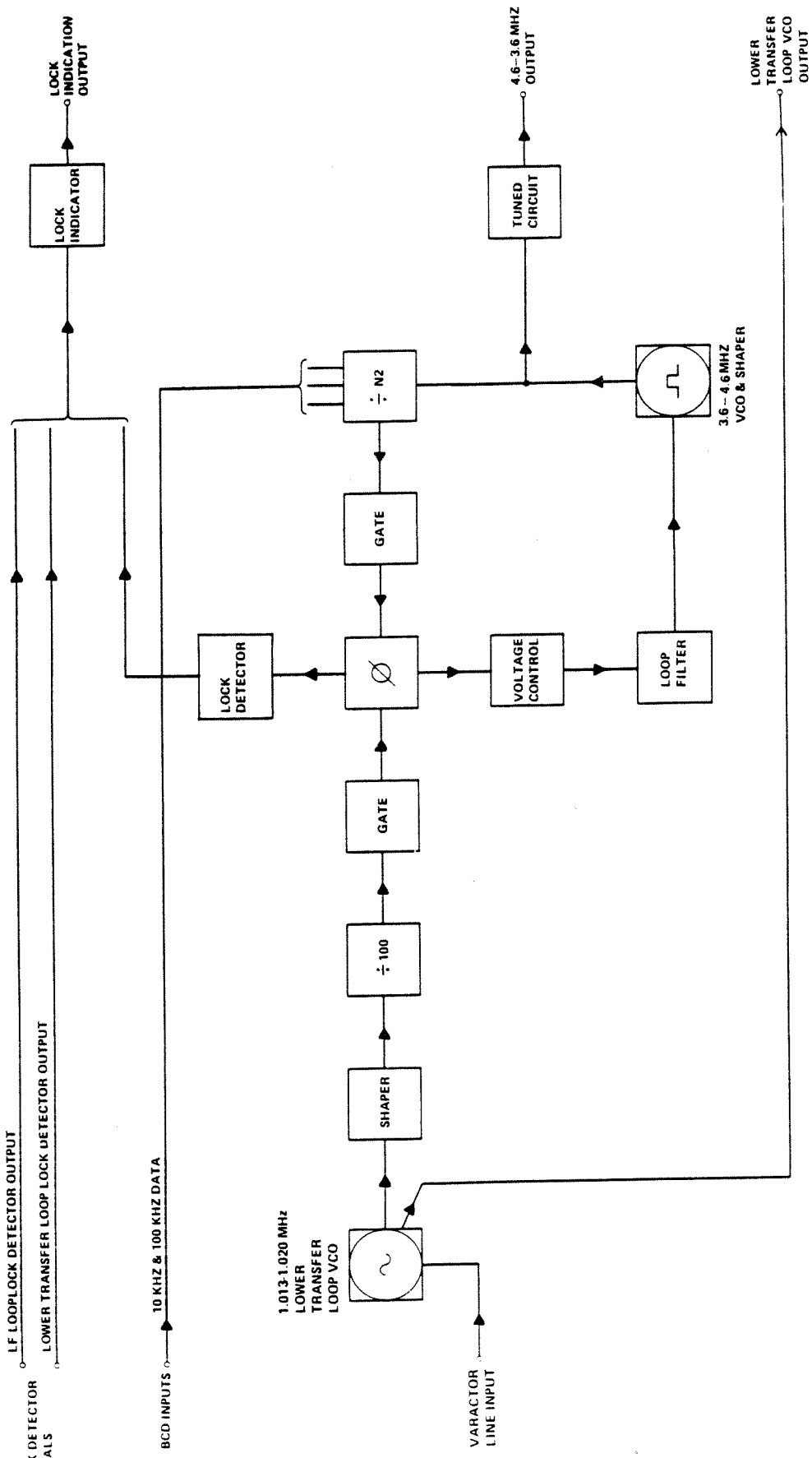


Figure 10-6. Block Diagram, Upper Loop Board, A11A2

10.1.2.5 Phase Comparator

The phase comparator consists of two D-type flip-flops, U8B, U9B, NAND gate U10A; and a voltage control circuit, Q16, Q17 and Q18. It compares the output signal frequency from the programmed divider with the output signal frequency from the fixed divider. Any error between these two frequencies is used to develop a dc voltage which is applied to the 3.6 to 4.6 MHz VCO to eliminate the error. The action of the circuit is identical to that described for lower loop phase comparator in paragraph 10.1.1.4.

10.1.2.6 Upper Loop Out-of-Lock Detector

This consists of a bistable latch, U11A and U11B, and an output buffer, U11C. It is fed from the $\overline{Q}$ outputs of the phase comparator flip-flops (U8B and U9B) and produces a steady '0' inlock signal (or an alternating '0' - '1' out-of-lock signal) at U11 pin 8. The action of this circuit is identical to that of the LF loop out-of-lock detector, described in paragraph 10.1.1.5.

10.1.2.7 Out-of-Lock Indicator

The out-of-lock indicator circuit consists of five NAND gates,U10B, C and D, and U12A and B. The lock detector outputs from the LF and lower transfer loop, A11A1, are applied to U10C and U10B via board pins E13 and E14, respectively, while the upper loop lock detector output, at U11 pin 8, is applied to U10D. The output from U12B ('1' for in-lock, '0' for out-of-lock) is applied to the receiver fault logic on latch board A8 through board pin E12.

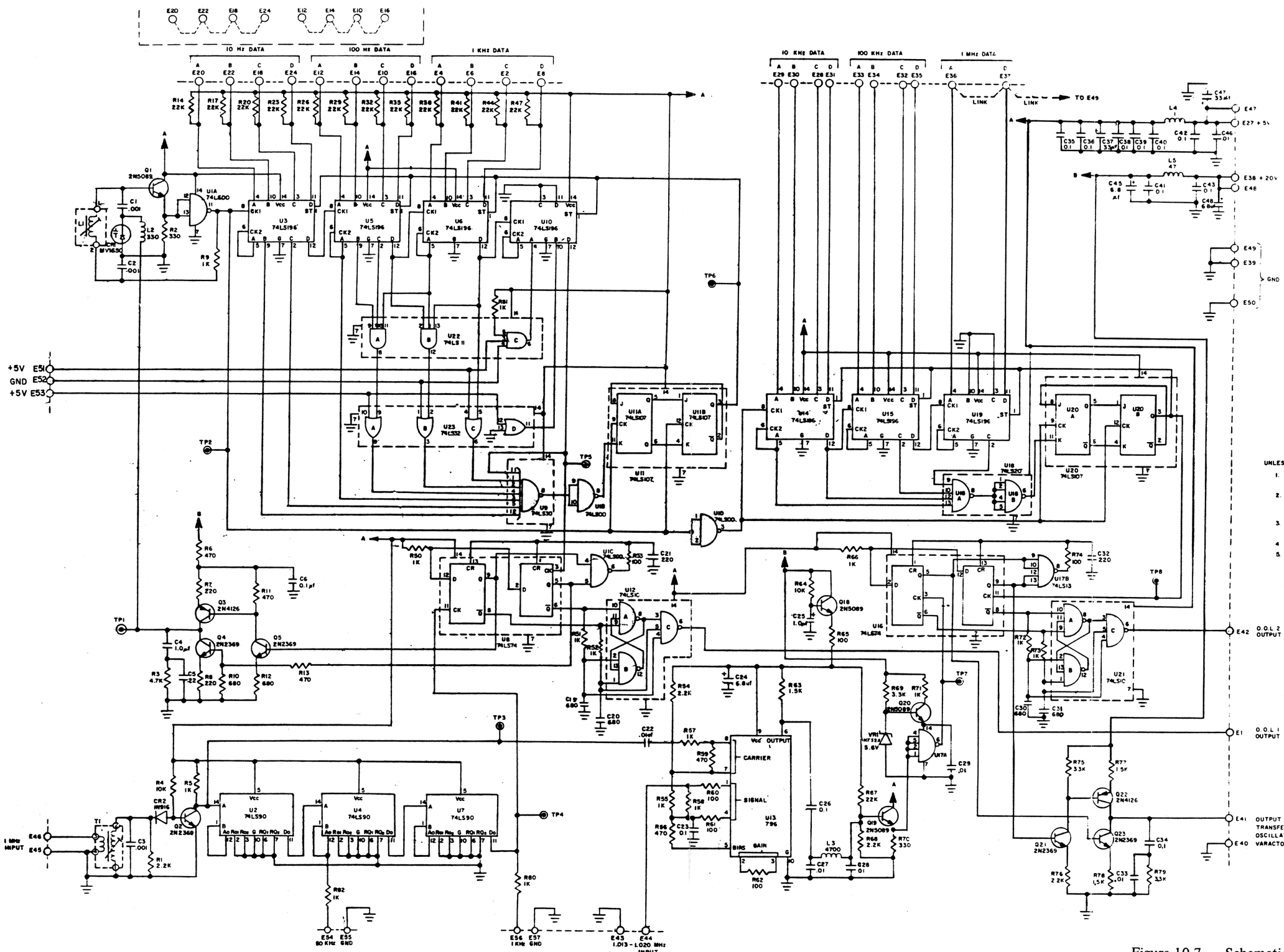
10.2 LOWER AND UPPER LOOP SYNTHESIZER A11, TEST FIXTURE

Troubleshooting and alignment of the upper and lower loop synthesizer module A11 is accomplished through the use of the RACAL upper and lower loop synthesizer A11 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A11 module for testing, while also providing easy access to the two printed circuit boards within the module. The front apron of the test fixture contains the frequency controls, offset switch, range blank control, and output port.

A 1 MHz oscillator is contained within the test fixture as an internal signal source for the module under test as well as for external sync of associated test equipment. An internal timing circuit provides for using the VCO's in the module under test, in that it permits the VCO to tune its complete range in a repetitive fashion to check settling time. Front panel frequency switches provide BCD inputs for manual setting of the VCO in the module under test. An external trigger out port, on the rear apron, provides for sync of external equipment. Provisions are also made to display an out of lock condition on the test fixture. Figure 10-10 shows the A11 module test fixture. Figure 10-11A shows the overall assembly of the A11A1 module, while Figure 10-11B shows the circuit card assembly. Figure 10-12A shows the overall assembly of the A11A2 module, while Figure 10-12B shows the circuit card assembly.

10.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required are listed in Table 10-1.



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT, K = 1,000 M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN
4. CKT SYMBOLS NOT USED: C44, E26
5. CONNECT PINS E20, 22, 18 AND 24, ALSO PINS E12, 14, 10 AND 16 TO GROUND AS SHOWN FOR DASH 2 ONLY.

Figure 10-7. Schematic Diagram, Lower Loop Board, A11A1

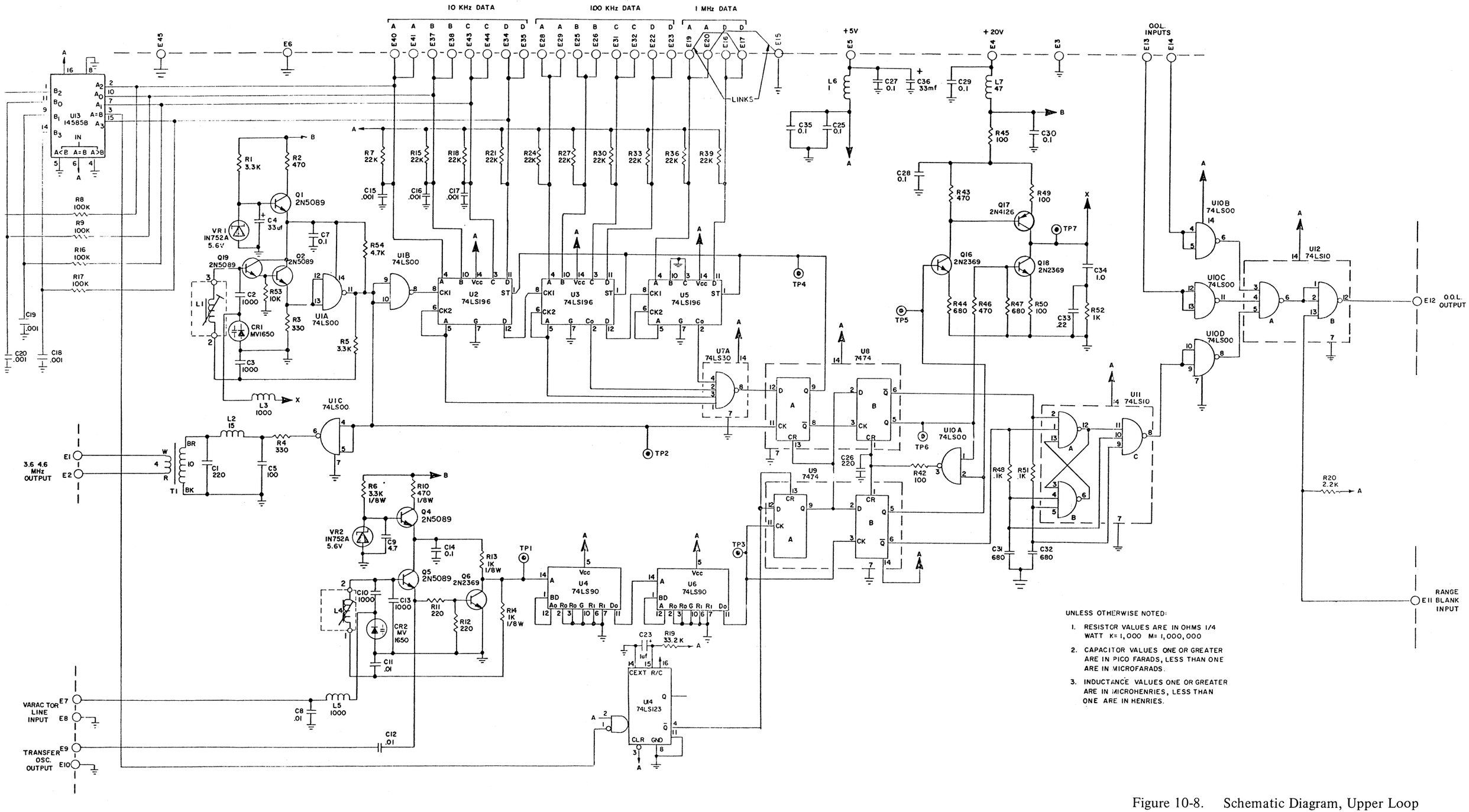


Figure 10-8. Schematic Diagram, Upper Loop Board, A11A2

10-17/10-18

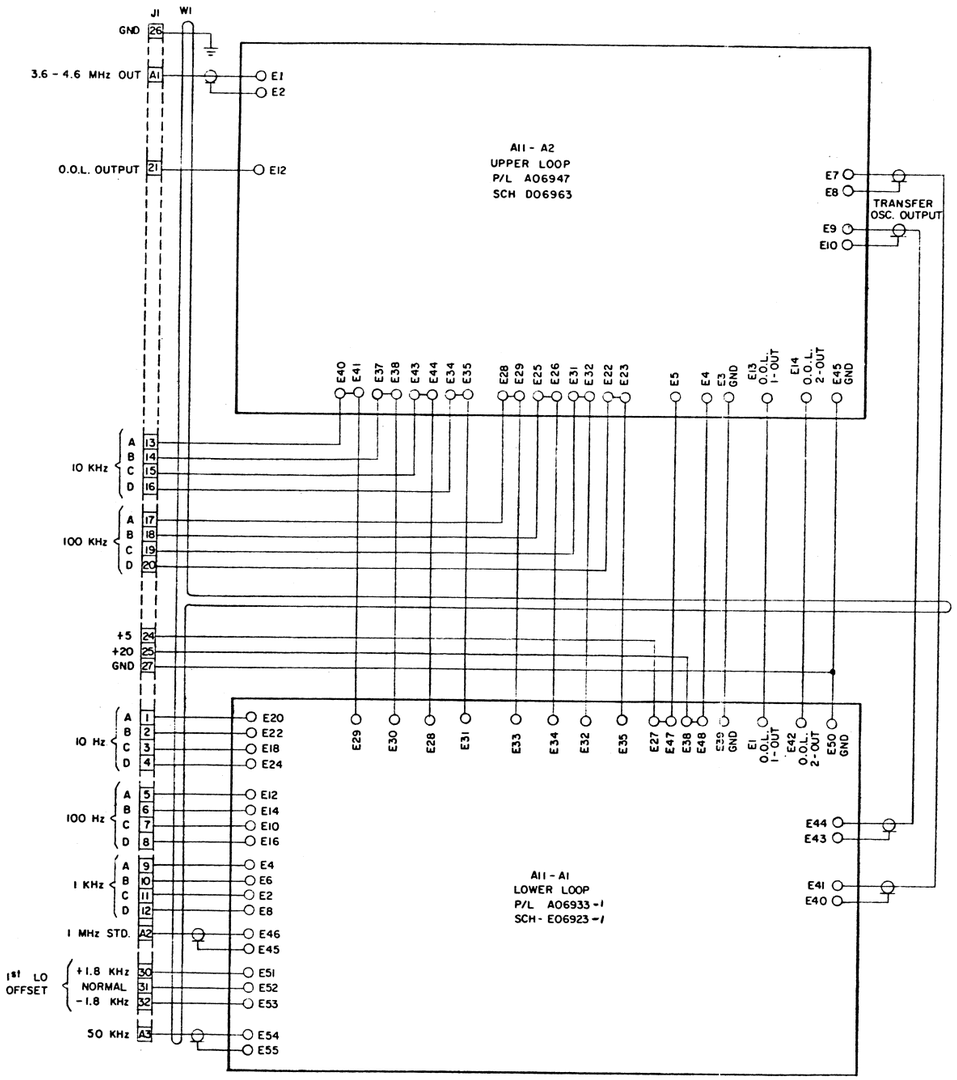


Figure 10-9. Interconnect Diagram, Upper/Lower Loop Module, A11

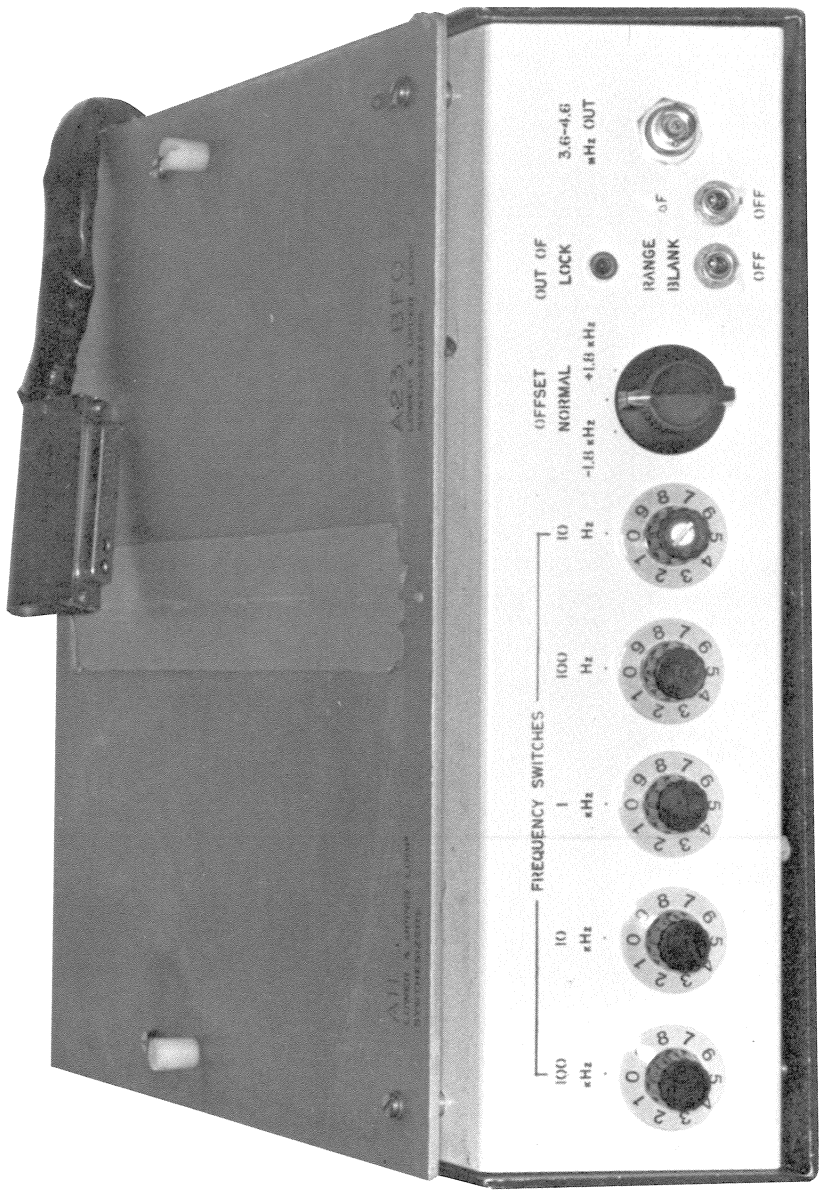


Figure 10-10. Lower/Upper Loop Synthesizer, A11, Test Fixture

Table 10-1. Test Equipment and Accessories

Item	Description	Recommended Equipment or Equal
1	RF Voltmeter	Boonton 92B
2	Digital Multimeter	Data Precision 24B
3	Frequency Counter	Dana 8030B
4	Oscilloscope	Tektronix 465
5	DC Power Supply	Racal
6	A11 Test Fixture	Racal
7	Unterminated Adapter	Boonton 91-6C
8	50 ohms Adapter	Boonton 91-8B
9	Tuning Tool	Micrometals RCI 82007

10.4. TEST AND ALIGNMENT

The following procedures are provided to properly test the A11 module. All tests should be conducted at room ambient temperature and results recorded on test data sheet, page 10-32.

10.4.1 Lower Loop VCO Alignment (A11A1)

1. Place the A11 module to be tested into the test fixture.
2. Set all the FREQUENCY SWITCHES to the 0 position.
3. Place the OFFSET switch to NORMAL position.
4. Place the RANGE BLANK switch to OFF. Place the AF switch off.
5. Apply DC power to the rear apron on the test fixture via the octal plug. Turn the power supply on.
6. Ignore the status of the OUT OF LOCK lamp until told to check its' status.
7. Using the unterminated adapter connect the R.F. voltmeter to the cathode side of CR-2. Use as short a lead as possible here. Slowly adjust T-1 for a maximum level read on the R.F. voltmeter. This level should be 1.5 Volt ±0.5 Volt R.F. Record on test data sheet.

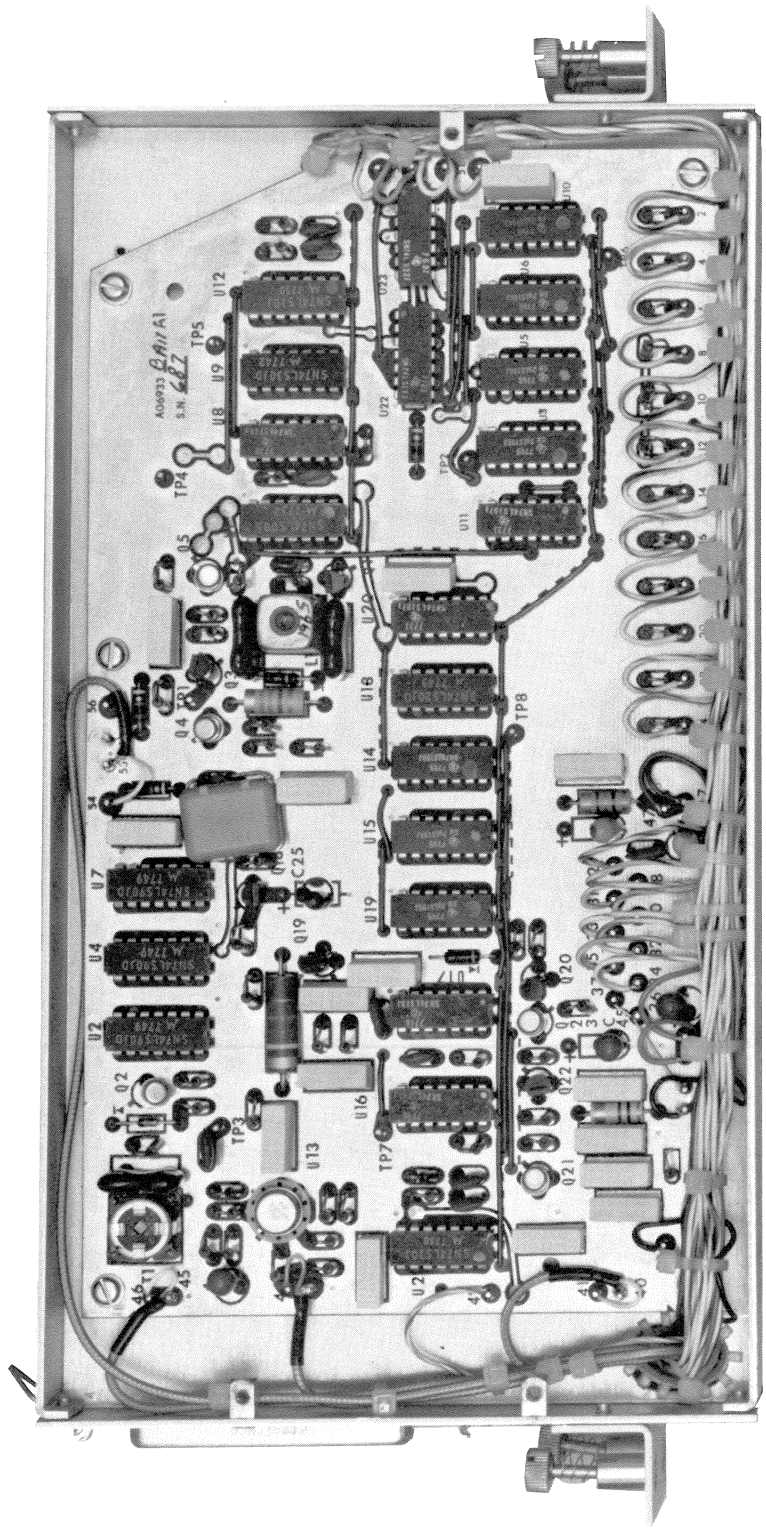


Figure 10-11A. Lower Frequency Loop A11A1, Overall Assembly

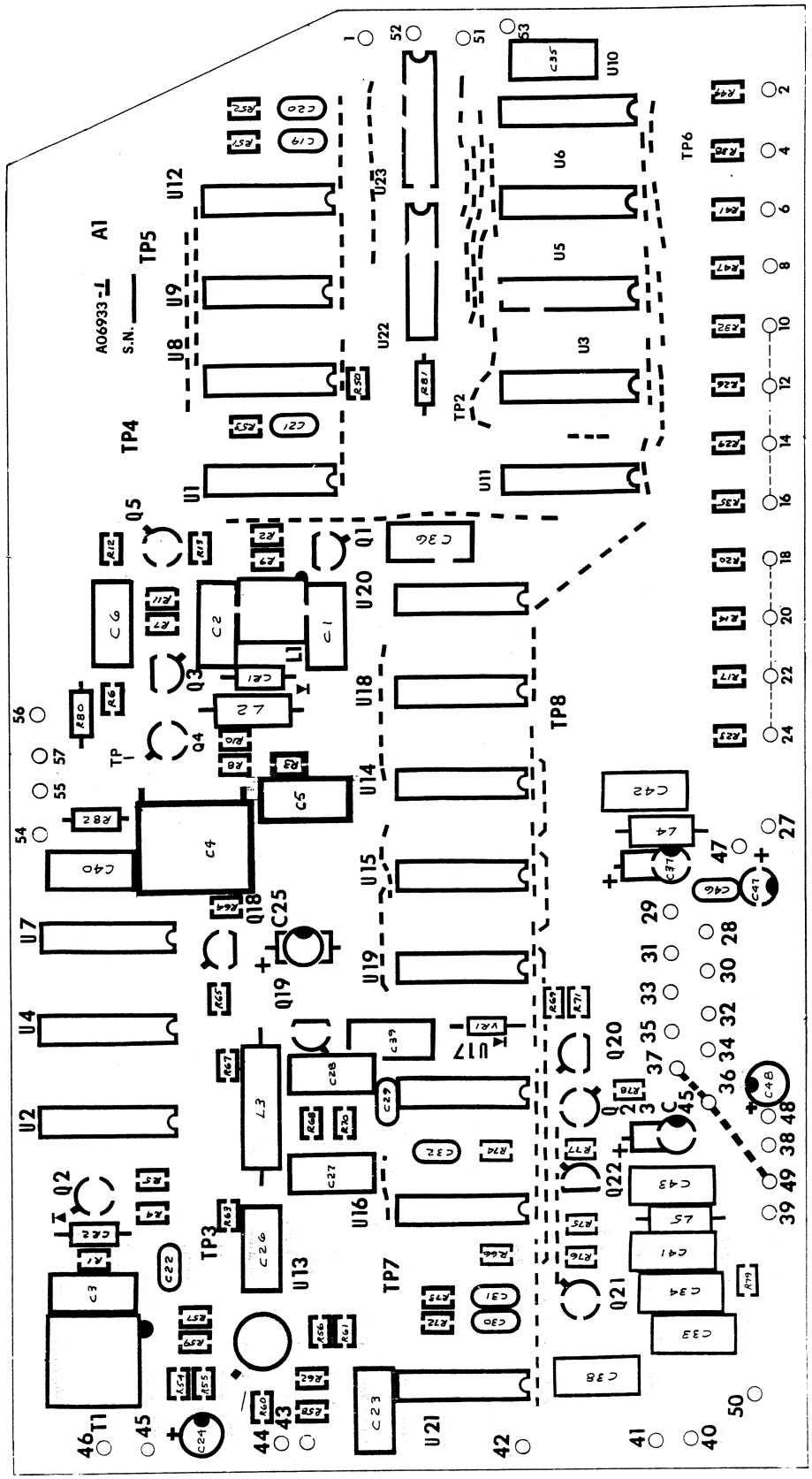


Figure 10-11B Lower Loop Board A11A1, Circuit Card Assembly

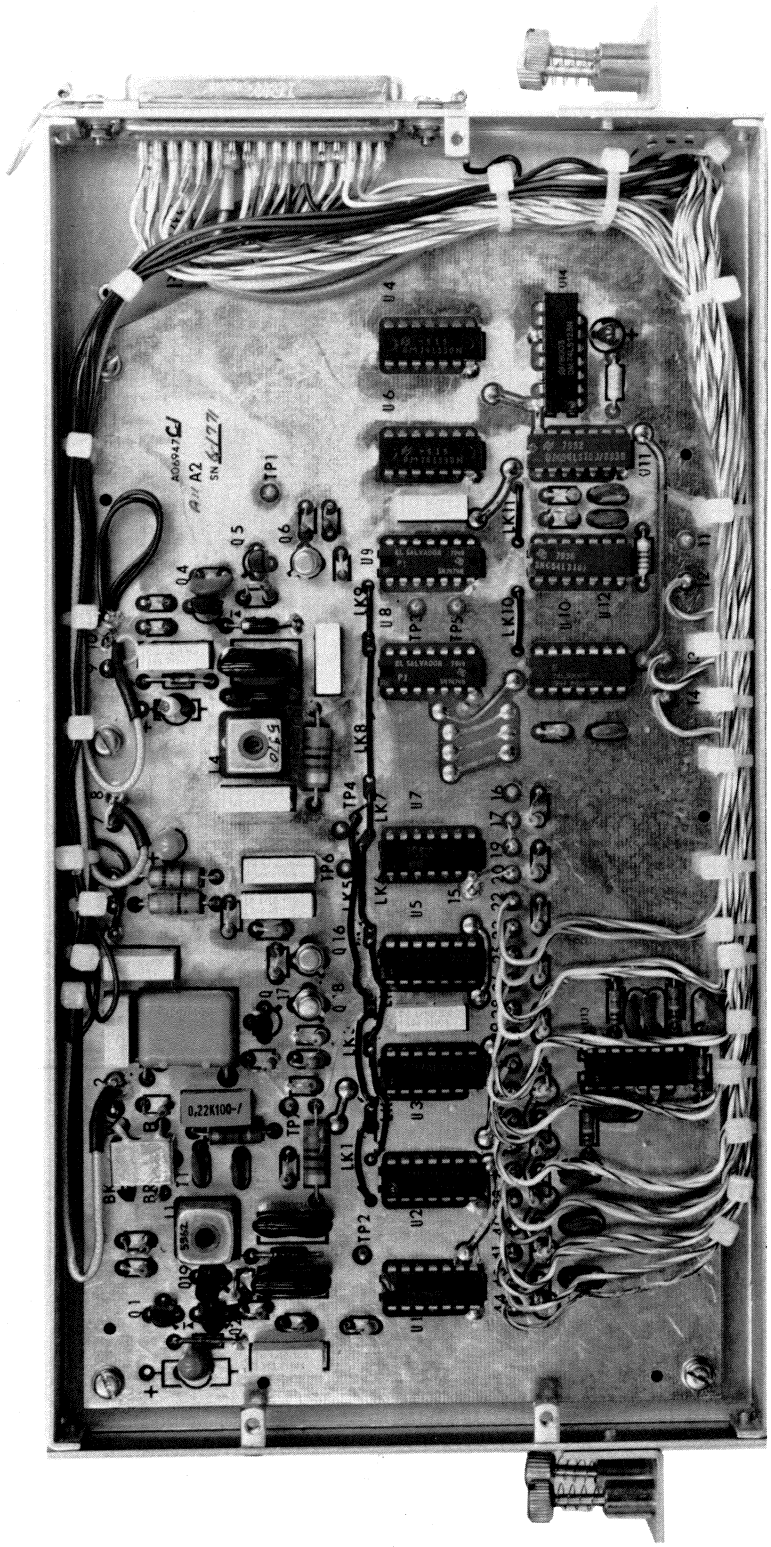


Figure 10-12A. Upper Frequency Loop A11A2, Overall Assembly

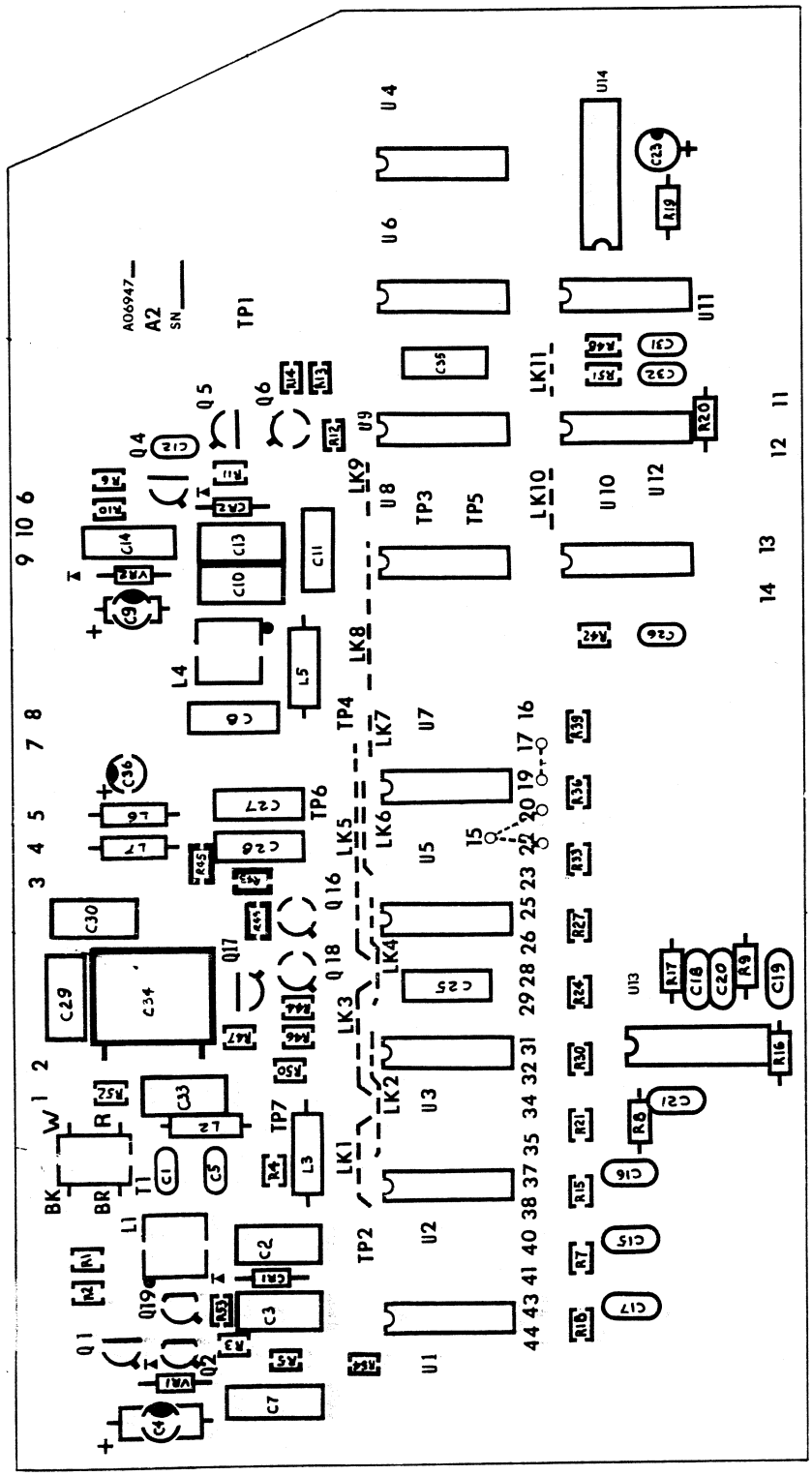


Figure 10-12B Upper Loop Board A11A2, Circuit Card Assembly

8. Connect the digital multimeter, using a scale suitable to measure 6 Volts DC, to TP-1. Adjust L-1 to obtain a reading of 6.0 Volts ±0.5 Volt DC. Record results.

10.4.2 Upper Loop VCO Alignment (A11A2)

1. Connect the digital multimeter to E7 of the A2 board.

2. Set the FREQUENCY SWITCHES to 990 00. Adjust L-4 to obtain a reading of 14.0 ±0.5 Volts DC. Record on test data sheet.

3. Set the FREQUENCY SWITCHES to 000 00.

4. Connect the digital multimeter to TP-7 of the A2 board. Adjust L-1 to obtain a reading of 16.0 ±0.5 Volts DC. Record results.

5. Ensure the OUT OF LOCK lamp is out at this time. Check on test data sheet.

10.4.3 Lower Loop and Upper Loop Frequency Accuracy Check

1. Set the counter to gate to 100 mS.

2. Connect the A input of the frequency counter to the 3.6 – 4.6 MHz OUTPUT port on the front of the test fixture.

3. Set the function switch on the frequency counter to A/B position.

4. Connect the B input of the frequency counter to the 1 MHz REF OUT port located on the rear apron of the test fixture.

5. Perform the requirements of Table 10-2 ensuring the OUT OF LOCK lamp remains out for each position. The accuracy of the display reading should be ±1 count. Check on test data sheet.

10.4.4 Lower Loop and Upper Loop Output Level Check

1. Disconnect the frequency counter from the 3.6 – 4.6 MHz OUT port on the front of the test fixture and connect the R.F. voltmeter using the 50 ohms adapter to this port.

2. Ensure the output level is 220 ±50 mVolts for the following FREQUENCY SWITCH settings:

   000 00
   500 00
   990 00

   Record on test data sheet.

Table 10-2. Frequency Accuracy Check

Frequency Switches	Frequency Counter
000 00	46 000 00
100 00	45 000 00
200 00	44 000 00
300 00	43 000 00
400 00	42 000 00
500 00	41 000 00
600 00	40 000 00
700 00	39 000 00
800 00	38 000 00
900 00	37 000 00
600 00	40 000 00
611 11	39 888 90
622 22	39 777 80
633 33	39 666 70
644 44	39 555 60
655 55	39 444 50
666 66	39 333 40
677 77	39 222 30
688 88	39 111 20
699 99	39 000 10
700 00	39 000 00

Note: The OUT OF LOCK lamp may flicker when changing the FREQUENCY SWITCHES but should be out when the switches have settled. The accuracy of the Display Reading should be ±1 count.

10.4.5 VCO Frequency Offset Check

1. Set the frequency counter as in Paragraph 10.4.3 steps 1 through 4.
2. Set the FREQUENCY SWITCHES to 600 00.
3. The frequency counter should read 40 000 00.
4. Set the OFFSET switch to the −1.8 kHz position. The frequency counter should now display 39 982 00. Check on test data sheet.
5. Set the OFFSET switch to the +1.8 kHz position. The frequency counter should now display 40 018 00. Check on test data sheet.

10.4.6 VCO Settling Time Check and Adjustment

1. Set the controls of the oscilloscope as follows:

Vertical Mode	Chop
Vertical Sensitivity	2 Volts/cm
Horizontal Time Base	5 mSec/cm
Trigger Mode	Normal
Coupling	AC
Source	Ch. 1
A Trigger	Slope (+)
	Level (as required)

2. Place the OFFSET switch to NORMAL position.

3. Connect the Channel 1 input of the oscilloscope to the TRIGGER OUT port located on the rear apron of the test fixture.

4. Place the AF switch to the ON position.

5. Set the oscilloscope to trigger on the positive edge of the waveform on Channel 1 as shown in Figure 10-13, Waveform I. Adjust the red inner knob of the Time/Div. Knob until the falling edge appears on the RH edge of the oscilloscope.

6. Place the Channel 2 input probe of the oscilloscope to E-1 of the A1 board.

7. Place the FREQUENCY SWITCHES to 01999 position.

8. Observe Channel 2 waveform on the oscilloscope. The waveform should be a square wave the trailing edge of which may jitter. Tune L1 on the lower loop for the minimum pulse width on each position of the OFFSET switch. Continue to do this until no further improvement can be obtained, then turn the red inner knob of the time/div knob until the uncal light goes out. The maximum pulse width in any position of the OFFSET switch should not exceed 60 mS. Refer to waveform II of Figure 10-13. **Check on test data sheet.**

9. Place the Channel 2 input of the oscilloscope to E-42 on the A1 board. The waveform observed should be similar to waveform III of Figure 10-13. **Check on data sheet.**

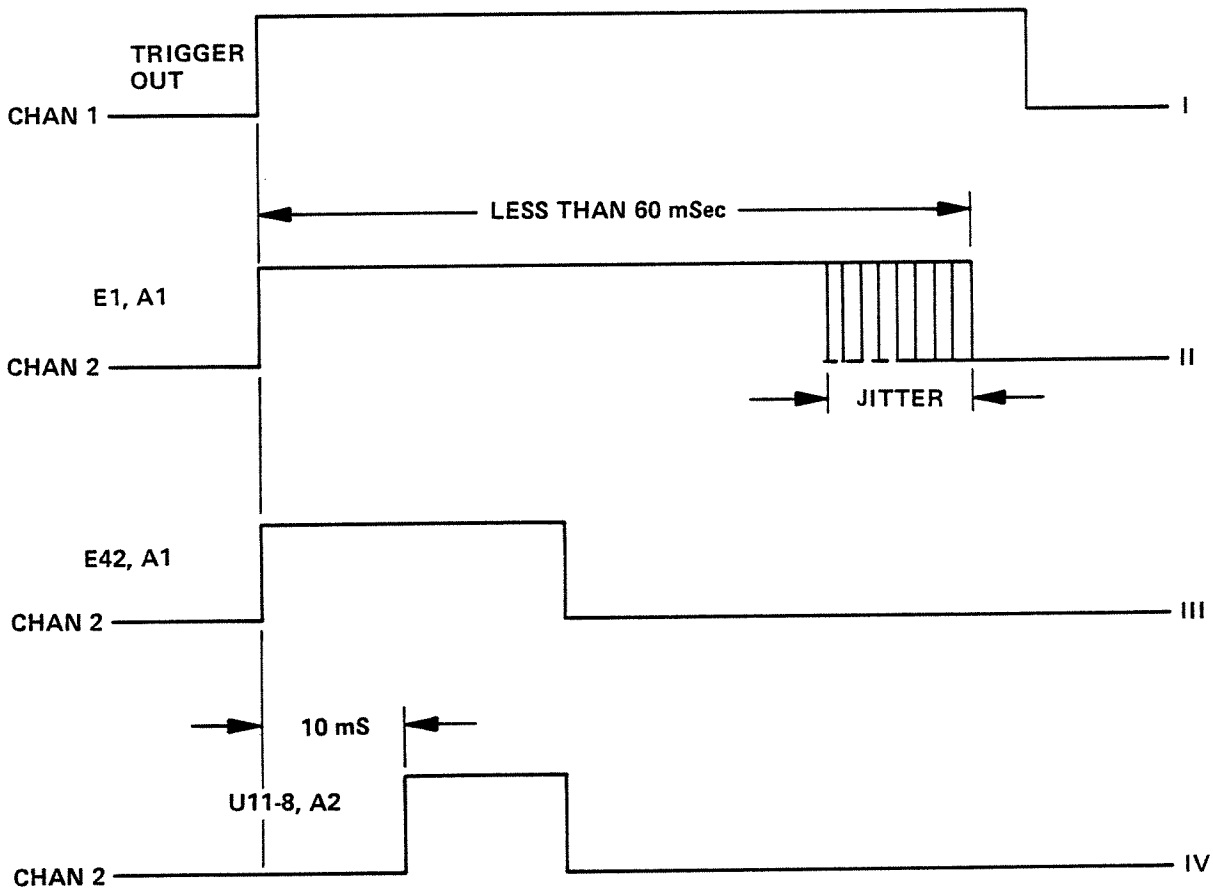
10. Place the FREQUENCY SWITCHES to the 19999 position.

11. Place the Channel 2 input of the oscilloscope to pin 8 of U-11 on the A2 board. The waveform should be similar to waveform IV of Figure 10-13. **Check on test data sheet.**

10.4.7 Microphonic Check

1. Check that L1 has the PTFE tape (teflon) with its tuning slug on the A1 board.

2. Ensure that C1 and C2 are pushed away from L1 as far as possible without damage to components.



NOTE: By setting switches to 19999 before checking the output of pin 8 of U11, a longer OOL pulse is generated that is not completely masked by the operation of U14.

Figure 10-13. Timing Diagram for A11 Out-of-Lock Circuitry

3. Knock firmly on the top and back of the modules, (as if knocking on a door) and check that the OUT-OF-LOCK light remains out. Check on test data sheet.

4. Turn power off and remove B.U.T. from the text fixture.

10.4.8 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (VCO alignment, frequency, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failures of specific frequency counts can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope or voltmeter, to trace the fault to a single component. Maximum use, should also be made, of the test points provided on the A11 modules, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconducts and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 10.4.1 through 10.4.7.

10.5. PARTS LIST, LOWER/UPPER LOOP MODULE, A11

The parts list for the A11 module is contained in Table 10-3. Tables 10-4 and 10-5 contain a detailed listing of the components contained on the A11A1 and A11A2 Circuit Card Assemblies.

DATE _____
CKD BY _____

MODULE A11
USED ON _____

TEST DATA SHEET

PART NAME: A11 Lower and Upper Loop Synthesizers
PART NUMBER: 06903-1
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS MIN	LIMITS MAX	UNITS
10.4.1(7)	T1 RF Signal Level (RMS)		1.0	2.0	volts
10.4.1(8)	Voltage at TP-1 (A1)		5.5	6.5	volts
10.4.2(2)	Voltage at E7 (A2)		13.5	14.5	volts
10.4.2(4)	Voltage at TP7 (A2)		15.5	16.5	volts
10.4.2(5)	Out-of-Lock Lamp Out		Pass	Fail	
10.4.3(5)	Table 10.2 verified		Pass	Fail	
10.4.4	Output Level check 000 00		170	270	mV
	500 00		170	270	mV
	990 00		170	270	mV
10.4.5(4)	- 1.8 kHz Offset		Pass	Fail	
10.4.5(5)	+1.8 kHz Offset		Pass	Fail	
10.4.6(8)	Timing Diagram Waveform II			60	mSec
10.4.6(9)	Timing Diagram Waveform III		Pass	Fail	
10.4.6(11)	Timing Diagram Waveform IV		Pass	Fail	
	(delay respect to waveform I)			15	mSec
10.4.7(3)	Microphonic Check		Pass	Fail	

TABLE 10-3. PARTS LIST, UPPER LOWER LOOP SYNTHESIZER MODULE ASSEMBLY (A11) 06903-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A1	Lower Loop Circuit Card Assembly (See Table 10-4, for further breakdown)	06933	
A2	Upper Loop Circuit Card Assembly (See Table 10-5, for further breakdown)	06947-1	
W1	Cable Form	07147	
–	Spring Latch Assembly	61183	D110279
J1	Connector, Multi-pin (Cannon)	61167	DDM 36W4P
J1A1, J1A2, J1A3	Connector, Coaxial (Cannon)	60021	DM-53740-5008

TABLE 10-4. PARTS LIST, LOWER LOOP CIRCUIT CARD ASSEMBLY (A11A1) 06933

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-3	Capacitor, Mica, 1000 pF, ±2%	22110	CM06F102G03
C4	Capacitor, Polycarbonate, 1.0 uF, ±20%, 50 VDC	26893	PMC2R-1R0100
C5	Capacitor, Polycarbonate, 0.22 uF, ±20% (Mepco)	26872	C280MCH/A220K
C6, 23, 26, 34-36, 38-43	Capacitor, Polycarbonate, 0.1 uF, ±20% (Mepco)	26871	C280MCH/A100K
C7-18, 44	Not used		
C19, 20, 30, 31	Capacitor, Ceramic, 680 pF, ±10% (Erie)	21743	8131-000-X5R-681K
C21, 32	Capacitor, Ceramic, 220 pF, ±10% (Erie)	21328	835-000-G3C0-221K
C22, 29, 46	Capacitor, Ceramic, 0.01 uF, +80% –20% (Erie)	21740	805-000-25V0-103Z
C24, 45, 48	Capacitor, Tantalum, 6.8 uF, ±20% (Union Carbide)	25032	T360B685M035
C25	Capacitor, Tantalum, 1.0 uF, ±20% (Union Carbide)	25033	T360A105M035
C27, 28, 33	Capacitor, Polycarbonate, 0.01 uF, ±20% (Mepco)	26870	C280MCF/A10K
C37, 47	Capacitor, Tantalum, 33 uF, ±20% (Union Carbide)	25019	K33E10
CR1	Diode, Varicap	29006	Motorola MV1650
CR2	Diode	35514	1N916
L1	Coil, Variable	05961	
L2	Choke, 330 uH, ±5%, RF	43036	Delevan 2500-04
L3	Choke, 4700 uH, ±5%, RF	43039	Delevan 2500-60
L4	Choke, 1 uH, ±5%, RF	43024	Delevan 1537-12
L5	Choke, 47 uH, ±5%, RF	43032	Delevan 1537-60
Q1, 18-20	Transistor	32021	2N5089
Q2, 4, 5, 21, 23	Transistor	32255	2N2369A
Q3, 22	Transistor	31508	2N4126
Q6-17	Not Used		
R1, 54, 68, 76	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF 222J
R2, 70	Resistor, Composition, 330 Ohms, ±5%, 1/4W	10651	RC07GF331J
R3	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J
R4, 64	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R5, 9, 50-52, 55, 57, 58, 66, 71-73, 80-82	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R6, 11, 13, 56, 59	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J
R7, 8	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R10, 12	Resistor, Composition, 680 Ohms, ±5%, 1/4W	10659	RC07GF681J
R14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 67	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R15, 16, 18, 19, 21, 22, 24, 25, 27, 28, 30, 31, 33, 34, 36, 37, 39, 40, 42, 43, 45, 46, 48, 49,	Not Used		
R53, 60, 61, 62, 65, 74	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R63, 77, 78	Resistor, Composition, 1.5K Ohms, ±5%, 1/4W	10667	RC07GF152J
R69, 75, 79	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	10675	RC07GF332J
T1	Transformer	05964	
U1	Integrated Circuit (Fairchild)	36632	74LS00J
U2, 4, 7	Integrated Circuit (Fairchild)	36637	74LS90J
U3, 5, 6, 10, 14, 15, 19	Integrated Circuit (Fairchild)	36621	74LS196J

TABLE 10-4. PARTS LIST, LOWER LOOP CIRCUIT CARD ASSEMBLY (A11A1) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U8, 16	Integrated Circuit (Fairchild)	36636	74LS74J
U9	Integrated Circuit (Fairchild)	36635	74LS30J
U11, 20	Integrated Circuit (Fairchild)	36638	74LS107J
U12, 21	Integrated Circuit (Fairchild)	36633	74LS10J
U13	Integrated Circuit (Fairchild)	36543	uA796HC
U17	Integrated Circuit (Fairchild)	36641	74LS13J
U18	Integrated Circuit (Fairchild)	36634	74LS20J
U22	Integrated Circuit (Fairchild)	36644	74LS11J
U23	Integrated Circuit (Fairchild)	36640	74LS32J
VR1	Diode, Zener, 5.6V	33543	1N752A
-	Printed Wiring Board	06932	
-	Pad, Transistor for Q2, 4, 5, 21, 23	70760	7717-46N-WHITE
-	Pad, Transistor for U13	70768	RCT05140-10A

TABLE 10-5. PARTS LIST, UPPER LOOP CIRCUIT CARD ASSEMBLY (A11A2) 06947

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 26	Capacitor, Ceramic, 220 pF, ±10% (Erie)	21328	835-000-G3C0-221K
C2, 3, 10, 13	Capacitor, Mica, 1000 pF, ±2%	22110	CM06FD102G03
C4, 36	Capacitor, Tantalum, .33 uF, ±20%, 10V (UC)	25019	K33E10
C5	Capacitor, Ceramic, 100 pf, ±10% (Erie)	21327	831-000-X5F0-101K
C7, 14, 25, 27-30, 35	Capacitor, Polycarbonate, 0.1 uF, ±20%, 100V (M/E)	26871	C280MCH/A100K
C8, 11	Capacitor, Polycarbonate, 0.01 uF, ±20% (M/E)	26870	C280MCF/A10K
C9	Capacitor, Tantalum, 4.7 uF, ±20%, 10V (UC)	25031	T360A475M010
C12	Capacitor, Ceramic, 0.01 uF, +80% –20% (Erie)	21740	805-000-25V0-103Z
C15-17, 18-21	Capactior, Ceramic, 0.001 uF, ±20% (Erie)	21747	831-000-X5T-102M
C22, 24	Not Used		
C23	Capacitor, Tantalum, 1 uF, ±5% (UC)	25054	T368A105J020AS
C31, 32	Capacitor, Ceramic, 680 pF, ±10% (Erie)	21743	8131-000-X5R-681K
C33	Capacitor, Polycarbonate, 0.22 uF, ±20%, 100V (M/E)	26872	C280MCH/A220K
C34	Capacitor, Ceramic, 1.0 uF, ±20% (Erie)	26893	PMC2R-1R0100
CR1, 2	Diode, Varicap	29006	Motorola MV1650
L1	Coil, Variable, RF	05962	
L2	Choke, 15 uH, RF	43030	Delevan 1537-40
L3, 5	Choke, 1000 uH, RF	43038	Delevan 2500-28
L4	Coil, Variable	05970	
L6	Choke, 1 uH	43024	Delevan 1537-12
L7	Choke, 47 uH	43032	Delevan 1537-60
Q1, 2, 4, 5, 19	Transistor	32021	2N5089
Q6, 16, 18	Transistor	32255	2N2369A
Q3, 7-15	Not Used		
Q17	Transistor	31508	2N4126
R1, 5	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	10675	RC07GF332J
R2, 43, 46	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J
R3, 4	Resistor, Composition, 330 Ohms, ±5%, 1/4W	10651	RC07GF331J
R6	Resistor, Composition, 3.3K Ohms, ±5%, 1/8W	18375	RC05GF332J
R7, 15, 18, 21, 24, 27, 30, 33, 36, 39	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R8, 9, 16, 17	Resistor, Composition, 100K Ohms, ±5%, 1/4W	10711	RC07GF104J
R10	Resistor, Composition, 470 Ohms, ±5%, 1/8W	18355	RC05GF471J
R11, 12	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R13, 14	Resistor, Composition, 1K Ohms, ±5%, 1/8W	18363	RC05GF102J
R19	Resistor, Composition, 33.2K Ohms, ±1%, 1/10W	12135	RN55D3322F
R20	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R22,23,25,26,28,29,31, 32,34,35,37,38,40,41	Not Used		
R42, 45, 49, 50	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R44, 47	Resistor, Composition, 680 Ohms, ±5%, 1/4W	10659	RC07GF681J
R48, 51, 52	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R53	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R54	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J
T1	Transformer	05963	
U1, 10	Integrated Circuit (Fairchild)	36632	74LS00J

TABLE 10-5. PARTS LIST, UPPER LOOP CIRCUIT CARD ASSEMBLY (A11A2) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U2,3,5	Integrated Circuit (Fairchild)	36621	74LS196J
U4, 6	Integrated Circuit (Fairchild)	36637	74LS90J
U7	Integrated Circuit (Fairchild)	36635	74LS30J
U8, 9	Integrated Circuit (Fairchild)	36528	7474DC
U11, 12	Integrated Circuit (Fairchild)	36633	74LS10J
U13	Integrated Circuit (Motorola)	36618	MC14585BCLD
U14	Integrated Circuit (Fairchild)	36659	74LS123J
VR1, 2	Diode, Zener	33543	1N752A
-	Printed Wiring Board	06946	
-	Clamp, Transformer used with T1	05806	
-	Pad, Transistor for R6, 16, 18	70760	7717-7NWHITE

CHAPTER 11
TRANSFER LOOP, A13

11.1 THEORY OF OPERATION

This chapter provides information on the transfer loop board, A13. This board is a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A13 module within the synthesizer section. Figure 10-1 in Chapter 10 shows a simplified function block diagram of the complete section, and paragraph 10.1 describes the overall synthesizer operation.

11.1.1 Transfer Loop Board, A13

The transfer loop board contains the upper transfer loop (with the exception of the upper transfer loop oscillator which is located on the HF loop board, A14), programmed divider N3, and the lock indicator circuits. This board, together with HF loop board, generates the 35.4 to 65.4 MHz local oscillator injection frequency for the first mixer. A block diagram of the two boards is shown in Figure 11-1. The schematic for the transfer loop board is shown in Figure 11-2. The 3.6 to 4.6 MHz frequency from the upper loop is divided by programmed divider, N3, and phase-compared with the output of a mixer. The mixer receives the 1 MHz reference and the output of the upper transfer loop VCO which is located in the high frequency loop board, A14. The VCO covers a range of from 884.950 to 948.116 kHz.

The programmed divider, N3, has a division ratio of from 40 to 69, which is equal to 40 plus the MHz setting. This is achieved by first converting 0 to 29 from the MHz selection into a nines complement code before application to the programmed divider. This allows a backward count from the total counter preload to 39, when reset occurs. Table 11-1 gives the conversion from decimal to nines complement code.

The 3.6 to 4.6 MHz output signal from upper loop, at board pin J3, is coupled by C3 to a shaper stage, Q4 and Q5. The squarewave output is inverted by U4A and is then applied to a programmed divider consisting of two presettable decade counters, U1 and U2; an inverter, U4B; a six-input NAND gate, U5; and a D-type flip-flop, U6.

11.1.1.1 Programmed Divider, N3

The two decade counters, U1 and U2, have strobed parallel-entry capability so that the starting points of count sequence may be preset. A '1' or a '0' at a data input (A, B, C or D) is transferred to the associated output when the strobe (ST) input is at '0'. The counting operation is performed on the negative-going edge of the input clock pulse.

The division ratio of the programmed divider, controlled by inputs from the control unit, is given by the expression, N3 = 40+ selected MHz digits. For example, if 00 MHz is selected, the division ratio is 40. When 29 MHz is selected, the division ratio is 69.

Input information is converted into a BCD nines-complement code (see Table 11-1). The nines complement coded inputs are applied to the data inputs of the two decade counters, 'units' to U1 and 'tens' to U2, to preset the starting points of a count sequence.

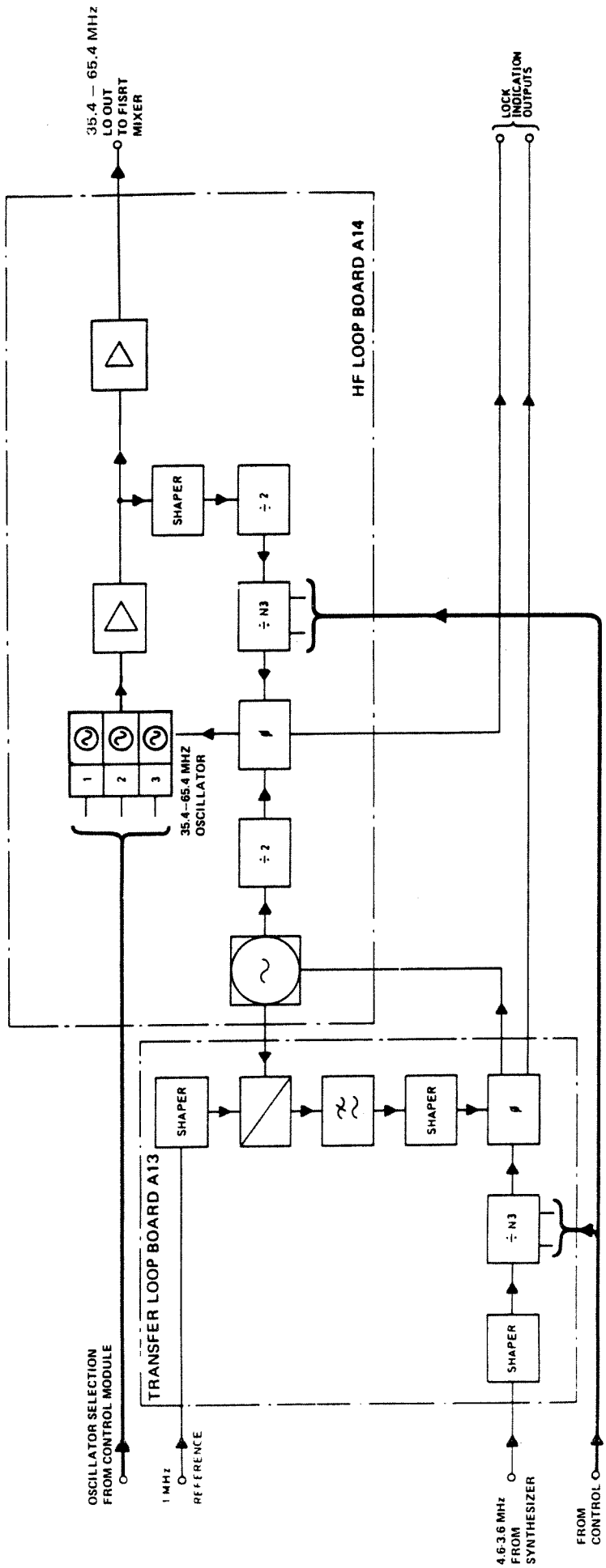
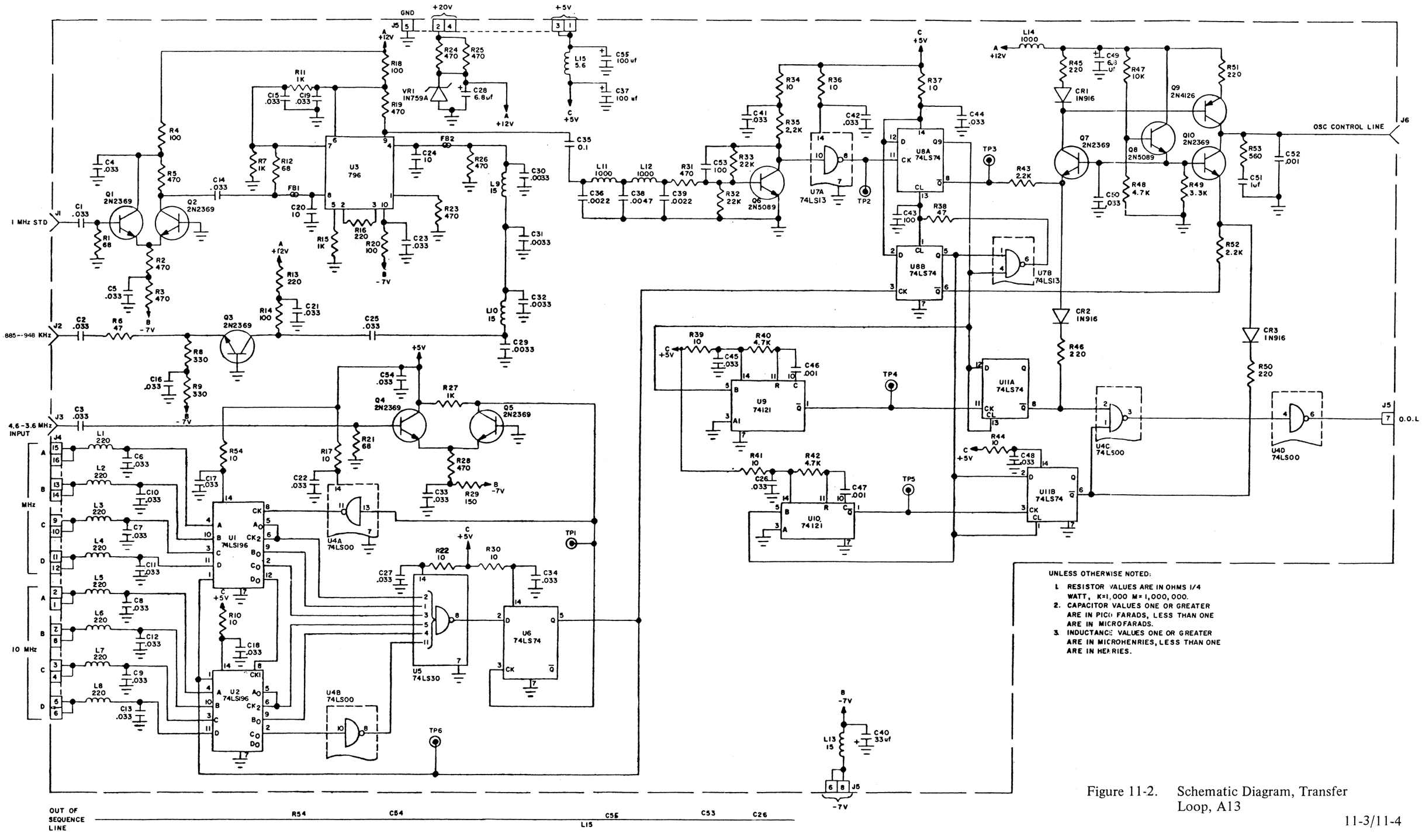


Figure 11-1. Block Diagram, Transfer & HF Loop Boards, A13 and A14



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT, K=1,000 M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN HENRIES.

OUT OF SEQUENCE LINE

R54 C54 C55 C53 C26 L15

Figure 11-2. Schematic Diagram, Transfer Loop, A13

To start the counting sequence, assume that a logic '0' strobe pulse is applied to the strobe (ST) inputs of both U1 and U2 (at pin 1). As previously described, this causes the logic level applied to each input line to be transferred to the corresponding output line. The negative-going edge of the clock pulse, from the shaper stage Q4 and Q5 and the inverter U4A, is now applied to the clock 1 input of U1 at pin 8. Each clock pulse is now counted until a count of 37 is reached; i.e., until the A, B and C outputs from U1 and the A and B outputs from U2 are all at logic '1'. The C output from U2 is applied to an inverter, U4B, to inhibit BCD 7.

When a count of 37 is reached, the input lines to NAND gate U5 are all at logic '1' and the '0' output, at U5 pin 8, is applied to the D input of flip-flop U6. The next clock pulse, applied to pin 3 of U6, transfers the '0' at U6 pin 2 to the Q output at U6 pin 5. This is applied as the next strobe pulse to the two decade counters, U1 and U2; ready for the next count. The output from U5 changes to logic '1' and the next clock pulse applied to U6 causes the Q output to change to logic '1', this output is applied to the phase comparator, U8.

Table 11-2 shows the operation of the divider for various input MHz frequency selections.

Table 11-1. Code Conversion

	BCD				Nines Complement				
Decimal	D	C	B	A	D9	C9	B9	A9	Decimal
0	0	0	0	0	1	0	0	1	9
1	0	0	0	1	1	0	0	0	8
2	0	0	1	0	0	1	1	1	7
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	0	1	5
5	0	1	0	1	0	1	0	0	4
6	0	1	1	0	0	0	1	1	3
7	0	1	1	1	0	0	1	0	2
8	1	0	0	0	0	0	0	1	1
9	1	0	0	1	0	0	0	0	0

Table 11-2. Programmed Divider Operation (A13)

'MHz' Setting	Nines Complement	Count Up To 100	Fixed Count	Strobe Begin	Pulse End	Total Division Ratio
00	99	1	37	1	1	40
07	92	8	37	1	1	47
14	85	15	37	1	1	54
21	78	22	37	1	1	61
29	70	30	37	1	1	69

11.1.1.2 Mixer

U3 is an integrated circuit mixer; the 1 MHz reference frequency signal, shaped by Q1 and Q2, is applied to pin 8 (clock 1) and the 885-948 kHz transfer loop oscillator output signal (from the HF loop board) is applied to pin 4 via Q3 and a low pass filter, L9, L10 and C29 to C32. The difference frequency output from the mixer, 115 kHz to 52 kHz, is coupled to a low-pass filter, L11, L12, C36, C38 and C39, and is then applied to a shaper stage, Q6. The squarewave output from Q6 is applied to the phase comparator, U8, via buffer U7A.

11.1.1.3 Phase Comparator

The phase comparator consists of a dual D-type flip-flop, U8; a two-input NAND gate, U7B; and a voltage control circuit, Q7, Q8, Q9 and Q10. It compares the output frequency from the programmed divider with the output signal frequency from the mixer; any error between these two frequencies is used to develop a dc voltage, which is applied to the transfer loop oscillator (on the HF loop board) to eliminate the error.

The output from the programmed divider, at U6 pin 5, consists of negative-going pulses; these are applied to the clock input of U8B. The output from the mixer (via the low-pass filter, shaper and buffer) at U7A pin 8 is applied to the clock input of U8A. The D inputs to both U8A and U8B are taken to +5V (logic '1'). Thus, when the positive edge from U6 pin 5 clocks U8B, the Q output at pin 5 changes to '1' and the $\overline{Q}$ output changes to '0'. Similarly, when the positive edge from U7A pin 8 clocks U8A, the Q output changes to '1' and the $\overline{Q}$ output changes to '0'. When both Q outputs are at '1', the output from NAND gate U7B changes to '0', clearing both U8 flip-flops via R38, resetting the Q outputs to (0' and the $\overline{Q}$ outputs to '1'.

When the frequency of the mixer output signal is high, the positive edge from U7A will occur before the edge from U6. The resultant setting and resetting of the flip-flops causes increased conduction of Q7, due to the Q1 output from U8A (see waveform diagram, Figure 10-4 in Chapter 10), as compared with the conduction of Q10, this causes the voltage of the collector of Q9 to become more positive, thereby increasing the varactor line voltage applied to the transfer loop oscillator on the HF loop board. This increases the oscillator frequency, but since this frequency is subtracted from the reference 1 MHz in the mixer, U3, the output frequency from the mixer is reduced.

If the mixer output signal frequency is low, the pulse from U7A occurs after the pulse from U6. The Q2 output waveform from U8B causes increased conduction of Q10, and the voltage at the collector of Q9 becomes less positive. Thus, the reduced varactor line voltage applied to the transfer loop oscillator causes a reduction in oscillator frequency and a corresponding increase in the mixer output signal frequency.

When the two frequencies are in phase, the two flip-flops of U8 are clocked at the same time. The two waveforms are equal and the varactor line voltage remains constant.

11.1.1.4 Out-of-Lock Detector and Fast Lock Circuit

This circuit comprises two monostable flip-flops, U9 and U10; a dual D-type flip-flop, U11; and NAND gates U4C and U4D. Its purpose is to augment the conduction of Q7 or Q10 in the out-of-lock condition to obtain a faster return to the locked condition. It also provides a lock indication output signal.

The 1 output from the phase comparator flip-flop, U8A, is applied to the B input of the monostable, U9, and to the D and clear inputs of a D-type flip-flop, U11A. Similarly, the Q output from U8B is applied to the B input of the monostable, U10, and to the D and clear inputs of a second D-type flip-flop, U11B. The two monostables, triggered when positive-going signals are applied to the respective B inputs, each produce a negative-going output pulse, ($\overline{Q}$), of approximately 1.5 microseconds duration.

From the waveform diagram, Figure 11-3, it will be seen that for the in-lock condition the $\overline{Q}$ outputs from the two flip-flops, U11A and U11B, are both at logic '1'. These two signals do not, however, affect the conduction of the voltage control transistors, Q7 and Q10, due to the presence of the two diodes CR2 and CR3. The logic '0' output from U4C is inverted by U4D to produce a logic '1' in-lock signal at board pin J5-7.

If the output frequency from the mixer is low as depicted by the out-of-lock waveform of Figure 11-3, the negative excursion of the $\overline{Q}$ output from U11B is applied to Q10, via diode CR3. The

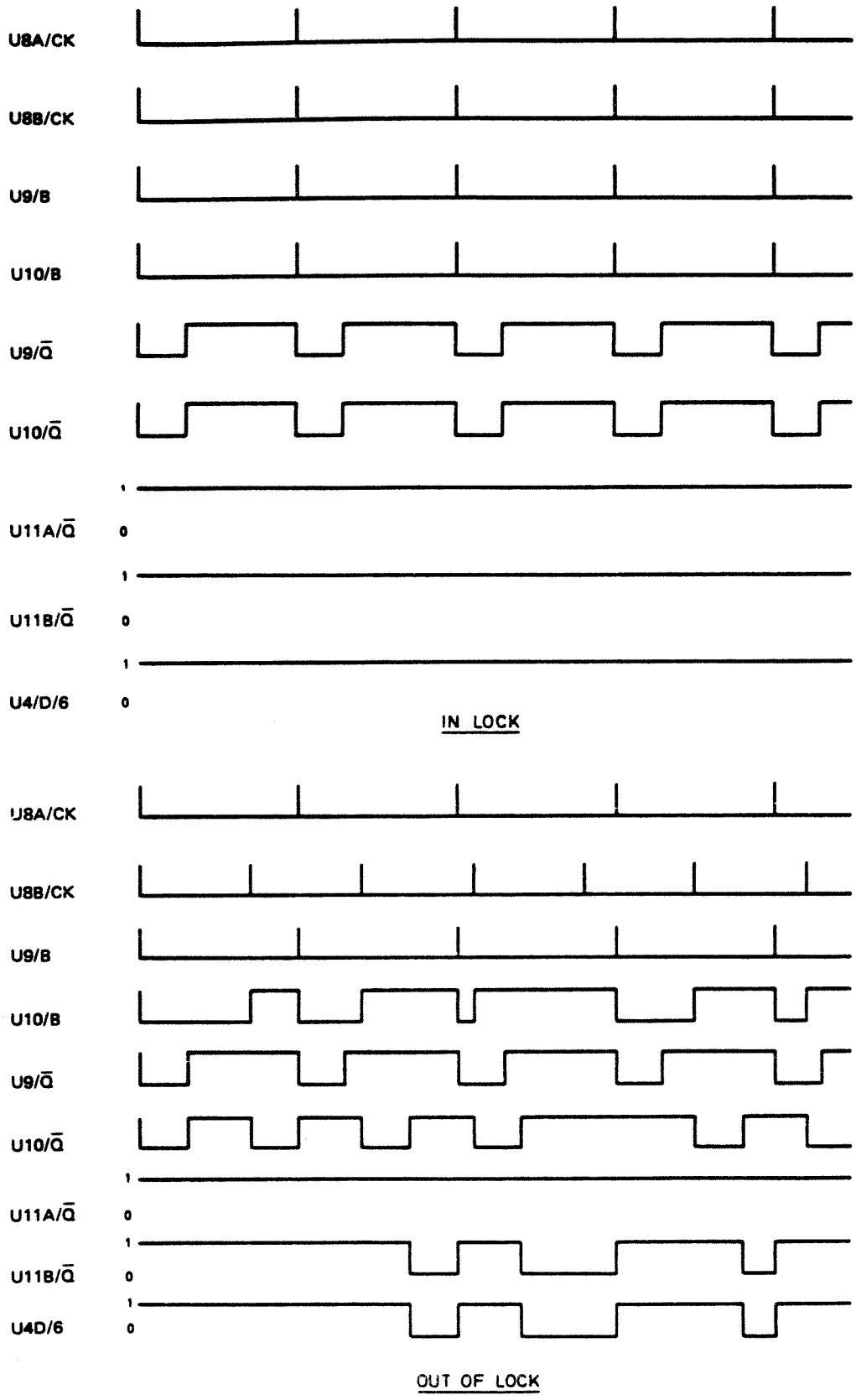


Figure 11-3. Waveform Diagram, Fast Lock and Indicator Upper Transfer Loop, A13

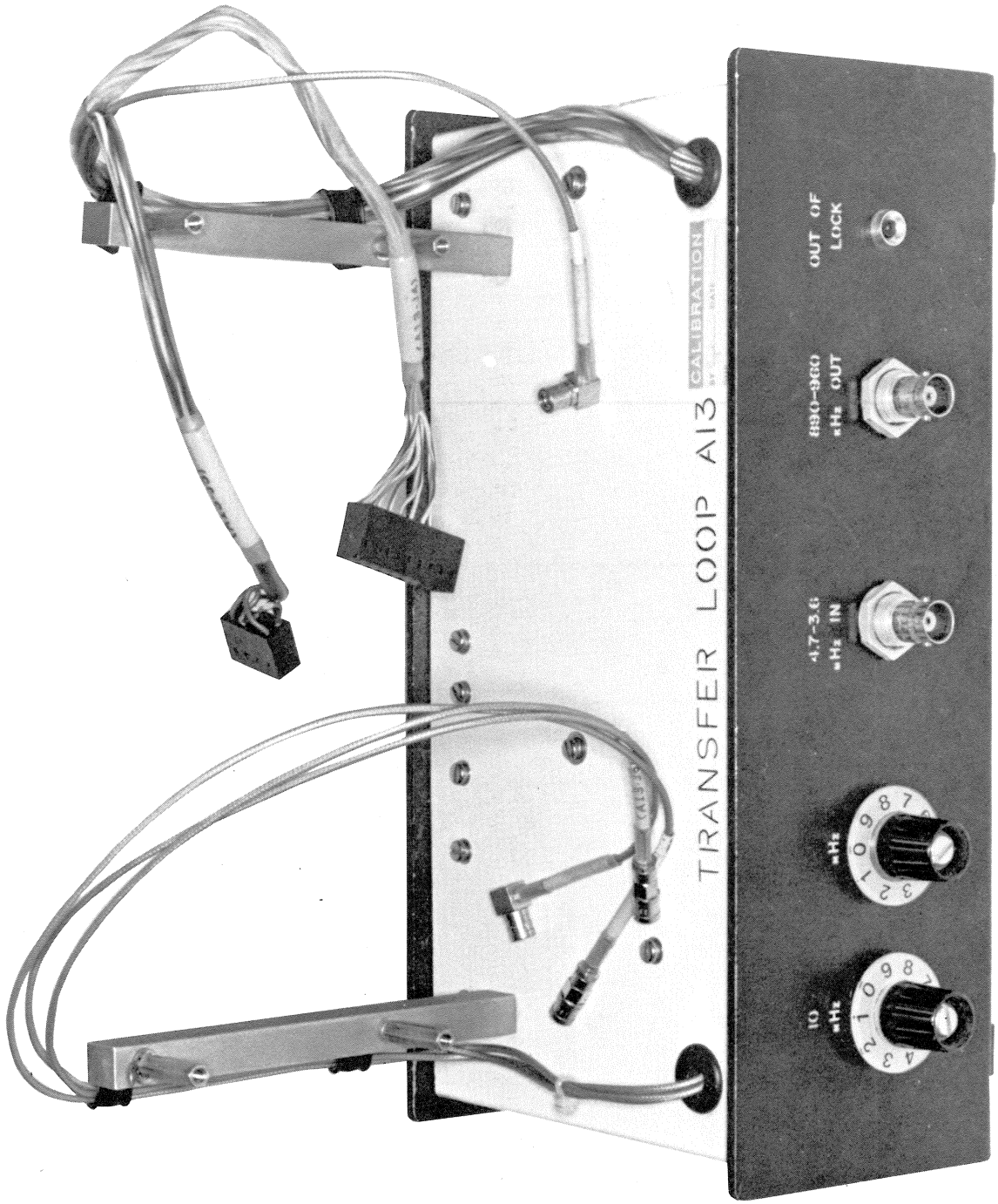


Figure 11-4. Transfer Loop A13, Test Fixture

conduction of Q10 is, therefore, increased rapidly to bring about a fast return to the in-lock condition. The $\overline{Q}$ output waveform from U11B is also applied to U4C to produce an alternating '0' - '1' out-of-lock signal at board pin J5-7.

Should the out-of-lock condition be due to a high mixer output frequency, the $\overline{Q}$ output from U11A causes a rapid return to the in-lock condition by increasing the conduction of Q7. The $\overline{Q}$ output from U11A is also applied to U4C to produce an alternating '0' - '1' out-of-lock signal at board pin J5-7.

11.2 TRANSFER LOOP SYNTHESIZER A13, TEST FIXTURE

Troubleshooting and alignment of the Transfer loop synthesizer module A13 is accomplished through the use of the RACAL transfer loop synthesizer A13 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A13 module for testing, while also providing easy access to the printed circuit board for troubleshooting. The front apron of the test fixture contains the frequency switches to control the VCO frequency.

A 1 MHz oscillator is contained within the test fixture as an internal signal source for the module under test as well as for external sync of associated test equipment. An internal timing circuit provides for using the VCO's in the module under test, in that it permits the VCO to tune its complete range in a repetitive fashion to check settling time. Front panel frequency switches provide BCD inputs for manual setting of the VCO in the module under test. An external trigger output, on the rear apron provides for sync of external equipment. Provisions are also made to display an out of lock condition on the test fixture. Figure 11-4 shows the A13 test fixture. Figure 11-5A shows the overall assembly of the A13 module, while Figure 11-5B shows the circuit card assembly.

11.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required are listed in Table 11-3.

Table 11-3. Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	Frequency Counter (Ratio measurement capability)	Hewlett Packard 5327C or Beckman 6401
2	RF Signal Generator	Hewlett Packard 606
3	DC Power Supply	Racal
4	Test Fixture, A13	Racal
5	Test Probe (oscilloscope, 1 megohm)	Tektronix P6101-X1 (2 required)
6	Oscilloscope	Tektronix P6101

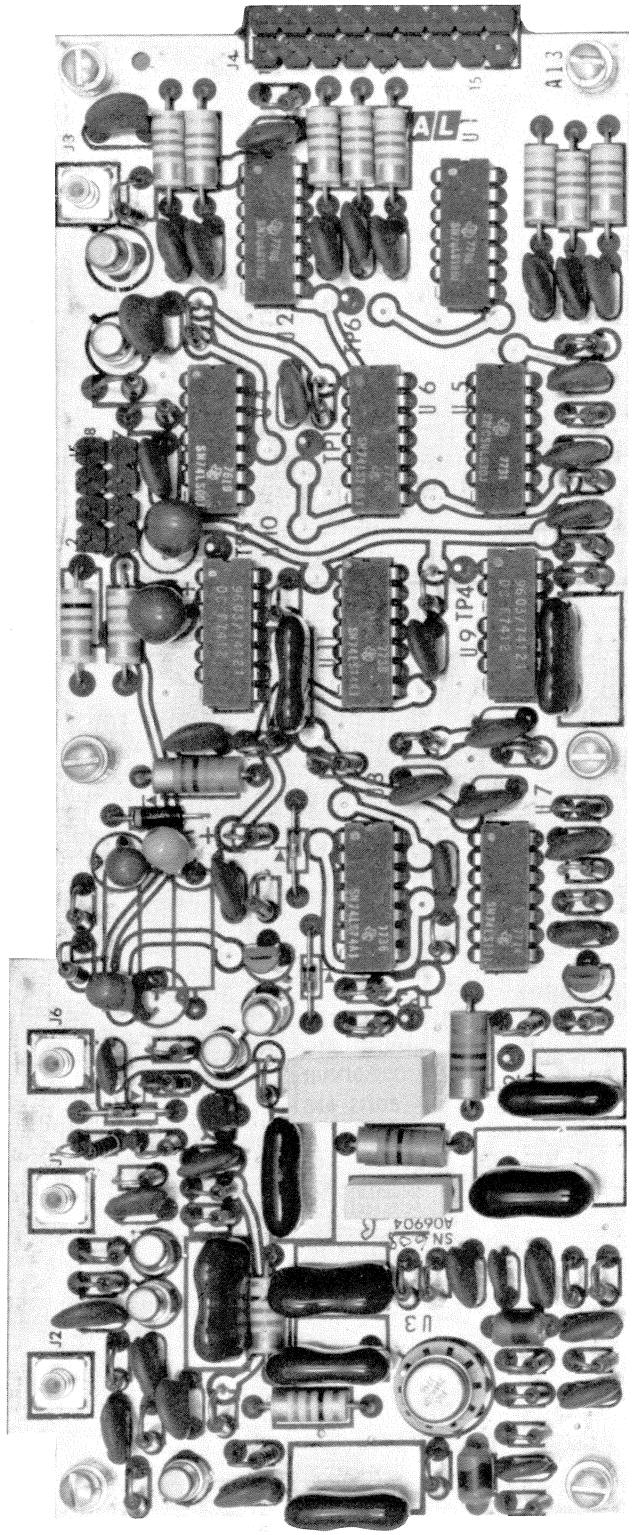


Figure 11-5A. Transfer Loop A13, Overall Assembly

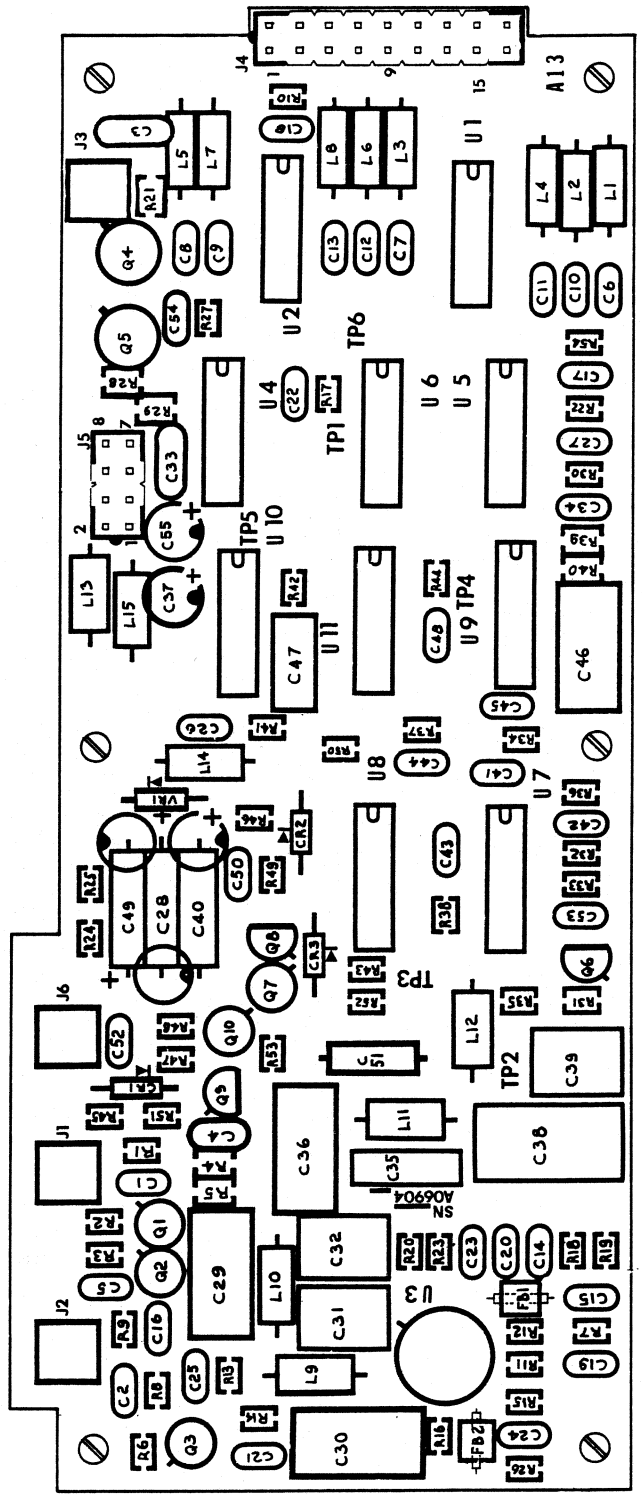


Figure 11-5B. Transfer Loop A13, Circuit Card Assembly

11.4 TEST AND ALIGNMENT

The following procedures are provided to properly test the A13 module. All tests should be performed at ambient room temperature. Record results on test data sheet, page 11-15.

11.4.1 Transfer Loop Divider Accuracy Check

1. Mount the board under test (B.U.T.) on the test fixture.
2. Make all connections between B.U.T. and test fixture, with power plugs red sides up.
3. Using frequency counter*, set the frequency of RF signal generator 4.7 MHz ±10 kHz. Set the signal generator level to 100 mV.
   *If using signal generator with frequency readout, just set the generator at required frequency and output level.
4. If Beckman frequency counter is to be used, proceed to step 8, if Hewlett-Packard counter is used perform steps 5, 6 and 7.
5. Connect the frequency counter input terminal to TP1 on B.U.T. using the 1 megohm oscilloscope test probe (X-1 probe). TP1 is located between U4 and U6.
6. Connect TP6 on B.U.T. (located between U1 and U2) to the external standard input on the rear of frequency counter using 1 megohm oscilloscope probe.
7. Set 'EXT-INT' switch on the rear of frequency counter to 'EXT' position. Proceed to step 9.
8. If using Beckman 6401 programmable frequency counter, connect TP1 to A input (left side) and connect TP6 to B input (right side) on the frequency counter. Set function switch of frequency counter to 'RATIO'.
9. Set 10 MHz and MHz switches on test fixture to '00'.
10. Connect the RF output terminal of signal generator to the '4.7-3.6 MHz' input port on the test fixture using a 50 ohm BNC-BNC coaxial cable.
11. Connect power plug from power supply to left side of test fixture. Turn power on to the test fixture.
12. Perform the frequency checks as required in Table 11-4. In each case the frequency counter reading shall be within ±1 count. Record on test data sheet.
13. Leave the frequency switches on test fixture to '29' MHz.
14. Alternative method of checking transfer loop divider accuracy.
    a. Connect the frequency counter to TP1 on B.U.T. using 1 megaohm oscilloscope test probe.
    b. Perform the frequency checks as required in Table 11-4.

Table 11-4. Frequency Checks

10 MHz Switch	MHz Settings	Frequency Counter Reading Ratio	Direct	Remarks
0	0	40	117.500 kHz	In each case the counter reading shall be within ±1 count. The 'out of lock' lamp on fixture may come on momentarily during switching intervals only if all the circuitry on the rest of the board is functioning correctly; otherwise it may be either ON or OFF all the time for any switch setting.
0	1	41	114.634 kHz	
0	2	42	111.905 kHz	
0	3	43	109.302 kHz	
0	4	44	106.818 kHz	
0	5	45	104.444 kHz	
0	6	46	102.174 kHz	
0	7	47	100.000 kHz	
0	8	48	97.917 kHz	
0	9	49	95.918 kHz	
1	0	50	94.000 kHz	
1	1	51	92.157 kHz	
1	2	52	90.385 kHz	
1	3	53	88.679 kHz	
1	4	54	87.037 kHz	
1	5	55	85.454 kHz	
1	6	56	83.928 kHz	
1	7	57	82.456 kHz	
1	8	58	81.034 kHz	
1	9	59	79.661 kHz	
2	0	60	78.333 kHz	
2	1	61	77.049 kHz	
2	2	62	75.806 kHz	
2	3	63	74.603 kHz	
2	4	64	73.437 kHz	
2	5	65	72.308 kHz	
2	6	66	71.212 kHz	
2	7	67	70.149 kHz	
2	8	68	69.117 kHz	*Leave in this position until told to change these switches.
2	9*	69	68.116 kHz	

11.4.2 Transfer Loop Frequency Accuracy Check

1. Set the frequency of RF signal generator to 3.6 MHz ±10 kHz and the output amplitude to 100 mV. Use frequency counter to monitor the signal generator frequency, if applicable.

2. Set 'EXT-INT' switch on the rear of frequency counter to 'INT' position and remove both 1 megaohm (X-1) probes from the frequency counter inputs (front and rear) and B.U.T. If using Beckman frequency counter, simply remove both connections with counter function switch set at FREQ.

3. Connect a 50 ohm BNC-BNC coaxial cable to '890-960 kHz OUT' port on test fixture and the frequency input terminal on frequency counter front panel.

4. Frequency counter should read 947.827 ±0.1 kHz with five (5) figures or more stable and the 'out of lock' lamp should be OFF. Record on test data sheet.

5. Return the 10 kHz and MHz switches on test fixture to '00' position. Counter should read 910.0 ±0.1 kHz with five (5) figures or more stable and the 'out of lock' lamp should be OFF. Record results.

6. Turn off the power supply and disconnect all test equipment from test fixture and B.U.T.

11.4.3 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (divider, or frequency) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function for instance, failure of certain frequency counts can be traced to specific components. Further signal tracing may then be accomplished using the oscilloscope or Voltmeter, to trace the fault to a single component. Maximum use, should also be made of the test points provided on the A13 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component adjacent components or the printed circuit card is not damaged. Heat sinks should be used on semiconductors and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 11.4.1 and 11.4.2.

11.5 PARTS LIST, TRANSFER LOOP MODULE, A13

The parts list for the A13 circuit card is contained in Table 11-5.

DATE _____
CKD BY _____

MODULE A13
USED ON _____

TEST DATA SHEET

PART NAME: A13 Transfer Loop Board
PART NUMBER: 06904
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
11.4.1(12)	Counter reading each case is correct		–	–	Check
11.4.2(4)	Counter reading on "29" position		947.727	947.927	kHz
	Out-of-Lock lamp OFF				Check
11.4.2(5)	Counter reading on "00" position		909.900	910.100	kHz
	Out-of-Lock lamp OFF				Check

TABLE 11-5. PARTS LIST, TRANSFER LOOP CIRCUIT CARD ASSEMBLY (A13) 06904

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-19, 21, 22, 23, 25, 26, 27, 33, 34, 41, 42, 44, 45, 48, 50, 54	Capacitor, Ceramic, 0.033 uF, +80%, –20% (Erie)	21744	5705-000-X5F-333M
C20, 24	Capacitor, Ceramic, 10 pF, ±.5 pF (Erie)	21347	831-000-C0G0-100C
C28, 49	Capacitor, Tantalum, 6.8 uF, ±20%, 35V (UC)	25032	T368B685M035AS
C29-32	Capacitor, Mica, 3300 pF, ±2%	22145	CM06F332G03
C35	Capacitor, Polycarbonate, 0.1 uF, ±20%, 100V(M/E)	26871	C280MCH/A100K
C36, 39	Capacitor, Mica, 2200 pF, ±2%	22134	CM06F222G03
C37, 55	Capacitor, Tantalum, 100 uF(UC)	25025	T362C107M010AS
C38	Capacitor, Mica, 4700 pF, ±2%	22130	CM06F472G03
C40	Capacitor, Tantalum, 33 uF, ±20%, 10V (UC)	25019	T368B336K010AS
C43, 53	Capacitor, Ceramic, 100 pF, ±10% (Erie)	21327	831-000-S3B0-101K
C46, 47	Capacitor, Mica, 1000 pF, ±2%	22110	CM06F102G03
C51	Capacitor, Polycarbonate, 1 uF, ±20%, 100V	26875	C280MCF/A1M
C52	Capacitor, Ceramic, 0.001 uF, ±20% (Erie)	21747	831-000-X5T-102M
CR1-3	Diode	35514	1N916
FB1, 2	Ferrite Bead (Mullard)	45051	FX1242
L1-8	Choke, 220 uH, RF	43034	MS90538-20
L9, 10, 13	Choke, 15 uH, RF	43030	MS14046-6
L11, 12, 14	Choke, 1000 uH	43038	MS90539-15
L15	Choke, 5.6 uH	43027	MS14046-1
Q1-5, 7, 10	Transistor	32255	2N2369A
Q6, 8	Transistor	32021	2N5089
Q9	Transistor	31508	2N4126
R1, 12, 21	Resistor, Composition, 68 Ohms, ±5%, 1/4W	10635	RC07GF680J
R2, 3, 5, 19, 23-26, 28 31	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J
R4, 14, 18, 20	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R6, 38	Resistor, Composition, 47 Ohms, ±5%, 1/4W	10631	RC07GF470J
R7, 11, 15, 27	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R8, 9	Resistor, Composition, 330 Ohms, ±5%, 1/4W	10651	RC07GF331J
R10, 17, 22, 30, 34, 36, 37, 39, 41, 44, 54	Resistor, Composition, 10 Ohms, ±5%, 1/4W	10615	RC07GF100J
R13, 16, 45, 46, 50, 51	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R29	Resistor, Composition, 150 Ohms, ±5%, 1/4W	10643	RC07GF151J
R32, 33	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R35, 43, 52	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R40, 42, 48	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J
R47	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R49	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	10675	RC07GF332J
R53	Resistor, Composition, 560 Ohms, ±5%, 1/4W	10657	RC07GF561J
U1, 2	Integrated Circuit (Fairchild)	36621	74LS196J
U3	Integrated Circuit (Fairchild)	36543	uA796HC
U4	Integrated Circuit (Fairchild)	36632	74LS00J
U5	Integrated Circuit (Fairchild)	36635	74LS30J

TABLE 11-5. PARTS LIST, TRANSFER LOOP CIRCUIT CARD ASSEMBLY (A13) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U6, 8, 11	Integrated Circuit (Fairchild)	36636	74LS74J
U7	Integrated Circuit (Fairchild)	36641	74LS13J
U9, 10	Integrated Circuit (Fairchild)	36530	74121DC
VR1	Diode, Zener, 12V	33545	
–	Printed Wiring Board	06738	
J1, 2, 3, 6	Connector, Coaxial (Cable Wave)	60044	700209
J4	Connector, Control	06846-9	
J5	Connector, Control	06846-4	
–	Pad, Transistor for U3	70768	RCT05140-10A
–	Pad, Transistor for Q1, 2, 3, 5, 7, 10	70760	7717-46N-WHITE

CHAPTER 12
HIGH FREQUENCY LOOP, A14

12.1 THEORY OF OPERATION

This chapter provides information on the high frequency loop board A14, however, this board is only a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A14 module within the synthesizer section. Figure 10-1 in Chapter 10 shows a simplified function block diagram of the complete section, and paragraph 10.1 describes the overall synthesizer operation.

12.1.1 High Frequency Loop Board, A14

The output signal from the upper transfer loop is divided by two and applied to one input of a phase comparator. The other input originates from the HF loop oscillator which is divided by two, then further divided by N3. The oscillator covers the frequency range of from 35.410 to 65.4 MHz. The A14 board contains three oscillators for low, medium and high frequency ranges, controlled by the frequency selection.

This board also contains the 885-948 kHz upper transfer loop oscillator. The block diagram of the HF loop board, together with the transfer loop board, is shown in Figure 11-1 in Chapter 11. The schematic diagram is shown in Figure 12-1.

12.1.1.1 Transfer Loop Oscillator

Transistors Q17 and Q20, together with associated components, form a variable frequency LC oscillator, tunable by the voltage applied to the varactor diode, CR19. The varactor line voltage at J6, from the transfer loop board, is applied to CR19 via a filter composed of C66, C67, R62, C69 and L19.

The oscillator output signal, at the collector of Q20, is applied to the clock input of a divide-by-two stage, U12. The output from U12, at pin 5, is applied as one signal input to the phase comparator, U7.

A second output from the oscillator is coupled by C76 to a buffer amplifier, Q21. The output from Q21 is applied to the mixer on the transfer loop board, via C81 and J5.

12.1.1.2 HF Loop Oscillators

Three separate switched oscillators are provided to cover the frequency range of 35.410 to 65.3999 MHz. Oscillator selection is controlled by circuits in the front panel control module, A8. A ground (0 V) is connected to the appropriate switching transistor Q1, Q2 or Q3 (via board pins J2-3, J2-1 or J2-2, respectively) and the supply voltage to the selected oscillator is switched on. The oscillator function is as shown in Table 12-1.

Table 12-1. Oscillator Function

Oscillator	Frequency Range (MHz)	MHz Selection
1	35.410 to 43.9999	1 to 7
2	43.40000 to 53.9999	8 to 17
3	53.40000 to 65.39999	18 to 29

The three oscillators are similar in construction and operation. Frequency is controlled by the voltage applied to a pair of varactor diodes. This voltage, derived by the phase comparator, is applied via a common line and an inductor (L21, L22 and L23) to each oscillator. The gain of the selected oscillator stage is automatically controlled by peak-detecting diodes, CR13 and CR14, and the current source transistor, Q13. The controlled gain level is preset by R38.

The output from the selected oscillator transistor and associated buffer, Q7, Q8, or Q9, is amplified by Q10 and applied to a; the automatic gain control stage, Q13, via C26, b; a programmed divider, via C24, and c; an output buffer amplifier stage, Q14, via C36.

Table 12-2. Oscillator Selection

Oscillator Number	Voltage Switch	Oscillator Circuit	Output Buffer
3	Q3	Q6, CR8, CR9, L6	Q9
2	Q2	Q5, CR6, CR7, L5	Q8
1	Q1	Q4, CR4, CR5, L4	Q7

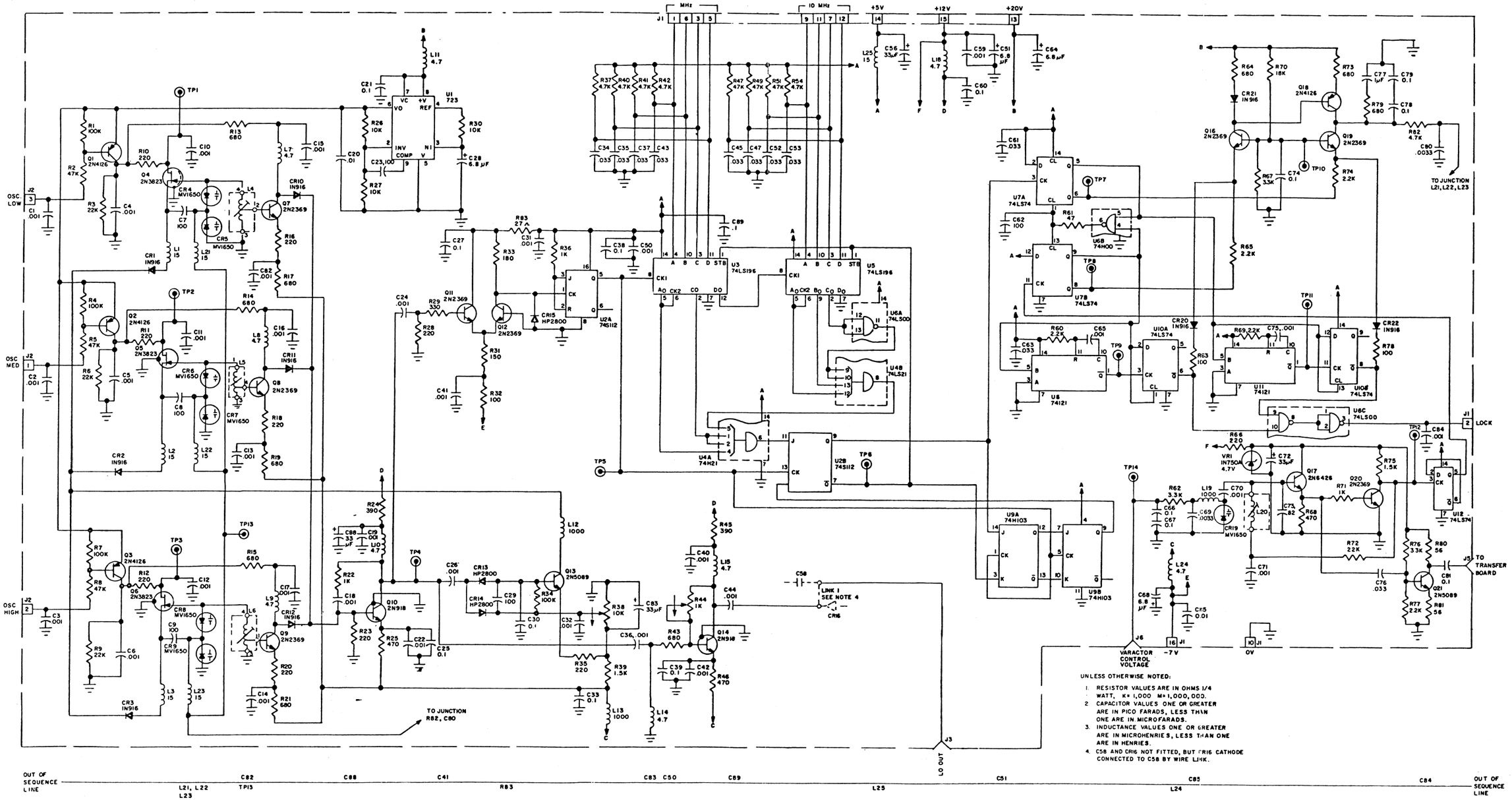
12.1.1.3 LO Output Buffer

The output of the local oscillator is buffered by an amplifier stage, Q14. The gain of this stage is set by potentiometer R44. The output of Q14 is applied through C44 and link LK1 to connector J3 and the First Mixer Board, A2.

12.1.1.4 Programmed Divider, N3

The programmed divider, which is set to the same division ratio as that of the upper transfer loop board programmed divider, consists of a shaper stage, Q11 and Q12; a divide-by-two stage, U2A; two presettable decade counters, U3 and U5, with associated gates; and three J-K flip-flops, U2B, U9A and U9B. For a description of its operation, refer to paragraph 11.1.1.1 in Chapter 11.

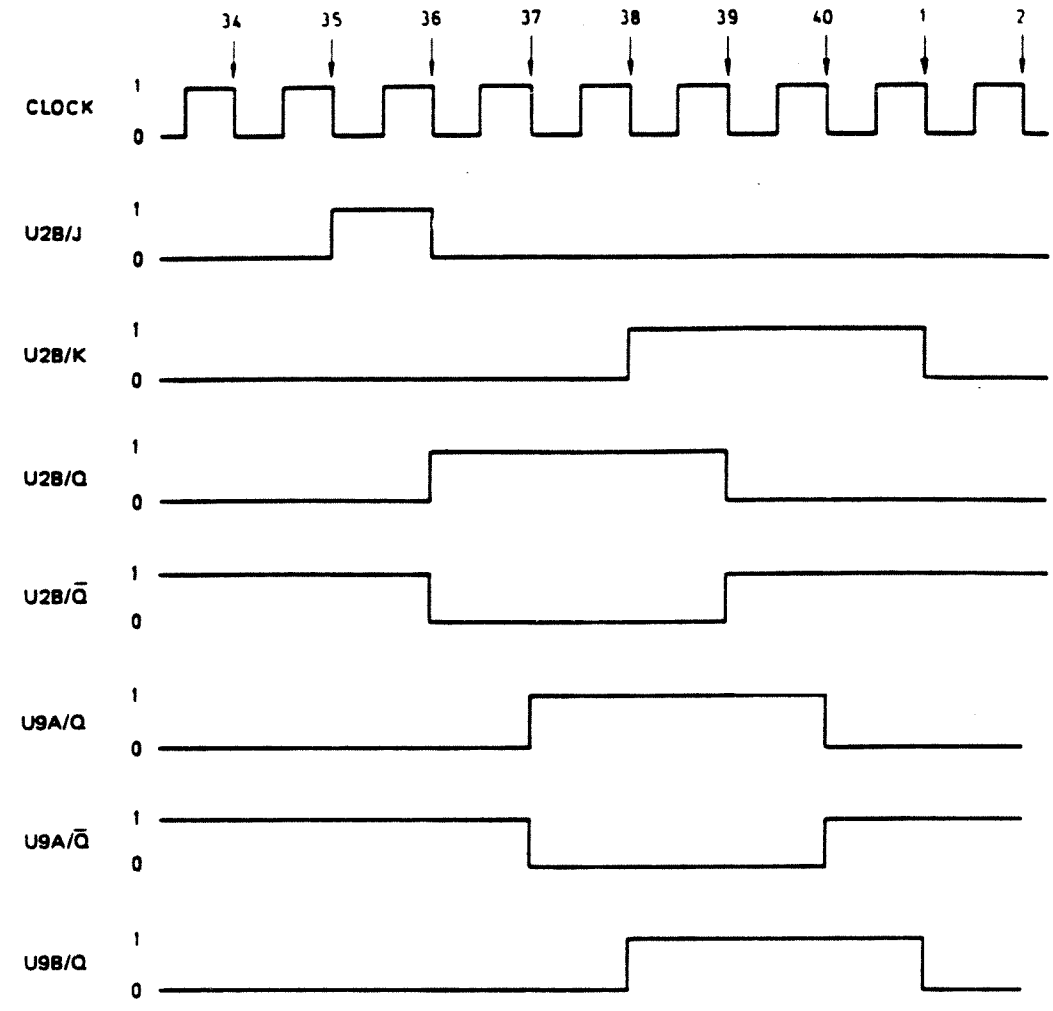
When a count of 35 is reached, the input lines to the AND gate U4A are all at logic '1' and the '1' output, at U4 pin 6, is applied to the J input of flip-flop U2B. Both Q outputs from U2B are fed to the dual J-K flip-flop U9 (Q to J, $\overline{Q}$ to K), and the Q output of U9B is fed back to the K input of U2B. The effect of this circuit is to produce a logic '0' strobe pulse (U2B$\overline{Q}$) sufficient in width for the two decade counters, U3 and U5. Shown in the waveform diagram, Figure 12-2, the strobe pulse is extended to the negative-going edge of the 39th clock pulse; at which point the counting sequence is repeated. Table 12-3 shows the operation of the programmed divider for various MHz selections.



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT, K= 1,000 M=1,000,000.
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN HENRIES.
4. C58 AND CR16 NOT FITTED, BUT CR16 CATHODE CONNECTED TO C58 BY WIRE LINK.

Figure 12-1. Schematic Diagram, High Frequency Loop, A14



TRUTH TABLE (Each Section)		
tn		tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}n$

Figure 12-2. Waveform Diagram, Strobe Pulse Generation HF Loop, A14

Table 12.3. Programmed Divider Operation (A14)

MHz Selection	Nines Complement	Count Up To 100	Fixed Count	Strobe Pulse Generation	Total Division Ratio
00	99	1	35	4	40
07	92	8	35	4	47
14	85	15	35	4	54
21	78	22	35	4	61
29	70	30	35	4	69

12.1.1.5 Phase Comparator

The phase comparator comprises a dual D-type flip-flop, U7; a two-input NAND gate, U6B, pins 4, 5 and 6; and a voltage control circuit, Q16, Q18 and Q19. It compares the output signal frequency from the transfer loop oscillator, after division by two in U12, with the output signal frequency from the programmed divider. Any error between these two frequencies is used to develop a DC voltage which is similar to that of the transfer loop board (A13), as described in paragraph 11.1.1.3 in Chapter 11.

12.1.1.6 Out-of-Lock Detector and Fast Lock Circuit

This circuit comprises two monostables, U8 and U11; a dual D-type flip-flop, U10; and NAND gate U6C. Its purpose is to augment the conduction of Q16 or Q19 in the out-of-lock condition and so obtain a faster return to the locked condition. It also provides a lock indication output signal. The operation of the circuit is described in paragraph 11.1.1.4 in chapter 11.

12.2 HIGH FREQUENCY LOOP SYNTHESIZER A14, TEST FIXTURE

Troubleshooting and alignment of the high frequency loop synthesizer module A14 is accomplished through the use of the RACAL high frequency loop synthesizer A14 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A14 module for testing, while also providing easy access to the printed circuit board for troubleshooting. The front apron of the test fixture contains the frequency controls, offset switch, range blank control, and output port.

A 1 MHz oscillator is contained within the test fixture as an internal signal source for the module under test as well as for external sync of associated test equipment. A transfer loop board is included in the test fixture with a buffer amplifier that isolates the transfer loop while providing a convenient test point. Front panel frequency switches provide BCD inputs for manual setting of the VCO in the module under test. An external trigger out port, on the rear apron, provides for sync of external equipment. Provisions are also made to display an out of lock condition on the test fixture. Figure 12-3 shows the A14 test fixture. Figure 12-4A shows the overall assembly of the A14 module, while Figure 12-4B shows the circuit card assembly.

12.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required are listed in Table 12-4.

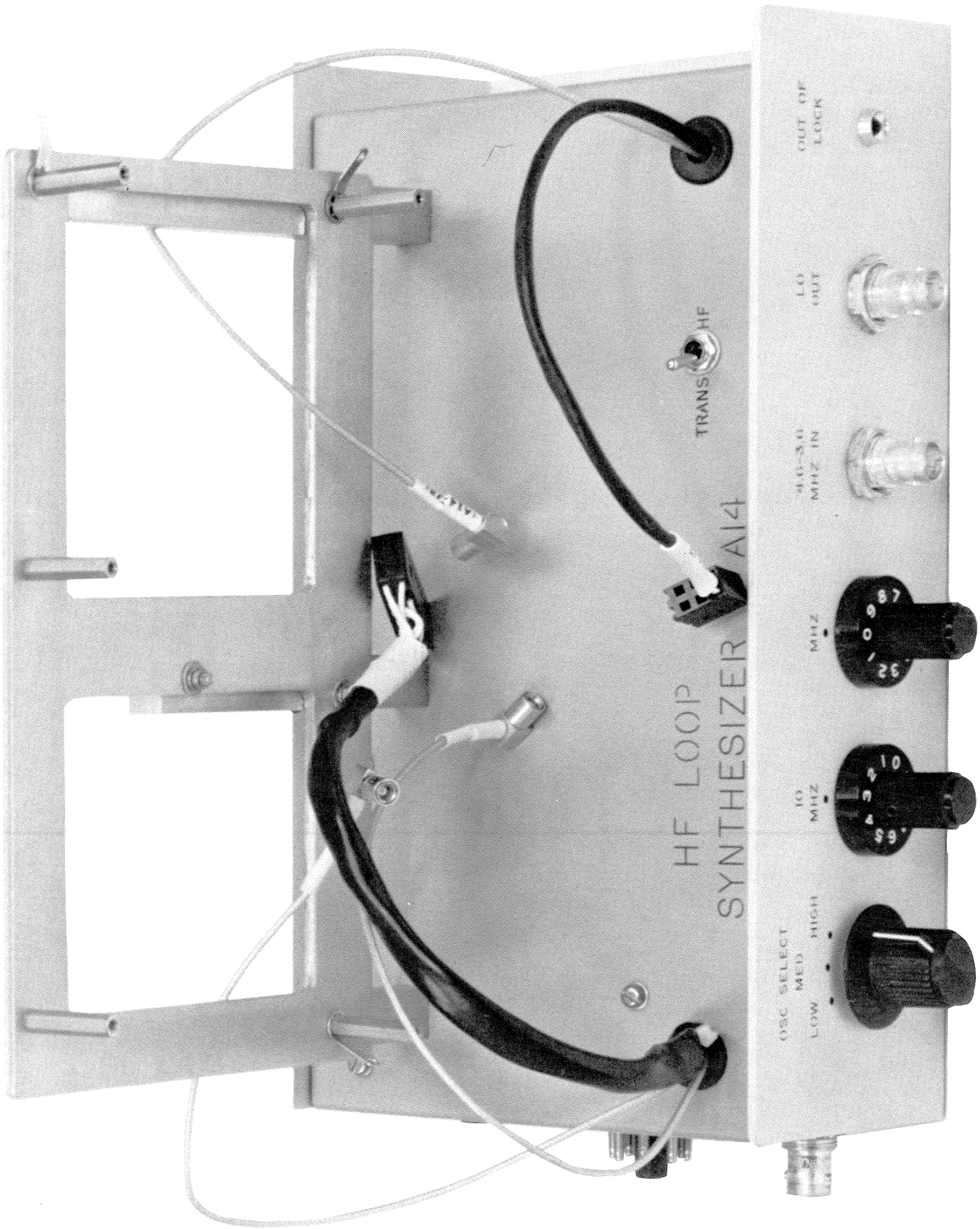


Figure 12-3. High Frequency Loop A14, Test Fixture

Table 12-4. Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	RF Voltmeter	Boonton 92BD
2	Spectrum Analyzer	Hewlett Packard 141T
3	Frequency Counter	Hewlett Packard 5327C
4	Synthesized Generator	Output, 0 dBm - 3.6 to 4.6 MHz
5	Digital Multimeter	Data Precision 248
6	DC Power Supply	Racal
7	Test Fixture A14	Racal
8	Adapter, 50 ohms	Boonton 91-8B
9	Unterminated Adapter	Boonton 91-6C
10	Tuning Tool	Micrometal RCI82007
11	AGC Adapter	

12.4 TEST AND ALIGNMENT

The following procedures are provided to properly test the A14 module. The tests should be performed at ambient room temperature. Record results on test data sheet, page 12-15.

12.4.1 Preliminary Set-Up Process

1. Place A14 board under test (B.U.T.) on test fixture, and make required connections. Ensure that power plugs are connected red-side-up.

2. Set the '10 MHz' and 'MHz' switches on test fixture to 2 and 9 positions respectively.

3. Set potentiometers R44 and R38 on B.U.T. to their mid positions.

4. Connect the frequency counter to TRANSFER OSCILLATOR OUT port on the left side of test fixture.

5. Connect the digital multimeter to VARACTOR CONTROL OUT jacks on the left side of test fixture. Set the multimeter scale suitable to read 8 VDC.

6. Set Synthesized Signal Generator for frequency of 3.6000 MHz and output amplitude of 0 dBm. Connect the RF output of signal generator to '4.6 - 3.6 MHz IN' port on test fixture.

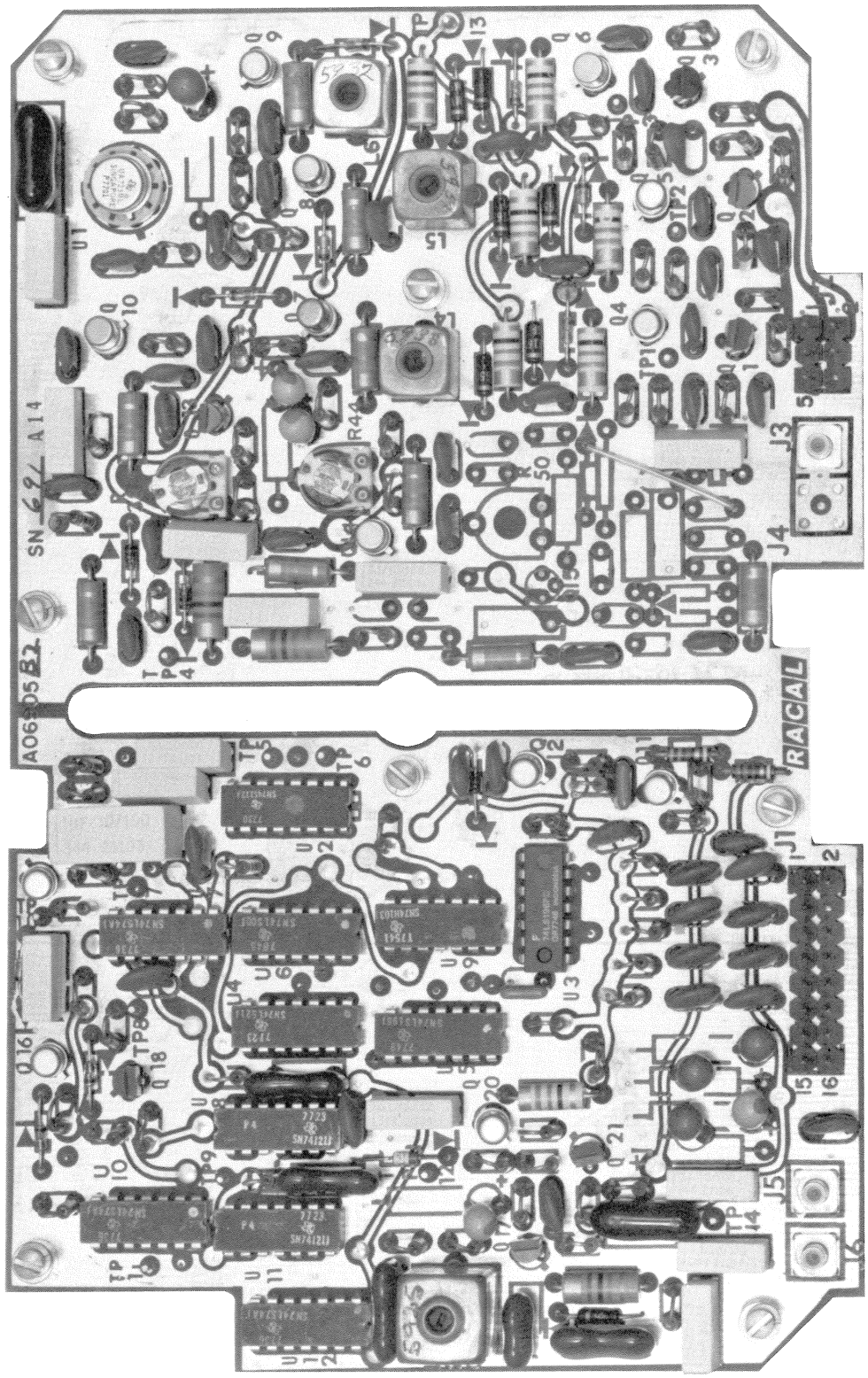


Figure 12-4A. High Frequency Loop A14, Overall Assembly

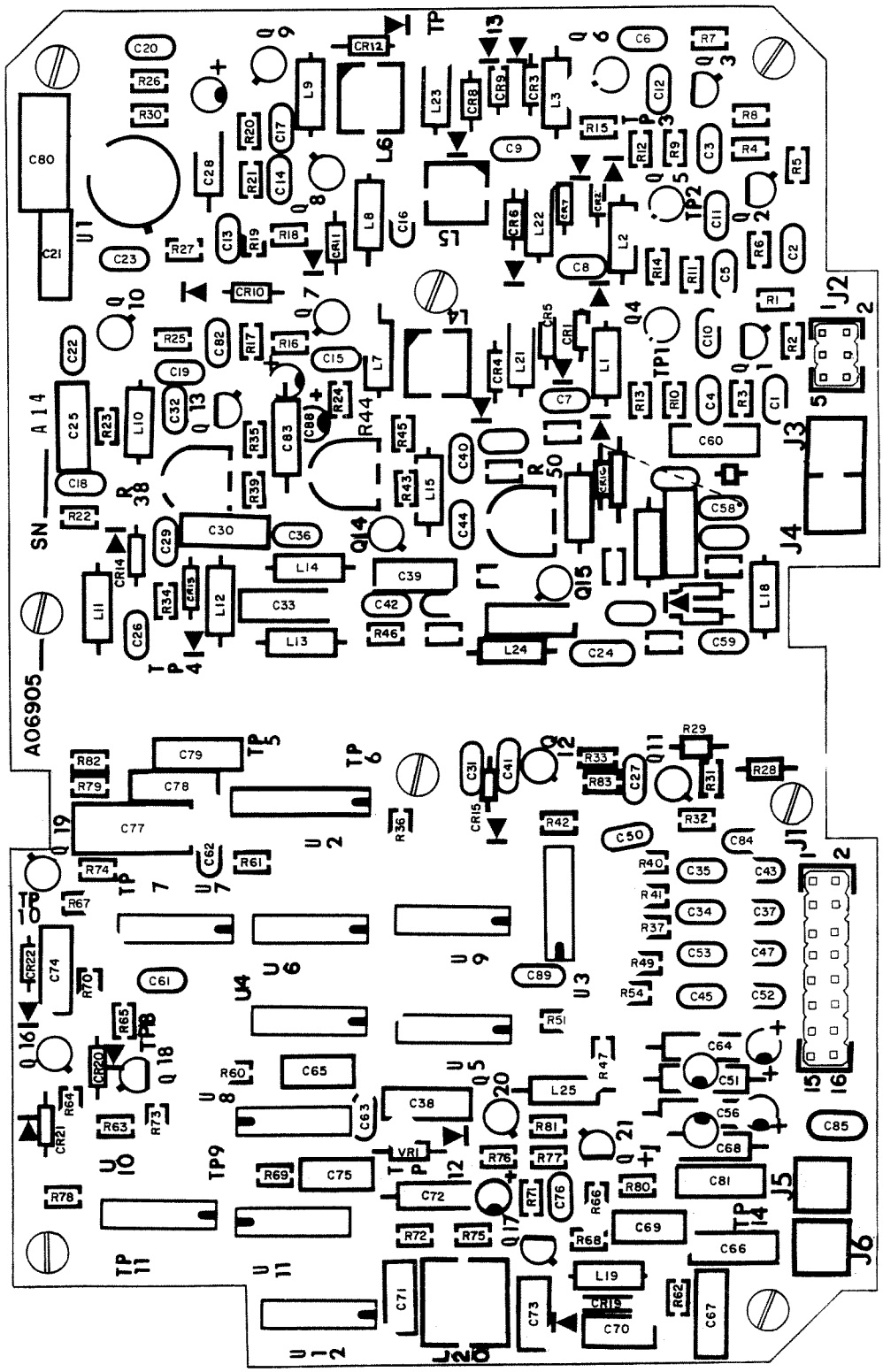


Figure 12-4B. High Frequency Loop A14, Circuit Card Assembly

7. Make remainder of test fixture settings as follows:

OSC SELECT	HIGH
TRANS - HF	TRANS

8. Turn power on to test fixture.

12.4.2 Transfer Oscillator Alignment Procedure

1. Adjust coil L20 on left hand edge of B.U.T. to obtain 8.0 ±0.5 VDC on digital multimeter. Ensure that OUT OF LOCK lamp of test fixture is out.

2. The frequency counter should read 947.85 ±0.1 kHz. Record on test data sheet.

3. Set Synthesized Signal Generator frequency to 4.0000 MHz with output amplitude of 0 dBm.

4. The frequency counter should read 942.029 kHz ±20 Hz. Record on test data sheet.

12.4.3 HF VCO Alignment Procedure

1. Set Synthesized Signal Generator to 3.6000 MHz with the output amplitude of 0 dBm.

2. Set the TRANS–HF switch on test fixture to HF position.

3. Connect the digital multimeter to TP13 on right hand side of B.U.T. with a suitable range to measure 14 VDC.

4. Adjust coil L6 on B.U.T. (at right hand side of board) to obtain a reading of 14.0 ±0.5 Volts on digital multimeter. Ensure the OUT OF LOCK lamp is out.

5. Set the 10 MHz, and MHz switches on test fixture to 1 and 7 positions respectively.

6. Set the OSC SELECT switch on test fixture to MED position.

7. Adjust coil L5 on B.U.T. to obtain reading of 14.0 ±0.5 Volts at TP13.

8. Set the 10 MHz and MHz switches on test fixture to 0 and 7 positions respectively.

9. Set the OSC SELECT switch on test fixture to LOW position.

10. Adjust L4 on B.U.T. to obtain 14.0 ±0.5 Volts at TP13. Ensure the OUT OF LOCK lamp is out.

12.4.4 AGC Level Adjustment and Check Procedure

1. Set the 10 MHz and MHz switches on test fixture to 0 and 0 positions respectively.

2. Using the unterminated adapter for RF Voltmeter, connect the RF Voltmeter to TP4 on B.U.T., via AGC adapter with its color-striped end connected to RF Voltmeter side.

   Note: Be sure to use shortest cable possible between the RF Voltmeter and probe tip to TP4.

3. Adjust potentiometer R38 on B.U.T. to obtain 35 mVolts on RF Voltmeter.

4. Slowly rotate the 10 MHz and MHz switches on test fixture through all positions, 00 through 29. When changing the MHz switches, place the OSC SELECT switch to its appropriate position as follows:

29 - 18	HIGH
17 - 08	MED
07 - 00	LOW

5. Ensure the RF output level is greater than 25 mVolts at each position. Should a reading be less than 25 mVolts, readjust R38 at that position to 25 mVolts, then recheck ALL positions again. Record on test data sheet.

12.4.5 Local Oscillator Output Level Adjustment Procedure

1. Set the 10 MHz and MHz switches on test fixture to 2 and 9 positions respectively.
2. Set the OSC SELECT switch to HIGH position.
3. Remove RF Voltmeter from TP4. Then using a 50 ohm terminated adapter, connect RF Voltmeter to LO OUTPUT port on test fixture.
4. Adjust potentiometer R44 on B.U.T. to obtain 225 ±10 mVolts.

12.4.6 HF VCO Frequency Accuracy Check Procedure

1. Remove the RF Voltmeter from LO OUTPUT port on test fixture and connect frequency counter to LO OUTPUT port.
2. Set Synthesized Signal Generator to give an output of 4.000 MHz.
3. Set the OSC SELECT switch on test fixture to LOW position.
4. Perform the requirements of Section A, Table 12-5. Record results.
5. Set the OSC SELECT switch to MED position.
6. Perform the requirements of Section B, Table 12-5. Record results.
7. Set the OSC SELECT switch to HIGH position.
8. Perform the requirements of Section C, Table 12-5. Record results.

Table 12-5. Frequency Check

Switch			Frequency (MHz)
10 MHz	MHz		±1.0 kHz
0	0		36.000
0	1		37.000
0	2		38.000
0	3	SECTION A	39.000
0	4		40.000
0	5		41.000
0	6		42.000
0	7		43.000
0	8		44.000
0	9		45.000
1	0		46.000
1	1		47.000
1	2	SECTION B	48.000
1	3		49.000
1	4		50.000
1	5		51.000
1	6		52.000
1	7		53.000
1	8		54.000
1	9		55.000
2	0		56.000
2	1		57.000
2	2		58.000
2	3	SECTION C	59.000
2	4		60.000
2	5		61.000
2	6		62.000
2	7		63.000
2	8		64.000
2	9		65.000

12.4.7 Noise Spectrum Analysis

1. Set the 10 MHz and 1 MHz switches to 0 and 0.
   Select LOW Oscillator
   Connect LO port via 50 ohms Coax to RF input of Spectrum Analyzer.

2. Set the Synthesized Signal Generator to give an output frequency of 3.6000 MHz.

3. Set the Spectrum Analyzer controls as follows:

Log Ref. Level	0 dBm
Input Attenuation	20 dB
Scan Width	0.1 kHz/div.

Bandwidth	0.01 kHz
Scan Time	2 Seconds
Video Filter	100 Hz
Center Frequency	36.4000 MHz

4. Adjust Reference Level on the Analyzer so that the displayed spectrum is referenced at the top of the display screen.

5. Ensure that the Basic Noise Level is less than –60 dB and that any Spurious Sidebands are less than –50 dB down on the reference level. Record results.

6. Set the 10 MHz and 1 MHz switches on the Test Fixture to 0 and 7. Reset Spectrum Analyzer Center Frequency to 43.4000 MHz.

7. Ensure that the Basic Noise Level is less than –55 dB and that any Spurious Sidebands are less than –50 dB down on the reference level. Record results.

8. Select the MED OSC and repeat step 7. Record results.

9. Set 10 MHz and 1 MHz switches on the Test Fixture to 1 and 7. Reset the Analyzer Center Frequency to 53,4000 MHz.

10. Ensure that the Basic Noise Level is less than –50 dB and that any Spurious Sidebands are less than –50 dB down on the Ref. Freq. Record results.

11. Select the HIGH OSC on the Test Fixture and repeat step 10. Record results.

12. Set 10 MHz and 1 MHz switches to 2 and 9. Reset the Analyzer Center Frequency to 65.4000. Repeat step 10. Record results.

12.4.8 Corrective Action

If any of the above tests, fail to produce the required results isolate the fault to a function (oscillator alignment, AGC level, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failure of specific frequency counts can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope or Voltmeters, to trace the fault to a single component. Maximum use, should also be made, of the test points provided on the A14 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductor and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 12.4.1 through 12.4.7.

12.5 PARTS LIST, HIGH FREQUENCY LOOP, A14

The parts list for the A14 circuit card is contained in Table 12-6.

DATE _____
CKD BY _____

MODULE A14
USED ON _____

TEST DATA SHEET

PART NAME: A14 HF Loop Synthesizer Board
PART NUMBER: 06905
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS MIN	LIMITS MAX	UNITS
	Transfer Oscillator Frequency				
12.4.2(2)	947.850 kHz		- 100	+100	Hz
12.4.2(4)	942.029 kHz		- 20	+20	Hz
12.4.4(5)	AGC Level Check		25	–	mV
12.4.6(4)	HF VCO Frequency Check		- 1	+1	kHz
12.4.6(6)	HF VCO Frequency Check		- 1	+1	kHz
12.4.6(8)	HF VCO Frequency Check		- 1	+1	kHz
12.4.7(5)	Noise Level 36.4 MHz		- 60		dB
	Spurious Sideband		- 50		dB
12.4.7(7)	Noise Level 43.4 MHz		- 55		dB
	Sidebands		- 50		dB
12.4.7(8)	Noise Level 43.4 MHz		- 55		dB
	Sidebands		- 50		dB
12.4.7(10)	Noise Level 53.4 MHz		- 50		dB
	Sidebands		- 50		dB
12.4.7(11)	Noise Level 53.4 MHz		- 50		dB
	Sidebands		- 50		dB
12.4.7(12)	Noise Level 65.4 MHz		- 50		dB
	Sidebands		- 50		dB

TABLE 12-6. PARTS LIST, HF LOOP CIRCUIT CARD ASSEMBLY (A14) 06905

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-6, 10-19, 22, 24, 26, 31, 32, 36, 40-42, 44, 50, 59, 82, 84	Capacitor, Ceramic, 0.001 uF, ±20% (Erie)	21747	831-000-X5T-102M
C7-9, 23, 29, 62	Capacitor, Ceramic, 100 pF, ±10% (Erie)	21327	831-000-S3B0-101K
C20, 85	Capacitor, Ceramic, 0.01 uF, +80% −20% (Erie)	21740	805-000-25V0-103Z
C21, 25, 30, 33, 38, 39, 60, 66, 67, 74, 78, 79, 81	Capacitor, Polycarbonate, 0.1 uF, ±20%, 100V (M/E	26871	C280MCF/A100K
C27, 89	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
C28, 51, 64, 68	Capacitor, Tantalum, 6.8 uF, ±20%, 35V (UC)	25032	T368B685M035AS
C34, 35, 37, 43, 45, 47, 52, 53, 61, 63, 76	Capacitor, Ceramic, 0.033 uF, +80% −20% (Erie)	21744	5705-000-X5F-333M
C46, 48, 49, 54, 55, 57, 58, 86, 87	Not Used		
C56, 72, 83, 88	Capacitor, Tantalum, 33 uF, ±10%, 10V (UC)	25019	T368B336K010AS
C65, 70, 71, 75	Capacitor, Mica, 1000 pF, ±2%	22110	CM06F102G03
C69, 80	Capacitor, Mica, 3300 pF, ±2%	22145	CM06FD332G03
C73	Capacitor, Mica, 82 pF, ±2%	22108	CM05E820G03
C77	Capacitor, Polycarbonate, 1.0 uF, ±20%, 100V(M/E)	26875	C280MCF/A1M
CR1-3, 10-12, 20-22	Diode	35514	1N916
CR4-9, 19	Diode (Motorola)	29006	MV1650
CR13-15	Diode (HP)	36003	5082-2800
CR16-18	Not Used		
L1-3, 21-23, 25	Choke, 15 uH, RF	43030	MS14046-6
L4	Coil, Variable, RF	05938	
L5	Coil, Variable, RF	05939	
L6	Coil, Variable, RF	05932	
L7-11, 14, 15, 18, 24	Choke, 4.7 uH, RF	43026	MS18130-16
L12, 13, 19	Choke, 1000 uH, RF	43038	MS90539-15
L16, 17	Not Used		
L20	Coil, Variable, RF	05925	
Q1-3, 18	Transistor	31508	2N4126
Q4-6	Transistor	32511	2N3823
Q7-9, 11, 12, 16, 19, 20	Transistor	32255	2N2369A
Q10, 14	Transistor	31500	2N918
Q13, 21	Transistor	32021	2N5089
Q15	Not Used		
Q17	Transistor	31265	2N6426
R1, 4, 7, 34	Resistor, Composition, 100K Ohms, ±5%, 1/4W	10711	RC07GF104J
R2, 5, 8	Resistor, Composition, 47K Ohms, ±5%, 1/4W	10703	RC07GF473J
R3, 6, 9, 72	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R10-12, 16, 18, 20, 23, 28, 35, 66	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R13-15, 17, 19, 21, 43, 64, 73, 79	Resistor, Composition, 680 Ohms, ±5%, 1/4W	10659	RC07GF681J
R22, 36, 71	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R24, 45	Resistor, Composition, 390 Ohms, ±5%, 1/4W	10653	RC07GF391J
R25, 46, 68	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J

TABLE 12-6. PARTS LIST, HF LOOP CIRCUIT CARD ASSEMBLY (A14) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R26, 27, 30	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R29	Resistor, Composition, 330 Ohms, ±5%, 1/4W	10651	RC07GF331J
R31	Resistor, Composition, 150 Ohms, ±5%, 1/4W	10643	RC07GF151J
R32, 63, 78	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R33	Resistor, Film, 180 Ohms, 2%, ¼W	12161-181	RL07S181G
R37, 40-42, 47, 49, 51, 54, 82	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J
R38	Resistor, Variable, 10K Ohms (Bourns)	16074	3359P-1-103
R39, 75	Resistor, Composition, 1.5K Ohms, ±5%, 1/4W	10667	RC07GF152J
R44	Resistor, Variable, 1K Ohms (Bourns)	16072	3359P-1-102
R48, 50, 52, 53, 55, 56, 57, 58, 59	Not Used		
R60, 65, 69, 74, 77	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R61	Resistor, Composition, 47 Ohms, ±5%, 1/4W	10631	RC07GF470J
R62, 67, 76	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	10675	RC07GF332J
R70	Resistor, Composition, 18K Ohms, ±5%, 1/4W	10693	RC07GF183J
R80, 81	Resistor, Composition, 56 Ohms, ±5%, 1/4W	10633	RC07GF560J
R83	Resistor, Composition, 27 Ohms, ±5%, 1/4W	10625	RC07GF270J
U1	Integrated Circuit (Fairchild)	36515	uA723HC
U2	Integrated Circuit (Fairchild)	36537	74S112J
U3	Integrated Circuit (Fairchild) (only)	36825	74LS2196
U5	Integrated Circuit (Fairchild)	36621	74LS196J
U4	Integrated Circuit (Fairchild)	36643	74LS21J
U6	Integrated Circuit (Fairchild)	36632	74LS00J
U7, 10, 12	Integrated Circuit (Fairchild)	36636	74LS74J
U8, 11	Integrated Circuit (Fairchild)	36530	74121DC
U9	Integrated Circuit (Fairchild)	36535	74H103DC
VR1	Diode, Zener, 4.7V, ±5%	33542	1N750A
–	Printed Wiring Board	06728	
J1	Connector	06846-8	
J2	Connector	06846-3	
J4	Not Used		
J3, 5, 6	Connector (Cable Wave)	60044	700209
–	Pad, Transistor	70760	
–	Pad, IC	70768	

CHAPTER 13
FREQUENCY STANDARD, A15

13.1 THEORY OF OPERATION

This chapter provides information on the Frequency Standard Module A15; however, this module is only a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A15 module within the synthesizer section. Figure 10-1 in chapter 10 shows a simplified functional block diagram of the complete section, and paragraph 10.1 describes the overall synthesizer operation.

13.1.1 Frequency Standard, A15

This module generates the 5 MHz frequency reference standard. It is a temperature-controlled AT-cut crystal oscillator with a single adjustable trimmer to set the frequency precisely to 5 MHz. Provisions exist in the receiver for use of external frequency standards. The oscillator is housed in a proportionally controlled oven which maintains the crystal at its optimum operating temperature. The schematic diagram for A15 is shown in Figure 13-1. Oscillator output is at J4.

13.2 FREQUENCY STANDARD MODULE A15, TESTING AND TROUBLESHOOTING

The testing and troubleshooting procedures for Frequency Standard Module A15 are designed to check the internal frequency standard of the module. The internal frequency standard is checked with an external 20 VDC connected to the input of the module and then monitoring its output with a spectrum analyzer. A continuity check of the circuits of the internal frequency standard is also provided to aid in isolating specific problems. After a problem has been isolated and corrected the output of that function should then be rechecked, as outlined in the Procedures, before installing the unit into the Receiver. Figure 13-2 shows a suggested test set-up for the Frequency Standard Module. Figure 13-3A shows a top view of the module while Figure 13-3B shows the botton view. These illustrations along with the Schematic Diagram shown in Figure 13-1 should be referred to while testing and troubleshooting the unit.

13.3 TEST EQUIPMENT AND ACCESSORIES

To perform testing and troubleshooting using the test fixture, requires the use of a power supply, test equipment and accessories. This additional equipment is used to inject signals, provide power, monitor signals and their levels, make connections and to signal trace. The test equipment and accessories required are listed in Table 13-1.

13.4 TEST PROCEDURE

The following procedures are provided to properly test the A15 module. All tests should be performed at ambient room temperature. Record results on test data sheet, page 13-9.

Table 13-1. Test Equipment And Accessories

ITEM	DESCRIPTION	EQUIPMENT RECOMMENDED OR EQUAL
1.	Spectrum Analyzer	Marconi TF 2370 or Hewlet Packard 8552B or 8553B
2.	Frequency Counter	HP5245L
3.	Multimeter	Simpson 260
4.	HF Voltmeter	Boonton 91H
5.	DC Power Supply	Racal
6.	Adapter, 50 ohms	Boonton 91-8B

13.4.1 Frequency Standard Performance

1. Connect the Frequency Standard Module to DC power as shown in Figure 13-2.

2. Connect the standard output, of J4 on the module, to the R.F. input on the spectrum analyzer, through a 50 ohm cable as shown in Figure 13-2.

3. Tune the spectrum analyzer to 5.0 MHz center frequency.

4. Frequency Standard output shall be between 0 and 5 dBm. Record results.

5. Disconnect spectrum analyzer and connect frequency counter. Counter should read 5 000 000 ±1 count.

6. Disconnect the DC power and frequency counter.

13.4.2 Continuity Check of Internal Standard Socket

1. Connect the Simpson volt-Ohm meter, using a RX 1 position to pin 4 (measured CCW from the index on the octal socket) of the internal standard on the A15 module. Connect the other probe to pin 7 of the DC POWER IN port of the test fixture. Record on test data sheet.

2. Connect the probes of the simpson VOM to pin 1 of the internal standard octal socket and the other probe to the INTERNAL STANDARD OUT BNC center pin. There should be continuity. Record on test data sheet.

3. Check for continuity between pins 2, 3, and 5 of the octal socket and chassis ground, Record.

4. Remove all connections and the module under test from test fixture.

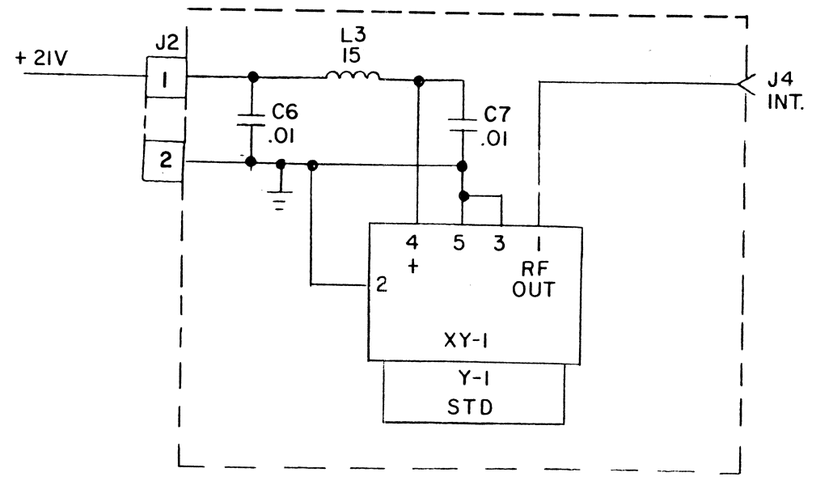


Figure 13-1. Schematic Diagram, Frequency Standard, A15

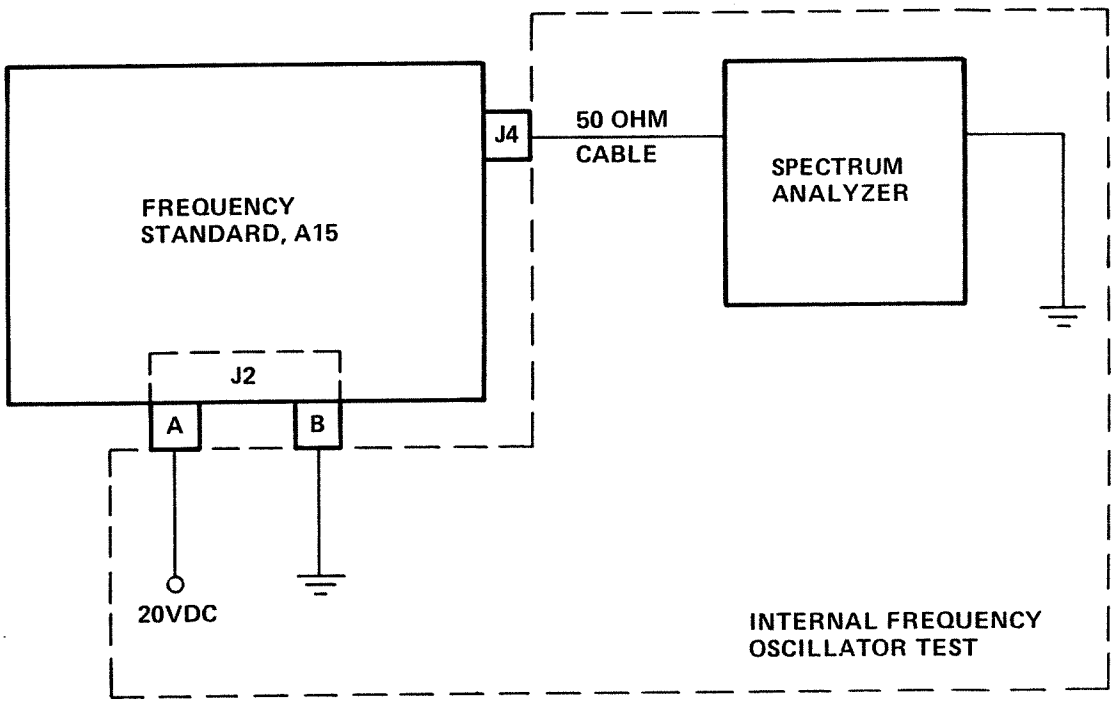


Figure 13-2. Frequency Standard A15, Test Set-Up Diagram

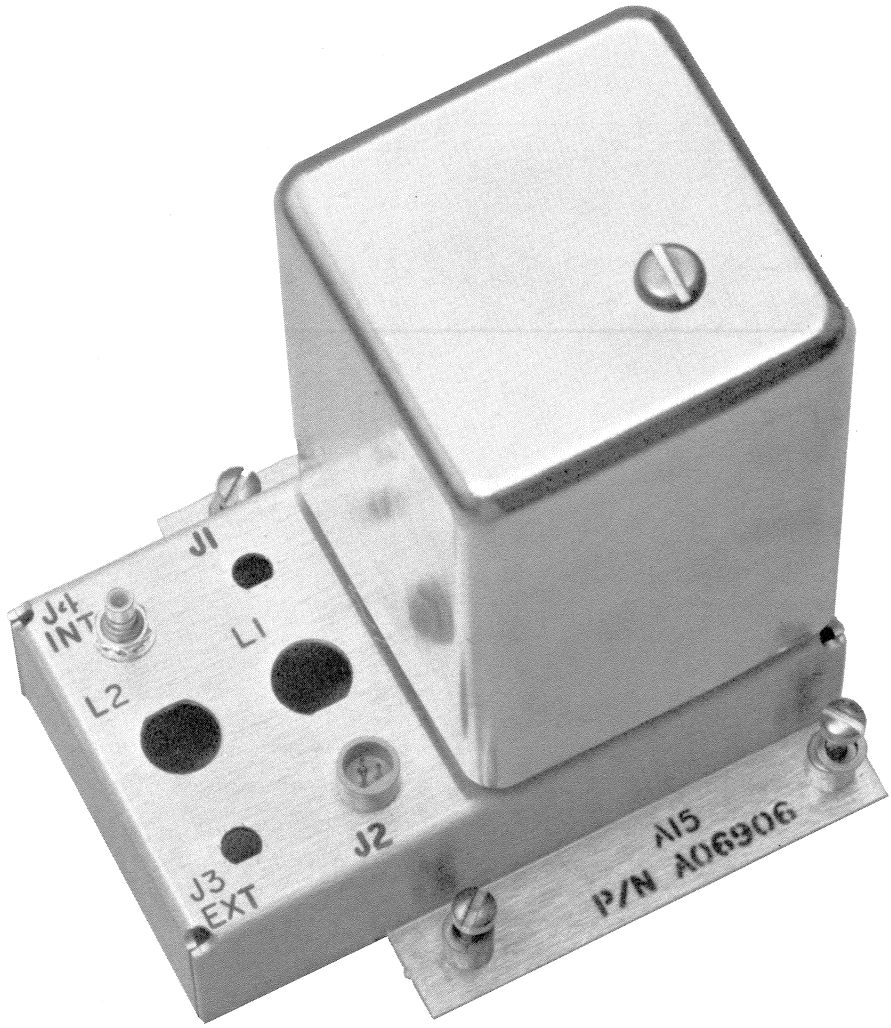


Figure 13-3A. Frequency Standard A15, Top View

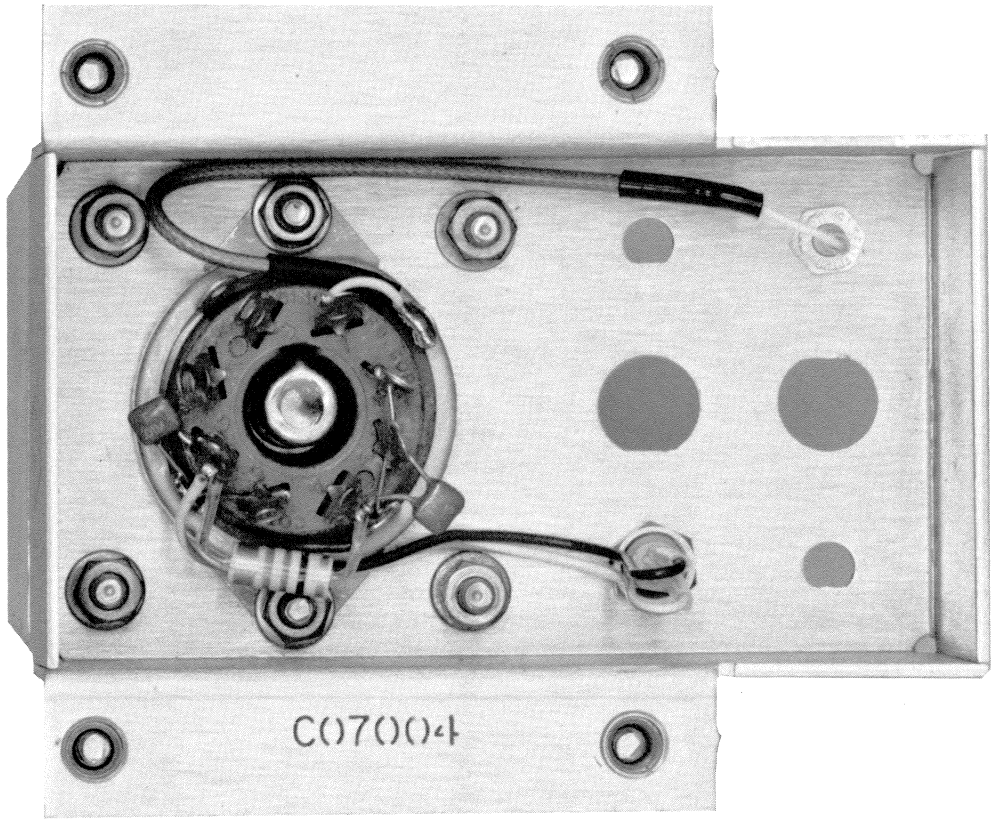


Figure 13-3B. Frequency Standard A15, Bottom View

13.4.3 Corrective Action

If any of the above tests fail to produce the required results, isolate the fault to a function (frequency output or continuity) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function; for instance, step 1 in Paragraph 14.4.2 isolates the fault to L1 and associated wiring. Further signal tracing may then be accomplished using the oscilloscope or voltmeters to trace the fault to a single component.

When replacing faulty components, care should always be taken, so that the new component or adjacent components, are not damaged. Heat sinks should be used on sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to adjacent components as well as to the new component being installed.

After any component has been replaced, procedures for that function must be checked as outlined in Paragraphs 13.4.1 and 13.4.2.

13.5 PARTS LIST, FREQUENCY STANDARD, A15

The parts list for the A15 module is contained in Table 13-2.

DATE _____
CKD BY _____

MODULE A15
USED ON _____

TEST DATA SHEET

PART NAME: A15 Frequency Standard
PART NUMBER: 06906
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
13.4.1(4)	Standard Output Power Level		0	+5	dBm
13.4.2(1)	Continuity Check (pin 4 – pin 7)		Pass	Fail	
13.4.2(2)	Continuity Check (pin 1 – Int. STD)		Pass	Fail	
13.4.2(3)	Continuity Checks				
	pin 2 – Chassis GND		Pass	Fail	
	pin 3 – Chassis GND		Pass	Fail	
	pin 5 – Chassis GND		Pass	Fail	

TABLE 13-2. PARTS LIST, FREQUENCY STANDARD MODULE ASSEMBLY (A15) 06906-4

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-5	Not used		
C6, 7	Capacitor, Ceramic, .01 uF, ±20% (Erie)	21733	8121-050-651-103M
J2	Connector, Male 3-Contact (Winchester)	61163	SM3PMN
J4	Connector, Coaxial(Sealectro)	60058	051-043-0000
L1, 2	Not Used		
L3	Coil, RF Choke, 15 mH	43030	MS14046-6
XY1	Connector, Octal (Cinch)	70619	8EM
	Mounting Bracket	07004	
Y1	Temperature Controlled Crystal Oscillator Assembly 5 MHz	09221	

CHAPTER 14
34 MHz GENERATOR, A16

14.1 THEORY OF OPERATION

This chapter provides information on the 34 MHz board A16, however, this circuit board is only a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A16 module within the synthesizer section. Figure 10-1 in Chapter 10 shows a simplified functional block diagram of the complete section, and paragraph 10.1 describes the overall operation of the synthesizer.

14.1.1 34 MHz Generator, A16

This board contains the 34 MHz VCO and a divide-by-five circuit to produce a 1 MHz reference frequency from the 5 MHz frequency standard. The board also provides 1 MHz to the BFO synthesizer, which is used to produce a variable frequency. This frequency is used by A16 to produce 1.4 MHz plus the BFO offset. The 34 MHz output is the injection frequency for the second mixer. The 1 MHz reference is applied to the frequency synthesizer boards, A11 and A13, and the 1.4 MHz output is applied to the product detector. The block diagram is shown in Figure 14-1 and the schematic diagram in Figure 14-2.

14.1.1.1 34 MHz Oscillator

The 34 MHz oscillator consists of transistors Q6 and Q7, and the frequency-determining components L2, C12 and CR1. A 12 volt supply for the oscillator is regulated by transistor Q1 and zener diode VR1. The oscillator frequency from the base of Q6 is applied to a buffer amplifier, Q3 and Q5, and then to balanced amplifier Q11/Q12 which provides the 34 MHz output to the second mixer through transformer T1.

14.1.1.2 Divide-by-34 Stage

A second output from the 34 MHz oscillator is buffered by NAND gate U2A before being applied to a divide-by-34 stage. This consists of a dual J-K flip-flop, U3; a divide-by-ten divider, U4; and NAND gates, U2B and U2C. The buffered 34 MHz output from the U2A is applied to the clock input of U4. The 1 MHz output is taken from pin 2 of U4 to be applied to the phase comparator, U6. The divide-by-34 operation is accomplished through the additional gating performed by gate U2, and the dual flip-flops U3A and U3B.

14.1.1.3 1 MHz Divider

The output from the 5 MHz frequency standard, A15 connected to A16 through connector J1, is applied to a buffer amplifier, Q2, and then to a shaper stage, Q4. The squarewave output from Q4 is applied to a divide-by-five stage, U1, which outputs a 1 MHz square wave. The 1 MHz squarewave

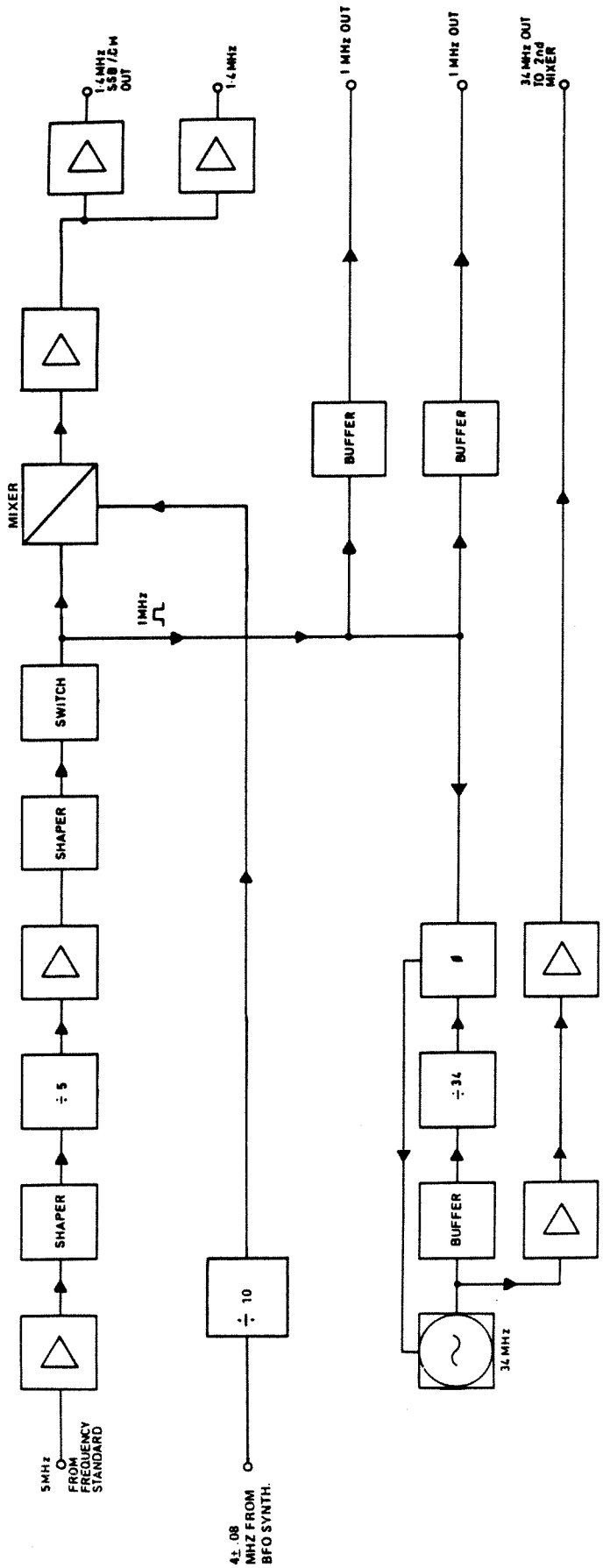


Figure 14-1. Block Diagram, 34 MHz Generator Board, A16

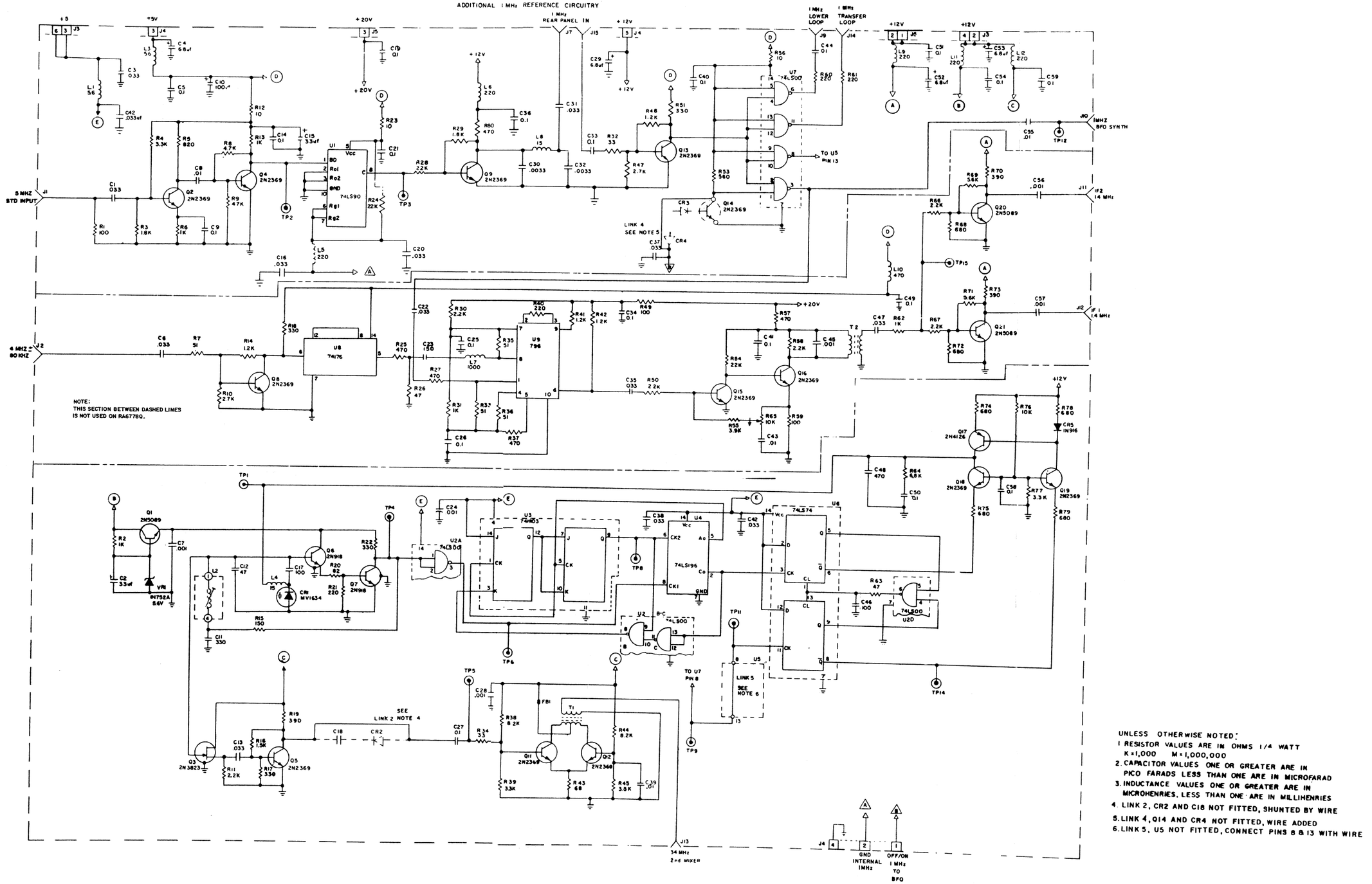


Figure 14-2. Schematic Diagram, 34 MHz Generator, A16

output from Q13 is applied to U7, which consists of four NAND gate buffers. The output from U7A, at pin 6, is taken to the lower-loop synthesizer via J9. The output from U7B, at pin 11, is taken to the transfer loop via connector J14, and the output from U7C, at pin 8, is taken to a phase comparator, U5. U7D is used as part of the 1.4 MHz carrier re-insertion generation and BFO offset circuit, as described in paragraph 14.1.1.5.

14.1.1.4 Phase Comparator

The output signal from the 34 MHz oscillator is divided to provide a frequency of 1 MHz when the oscillator frequency is correct. This frequency is compared with a reference 1 MHz frequency. Any error between the two frequencies is used to develop a dc voltage which adjusts the oscillator frequency to eliminate the error. This voltage is generated in the phase comparator, and is applied to 34 MHz oscillator varactor diode, CR1, via L4.

The phase comparator consists of a dual D-type flip-flop, U6; a two-input gate, U2D; and an output voltage control circuit, Q17, Q18, Q19. The action of the circuit is described in paragraph 10.1.1.4 in Chapter 10.

14.1.1.5 1.4 MHz Generation and BFO Offset

The 1.4 MHz plus and minus the BFO offset, required for the IF board, A5, is derived from a 4 MHz ±80 kHz signal (in 10 Hz increments) received from the BFO synthesizer board, A23. The 4 MHz is divided by 10, then mixed with 1 MHz from U7D to produce 1.4 MHz ±8 kHz in 10 Hz increments.

The 4 MHz ±80 kHz is received at board pin J2, then amplified by Q8 to drive the input to decade divider U8, at TTL levels (+5 V). At the input, C6 blocks DC and R7 provides impedance matching. The amplified signal is then received at U8, pin 6. The output from U8, centered at 0.4 MHz, is voltage-divided by R25 and R26, and applied via C23 and L7 to mixer U9. The other input to the mixer is 1 MHz received from U7D through C22. The mixer output, now centered at 1.4 MHz, is applied to amplifier Q15 and Q16 via C35 and R50. Variable resistor R65 adjusts the amplitude of the 1.4 MHz-centered waveform. The signal is transformer-coupled by T2 to the two output amplifiers, Q20 and Q21. The output at board pin J12 is used by the IF board, A5, to detect the upper and lower sidebands or CW receiver input signals.

14.2 34 MHz GENERATOR A16, TEST FIXTURE

Troubleshooting and alignment of the 34 MHz Generator module A16 is accomplished through the use of the Racal 34 MHz Generator A16 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A16 module for testing, while also providing easy access to the printed circuit board for troubleshooting. The front apron of the test fixture contains a switch for control of the BFO Synthesizer. Connectors are provided on the rear apron to connect the PC board under test to external test equipment. A 5 MHz oscillator is contained within the test fixture as a convenient reference for the module under test. Figure 14-3 shows the A16 test fixture. Figure 14-4A shows the overall assembly of the A16 module while Figure 14-4B shows the circuit card assembly.

14.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required are listed in Table 14 -1.

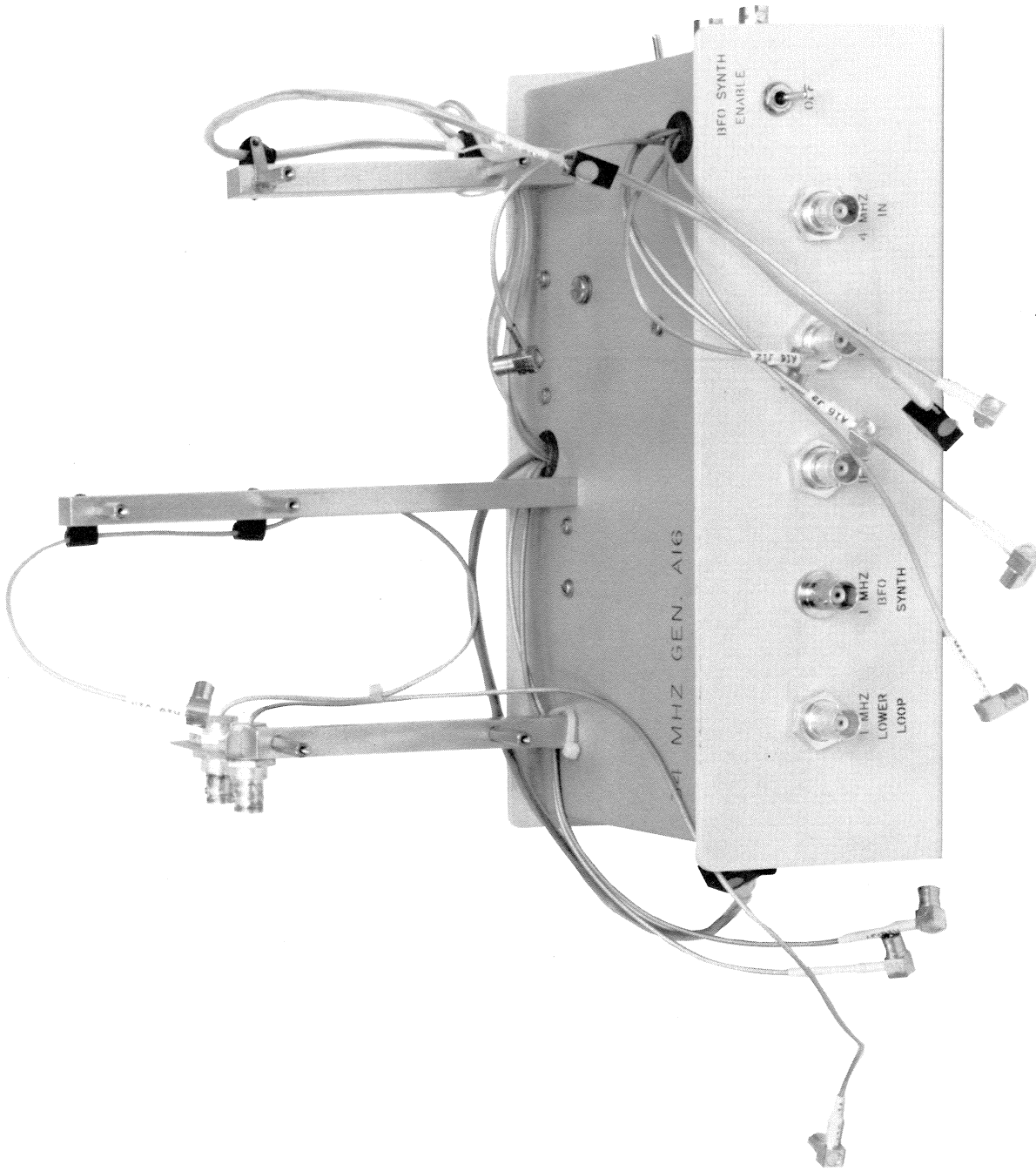


Figure 14-3. 34 MHz Generator A16, Test Fixture

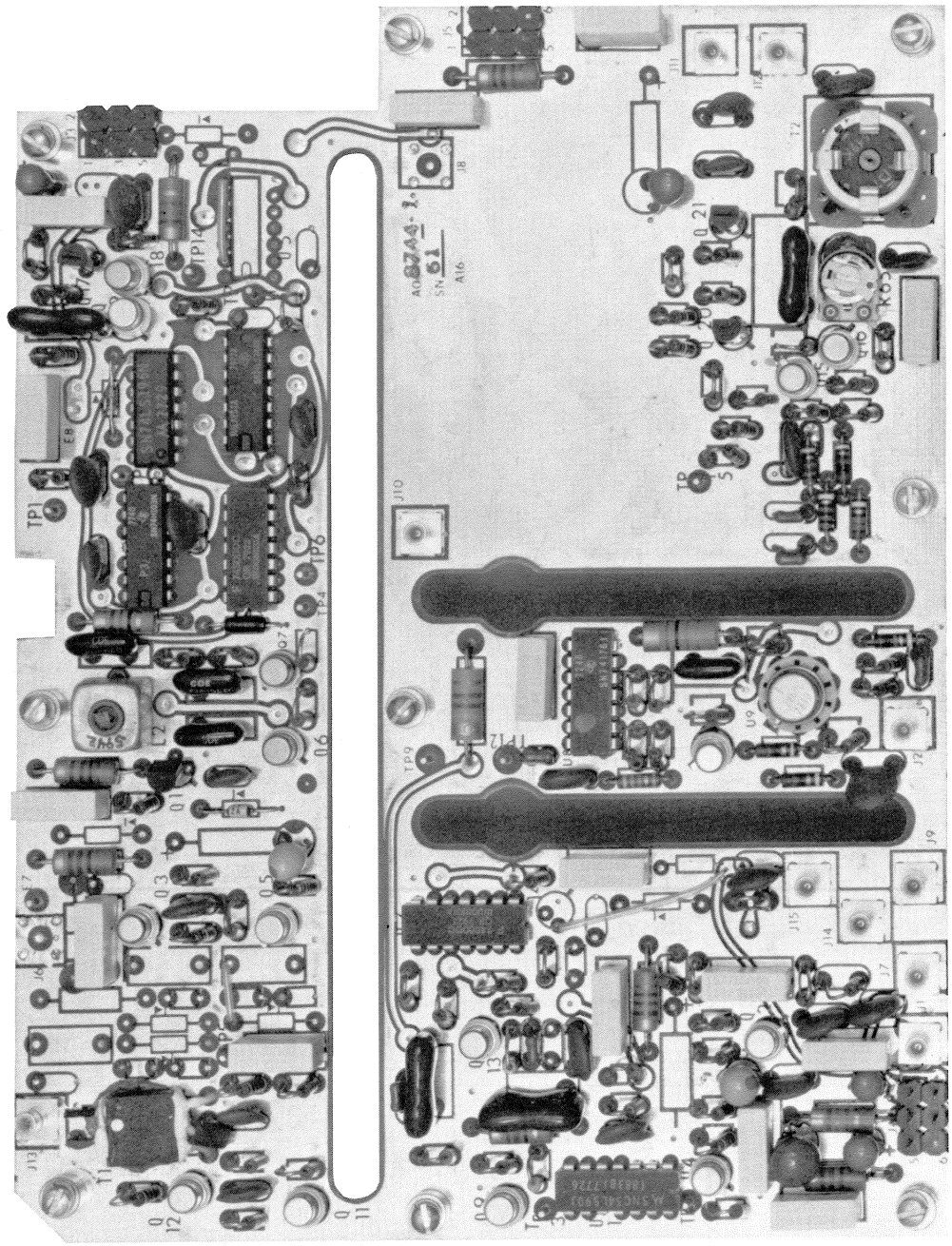


Figure 14-4A. 34 MHz Generator A16, Overall Assembly

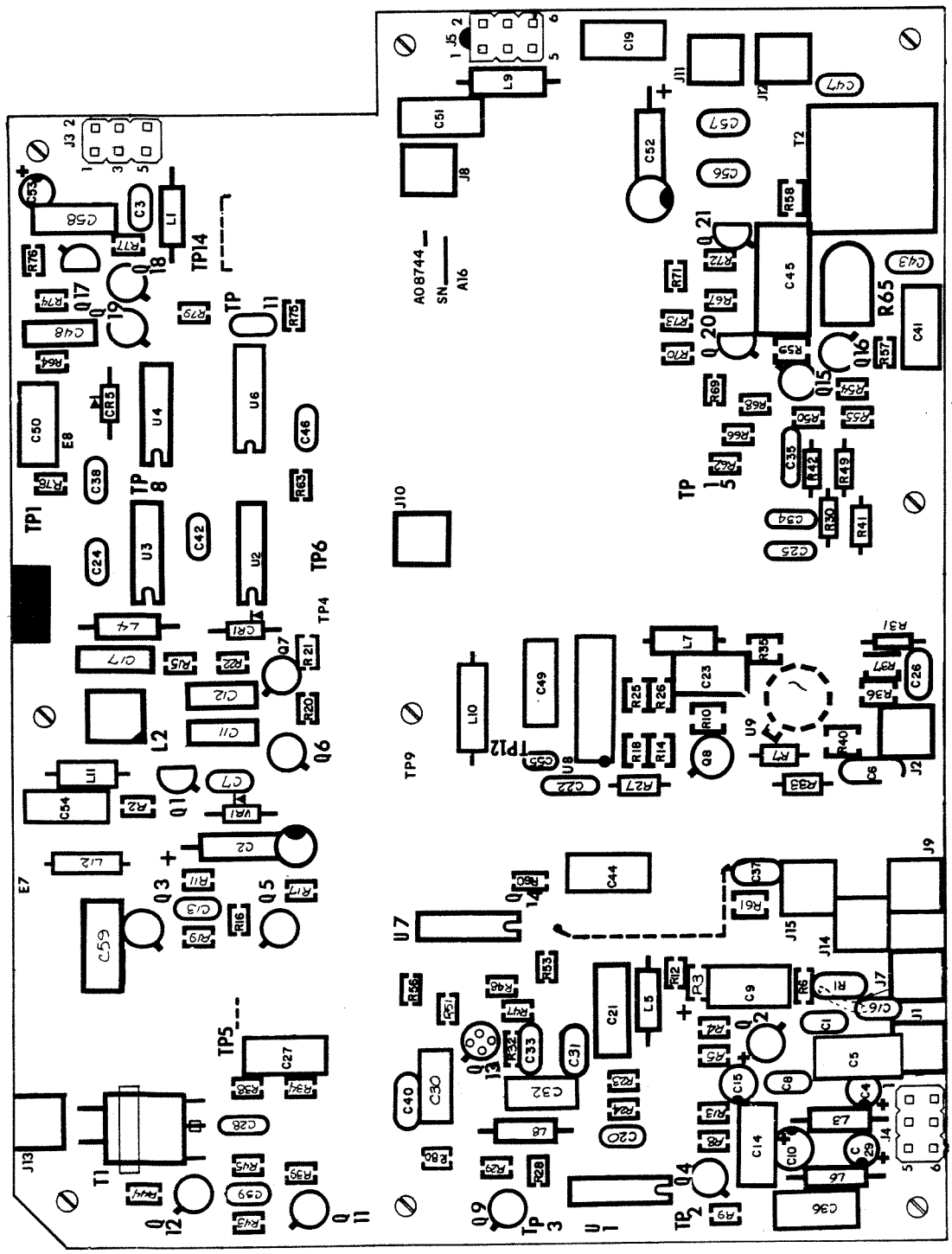


Figure 14-4B. 34 MHz Generator A16, Circuit Card Assembly

Table 14-1. Test Equipment and Accessories

Item	Description	Recommended Instrument or Equal
1	Digital Multimeter	Fluke 8000A
2	Spectrum Analyzer	Marconi TF2370 or HP141T, 8552B, 8553B with Tracking Generator 8443A
3	Frequency Counter	Dana 8030B
4	RF Signal Generator	Logmetrics 921
5	Oscilloscope	Tektronix 465
6	DC Power Supply	Racal
7	A16 Test Fixture	Racal
8	Tuning Tool	Micrometals RCI82007
9	BNC Coax Connectors	As required.

14.4 TEST AND ALIGNMENT

The following procedures are provided to properly test the A16 module. All test data should be performed at ambient room temperature. Record results on test data sheet, page 14-13.

14.4.1 1 MHz Output Test

1. Install the 34 MHz Generator board A16 to be tested on the test fixture.
2. Make all connections between the A16 board and the test fixture. Be sure that the red sides of plugs J3, J4, and J5 are faced up.
3. Connect power plug from power supply to left side of test fixture. Turn test fixture power on.
4. Set oscilloscope settings at 1 volt/cm and 1 usec/cm.
5. Set the BFO SYNTH ENABLE switch on test fixture to ENABLE position.
6. Set "Internal-External" reference switch to "Internal".
7. Connect oscilloscope probe to TP3 on B.U.T. Ensure that frequency of the waveform is 1 MHz with an output amplitude not less than 2 volts peak-to-peak (one cycle of waveform per division horizontally and more than two divisions vertically). Record on test data sheet.

8. With a BNC coax cable, connect oscilloscope and 1 MHz LOWER LOOP OUTPUT port on test fixture. Ensure that the amplitude is not less than 2 volts peak-to-peak. Record.

9. Connect oscilloscope to 1 MHz TRANSFER LOOP OUTPUT port on left side of test fixture. Ensure that the ampltiude is not less than 2 volts peak-to-peak. Record results.

10. Connect the frequency counter to the 1 MHz TRANSFER LOOP OUTPUT port on test fixture and ensure the frequency is 1 MHz ±10 Hz. Record results.

11. Connect oscilloscope to 1 MHz BFO SYNTH OUTPUT port on test fixture and ensure the amplitude of the waveform is not less than 2 volts peak-to-peak. Record results.

12. Connect oscilloscope probe to TP9 on B.U.T. and ensure that the waveform amplitude in not less than 2 volts peak-to-peak. Record results.

14.4.2 BFO Frequency and 1.4 MHz Output Test

1. Connect the frequency counter to the TP2 on the left-hand side of the B.U.T. and ensure that the frequency is 5 MHz ±10 Hz. Record results.

   Note: If not within these limits, carefully adjust the trimmer on the internal standard located inside the test fixture through the access hole nearest the right support post for the board.

2. Tune Signal Generator to approximately 4 MHz with output level of 220 mVolts. Connect the Signal Generator to 4 MHz port on test fixture via BNC coax cable.

3. Connect frequency counter to IF 1 port on test fixture and carefully adjust frequency of signal generator to obtain 1.4 MHz ±10 Hz on frequency counter. Note frequency.

4. Connect oscilloscope to IF 2 port on the test fixture. Tune transformer T2 on lower right-hand corner of B.U.T. for a maximum level as observed on the oscilloscope.

5. Adjust potentiometer R65 (right next to T2) on B.U.T. until the waveform amplitude on oscilloscope is 800 mVolts peak-to-peak.

6. Set Signal Generator on cal x 100 resolution. Record results. Adjust the Signal Generator frequency to 4.0800 MHz.

7. The frequency counter should now read approximately 8 kHz higher than the noted frequency in step 3. Record results.

8. Adjust the Signal Generator frequency to 3.9200 MHz.

9. The frequency counter should now read approximately 8 kHz lower than the noted frequency in step 3. Record results.

10. The oscilloscope connected to IF 2 OUT test fixture should read an amplitude not less than 500 mVolts peak-to-peak. Set BFO SYNTH switch to OFF position and ensure that the output goes to 0. Record results. Set BFO SYNTH switch back on.

11. Remove frequency counter connection from IF 1 OUTPUT port and connect oscilloscope to IF 1 OUTPUT port. Oscilloscope should read at least 500 mVolts peak-to-peak. Record results.
12. Disconnect oscilloscope, signal generator and frequency counter from the test fixture.

14.4.3 34 MHz Output Test

1. Set the digital multimeter to read a DC voltage of 6 volts.

2. Connect the digital multimeter to TP1 on B.U.T. and frequency counter to 34 MHz MIXER OUTPUT port on the left-hand side of test fixture.

3. Connect the 1 MHz TRANSFER LOOP port on test fixture to EXTERNAL STANDARD input at the rear of the frequency counter. Set the frequency counter function mode to EXT. STANDARD.

4. Slowly adjust coil L2 located on Upper side of B.U.T. until 6.00 ±.5 V on multimeter and 34,000,000 MHz ±1 Hz on frequency counter readings are obtained. Record results.

5. Disconnect the counter and connect a 50 ohm load and T connector to oscilloscope input. Connect the oscilloscope to the 34 MHz MIXER OUT port via a short length of 50 ohm coax.

6. Ensure the output voltage is greater than 2 volts p-p and less than 3 volts p-p. Record results and disconnect the oscilloscope from the test fixture.

14.4.4 34 MHz Spectrum Analysis Noise and Spurious Response Check

1. Connect the Spectrum Analyzer using a 50 ohm coaxial cable to the 34 MHz MIXER OUT port on test fixture.

2. Set the controls on the spectrum analyzer as follows:

Ref. Freq.	Center
Counter Freq.	Bright Line
Sweep Mode	Manual (Auto for H-Q)
Vertical Scale Range	10 dB/div
Store	A (Medium Persistance On 141T)
Display	A (Only A is pushed in)
Counter	On
Vertical Scale	+20 dB (on blue lighted scale)
Vertical Add	0 dB
Horizontal Scale	0.5
Range	MHz/div
Filter Bandwidth	Narrow
Sweep Speed	None selected
Graticule Controls	Calibrated position as required
Intensity	As required (Bright Marker for H-P)

3. Adjust the Bright Line for the center of the screen, then adjust the REFERENCE FREQUENCY controls for 34.000 MHz.

4. Select Auto Sweep, then adjust the Vertical Scale to locate the top of 34 MHz signal on the top datum line.

5. Ensure that any spurious responses are greater than −55 dBm down from the datum level. Record on test data sheet.

14.4.5 1 MHz External Standard Check

1. Connect the spectrum analyzer using a 50 ohm coaxial cable to the 1 MHz in/out port on the test fixture.

2. Check to see that 1 MHz signal at '-6' dBm minimum level, is present. Record results.

3. Change the setting of the 'Internal-External' reference switch to 'External.'

4. Check the '1 MHz Out' port to see that the internal 1 MHz signal is disabled. Record.

5. Connect an RF signal generator to the '1 MHz in/out' port on the test fixture. Adjust generator output to −10 dBm. Check to see that 34 MHz is available at the 'Mixer output' on the test fixture. Record on test data sheet.

14.4.6 Corrective Action

If any of the above tests, fail to produce the required results isolate the fault to a function (1 MHz, BFO output, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, failure of specific frequency counts can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope or Voltmeters, to trace the fault to a single component. Maximum use, should also be made, of the test points provided on the A16 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductor and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 14.4.1 through 14.4.5.

14.5 PARTS LIST, 34 MHz GENERATOR, A16

The parts list for the A16 circuit card is contained in Table 14-2.

DATE _____
CKD BY _____

MODULE A16
USED ON _____

TEST DATA SHEET

PART NAME: A16 34 MHz Generator Board
PART NUMBER: 06742
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
	1 MHz Output Test		Nominal		
14.4.1(7)	Amplitude		2.0		volt, P
14.4.1(8)	1 MHz Lower Loop Output		2.0		volt, P
14.4.1(9)	1 MHz Transfer Loop Output		2.0		volt, P
14.4.1(10)	1 MHz Output		-10	+10	Hz
14.4.1(11)	BFO Synthesizer Output		2.0		volt, P
14.4.1(12)	TP9 Output		2.0		volt, P
14.4.2(1)	TP2 Frequency 5,000,000 Hz		-10	+10	Hz
14.4.2(6)	Gen Frequency		Nominal		
14.4.2(7)	IF 1 Frequency +8 kHz		Nominal		
14.4.2(9)	IF 1 Frequency - 8 kHz		Nominal		
14.4.2(10)	IF 2 Output		500		mV, P-P
	BFO Disabled		No Output		
14.4.2(11)	IF 1 Output		500		mV, P-P
14.4.3(4)	34.0 MHz		-1	+1	Hz
14.4.3(6)	34 MHz Mixer Output		2	3	volt, P
14.4.4(5)	34 MHz Spectrum		-55		dBm
14.4.5(2)	1 MHz Reference Output		-6	+6	dBm
14.4.5(4)	1 MHz Output Disable		Pass	Fail	
14.4.5(5)	34 MHz Output Operational		Pass	Fail	

TABLE 14-2. PARTS LIST, 34 MHz GENERATOR CIRCUIT CARD ASSEMBLY (A16) 08744-1

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 3, 6, 13, 16, 20, 22, 31, 35, 37, 38, 42, 47	Capacitor, Ceramic, .033 uF, +80% −20% (Erie)	21744	5705-000-X5F-333M
C2, 15	Capacitor, Tantalum, 33 uF, ±20%, 10V (UC)	25019	T368B336K010AS
C4, 29, 52, 53	Capacitor, Tantalum, 6.8 uF, ±20%, 35V (UC)	25032	T368B685M035AS
C5, 9, 14, 19, 21, 27, 36, 41, 44, 49, 50, 51, 54, 58, 59	Capacitor, Polycarbonate, .1 uF, ±20% (M/E)	26871	C280MCF/A100K
C7, 24, 28, 56, 57	Capacitor, Ceramic, .001 uF, ±20% (Erie)	21747	831-000-X5T-102M
C8, 39, 43	Capacitor, Ceramic, .01 uF, ±20% (Erie)	21740	805-000-Z5V0-103Z
C10	Capacitor, Tantalum, 100 uF, ±20% (UC)	25025	T362C107M010AS
C11	Capacitor, Mica, 330 pF, ±2%	22117	CM05FD331G03
C12	Capacitor, Mica, 47 pF, ±2%	22112	CM05ED470G03
C17	Capacitor, Mica, 100 pF, ±2%	22109	CM05FD101G03
C18	Not Used		
C23	Capacitor, Mica, 150 pF, ±5%	22027	CM05FD151JN3
C25, 26, 33, 34, 40	Capacitor, Ceramic, .1 uF, ±20% (Erie)	21732	8131-050-651-104M
C30, 32	Capacitor, Mica, 3300 pF, ±2%	22145	CM06FD332G03
C45	Capacitor, Mica, 1000 pF, ±2%	22110	CM06FD102G03
C46	Capacitor, Ceramic, 100 pF, ±10% (Erie)	21327	831-000-53B0-101K
C48	Capacitor, Mica, 470 pF, ±2%	22114	CM06FD471G03
C55	Capacitor, Ceramic, .01 uF, ±20% (Erie)	21733	8121-050-651-103M
CR1	Diode	29013	MV1634
CR2, 3, 4	Not Used		
CR5	Diode	35514	1N916
FB1	Ferrite Bead (Mullard)	45051	FX1242
J1, 2, 7, 9-15	Connector (Cable Wave)	60044	700209
J3-5	Connector, Control	06846-3	

TABLE 14-2. PARTS LIST, 34 MHz GENERATOR CIRCUIT CARD ASSEMBLY (A16) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
J6, 8	Not Used		
L1, 3	Choke, RF, 5.6 uH	43027	MS14046-1
L2	Coil, RF Variable	05942	
L4, 8	Choke, RF, 15 uH	43030	MS14046-6
L5, 6, 9, 11, 12	Choke, RF, 220 uH	43034	MS90538-20
L7	Choke, RF, 1000 uH	43038	MS90539-15
L10	Choke, RF, 470 uH	43037	MS90539-7
Q1, 20, 21	Transistor	32021	2N5089
Q2, 4, 5, 8, 9, 11, 12, 13, 15, 16, 18, 19	Transistor	32255	2N2369A
Q3	Transistor	32511	2N3823
Q6, 7	Transistor	31500	2N918
Q10, 14	Not Used		
Q17	Transistor	31508	2N4126
R1, 49, 59	Resistor, Film, 100 Ohms, ±2%, ¼W	12161-101	RL07S101G
R2, 6, 13, 31, 62	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R3, 29	Resistor, Film, 1.8K Ohms, ±2%, ¼W	12161-182	RL07S182G
R4, 39, 45, 77	Resistor, Film, 3.3K Ohms, ±2%, ¼W	12161-332	RL07S332G
R5	Resistor, Film, 820 Ohms, ±2%, ¼W	12161-821	RL07S821G
R7, 33, 35, 36	Resistor, Film, 51 Ohms, ±2%, ¼W	12161-510	RL07S510G
R8, 9	Resistor, Film, 4.7K Ohms, ±2%, ¼W	12161-472	RL07S472G
R10, 47	Resistor, Film, 2.7K Ohms, ±2%, ¼W	12161-272	RL07S272G
R11, 28, 30, 50, 58, 66, 67	Resistor, Film, 2.2K Ohms, ±2%, ¼W	12161-222	RL07S222G
R12, 23, 56	Resistor, Film, 10 Ohms, ±2%, ¼W	12161-100	RL07S100G
R14, 41, 42, 48	Resistor, Film, 1.2K Ohms, ±2%, ¼W	12161-122	RL07S122G
R15	Resistor, Film, 150 Ohms, ±2%, ¼W	12161-151	RL07S151G

TABLE 14-2. PARTS LIST, 34 MHz GENERATOR CIRCUIT CARD ASSEMBLY (A16) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R16	Resistor, Film, 1.5K Ohms, ±2%, ¼W	12161-152	RL07S152G
R17, 18, 22, 51	Resistor, Film, 330 Ohms, ±2%, ¼W	12161-331	RL07S331G
R19, 70, 73	Resistor, Film, 390 Ohms, ±2%, ¼W	12161-391	RL07S391G
R20	Resistor, Film, 82 Ohms, ±2%, ¼W	12161-820	RL07S820G
R21, 40, 60, 61	Resistor, Film, 220 Ohms, ±2%, ¼W	12161-221	RL07S221G
R24, 54	Resistor, Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S223G
R25, 27, 37, 57, 80	Resistor, Film, 470 Ohms, ±2%, ¼W	12161-471	RL07S471G
R26, 63	Resistor, Film, 47 Ohms, ±2%, ¼W	12161-470	RL07S470G
R32, 34	Resistor, Film, 33 Ohms, ±2%, ¼W	12161-330	RL07S330G
R38, 44	Resistor, Film, 8.2K Ohms, ±2%, ¼W	12161-822	RL07S822G
R43	Resistor, Film, 68 Ohms, ±2%, ¼W	12161-680	RL07S680G
R46, 52	Not Used		
R53	Resistor, Film, 560 Ohms, ±2%, ¼W	12161-561	RL07S561G
R55	Resistor, Film, 3.9K Ohms, ±2%, ¼W	12161-392	RL07S392G
R64	Resistor, Film, 6.8K Ohms, ±2%, ¼W	12161-682	RL07S682G
R65	Resistor, Variable, 10K Ohms, (Bourns)	16074	3359P-1-103
R68, 72, 74, 75, 78, 79	Resistor, Film, 680 Ohms, ±2%, ¼W	12161-681	RL07S681G
R69, 71	Resistor, Film, 5.6K Ohms, ±2%, ¼W	12161-562	RL07S562G
R76	Resistor, Film, 10K Ohms, ±2%, ¼W	12161-103	RL07S103G
T1	Transformer, Wide Band	05969	
T2	Transformer, Wide Band	05950	
U1	Integrated Circuit (Fairchild)	36637	74LS90J
U2, 7	Integrated Circuit (Fairchild)	36632	74LS00J
U3	Integrated Circuit (Fairchild)	36535	74H103DC
U4	Integrated Circuit (Fairchild)	36621	74LS196J

TABLE 14-2. PARTS LIST, 34 MHz GENERATOR CIRCUIT CARD ASSEMBLY (A16) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U5	Not Used		
U6	Integrated Circuit (Fairchild)	36636	74LS74J
U8	Integrated Circuit (TI)	36582	SN74176J
U9	Integrated Circuit (Fairchild)	36543	uA796HC
VR1	Diode, Zener, 5.6V	33543	1N752A
–	Printed Wiring Board	08756	
–	Clamp, Transformer	05806	

CHAPTER 15
POWER SUPPLY, A18

15.1 THEORY OF OPERATION

The power supply section of the receiver consists of an AC line filter, power transformer and four regulator circuits. Figure 15-1 shows the schematic for the power supply, including chassis-mounted components.

15.1.1 Supply Input Filter

The AC line voltage is applied to the power supply through connector J1. The line voltage is filtered to remove high-frequency noise by the network consisting of C1 through C4, L1 and L2. The filtered AC is then applied through the POWER ON switch to the power supply transformer. T1.

15.1.2 −12V and −7V Regulator

The 13.5 VRMS AC voltage from pins 6 and 7 of T1 is rectified by bridge circuit CR1 and filtered by C5 and C9 before it is applied to integrated circuit regulator U1. The output of U1 at pin 2 is regulated −12V DC, which is supplied to receiver circuits through pins 17, 33 and 49 of J1. This −12V DC is also applied to the collector of Q1 which, in conjunction with zener diode VR2, produces a regulated −7V output to pins 14, 15, 30, 31, 46 and 47 of J1.

15.1.3 +20V Regulator

The 21.5 VRMS AC output from pins 12 and 13 of T1 is rectified by bridge circuit CR2, filtered by C6 and C10 and regulated by U2 to provide the +20V supply output.

15.1.4 +21V Unregulated and +12V Regulator

The circuit producing the +12V regulated supply operates as described above under 15.1.2 with the exception that an unregulated +21V DC voltage is taken off before regulator U3 and applied to output connector J2. Capacitors C7 and C11 provide filtering before output of the 21 volts or input to regulator U3.

15.1.5 +5V Regulator

The +5V regulator circuit operates as described under 15.1.3 to produce a +5V regulated output as well as an unregulated +10V output which is taken off before regulator U4. Capacitors C8 and C12 provide the necessary filtering.

15.2 POWER SUPPLY, A18 TESTING AND TROUBLESHOOTING

The testing and troubleshooting procedures for power supply module, A18 are designed to check each output of the unit under three different load conditions. The three conditions are: no load, maximum load, and short circuit. Each of these output conditions are checked under normal input voltage (120 VAC), low input voltage (108 VAC) and elevated input voltage (132 VAC). The procedures are presented to test each output in a certain order; however, if a particular output is suspected of malfunctioning then that output may be checked and the trouble isolated and corrected. After a problem has been corrected, all outputs should be checked, under the conditions described, before installing the module into the receiver. Figure 15-2 shows a suggested test set-up for accomplishing the power supply tests. Figure 15-3A shows a top view of the power supply while Figure 15-3B shows the rear view. These illustrations along with the schematic diagram shown in Figure 15-1 should be referred to while testing and troubleshooting the unit.

15.3 TEST EQUIPMENT

To perform the testing and troubleshooting procedures requires the use of test equipment and loads for monitoring voltage and current and for loading the various outputs of the power supply. The test equipment and loads required are listed in Table 15-1.

Table 15-1. Test Equipment Required

Item	Description	Equipment Recommended or Equal
1	Oscilloscope	Tektronix 465
2	Digital Multimeter	Data Precision 248
3	Multimeter	Simpson 260
4	AC Ammeter	0 - 100 milliamps
5	Variac	General Radio W5MT3A
6	100 ohm 10 watt Resistor	Resistance values given should be
7	100 ohm 1 watt Resistor	±5%. Wattage values given are
8	80 ohm 10 watt Resistor	approximately twice the amount of
9	47 ohm 2 watt Resistor	watts dissipated for safety factor.
10	30 ohm 10 watt Resistor	Larger wattage resistors may be used.
11	19 ohm 15 watt Resistor	
12	3 ohm 25 watt Resistor	

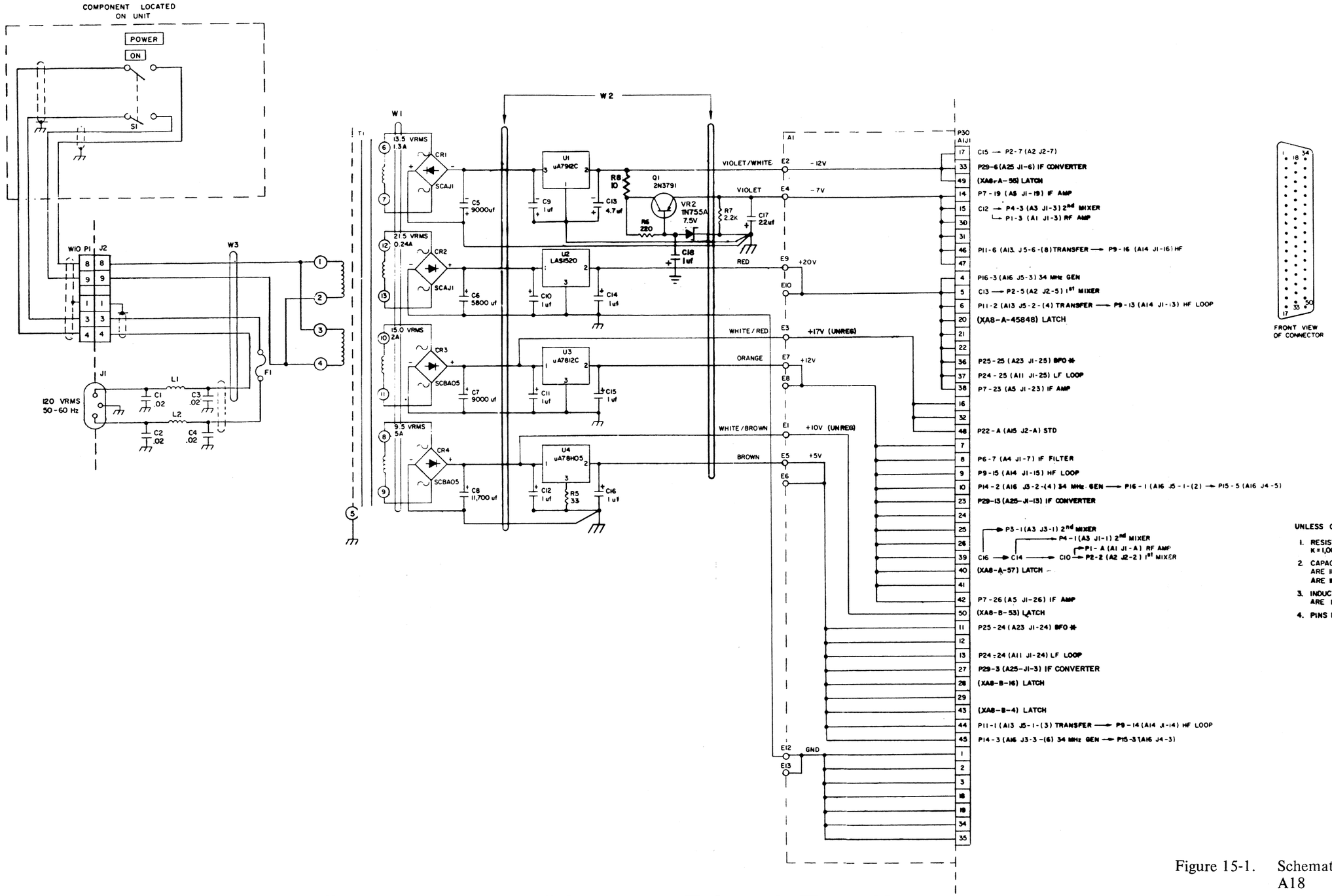


Figure 15-1. Schematic Diagram, Power Supply, A18

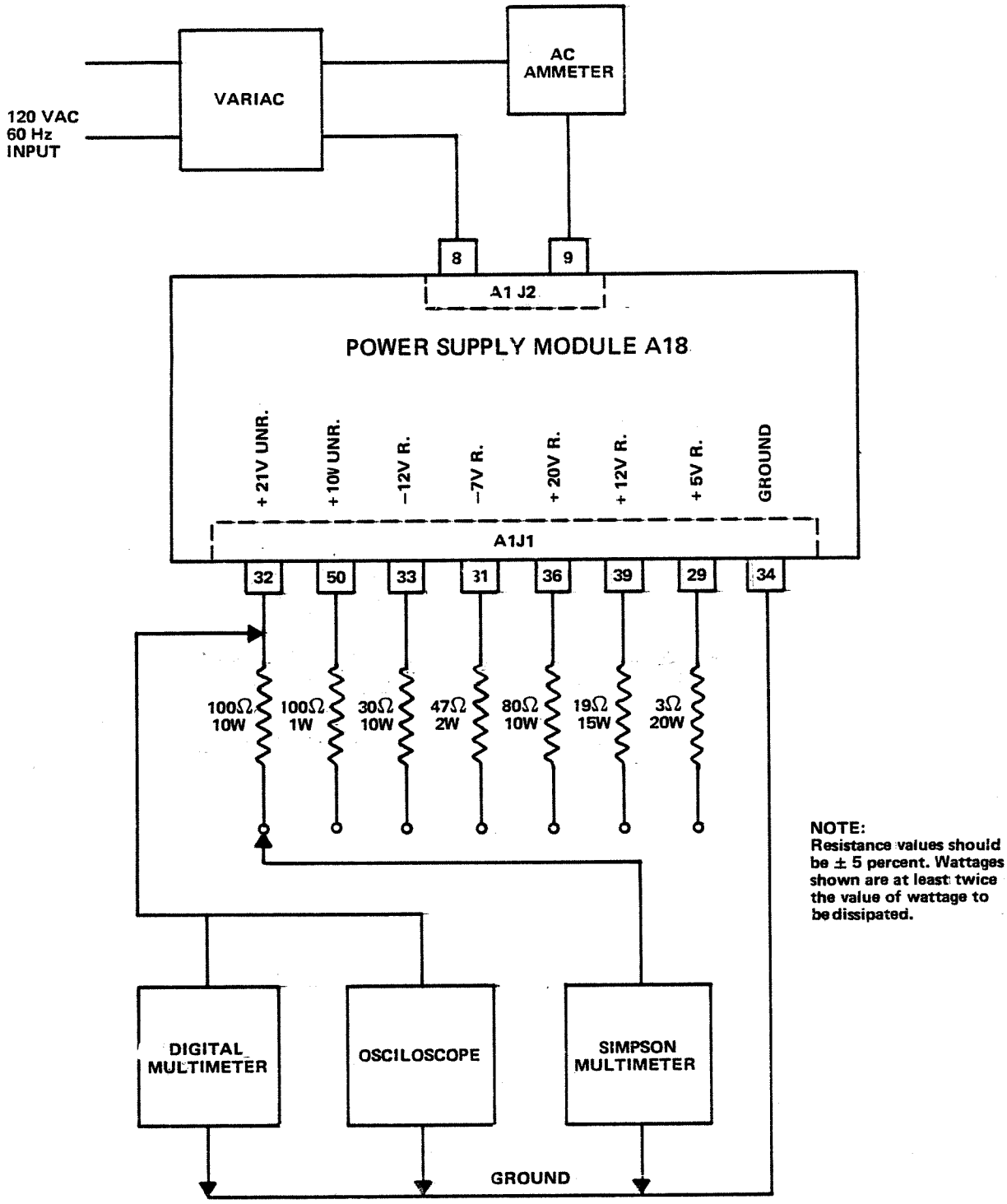


Figure 15-2. Power Supply A18, Test Set-up Diagram

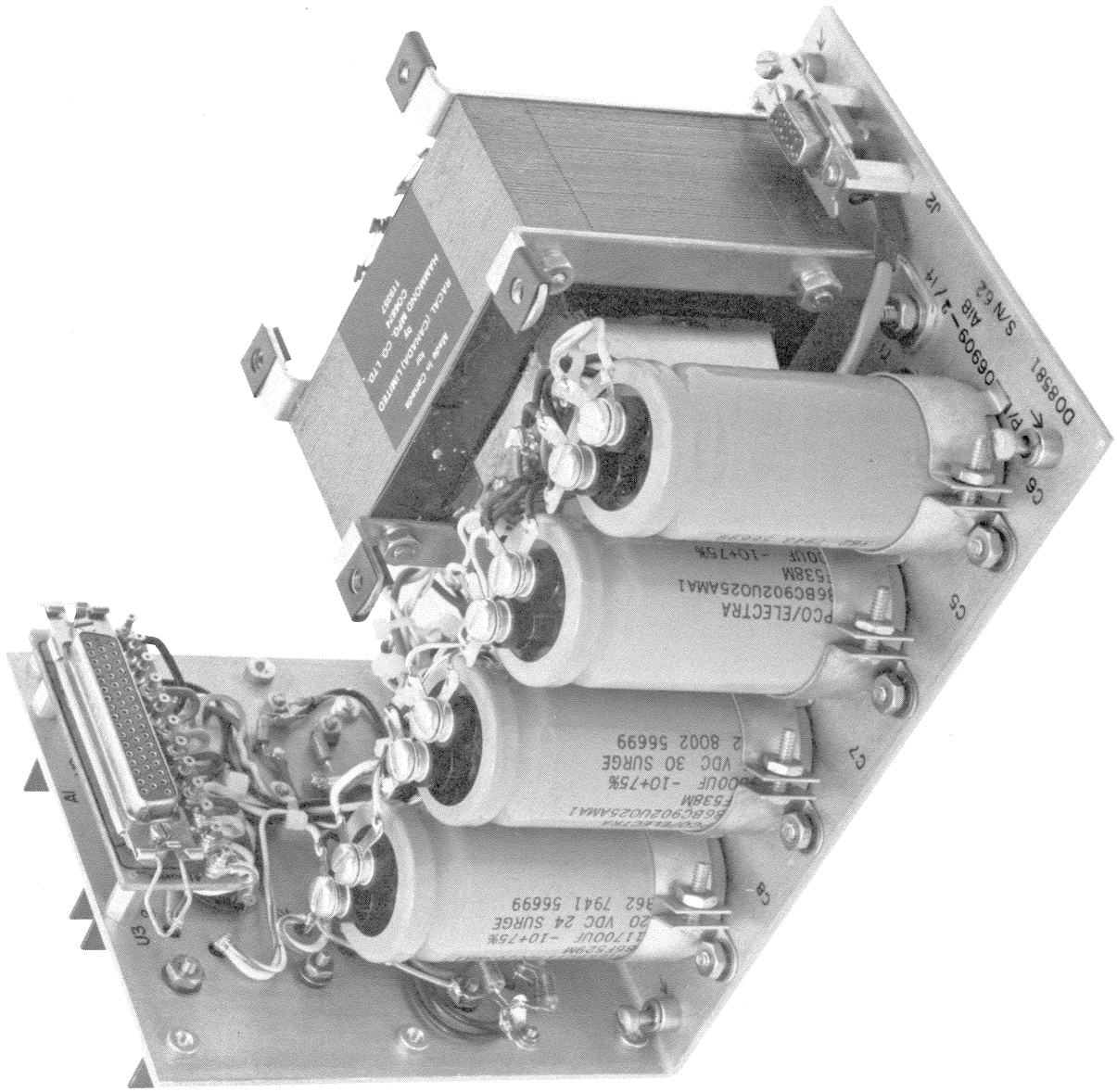


Figure 15-3A. Power Supply A18, Top View

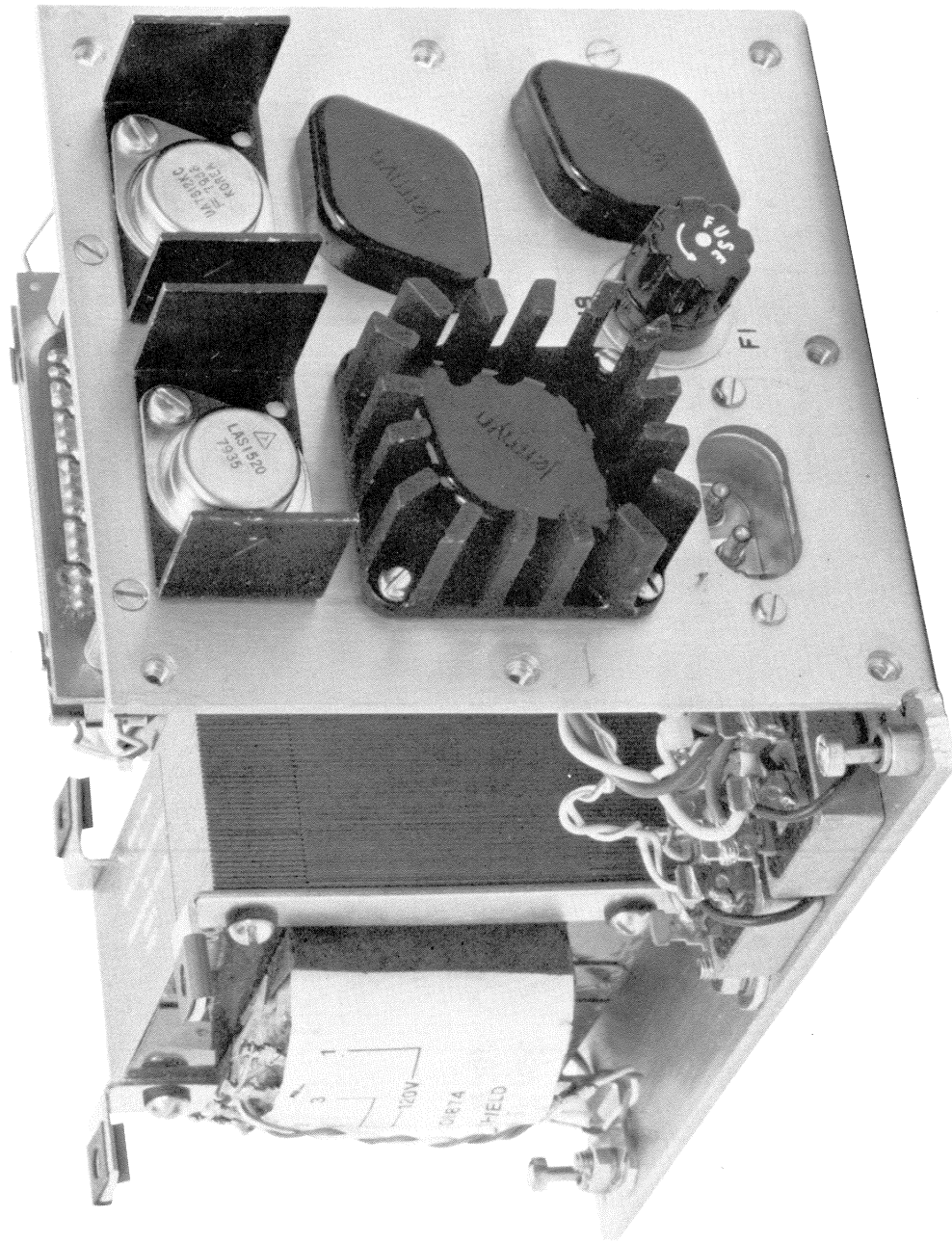


Figure 15-3B. Power Supply A18, Rear View

15.4 TEST PROCEDURE

The following procedures are provided to properly test the A18 module. Table 15-2 lists the voltages and currents for the various inputs and outputs of the power supply. All tests should be performed at ambient room temperature. Record the results on the test data sheet page 15-11.

15.4.1 Test Set-Up

1. Ascertain that the power supply is fused with a 2 ampere slow blow fuse.

2. Connect the variac output to pins 8 and 9 of J2 on the power supply with the AC ammeter connected in one line.

3. Connect the multimeter across the output lines of the variac and adjust the meter to read 120 VAC.

4. Connect the variac input to a 120 volt AC, 60 Hz source. Adjust the variac for a 120 volt reading on the multimeter. Check the ammeter reading and ascertain that it is within specified limits as shown in Table 15-2. Record on test data sheet.

15.4.2 Normal Input Voltage Test

1. Using the digital multimeter measure the output voltages at the connector pins as indicated in Table 15-2 for all DC outputs. Ascertain that the voltages read on the meter are within the specified no-load limits. Record results.

2. Using the oscilloscope, set for 5 mv/cm, check the ripple voltage between each regulated DC output and ground. Check the results against those listed in Table 15-2.

3. Connect the appropriate load between a DC output and the Simpson multimeter (observe polarity in terms of the DC voltage being monitored). Connect the opposite polarity of the multimeter to ground. Refer to Figure 15-3 and Table 15-2 for proper loads and polarities.

4. Check the current reading against those listed in the Table. Record.

5. Repeat steps 1 and 2 with the load connected as described in step 3. Ascertain that voltage, current and AC ripple are within specified limits.

6. Using a jumper lead short each of the regulated outputs to ground for at least five seconds. Repeat steps 1 and 2 with the load still connected. Ascertain that the regulated output recovers from the shorted condition and that voltage, current and AC ripple are within specified limits. Record results.

15.4.3 Low Input Voltage Test

1. With the multimeter connected across the variac output, rotate the variac control until 108 VAC is shown on the multimeter. Check the ammeter reading and ascertain it is within specified limits.

2. Repeat steps 1 through 6 in paragraph 15.4.2. Ascertain that all voltages, currents and ripple are within the limits as specified in Table 15-2. Record results.

15.4.4 Elevated Input Voltage Test

1. With the multimeter connected across the variac output, rotate the variac control until 132 VAC is shown on the multimeter, Check the ammeter reading and ascertain it is within specified limits.

2. Repeat steps 1 through 6 in paragraph 15.4.2. Ascertain that all voltages, currents and ripple are within the limits as specified in Table 15-2. Record results.

Table 15-2. Power Supply Test Data

Power Supply Test	Load Resistance	Connector/ Pin	Voltage - VDC No Load Min.	No Load Max.	Load Min.	Load Max.	Maximum Current Milliamps	Maximum Ripple Voltage
120 VAC		J2/8 & 9					750	
108 VAC		J2/8 & 9					750	
132 VAC		J2/8 & 9					750	
U.R.+21 VDC	100 ohms	J1/32	17.0	25.0	17.0	25.0	250	
U.R.+10 VDC	100 ohms	J1/50	8.0	14.0	8.0	14.0	60	
R. +5 VDC	3 ohms	J1/29	4.8	5.5	4.8	5.5	1750	5 MVP-P
R. +12 VDC	19 ohms	J1/39	11.5	12.75	11.5	12.75	650	5 MVP-P
R. +20 VDC	80 ohms	J1/36	19.0	21.0	19.0	21.0	250	5 MVP-P
R. –7 VDC	47 ohms	J1/31	–6.5	–7.5	–6.5	–7.5	150	5 MVP-P
R. –12 VDC	30 ohms	J1/33	–11.5	–12.5	–11.5	–12.5	400	5 MVP-P

15.4.5 Corrective Action

If any of the above tests fail to produce the required results, isolate the fault to a function (particular DC output) through the test procedures. The procedures may also be used to isolate certain components within a particular function for instance, if the peak-to-peak ripple is out of limits, then the filters should be checked.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductors and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, all the test procedures should be performed to evaluate the overall performance of the power supply module.

15.5 PARTS LIST, POWER SUPPLY, A18

The parts list for the A18 module is contained in Table 15-3.

DATE _____
CKD BY _____

MODULE _____
USED ON _____

TEST DATA SHEET

PART NAME: A18 Power Supply
PART NUMBER: 06909-2
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	120 VAC	108 VAC	132 VAC	LIMITS		UNITS
		Mea	Mea	Mea	MIN	MAX	
15.4.1(4)	Input Current		–	–		750	mA AC
15.4.2(1)	"No Load" UNREG +10		–	–	8.0	14.0	Volts
	UNREG +21V		–	–	17.0	25.0	Volts
	+5V		–	–	4.8	5.5	Volts
	Ripple		–	–	–	5	mV P-P
	+12V		–	–	11.5	12.75	Volts
	Ripple		–	–	–	5	mV p-p
	+20V		–	–	19.0	21.0	Volts
	Ripple		–	–	–	5	mV p-p
	-7V		–	–	-6.5	-7.5	Volts
	Ripple		–	–	–	5	mV p-p
	-12V		–	–	-11.5	-12.5	Volts
	Ripple		–	–	–	5	mV p-p
15.4.2(4),	"Full Load" -12V				-11.5	-12.5	Volts
15.4.3(2),	DC Current					400	mA
15.4.4(2)	Ripple					5	mV p-p
	-7V				-6.5	-7.5	Volts
	DC Current					150	mA
	Ripple					5	mV p-p
	+20V				19.0	21	Volts
	DC Current					250	mA
	Ripple					5	mV p-p
	+12V				11.5	12.75	Volts
	DC Current					650	mA
	Ripple					5	mV p-p
	+5V				4.8	5.5	Volts
	DC Current					1750	mA
	Ripple					5	mVp-p

DATE _____
CKD BY _____

MODULE A18
USED ON _____

TEST DATA SHEET

PART NAME: A18 Power Supply
PART NUMBER: 06909-2
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	120 VAC	108 VAC	132 VAC	LIMITS		UNITS
		Mea	Mea	Mea	MIN	MAX	
15.4.2(6)	"Short CKT" -12V	–	–		-11.5	-12.5	Volts
	-7V	–	–		-6.5	-7.5	Volts
	+20V	–	–		19.0	21.0	Volts
	+12V	–	–		11.5	12.5	Volts
	+5V	–	–		4.8	5.5	Volts

TABLE 15-3. PARTS LIST, POWER SUPPLY MODULE ASSEMBLY (A18) 06909-2

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-4	Capacitor, Ceramic, .02 uF, ±20% (Sprague)	21734	125L-S20
C5, 7	Capacitor, Electrolytic, 9000 uF, −10% +100% (GE)	24056	86F538M
C6	Capacitor, Electrolytic, 5800 uF, −10%, +100% (GE)	24055	86F556M
C8	Capacitor, Electrolytic, 11700 uF, −10%, +100%(GE)	24057	86F529M
C9-12, 14-16, 18	Capacitor, 1 uF, ±20%	25034	CS13BF105M
C13	Capacitor, 4.7 uF, +20% (U-C)	25042	T362B475M035AS
C17	Capacitor, 22 uF, ±5% (Kement)	25067	T110B226J015AS
CR1, 2	Diode (Sem Tech)	35540	SCAJ1
CR3, 4	Diode (Sem Tech)	35554	SCBA05
F1	Fuse, 2 amps, slow blow	40013	
J1	Connector (Switchcraft)	61069	LAC3G
A1J1	Connector	61169	M24308/23-17
J2	Connector	61166	M24308/2-1
L1, 2	Coil, Choke	05958	
Q1	Transistor	32032	2N3791
R1-4	Not Used		
R5	Resistor, Composition, 33 Ohms, ±5%, ¼W	10627	RC07GF330J
R6	Resistor, Composition, 220 Ohms, ±5%, ¼W	10647	RC07GF221J
R7	Resistor, Composition, 2.2K Ohms, ±5%, ¼W	10671	RC07GF222J
R8	Resistor, Film, 10 Ohms, ±2%, ¼W	12161-100	RL07S100G
T1	Transformer	06874	
U1	Integrated Circuit (Fairchild)	36625	UA7912KC
U2	Integrated Circuit (Lambda), +20V Reg.	36628	LAS1520
U3	Integrated Circuit (Fairchild)	36626	UA7812KC
U4	Integrated Circuit (Fairchild), +5V 5A	36627	MA78H05KC or SC
VR2	Zener Diode	33521	1N755A
W1	Cable, Power Supply	08583	
W2	Cable, Chassis Harness	08584	
W2A1	Assembly, Power Connector Board	06966	
W3	Cable, AC power	07175	
–	Chassis Assembly	08581	
–	Transformer Cover	06968	
–	Insulator, Transistor (Ref. Q1,U1,U4)	75114	
–	Cover, Transistor (Ref. Q1,U1,U4)	70772	
–	Printed Wiring Board	06967	

CHAPTER 16
LOWER/UPPER LOOP
BFO SYNTHESIZER, A23

16.1 THEORY OF OPERATION

This chapter provides information on the BFO lower frequency loop board A23A1 and the BFO upper frequency loop board A23A2; however, these two boards, combined in one module A23, are a part of a synthesizer section that supplies three different frequencies to the mixers and detector. For this reason, a general description on the operation of the synthesizer is presented to show the function of the A23 module within the synthesizer section. Figure 10-1 in Chapter 10 shows a simplified function block diagram of the complete section, and paragraph 10.1 describes the overall operation of the synthesizer.

16.1.1 BFO Synthesizer

The BFO synthesizer is composed of the BFO lower loop board, A23A1 and the BFO upper loop board, A23A2. The schematic diagrams for these two boards are Figures 16-2 and 16-3A. Figure 16-1 is a simplified block diagram for the BFO synthesizer. Figure 16-3B is the interconnect diagram for the A23 module.

16.1.1.1 BFO Lower Loop, A23A1

The operation of the lower loop board is similar to that of the lower loop synthesizer board A11A1, described in chapter 10. Thus, only those circuits in which there are differences will be described. Figure 16-2 is the schematic diagram.

Frequency divider N1, which is composed of counters U3, U5 and U10, has a division ratio which is equal to 700 minus the 10 Hz and 100 Hz frequency digits from the control modules. The three counters are loaded and enabled at a count of 896 (decoded by NAND gate U9) plus 4 more counts which clock flip-flops U11A and U11B. Thus, the number of clock pulses counted per cycle of the counter output on pin 12 of U10 is equal to 900 minus the preload of 200 (U10 "B" input) plus the 100 Hz and 10 Hz frequency data.

Frequency divider N2 is composed of counters U14, U15 and U19. The maximum count of N2 is 453, determined by NAND gate U18 and flip-flops U20A and B. The actual division ratio of counter N2 is determined by subtracting the preloaded value from the maximum count of 453. U19 is always preloaded with 0's, while U15 is preloaded with either a 5 or a 6, depending on the state of the BFO SIGN (−) and BFO SIGN (+) signals from the control module which are connected to the A and B inputs of U15. The preload of U14 is determined by the 1 kHz data from the control module which may range from 0 through 8 in the +BFO mode and 2 through 9 in the −BFO mode (9's complement +1). Thus, the division ratio will range from 385 to 401. This range includes 8 kHz of positive BFO range and 8 kHz of negative BFO range.

The output of divider N2 is applied to phase comparator U16 and regulates the transfer loop VCO frequency.

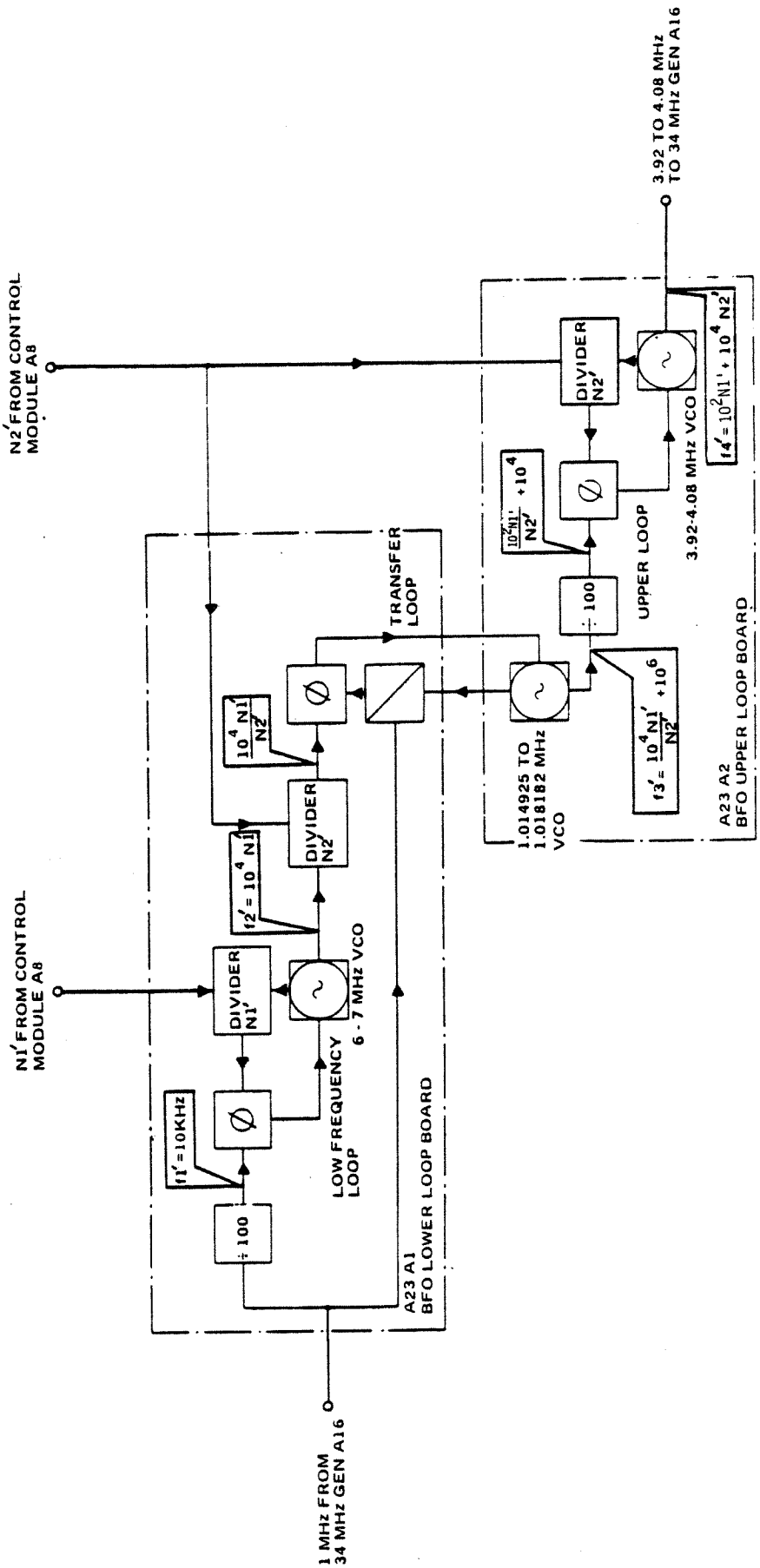
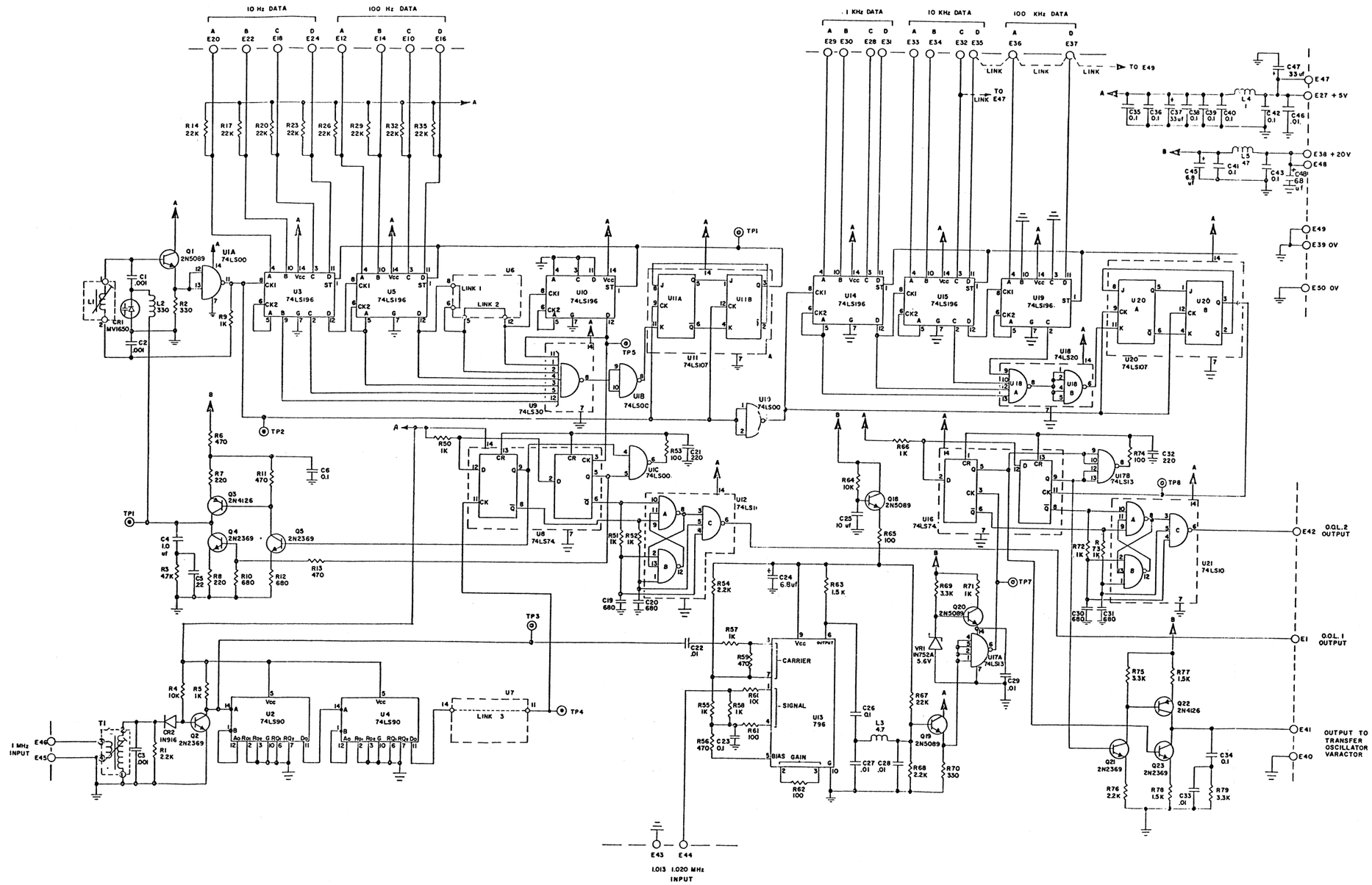


Figure 16-1. Simplified Block Diagram, BFO Synthesizer



UNLESS OTHERWISE NOTED:

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT, K=1,000 M=1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARADS, LESS THAN ONE ARE IN MICROFARADS.
3. INDUCTANCE VALUES ONE OR GREATER ARE IN MICROHENRIES, LESS THAN ONE ARE IN HENRIES.
4. U6 NOT FITTED, PINS 6-8 & 5-12 CONNECTED BY WIRE LINKS 1 & 2.
5. U7 NOT FITTED, PINS 11-14 CONNECTED BY WIRE LINK 3.
6. THIS SYNTHESIZER OPERATES WITH A 10 KHz PRESET OF 4. TO ACHIEVE THIS E35 IS GROUNDED AND E32 IS CONNECTED TO +5V

Figure 16-2. Schematic Diagram, Lower Loop BFO Synthesizer, A23A1

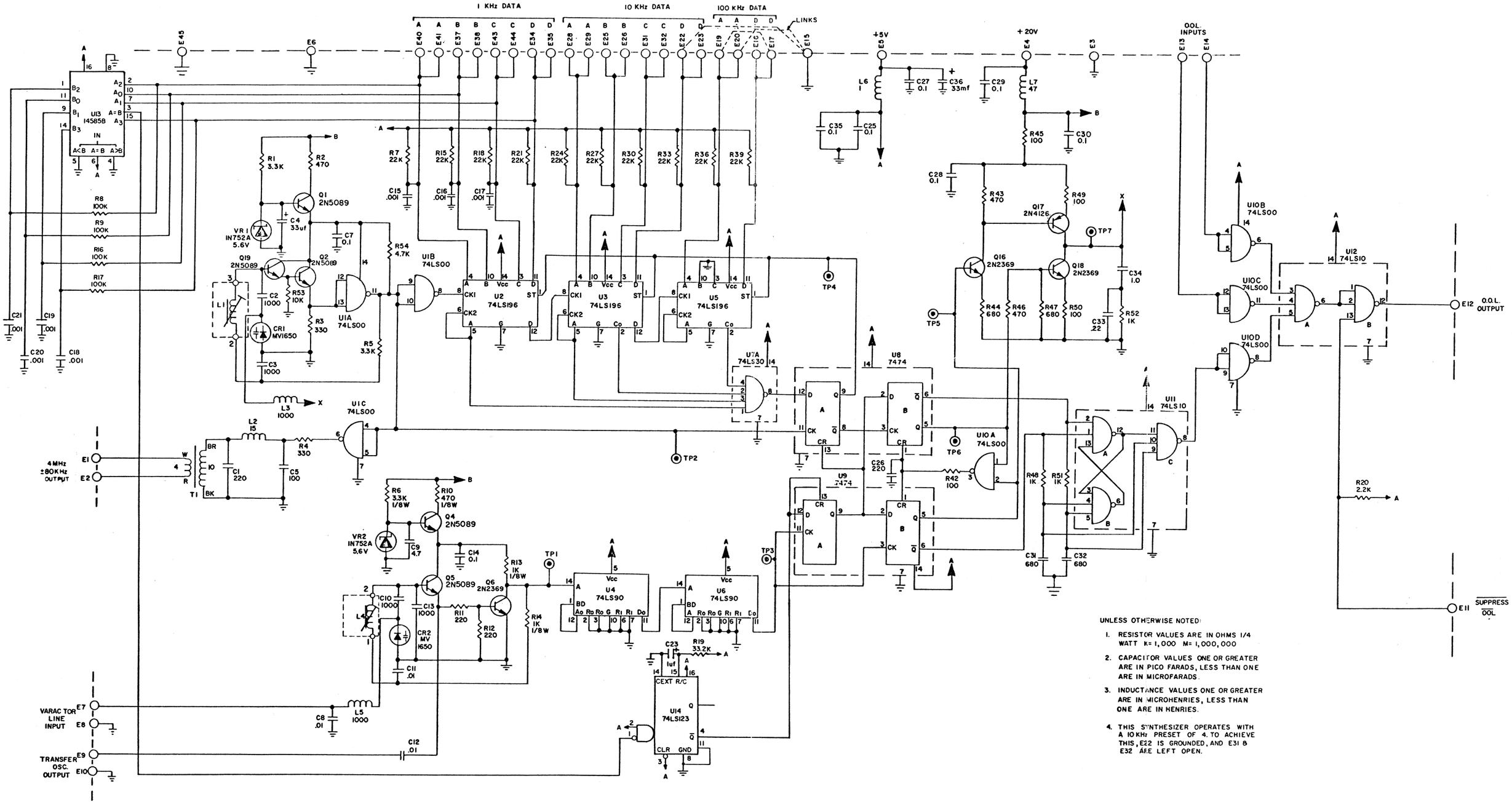


Figure 16-3A. Schematic Diagram, Upper Loop BFO Synthesizer, A23A2

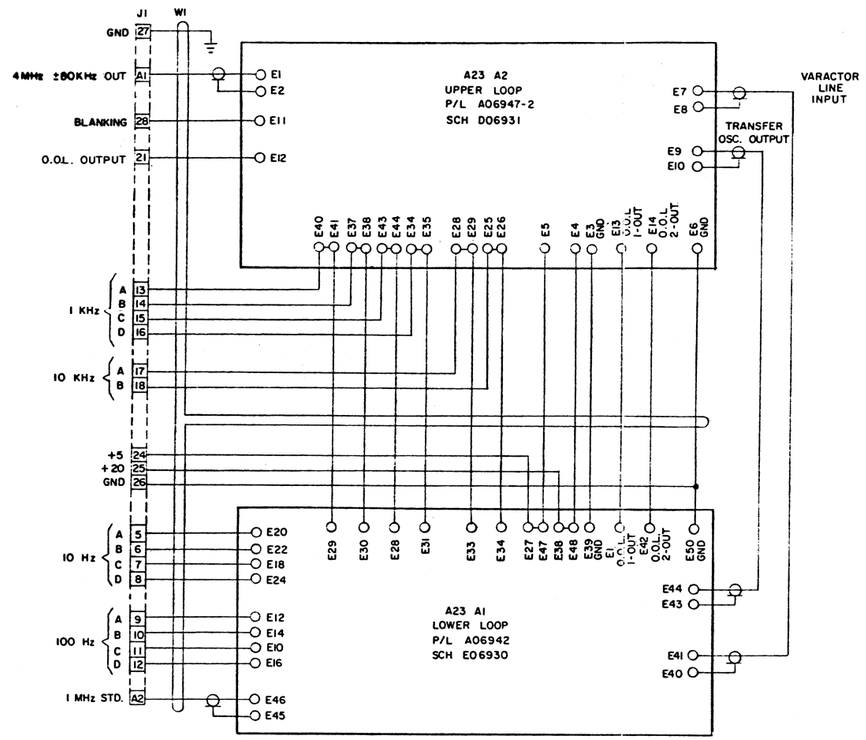


Figure 16-3B. Interconnect Diagram, Upper/ Lower Loop Module, A23

16.1.1.2 BFO Upper Loop, A23A2

The operation of the BFO upper loop board is identical to that described for the upper loop synthesizer board, A11A2, in Chapter 10. Figure 16-3A is the schematic diagram for A23A2.

16.2 LOWER AND UPPER LOOP SYNTHESIZER A23 TEST FIXTURE

Troubleshooting and alignment of the BFO upper and lower loop synthesizer module A23 is accomplished through the use of the RACAL upper and lower loop synthesizer A23 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A23 module for testing, while also providing easy access to the two printed circuit boards within the module. The front apron of the test fixture contains the frequency controls, offset switch, range blank control, and output port.

A 1 MHz oscillator is contained within the test fixture as an internal signal source for the module under test as well as for external sync of associated test equipment. An internal timing circuit provides for using the VCO's in the module under test, in that it permits the VCO to tune its complete range in a repetitive fashion to check settling time. Front panel frequency switches provide BCD inputs for manual setting of the VCO in the module under test. An external trigger out port, on the rear apron, provides for sync of external equipment. Provisions are also made to display an out of lock condition on the test fixture. Figure 16-4 shows the A23 module plugged into the test fixture. Figure 16-5A shows the overall assembly of the A23A1 module while Figure 16-5B shows the circuit card assembly. Figure 16-6A shows the overall assembly of the A23A2 module, while Figure 16-6B shows the circuit card assembly.

16.3 TEST EQUIPMENT AND ACCESSORIES

The test equipment and accessories required are listed in Table 16-1.

Table 16-1. Test Equipment and Accessories

Item	Description	Equipment Recommended or Equal
1	RF Voltmeter	Boontoon 91H
2	Digital Multimeter	Data Precision 248
3	Frequency Counter	Dana 8030B
4	Oscilloscope	Tektronix 465
5	DC Power Supply	Racal
6	A23 Test Fixture	Racal
7	Unterminated Adapter	Boontoon 91-6C
8	50 ohm Adapter	Boontoon 91-8B
9	Tuning Tool	Micrometals RCI 82007

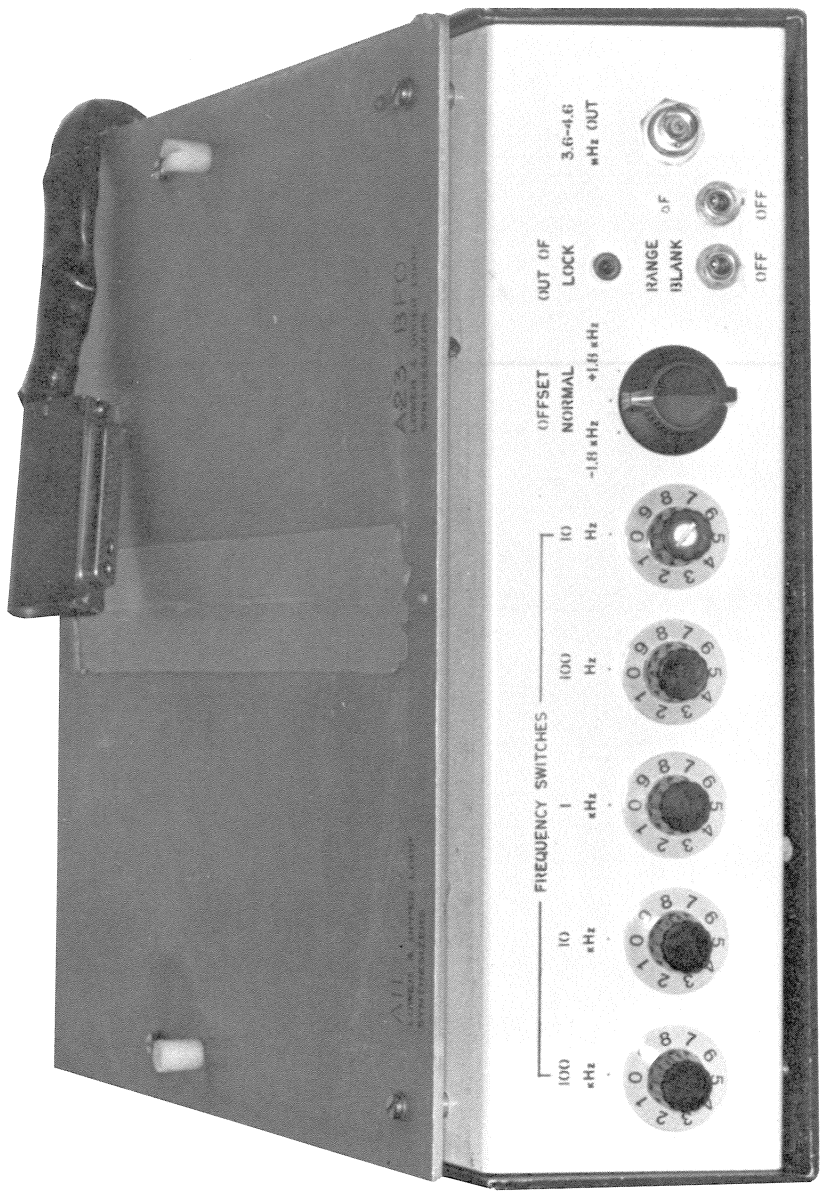


Figure 16-4. Lower/Upper Loop BFO Synthesizer A23, Test Fixture

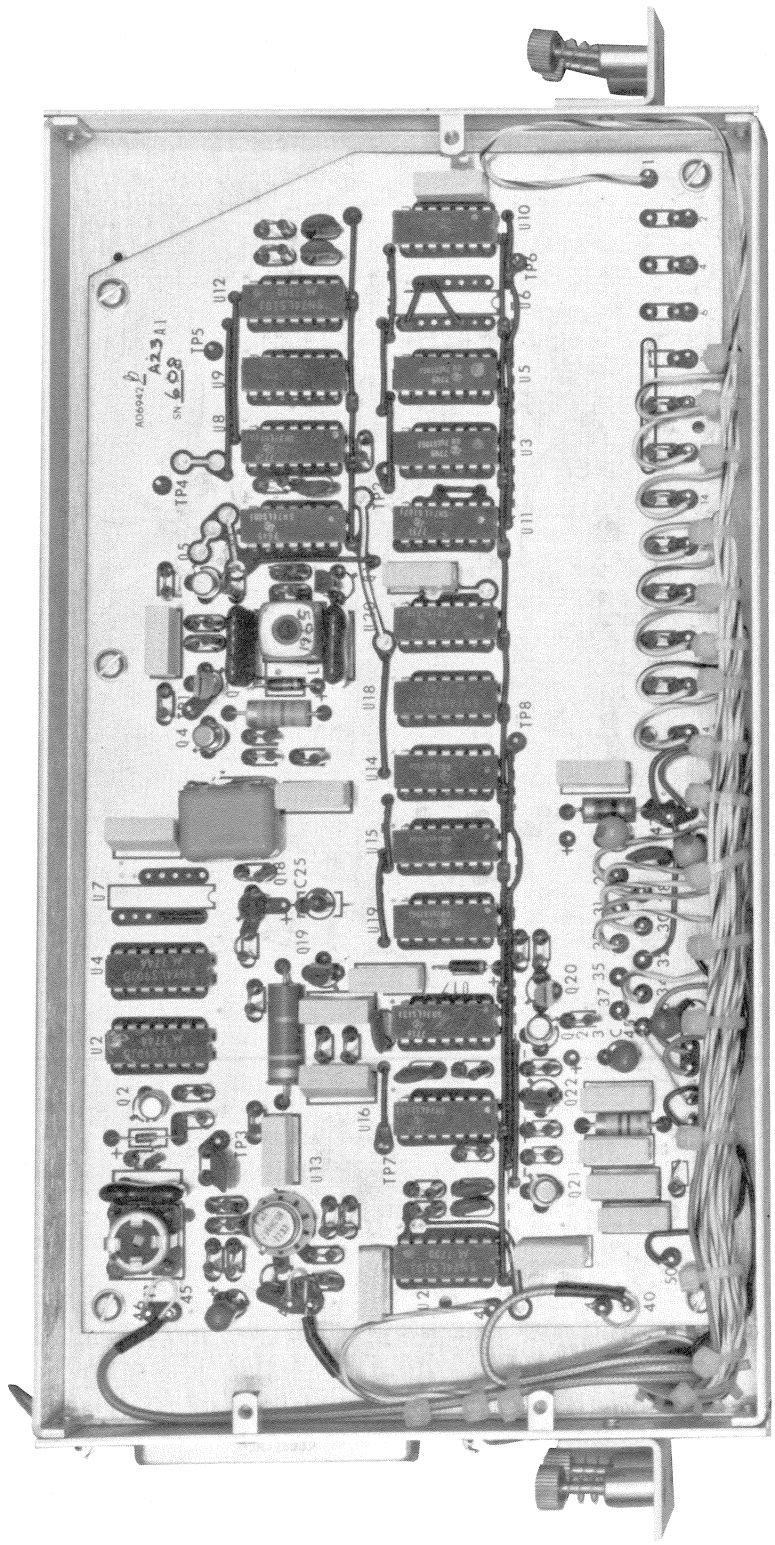


Figure 16-5A. BFO Lower Frequency Loop A23A1, Overall Assembly

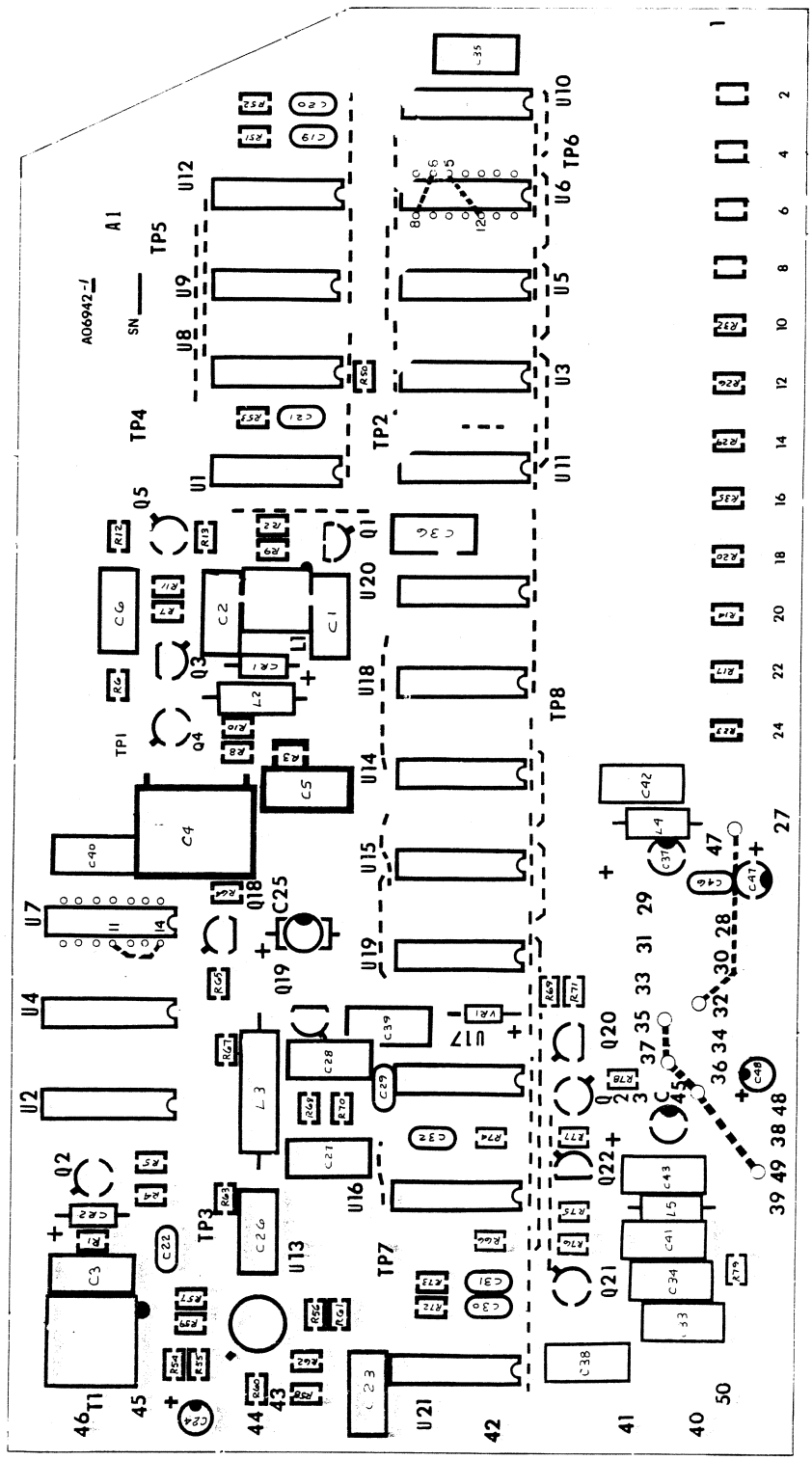


Figure 16-5B. Lower Loop BFO Synthesizer, A23A1, Circuit Card Assembly

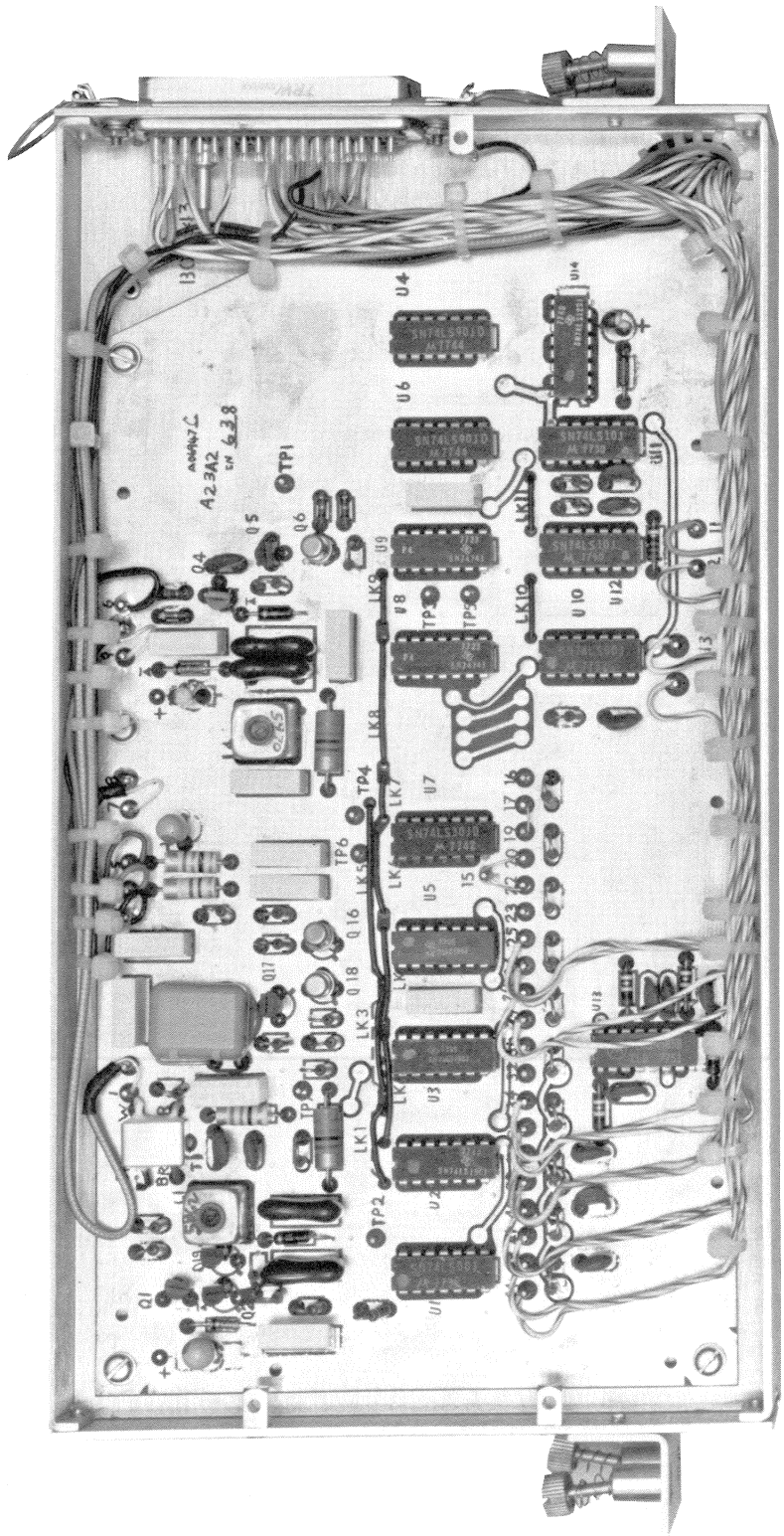


Figure 16-6A. BFO Upper Frequency Loop A23A2, Overall Assembly

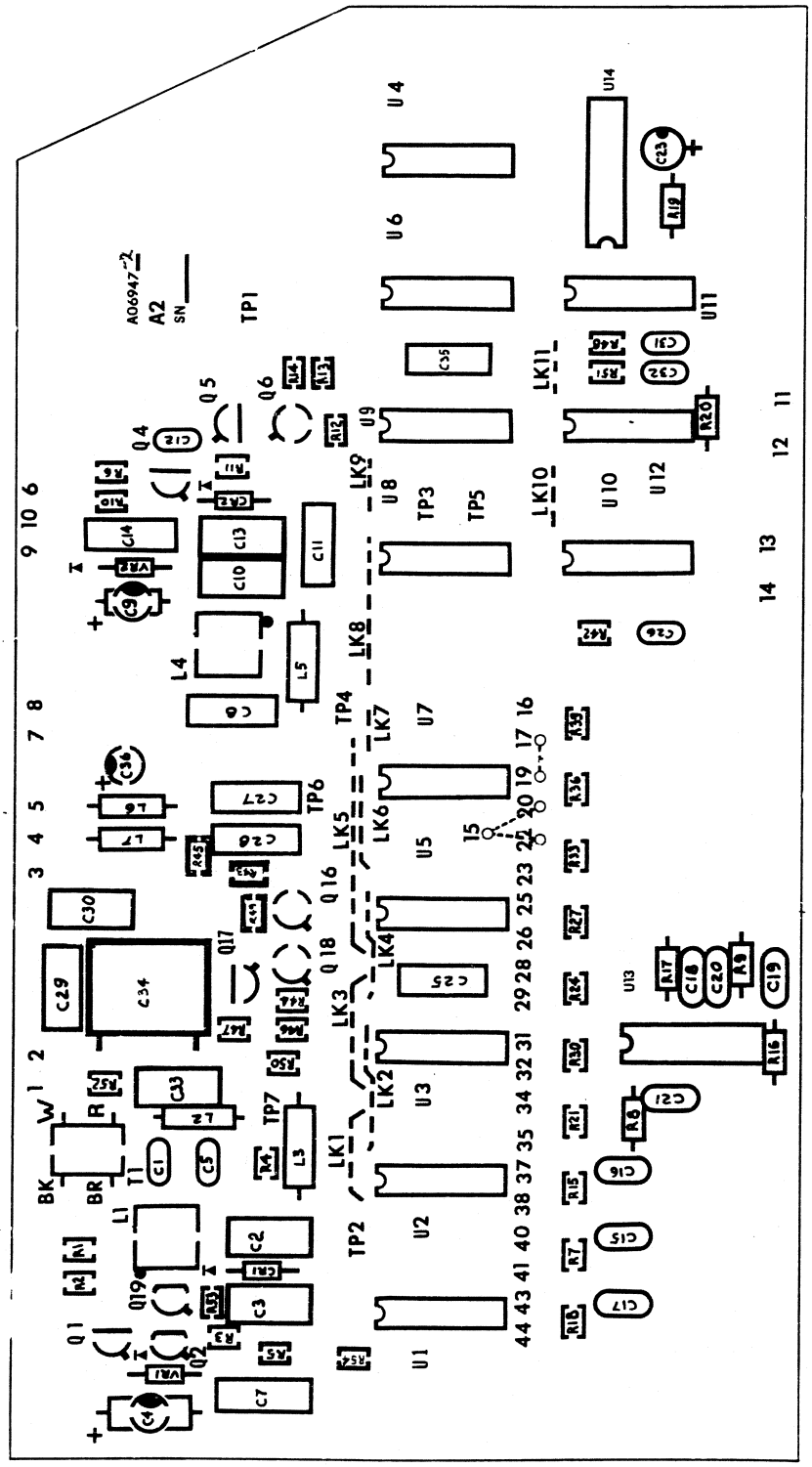


Figure 16-6B. Upper Loop BFO Synthesizer A23A2 Circuit Card Assembly

16.4 TEST AND ALIGNMENT

The following procedures are provided to properly test the A23 module. All tests should be performed at ambient room temperature. Record results on the test data sheet, page 16-18.

16.4.1 Lower Loop VCO Alignment (A23A1)

1. Place the A23 boards under test (B.U.T.) into the test fixture.
2. Set all the FREQUENCY SWITCHES on test fixture to the 0 position.
3. Place the OFFSET switch to the NORMAL position.
4. Place the RANGE BLANK switch to OFF.
5. Apply DC power to the rear apron of the test fixture via the octal plug. Turn the power supply on.
6. Ignore the status of the OUT OF LOCK lamp until told to check its' status.
7. Place the Delta Frequency switch (AF) to the OFF position.
8. Using the unterminated adapter probe, connect the R.F. voltmeter to the cathode side of CR-2 (on upper left-hand corner of B.U.T.) and adjust T-1 for a maximum indication on the R.F. voltmeter. This level should be 1.5 volts ±0.5 volts RMS. Record on test data sheet.
9. Connect the digital multimeter to TP-1 (on upper center of B.U.T.) and adjust L-1 to obtain a reading of 14.0 ±0.5 Volts DC.. Record results.

16.4.2 Upper Loop VCO Alignment (A23A2)

1. Connect the digital multimeter to pin E-7 (on upper center of B.U.T.) of the A2 board.
2. Set the FREQUENCY SWITCHES on test fixture to 99 000 and adjust L-4 for an indication of 14.0 ±0.5 Volts DC on the digital multimeter. Record results.
3. Set the FREQUENCY SWITCHES to 60 000 and connect the digital multimeter to TP-7 of the A2 board.
4. Adjust L-1 on the A2 board to obtain a reading of 8.0 ±0.5 Volts DC on the digital multimeter. Record results.
5. Ensure at this time the OUT OF LOCK lamp is OUT. Record on test data sheet.

16.4.3 Lower and Upper Loop Frequency Check

1. Set the counter GATE to 100 mSec.

2. Connect the A input of the frequency counter to the 3.6 to 4.6 mHz OUTPUT port on the text fixture.

3. Set the FUNCTION swtich on the frequency counter to the A/B position (if using DANA frequency counter). If using other frequency counter, just leave at present setting.

4. Connect the B input of the frequency counter to the 1 MHz REF OUT port located on the rear apron of the test fixture (if using DANA counter). If using other counter, connect EXT. OSC INPUT on the rear paron of the frequency counter to the 1 MHz REF OUT port of test fixture. INT-EXT switch should be placed at EXT position on the back of frequency counter.

5. Perform the requirements of Table 16-2 ensuring the OUT OF LOCK lamp remains out for each position. The accuracy of the counter display should be within ±1 count. Record results.

6. It should have been noted that when the FREQUENCY SWITCHES are rotated the OUT OF LOCK lamp ignites momentarily. Place the RANGE BLANK switch to the ON position.

7. Rotate any one of the FREQUENCY SWITCHES; the OUT OF LOCK lamp should remain out for any rotation of the switches. Record results.

16.4.4 Lower and Upper Output Level Check

1. Disconnect the frequency counter from the 3.6 MHz – 4.6 MHz OUT port on the front of the test fixture and connect the R.F. voltmeter using the 50 Ohms adapter to this port.

2. Ensure the output level is 220 ±50 mVolts for the following FREQUENCY SWITCH settings:

   600 00

   Record on test data sheet.

16.4.5 Microphonic Check

1. Check that L1 had the PTFE tape (teflon) with its tuning slug on the A1 Board.

2. Ensure that C1 and C2 are pushed away from L1 as far as possible without damage to components.

3. Knock firmly on the top and back of the module, (as if knocking on a door) and check that the OUT-OF-LOCK light remains out. Record on test data sheet.

4. Turn power off and remove B.U.T. from the fixture.

Table 16-2. Frequency Accuracy Check

Frequency Switches	Frequency Counter
500 00	4 100 00
600 00	4 000 00
700 00	3 900 00
600 00	4 000 00
611 10	3 988 90
622 20	3 977 80
633 30	3 966 70
644 40	3 955 60
655 50	3 944 50
666 60	3 933 40
677 70	3 922 30
688 80	3 911 20
699 90	3 900 10
700 00	3 900 00

Note: The OUT OF LOCK lamp may flicker when changing the FREQUENCY SWITCHES but should remain out when the switches have settled. The 10 Hz FREQUENCY SWITCH is not used in the A-23 module.

16.4.6 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (VCO alignment, frequency, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function for instance, failures of certain frequency counts can be traced to specific components. Further signal tracing may then be accomplished, using the oscilloscope or voltmeter, to trace the fault to a single component. Maximum use, should also be made, of the test points provided on the A23 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductor and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 16.4.1 through 16.4.5.

16.5 PARTS LIST, LOWER/UPPER LOOP-BFO SYNTHESIZER, A23

The parts list for the A23 module is contained in Table 16-3. Table 16-4 lists the parts for circuit card A23A1 while Table 16-5 lists the parts for circuit card A23A2.

DATE _____
CKD BY _____

MODULE A23
USED ON _____

TEST DATA SHEET

PART NAME: A23 BFO Lower and Upper Loop Synthesizer
PART NUMBER: 06913
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
16.4.1(8)	CR2 Level 1.5 VRMS		1.0	2.0	VRMS
16.4.1(9)	TP1 Level 14.0 VDC		13.5	14.5	VDC
16.4.2(2)	E7 Level 14.0 VDC		13.5	14.5	VDC
16.4.2(4)	TP7 Level 8.0 VDC		7.5	8.5	VDC
16.4.2(5)	Out-of-Lock Lamp Out		Check		
16.4.3(5)	Frequency Accuracy Check		Check		
16.4.3(7)	OOL Lamp out with Range Blank on		Check		
16.4.4(2)	Output Level 220 mV		170	270	mV
16.4.5(3)	Microphonic Check		Pass	Fail	

TABLE 16-3. PARTS LIST, BFO MODULE ASSEMBLY (A23) 06913

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A1	BFO Lower Loop Circuit Card Assembly (See Table 16-4 for further breakdown)	06942	
A2	BFO Upper Loop Circuit Card Assembly (See Table 16-5 for further breakdown)	06947-2	
J1	Connector, Multi-pin (Cannon)	61167	DDM-36W4P
J1A1, J1A2	Connector, Coaxial (Cannon)	60021	DM53740-5008
W1	Cable Form	07148	

TABLE 16-4. PARTS LIST, BFO LOWER LOOP CIRCUIT CARD ASSEMBLY (A23A1) 06942

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1-3	Capacitor, Mica, 1000 pF, ±2%	22110	CM06F102G03
C4	Capacitor, Polycarbonate, 1.0uF, +20% (ITT)	26893	PMC2R-1R0100
C5	Capacitor, Polycarbonate, 0.22 uF, ±20% (M/E)	26872	C280MCF/A220K
C6, 23, 26, 34-36, 38-43	Capacitor, Polycarbonate, 0.1 uF, ±20% (M/E)	26871	C280MCF/A100K
C7-18, 44	Not Used		
C19, 20, 30, 31	Capacitor, Ceramic, 680 pF, ±10% (Erie)	21743	8131-000-X5R-681K
C21, 32	Capacitor, Ceramic, 220 pF, ±10% (Erie)	21328	835-000-G3C0-221K
C22, 29, 46	Capacitor, Ceramic, 0.01 uF, +80%, −20% (Erie)	21740	805-000-Z5V0-103Z
C24, 45, 48	Capacitor, Tantalum, 6.8 uF, ±20% (UC)	25032	T368B685M035AS
C25	Capacitor, Tantalum, 1.0 uF, ±20% (UC)	25033	T368A105M035AS
C27, 28, 33	Capacitor, Polycarbonate, 0.01 uF, ±20% (M/E)	26870	C280MCF/A10K
C37, 47	Capacitor, Tantalum, 33 uF, ±20% (UC)	25019	T368B336K010AS
CR1	Diode, Varicap (Motorola)	29006	MV1650
CR2	Diode	35514	1N916
L1	Coil, Variable	05961	
L2	Choke, RF, 330 uH, ±5%	43036	MS90539-3
L3	Choke, RF, 4700 uH, ±5%	43039	MS90541-3
L4	Choke, RF, 1 uH, ±5%	43024	MS18130-8
L5	Choke, RF, 47 uH, ±5%	43032	MS90538-4
Q1, 18-20	Transistor	32021	2N5089
Q2, 4, 5, 21, 23	Transistor	32255	2N2369A
Q3, 22	Transistor	31508	2N4126
Q6-17	Not Used		
R1, 54, 68, 76	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R2, 70	Resistor, Composition, 330 Ohms, ±5%,1/4W	10651	RC07GF331J
R3	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J
R4, 64	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R5, 9, 50-52, 55, 57, 58, 66, 71-73	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R6, 11, 13, 56, 59	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J
R7, 8,	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R10, 12	Resistor, Composition, 680 Ohms, ±5%, 1/4W	10659	RC07GF681J
R14, 17, 20, 23, 26, 29, 32, 35, 67	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R15, 16, 18, 19, 21, 22, 24, 25, 27, 28, 30, 31, 33, 34, 36, 37, 38, 39, 40, 41, 42, 43, 44-49	Not Used		
R53, 60, 61, 62, 65, 74	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R63, 77, 78	Resistor, Composition, 1.5K Ohms, ±5%, 1/4W	11834	RC07GF152J
R69, 75, 79	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	11838	RC07GF332J
T1	Transformer	05964	
U1	Integrated Circuit (Fairchild)	36632	74LS00J
U2, 4	Integrated Circuit (Fairchild)	36637	74LS90J

TABLE 16-4. PARTS LIST, BFO LOWER LOOP CIRCUIT CARD ASSEMBLY (A23A1) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
U3, 5, 10, 14, 15, 19	Integrated Circuit (Fairchild)	36621	74LS196J
U6, 7	Not Used		
U8, 16	Integrated Circuit (Fairchild)	36636	74LS74J
U9	Integrated Circuit (Fairchild)	36635	74LS30J
U11, 20	Integrated Circuit (Fairchild)	36638	74LS107J
U12, 21	Integrated Circuit (Fairchild)	36633	74LS10J
U13	Integrated Circuit (Fairchild)	36543	μA796HC
U17	Integrated Circuit (Fairchild)	36641	74LS13J
U18	Integrated Circuit (Fairchild)	36634	74LS20J
VR1	Diode, Zener, 5.6V	33543	1N752A
–	Printed Wiring Board	06941	
–	Pad, Transistor (Ref. Q2,4,5,21,23)	70760	7717-46N-WHITE
–	Pad, IC (Ref. U13)	70768	RCT05140-10A

TABLE 16-5. PARTS LIST, BFO UPPER LOOP CIRCUIT CARD ASSEMBLY (A23A2) 06947-2

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 26	Capacitor, Ceramic, 220 pF, ±10% (Erie)	21328	835-000-G3C0-221K
C2, 3, 10, 13	Capacitor, Mica, 1000 pF, ±2%	22110	CM06F102G03
C4, 36	Capacitor, Tantalum, 33uF, ±20%, 10V (UC)	25019	T368B336K010AS
C5	Capacitor, Ceramic, 100 pF, ±10%(Erie)	21327	831-000-S3B0-101K
C7, 14, 25, 27-30, 35	Capacitor, Polycarbonate, 0.1uF, ±20%, 100V(M/E)	26871	C280MCH/A100K
C8, 11	Capacitor, Polycarbonate, 0.01uF, ±20% (M/E)	26870	C280MCF/A10K
C9	Capacitor, Tantalum, 4.7 uF, ±20%, 10V(UC)	25031	T360A475M010
C12	Capacitor, Ceramic, 0.01 uF, +80%, −20% (Erie)	21740	805-000-Z5V0-103Z
C15-21	Capacitor, Ceramic, 0.001 uF, ±20% (Erie)	21747	831-000-X5T-102M
C6,22,24	Not Used		
C23	Capacitor, Tantalum, 1 uF, ±5% (UC)	25054	T368A105J020AS
C31, 32	Capacitor, Ceramic, 680 pF, ±10% (Erie)	21743	831-000-X5R-681K
C33	Capacitor, Polycarbonate, 0.22 uF, ±20%, 100V(M/E)	26872	C280MCH/A220K
C34	Capacitor, Polycarbonate, 1.0uF, +20% 50VDCW	26893	PMC2R-1R0100
CR1, 2	Diode, Varicap (Motorola)	29006	MV1650
L1	Coil, Variable	05962	
L2	Choke, RF, 15 uH	43030	MS14046-6
L3, 5	Choke, RF, 1000 uH	43038	MS90539-15
L4	Coil, Variable	05970	
L6	Choke, RF, 1 uH	43024	MS18130-8
L7	Choke, RF, 47 uH	43032	MS90538-4
Q1, 2, 4, 5, 19	Transistor	32021	2N5089
Q6, 16, 18	Transistor	32255	2N2369A
Q3, 7-15	Not Used		
Q17	Transistor	31508	2N4126
R1, 5	Resistor, Composition, 3.3K Ohms, ±5%, 1/4W	10675	RC07GF332J
R2, 43, 46	Resistor, Composition, 470 Ohms, ±5%, 1/4W	10655	RC07GF471J
R3, 4	Resistor, Composition, 330 Ohms, ±5%, 1/4W	10651	RC07GF331J
R6	Resistor, Composition, 3.3K Ohms, ±5%, 1/8W	18375	RC05GF332J
R7, 15, 18, 21, 24, 27, 30, 33, 36, 39	Resistor, Composition, 22K Ohms, ±5%, 1/4W	10695	RC07GF223J
R8, 9, 16, 17	Resistor, Composition, 100K Ohms, ±5%, 1/4W	10711	RC07GF104J
R10	Resistor, Composition, 470 Ohms, ±5%, 1/8W	18355	RC05GF471J
R11, 12,	Resistor, Composition, 220 Ohms, ±5%, 1/4W	10647	RC07GF221J
R13, 14	Resistor, Composition, 1K Ohms, ±5%, 1/8W	18363	RC05GF102J
R19	Resistor, Metal Film, 33.2 K Ohms, ±1%, 1/10W	12135	RN55D3322F
R20	Resistor, Composition, 2.2K Ohms, ±5%, 1/4W	10671	RC07GF222J
R22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38, 40, 41	Not Used		
R42, 45, 49, 50	Resistor, Composition, 100 Ohms, ±5%, 1/4W	10639	RC07GF101J
R44, 47	Resistor, Composition, 680 Ohms, ±5%, 1/4W	10659	RC07GF681J
R48, 51, 52	Resistor, Composition, 1K Ohms, ±5%, 1/4W	10663	RC07GF102J
R53	Resistor, Composition, 10K Ohms, ±5%, 1/4W	10687	RC07GF103J
R54	Resistor, Composition, 4.7K Ohms, ±5%, 1/4W	10679	RC07GF472J

TABLE 16-5. PARTS LIST, BFO UPPER LOOP CIRCUIT CARD ASSEMBLY (A23A2) (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
T1	Transformer	05963	
U1, 10	Integrated Circuit (Fairchild)	36632	74LS00J
U2, 3, 5	Integrated Circuit (Fairchild)	36621	74LS196J
U4, 6	Integrated Circuit (Fairchild)	36637	74LS90J
U7	Integrated Circuit (Fairchild)	36635	74LS30J
U8, 9	Integrated Circuit (Fairchild)	36528	7474 DC
U11, 12	Integrated Circuit (Fairchild)	36633	74LS10J
U13	Integrated Circuit (Motorola)	36618	MC14585BCLD
U14	Integrated Circuit (Fairchild)	36659	74LS123J
VR1, 2	Diode, Zener	33543	1N752A
–	Printed Wiring Board	06946	
MP1	Clamp, Transformer, use w/T1	05806	
MP2	Pad, Transistor (Ref. Q6,16,18)	70760	7717-46N-WHITE

CHAPTER 17
IF CONVERTER, A25

17.1 THEORY OF OPERATION

This chapter provides information on the IF Converter module, A25. The module provides the 100 kHz IF signal output to the rear panel connectors J5 and J6. This is accomplished by mixing a 1.5 MHz signal, generated through a crystal oscillator on A25, with the incoming 1.4 MHz IF signal from module A5. The difference of these two signals, taken from a mixer is then filtered and amplified to provide the 100 kHz IF output. Figure 17-1 shows a simplified block diagram of the A25 module while Figure 17-2 shows its schematic diagram.

The 100 kHz IF Converter Module, A25, accepts the 1.4 MHz IF receiver output and converts, using the superheterodyne principle, to a 100 kHz center frequency to provide the receiver with an IF output. The 1.4 MHz signal is applied to a mixer, U2. The other input to the mixer is received from a 1.500 MHz crystal-stabilized local oscillator. The oscillator is also phase-locked to a 50 kHz reference input. The mixer output is applied to a low-pass filter which selects the low frequency or difference (1.500 – 1.400 = 0.100 MHz) output which is then applied to two output line drivers which outputs to two rear panel connectors, J5 and J6.

The local oscillator consists of field effect transistor Q1, crystal Y1 and associated components. It is voltage-controlled by means of varicaps, CR4 and CR5, which are capable of pulling the crystal frequency sufficiently to effect small corrections. The oscillator output is sampled and applied to a divide-by-300 counter, U4, U5 and U6, and compared by phase comparator U10 to the 50 kHz reference after dividing by 10 at U9. The net output of the phase comparator is a dc voltage, amplified by Q4, to adjust the oscillator frequency and phase. The 50 kHz reference is received from the A11A1 lower loop synthesizer.

The divide-by-300 counter consists of three decade counters U4, U5 and U6, connected in tandem and capable of a maximum count of 1000. The preset inputs are strapped to start a count with 700. Each time a full count has been reached (1000), a positive-going final carry pulse is used to re-apply the preset number to the input, thus allowing the counter to count between 700 and 1000 (1000 – 700 = 300). The 1.500 MHz from the oscillator is divided by 300 to give 5 kHz.

The mixer U2 output is applied to a low pass filter consisting of L2, L3, C15, C16 and C17. It is then amplified by Q2 and by operational amplifier U3 as one output while Q3 and U7 provide the second output. U3 and U7 are connected as line drivers, matched to the IF output for the receiver.

The A25 module contains braodband components and therefore its passband is wide compared to the IF filters. The low pass filter attenuates all other frequencies, except the desired 100 kHz IF signal, to +55 dB.

17.2 IF CONVERTER A25 TEST FIXTURE

Troubleshooting and alignment of the IF Converter module A25 is accomplished through the use of the RACAL IF Converter A25 test fixture and associated test equipment. The test fixture provides a convenient base to mount the A25 module for testing, while also providing easy access to all areas of the PC board. The input and output ports are located on the rear apron, the side and the front of the test fixture, with all controls located on the front apron.

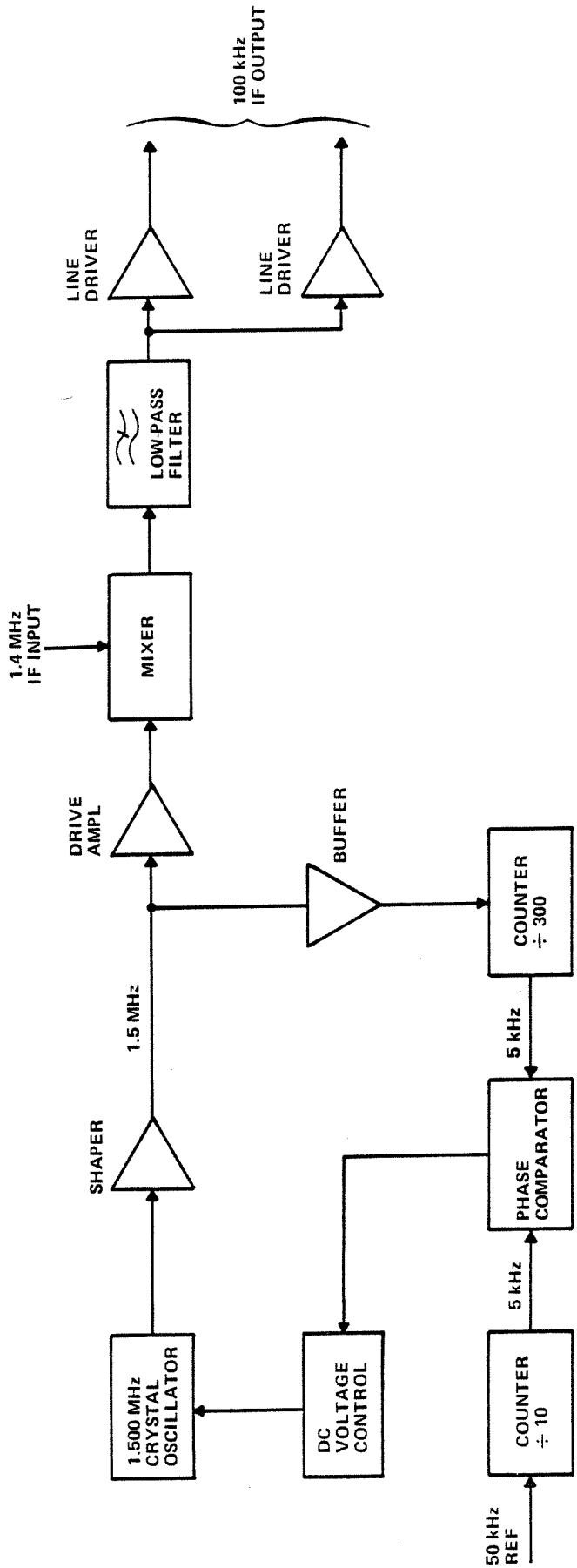


Figure 17-1. Simplified Block Diagram, 100 kHz IF Converter, A25

NOTES:

1. UNLESS OTHERWISE NOTED:
   ALL RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K= 1,000 M=1,000,000
2. ALL CAPACITOR VALUES ONE OR GREATER ARE IN PICO FARRADS, LESS THAN ONE ARE IN MICRO FARRADS
3. ALL INDUCTOR VALUES ONE OR GREATER ARE IN MICRO HENRIES, LESS THAN ONE ARE IN HENRIES

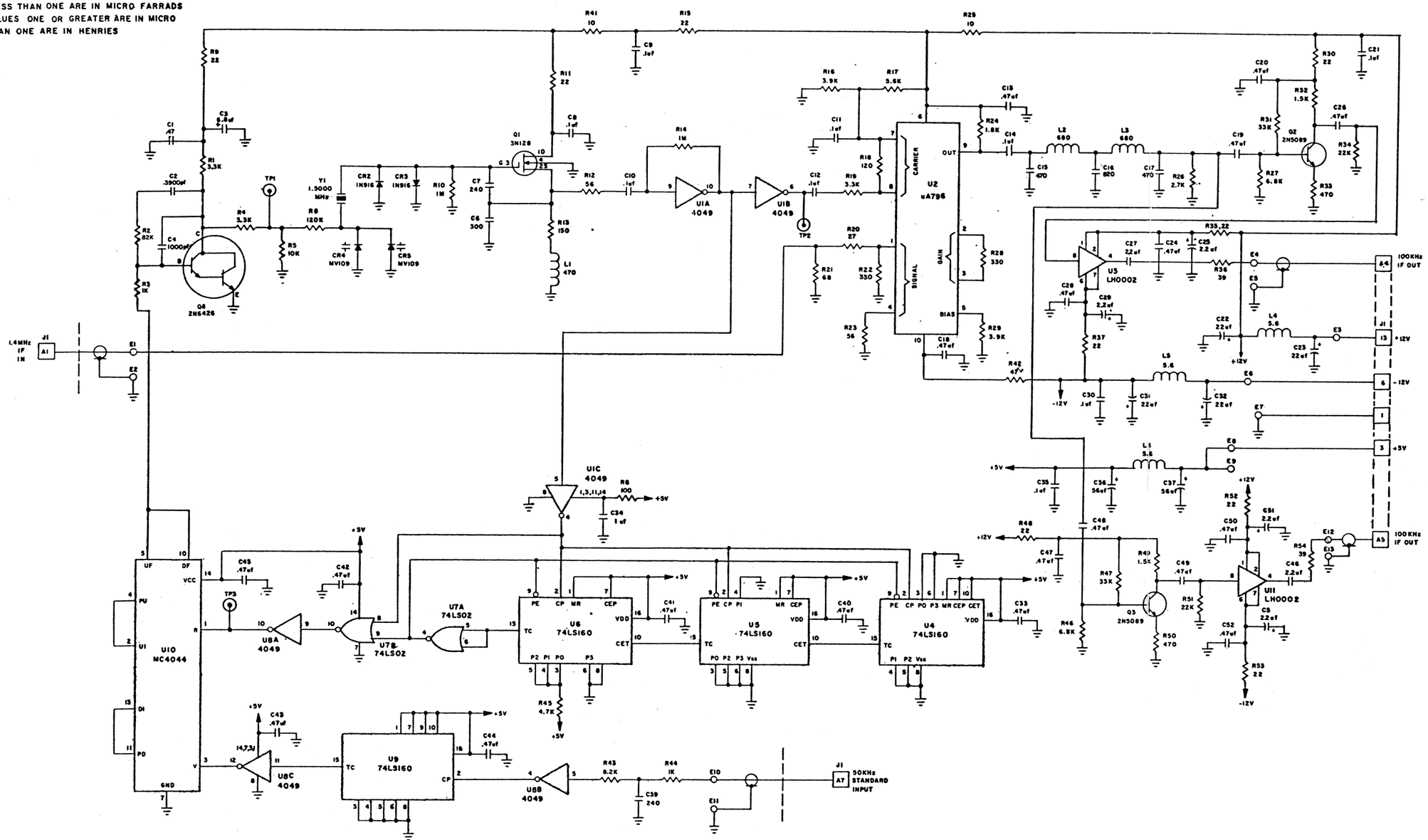


Figure 17-2. Schematic Diagram, IF Converter, A25

The front apron controls for the module, control the IF gain to the A25 module. Enclosed within the test fixture is a spectrally clean 1.4 MHz signal device for carrier re-insertion to the module under test. A 1 MHz oscillator with a divide-by-20 circuit provides the 50 kHz reference signal. All associated test equipment is interfaced to the test fixture via BNC chassis mounted connectors. Figure 17-3 shows the IF Converter A25 test fixture. Figure 17-4 shows the overall assembly of the A25 module, while Figure 17-4B shows the circuit card assembly.

17.3 TEST EQUIPMENT AND ACCESSORIES

To perform troubleshooting and alignment, using the test fixture, requires the use of additional test equipment and accessories. This additional equipment is used to inject signals, provide power, monitor signals and their levels, make connections and to signal trace. The test equipment and accessories required are listed in Table 17-1.

Table 17-1. Test Equipment and Accessories

Item	Description	Equipment Recommended or Equal
1	Spectrum Analyzer	HP141T, 8552B or 8553B
2	Frequency Counter	Dana 8030B
3	Oscilloscope	Tektronix 465
4	Digital Multimeter	Data Precision 248
5	DC Power Supply	Racal
6	Test Fixture	Racal
7	Coaxial Cable	50 ohm (RG58A)

17.4 TEST AND ALIGNMENT

The following procedures are provided to properly test the A25 module. All tests should be performed at ambient room temperature. Record all test data on test data sheet, page 17-12.

17.4.1 Test Set-Up

1. Connect the A25 Module under test into the test fixture and connect the cable to the module.
2. Connect the DC power supply to the test fixture via the octal plug on the side of the test fixture.
3. Apply DC power to the test fixture.

17.4.2 Phase Lock and Output Check

1. Connect the digital multimeter to TP1 using the 10 VDC scale. Ensure that the measured

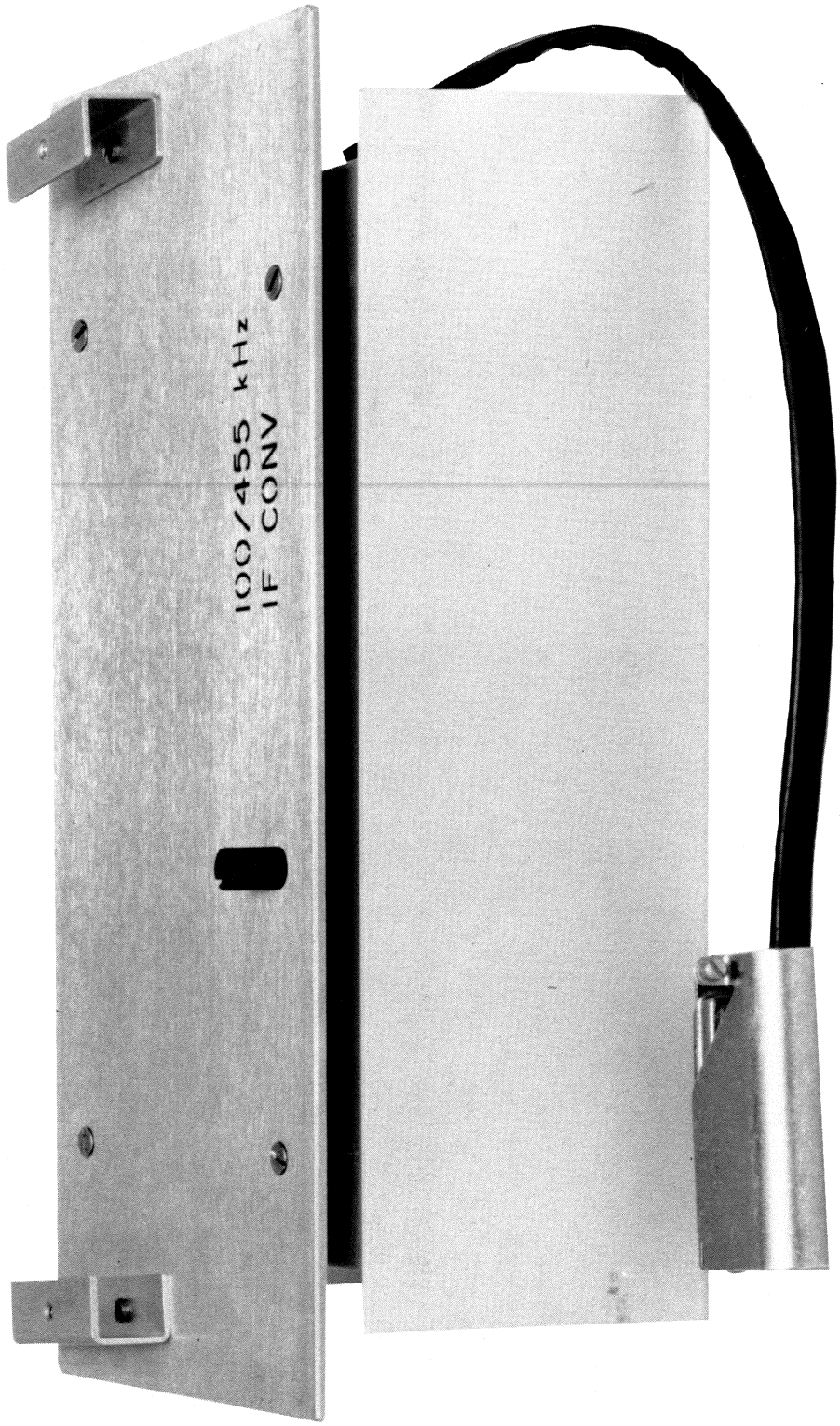


Figure 17-3. IF Converter A25, Test Fixture

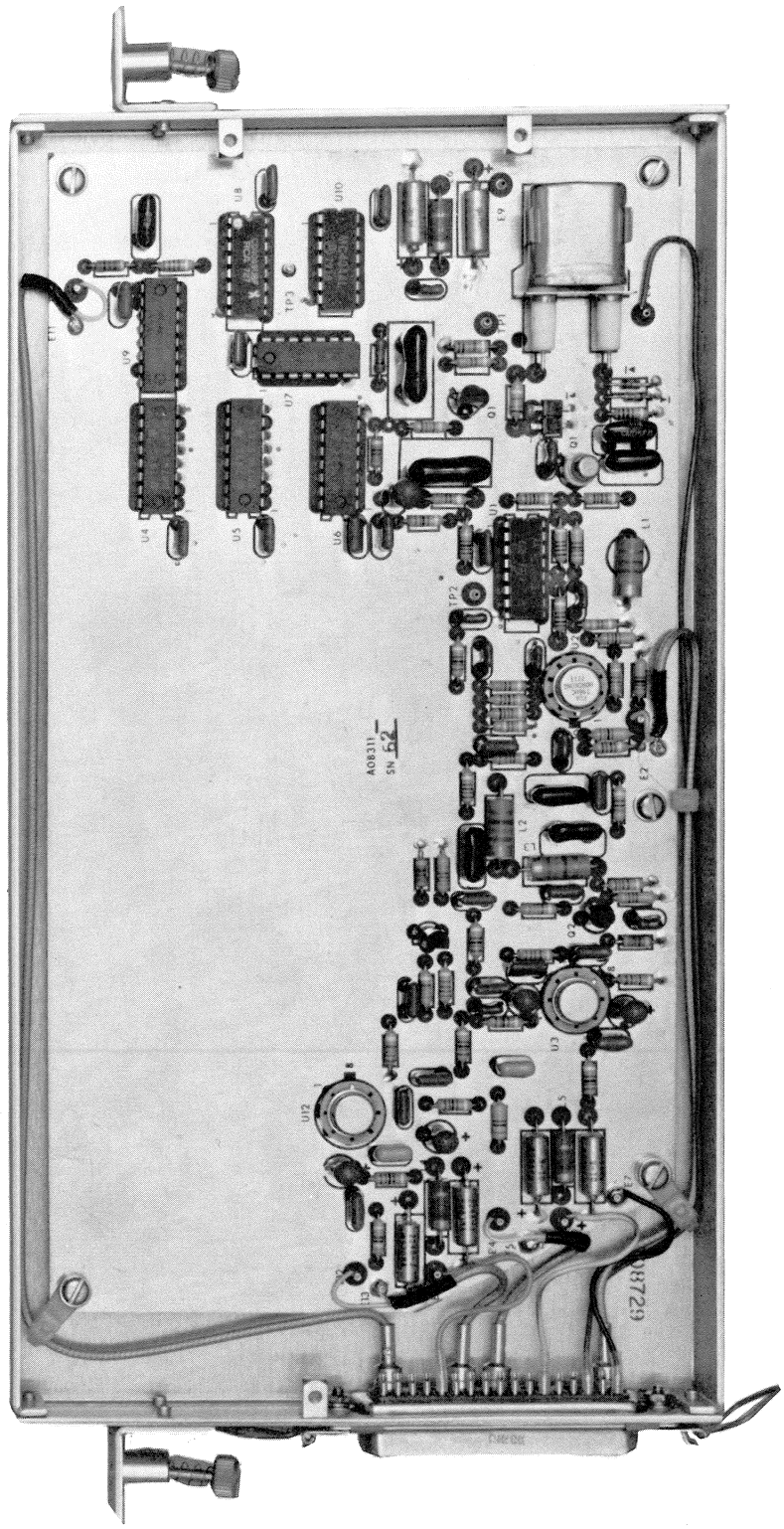


Figure 17-4A. IF Converter A25, Overall Assembly

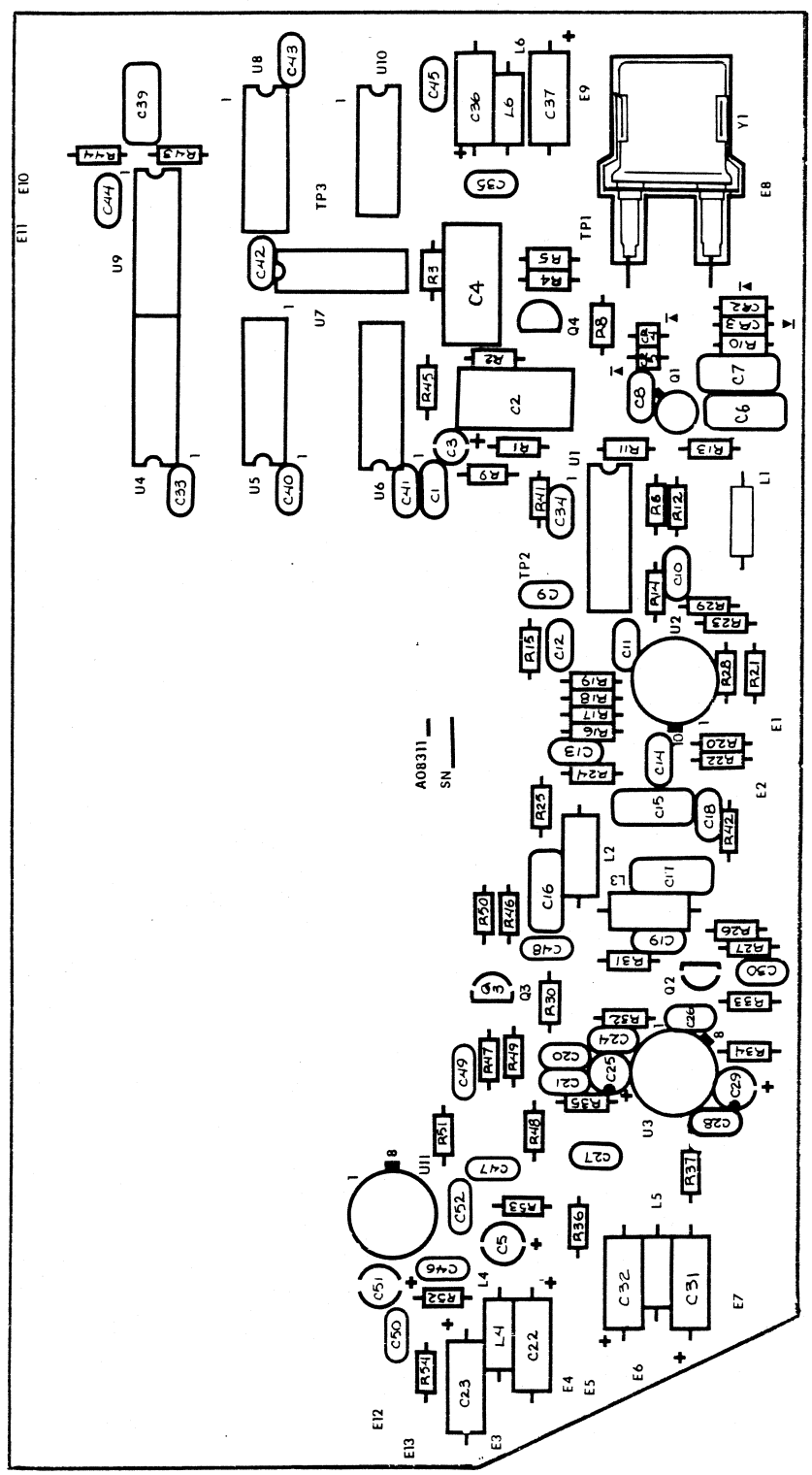


Figure 17-4B. IF Converter A25, Circuit Card Assembly

voltage is between 3.25 and 6.00 volts. Record on test data sheet.

2. Using the oscilloscope, 0.1 uSec/CM Time Base and 0.5 V/CM vertical scale sensitivity, place a 10X probe on the crystal lead nearest CR-2 and CR-3. Ensure the waveform is a good sine wave with an amplitude of approximately 1.4 p-p. Record results.

3. Using the frequency counter and a 1X oscilloscope probe, connect the counter to U1 pin 6 and ensure the frequency is 1.500000 MHz ±10 Hz. Record results.

4. Using the oscilloscope with Time Delay feature, connect Channel 1 input to U10 pin 1 and Channel 2 to U10 pin 3. Use 2V/CM vertical scale sensitivity. Place the A sweep Time Base to 50 uSec/CM and the B delayed sweep to 0.1 uSec/CM. Engage the Time Delay controls. The waveforms observed should be similar to Figure 17-5. Record results.

5. Preset the spectrum analyzer controls as follows:

Reference Frequency	Center
Counter Frequency	Past Center
Sweep Mode	Auto
Vertical Scale Range	1 dB/div
Store	High Defn
Display	Read in B/U and Peak Mem not selected
Horizontal Scale	10
Horizontal Range	kHz/div
Filter Bandwidth	Normal (2)
Sweep Speed	None Selected
Vertical Scale	−10 dBm
Add	as required
Reference Frequency	100 kHz
Graticule	All knobs in Cal Position

6. Connect the 100 kHz OUT port 1F1 on the rear of the test fixture to the 50 Ohms input port of the spectrum analyzer via a 50 Ohms coaxial cable (RG-58A).

7. Measure the output level of the module under test and ensure that its output level is within −10 to −8 dBm. Record results.

8. Reconnect the second 100 kHz OUT port 1.5.2 to the analyzer using 50 Ohms cable.

9. Measure the output level and check to see that it is within −10 to −8 dBm. Record results.

17.4.3 Spectrum Analysis and Spurious Emission Check

1. Change the following settings on the spectrum analyzer as follows:

Reference Frequency	L.H.
Vertical Scale Range	10 dB/div
Horizontal Scale	.5
Horizontal Range	MHz/div
Vertical Scale	+10 dBm
Filter Bandwidth	Narrow (1)

2. With the spectrum analyzer connected to the 100 kHz OUT port on the rear of the test fixture ensure that all signals within the range of frequencies from DC to 5 MHz are at

least −55 dB below the 100 kHz OUT frequency level of the I.F. Converter. Record.

3. Remove DC power from the test fixture and remove the module under test from the test fixture.

17.4.4 Corrective Action

If any of the above tests, fail to produce the required results, isolate the fault to a function (VCO, phase comparator, etc.) through the test procedures. The procedures may also be used to isolate certain groupings within a particular function, for instance, steps 2 and 3 in paragraph 17.4.2 could isolate a fault to the VCO and associated components, if the results of those steps are not correct. Further signal tracing may then be accomplished, using the oscilloscope or voltmeters, to trace the fault to a single component. Maximum use, should also be made, of the test points provided on the A25 module, and faults isolated between them before signal tracing to a particular component.

When replacing faulty components, care should always be taken, so that the new component, adjacent components, or the printed circuit card is not damaged. Heat sinks should be used on semiconductor and other sensitive components when soldering. Use the proper wattage soldering iron, too much heat can cause damage to the circuit card and or adjacent components as well as the new component being installed.

After any component has been replaced, alignment for that function and following functions must be checked as outlined in paragraphs 17.4.1 through 17.4.3.

17.5 PARTS LIST, IF CONVERTER, A25

The parts list for the A25 module is contained in Table 17-2.

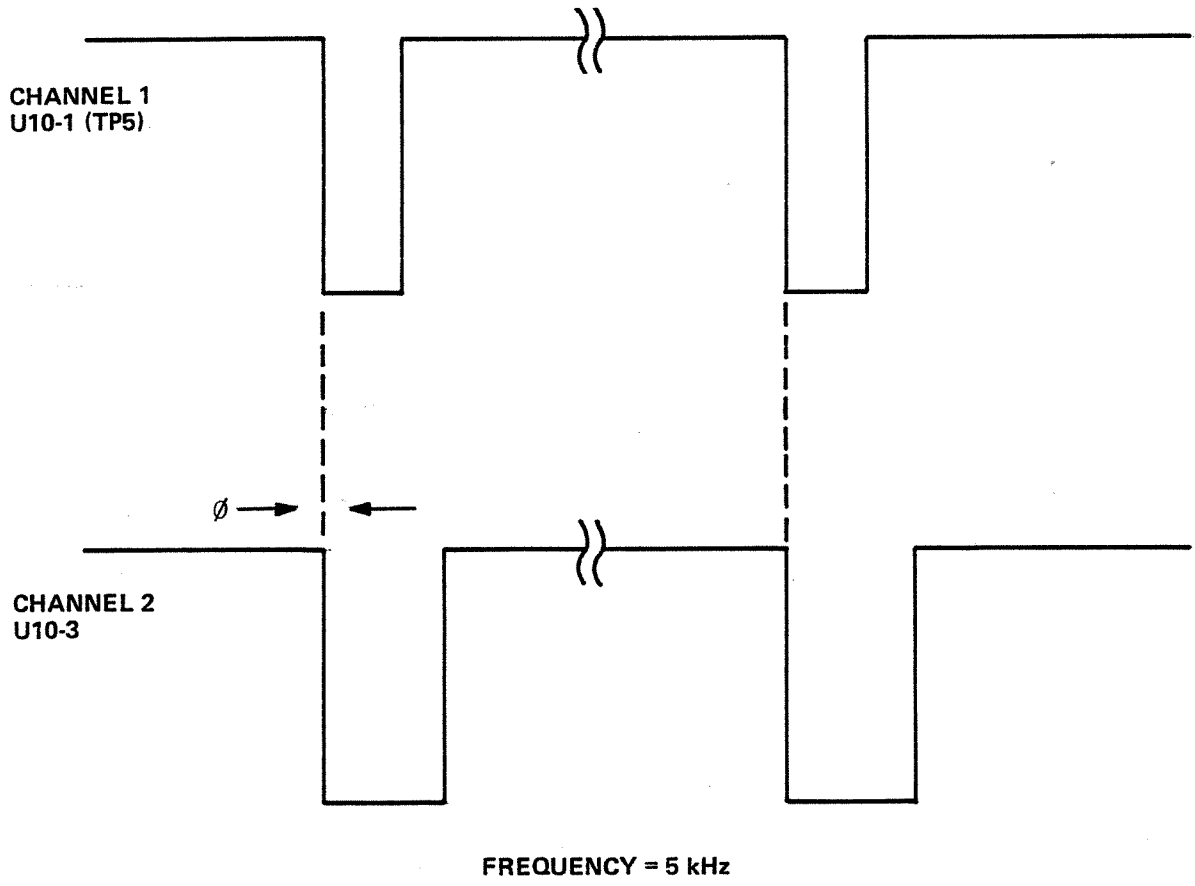


Figure 17-5. Phase Comparator Input Signals

DATE _____
CKD BY _____

MODULE A25
USED ON _____

TEST DATA SHEET

PART NAME: A25 100 kHz IF Converter
PART NUMBER: 08344
USED ON: _____

JOB NO: _____
SERIAL NO: _____

TEST PARA.	DESCRIPTION	MEAS	LIMITS		UNITS
			MIN	MAX	
17.4.2(1)	In Lock Voltage		3.25	6.00	Volts
17.4.2(2)	Crystal Activity Waveform		Pass	Fail	
	Amplitude		Pass	Fail	
17.4.2(3)	Crystal (Loop) Frequency 1.500 MHz		-10	+10	
17.4.2(4)	Phase Lock Check		Pass	Fail	
17.4.2(7)	OUTPUT Level (A4)		-10	-8	dBm
17.4.2(9)	OUTPUT Level (A5)		-10	-8	dBm
17.4.3(2)	Spectrum Check DC to 5 MHz		55		dB

TABLE 17-2. PARTS LIST, IF CONVERTER MODULE ASSEMBLY (A25) 08344

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
A1	IF Converter Circuit Card Assembly (See Table 17-3 for further breakdown)	08311	
J1	Connector (Cannon)	61186	DDM-24W7P
J1A1, J1A4, J1A5, J1A7	Connector (Cannon)	60021	DM53740-5008
W1	Cable Assembly	08941	
–	Module Case Assembly	08729	
–	Cover Assembly	06724	
–	Spring Latch	61183	D110279

TABLE 17-3. PARTS LIST, IF CONVERTER CIRCUIT CARD ASSEMBLY, A25A1 08311

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
C1, 13, 18-20, 24, 26, 28, 33, 40-45, 47-50, 52	Capacitor, Ceramic, 0.47 uF, ±20% (Erie)	21761	8131-050-651-474M
C2	Capacitor, Mica 3900 pF, ±5%	22131	CM06F392G03
C3	Capacitor, Tantalum, 6.8 uF, ±20% (Kement)	25032	T368B685M035AS
C4	Capacitor, Mica, 1000 pF, ±5%	22110	CM06F102G03
C5, 25, 29, 51	Capacitor, Tantalum, 2.2 uF, ±20% (Kement)	25048	K2R2E35
C6	Capacitor, Mica, 300 pF, ±5%	22035	CM05F301JN3
C7, 39	Capacitor, Mica, 240 pF, ±5%	22032	CM05F241JN3
C8-12, 14, 21, 30, 35	Capacitor, Ceramic, 0.1 uF, ±20% (Erie)	21732	8131-050-651-104M
C15, 17	Capacitor, Mica, 470pF, ±5%	22086	CM15F471J500
C16	Capacitor, Mica, 820 pF, ±5%	22156	CD15FC821G03
C22, 23, 31, 32	Capacitor, Tantalum, 22 uF, ±20%	25052	M39003/01-2272
C27, 46	Capacitor, Ceramic, 2.2 uF, ±20%	21766	8141-050-651-225M
C34	Capacitor, Ceramic, 1.0 uF, ±20% (Erie)	21748	8131-050-651-105M
C36, 37	Capacitor, Tantalum, 56 uF, ±10%	25053	M39003/01-2246
C38	Not Used		
CR1	Not Used		
CR2, 3	Diode, Silicon, Pin	35514	1N916
CR4, 5	Diode, Varicap, (Motorola)	29014	MV109
L1	Choke, RF, 470 uH, ±5%	43037	MS90539-7
L2, 3	Choke, RF, 680 uH	43043	MS75089-21
L4, 5, 6	Choke, RF, 5.6 uH, ±10%	43027	MS14046-1
Q1	Transistor, MOSFET	32516	3N128
Q2, 3	Transistor, NPN, high power	32021	2N5089
Q4	Transistor, NPN, Darlington	31265	2N6426
R1, 4, 19	Resistor, Film, 3.3K Ohms, ±2%, ¼W	12161-332	RL07S332G
R2	Resistor, Film, 82 Ohms, ±2%, ¼W	12161-823	RL07S823G

TABLE 17-3. PARTS LIST, IF CONVERTER CIRCUIT CARD ASSEMBLY, A25A1 (Cont.)

Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R3	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R5	Resistor, Film, 10K Ohms, ±2%, ¼W	12161-103	RL07S103G
R6	Resistor, Film, 100 Ohms, ±2%, ¼W	12161-101	RL07S101G
R7, 38-40	Not Used		
R8	Resistor, Film, 120K Ohms, ±2%, ¼W	12161-124	RL07S124G
R9, 11, 15, 30, 35, 37, 48, 52, 53	Resistor, Film, 22 Ohms, ±2%, ¼W	12161-220	RL07S220G
R10, 14	Resistor, Film, 1.0 meg Ohms, ±2%, ¼W	12161-105	RL07S105G
R12, 23	Resistor, Film, 56 Ohms, ±2%, ¼W	12161-560	RL07S560G
R13	Resistor, Film, 150 Ohms, ±2%, ¼W	12161-151	RL07S151G
R16, 29	Resistor, Film, 3.9K Ohms, ±2%, ¼W	12161-392	RL07S392G
R17	Resistor, Film, 5.6K Ohms, ±2%, ¼W	12161-562	RL07S562G
R18	Resistor, Film, 120 Ohms, ±2%, ¼W	12161-121	RL07S121G
R20	Resistor, Film, 27 Ohms, ±2%, ¼W	12161-270	RL07S270G
R21	Resistor, Film, 68 Ohms, ±2%, ¼W	12161-680	RL07S680G
R22,28	Resistor, Film, 330 Ohms, ±2%, ¼W	12161-331	RL07S331G
R24	Resistor, Film, 1.8K Ohms, ±2%, ¼W	12161-182	RL07S182G
R25, 41	Resistor, Film, 10 Ohms, ±2%, ¼W	12161-100	RL07S100G
R26	Resistor, Film, 2.7K Ohms, ±2%, ¼W	12161-272	RL07S272G
R27, 46	Resistor, Film, 6.8K Ohms, ±2%, ¼W	12161-682	RL07S682G
R31, 47	Resistor, Film, 33K Ohms, ±2%, ¼W	12161-333	RL07S333G
R32, 49	Resistor, Film, 1.5K Ohms, ±2%, ¼W	12161-152	RL07S152G
R33, 50	Resistor, Film, 470 Ohms, ±2%, ¼W	12161-471	RL07S471G
R34, 51	Resistor, Film, 22K Ohms, ±2%, ¼W	12161-223	RL07S223G
R36, 54	Resistor, Film, 39 Ohms, ±2%, ¼W	12161-390	RL07S390G
R42	Resistor, Film, 47 Ohms, ±2%, ¼W	12161-470	RL07S470G
R43	Resistor, Film, 8.2K Ohms, ±2%, ¼W	12161-822	RL07S822G

TABLE 17-3. PARTS LIST, IF CONVERTER CIRCUIT CARD ASSEMBLY, A25A1 (Cont.)

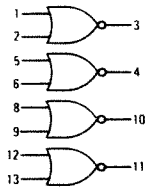
Reference Designation	Description	RACAL Number	Manufacturer /MIL Part Number
R44	Resistor, Film, 1K Ohms, ±2%, ¼W	12161-102	RL07S102G
R45	Resistor, Film, 4.7K Ohms, ±2%, ¼W	12161-472	RL07S472G
U1, 8	Integrated Circuit, Hex Inverter	36576	MC14049BCLD
U2	Integrated Circuit, IF Mixer	36543	UA796HC
U3, 11	Integrated Circuit, Operational Amplifier	36663	LH0002CH
U4, 5, 6, 9	Integrated Circuit, BCD Counter	36702	74LS160
U7	Integrated Circuit, Quad NOR gate	36660	74LS02
U10	Integrated Circuit, Phase Comparator	36662	MC14044BCLD
Y1	Crystal, 1.500000 MHz	37031	CR18A/U
XY1	Crystal, socket	70610	
–	Printed Wiring Board	08312	
–	Pad, Transistor, Ref. Q1	70752	

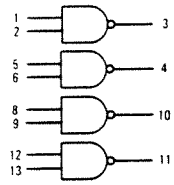
CHAPTER 18
SEMICONDUCTOR LOGIC DIAGRAMS AND PIN LOCATORS

18.1 INTRODUCTION

This section shows the logic diagrams for the various integrated circuits used in the RA6778C Receiver. These diagrams were taken from TEXAS INSTRUMENTS, MOTOROLA, and NATIONAL SEMICONDUCTOR data sheets. They will be useful in locating the various inputs, outputs, power and other connections when probing a circuit.

14001
QUAD 2 INPUT NOR

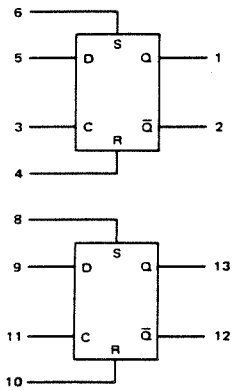




14011
QUAD 2 INPUT NAND

14013
DUAL D TYPE FLIP-FLOP

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

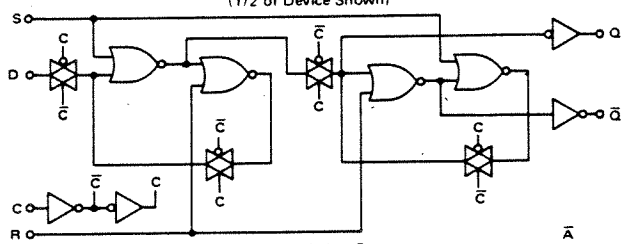
TRUTH TABLE

INPUTS				OUTPUTS	
CLOCK†	DATA	RESET	SET	Q	Q̄
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	Q	Q̄
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	•	•

No Change

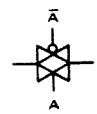
X = Don't Care
† = Level Change
• = Invalid Condition

LOGIC DIAGRAM
(1/2 of Device Shown)

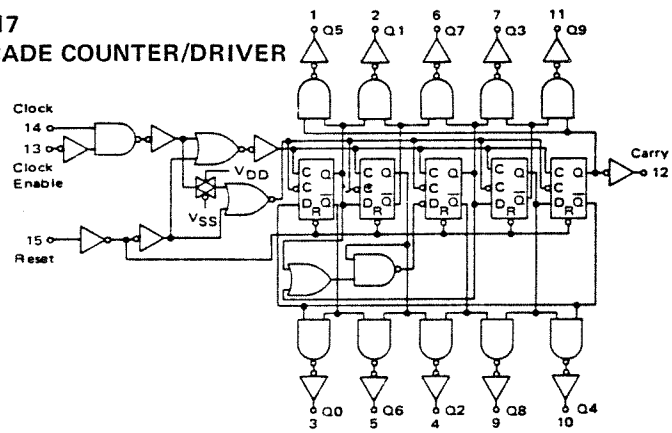


Transmission Gate

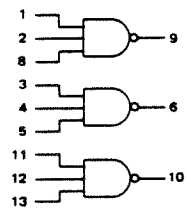
A	CHARACTERISTICS
0	Bidirectional Open Circuit
1	Bidirectional Short-Circuit



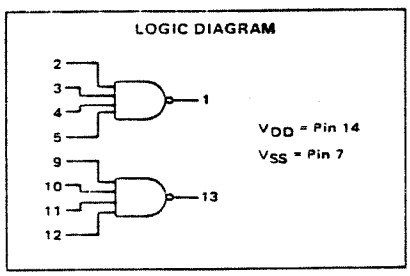
14017
DECADE COUNTER/DRIVER



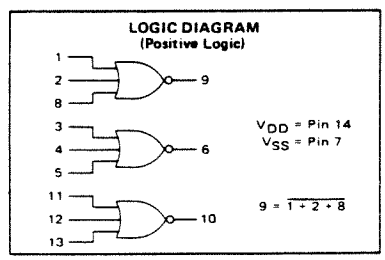
14023
TRIPLE 3 INPUT NAND



14012
DUAL 4 INPUT NAND

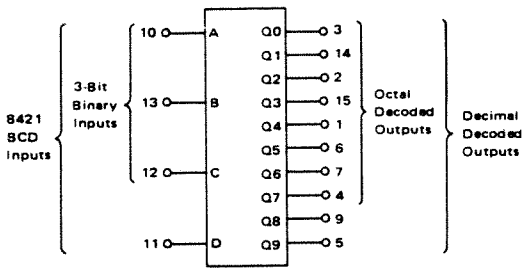


14025
TRIPLE 3 INPUT NOR



14028 BCD/DECIMAL DECODER; BINARY/OCTAL DECODER

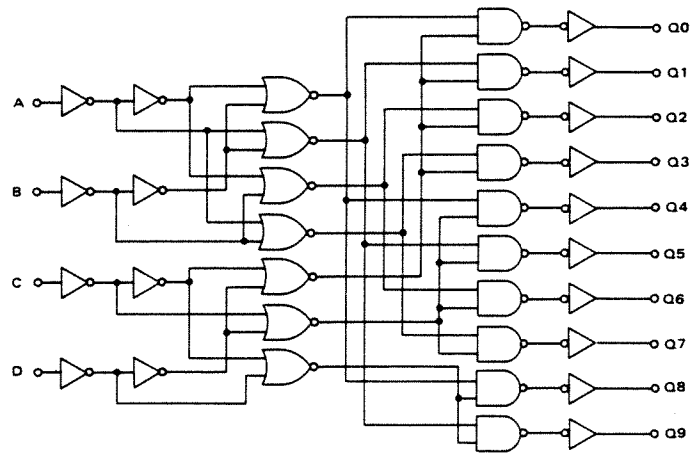
BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

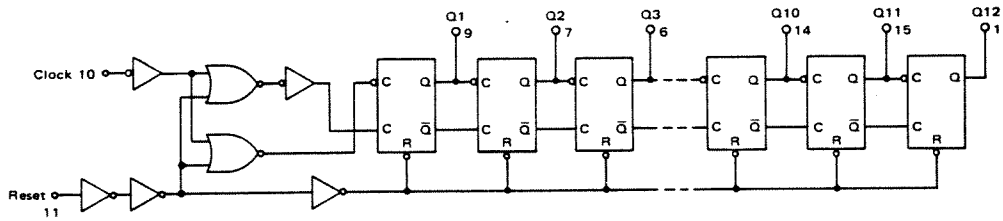
TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0



14040
12 BIT BINARY COUNTER

LOGIC DIAGRAM



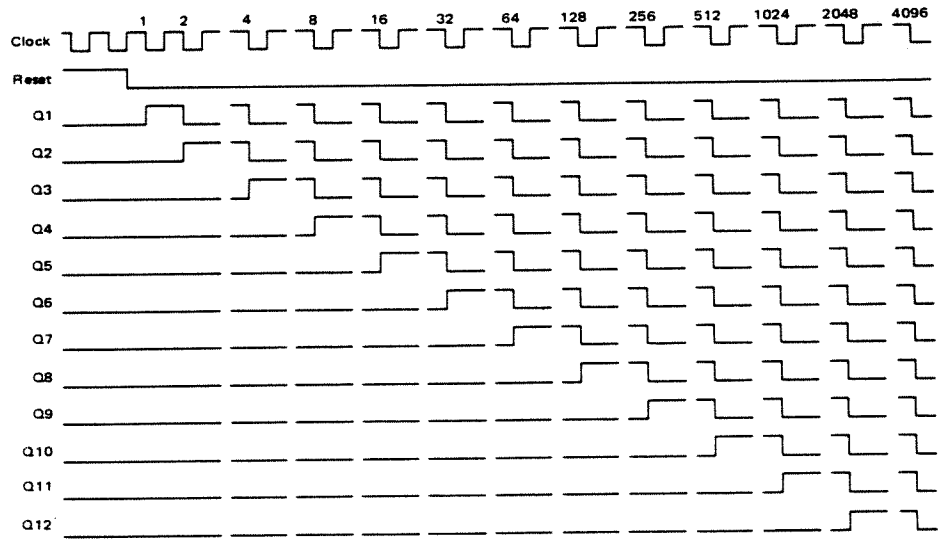
Q4 = Pin 5
Q5 = Pin 3
Q6 = Pin 2
Q7 = Pin 4
Q8 = Pin 13
Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

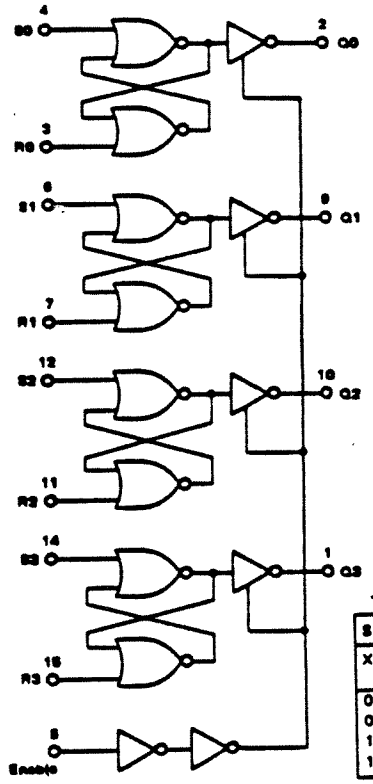
TRUTH TABLE

$\overline{CLOCK}$	RESET	OUTPUT STATE
⎍	0	No Change
⎎	0	Advance to next state
X	1	All Outputs are low

X = Don't Care



14043
QUAD NOR R-S LATCH



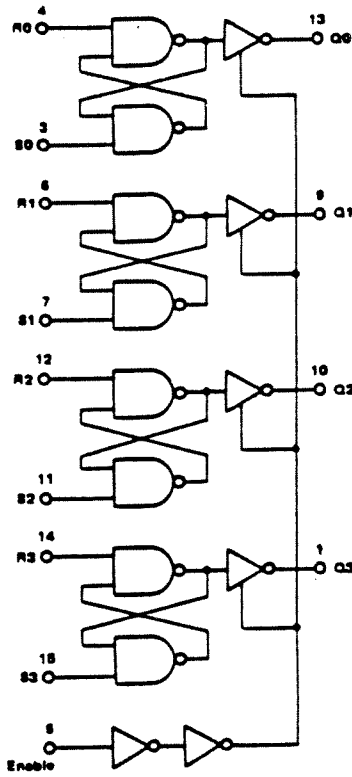
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

14044
QUAD NAND R-S LATCH



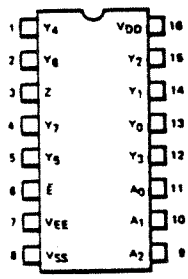
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

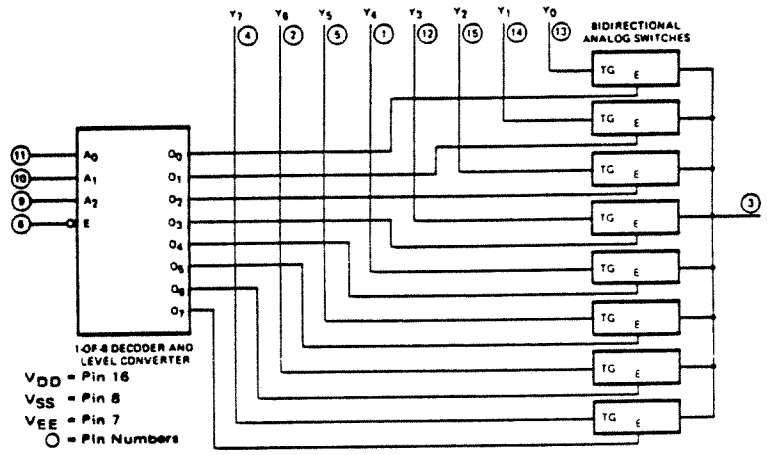
14051
8 CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



TRUTH TABLE

INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

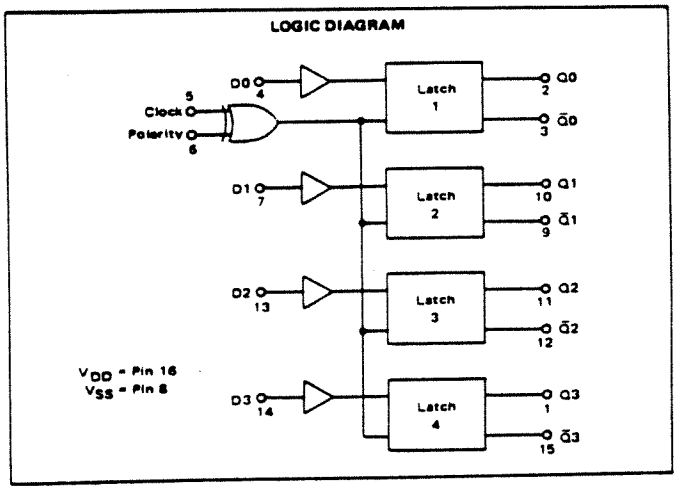
L = LOW Level
H = HIGH Level
X = Don't Care



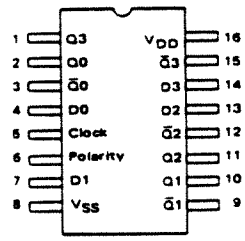
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Numbers

14042
QUAD LATCH

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
⌙	1	Latch

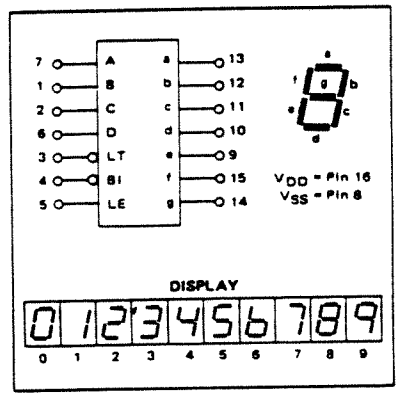
14511
BCD/7-SEGMENT DECODER/DRIVER

TRUTH TABLE

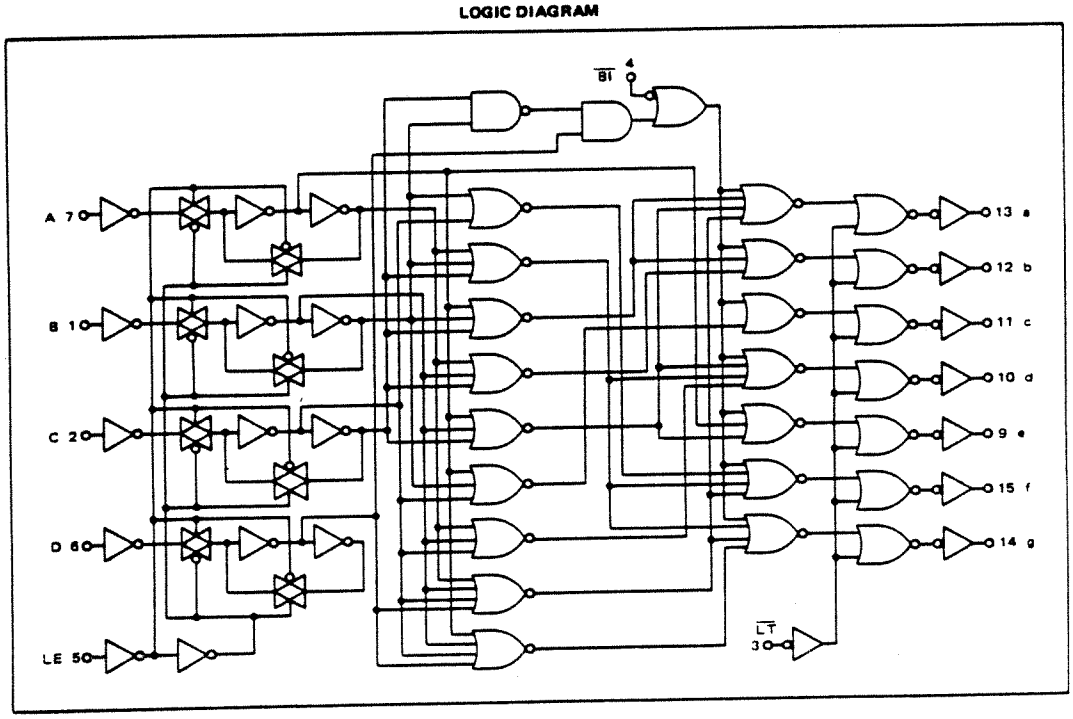
INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X								

X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

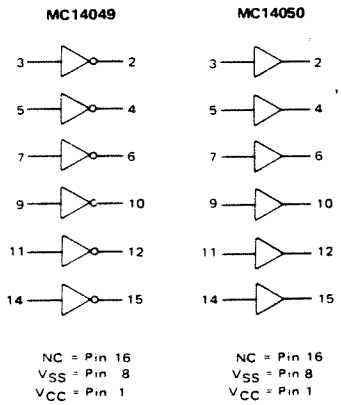


LOGIC DIAGRAM



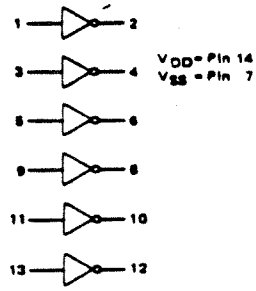
14049/14050
HEX BUFFER

LOGIC DIAGRAMS

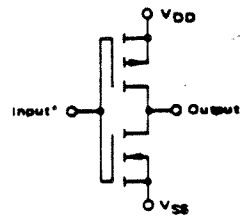


14069
HEX INVERTER

LOGIC DIAGRAM



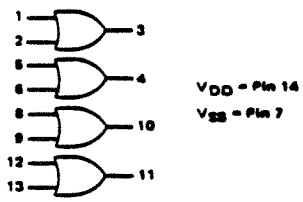
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



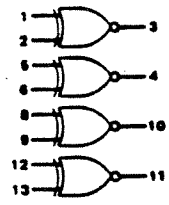
*Double diode protection on all inputs not shown.

14071
QUAD 2-INPUT OR

LOGIC DIAGRAM

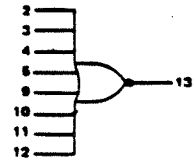


14077
QUAD EXCLUSIVE NOR



VDD = Pin 14
VSS = Pin 7

14078
8-INPUT NOR



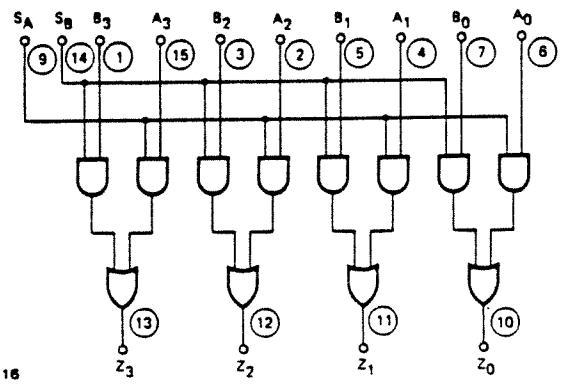
14019/4019
QUAD 2-INPUT MULTIPLEXER

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



VDD = Pin 16
VSS = Pin 8
○ = Pin Number

$Z_n = S_A A_n + S_B B_n$

14510

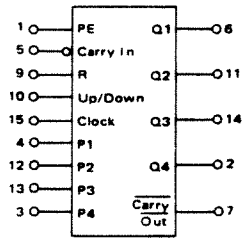
BCD UP/DOWN COUNTER

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

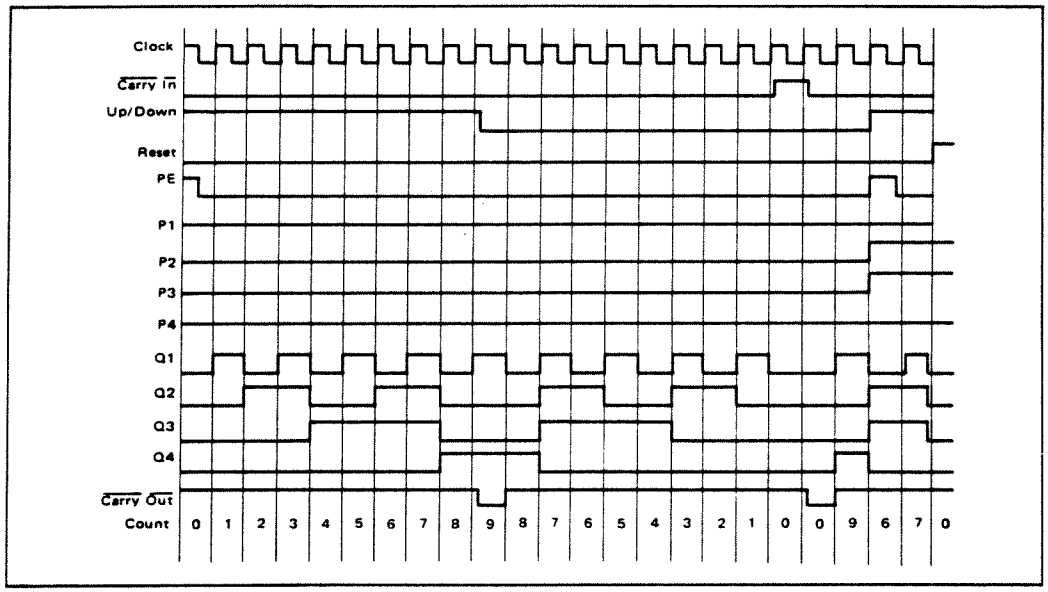
X = Don't Care

BLOCK DIAGRAM

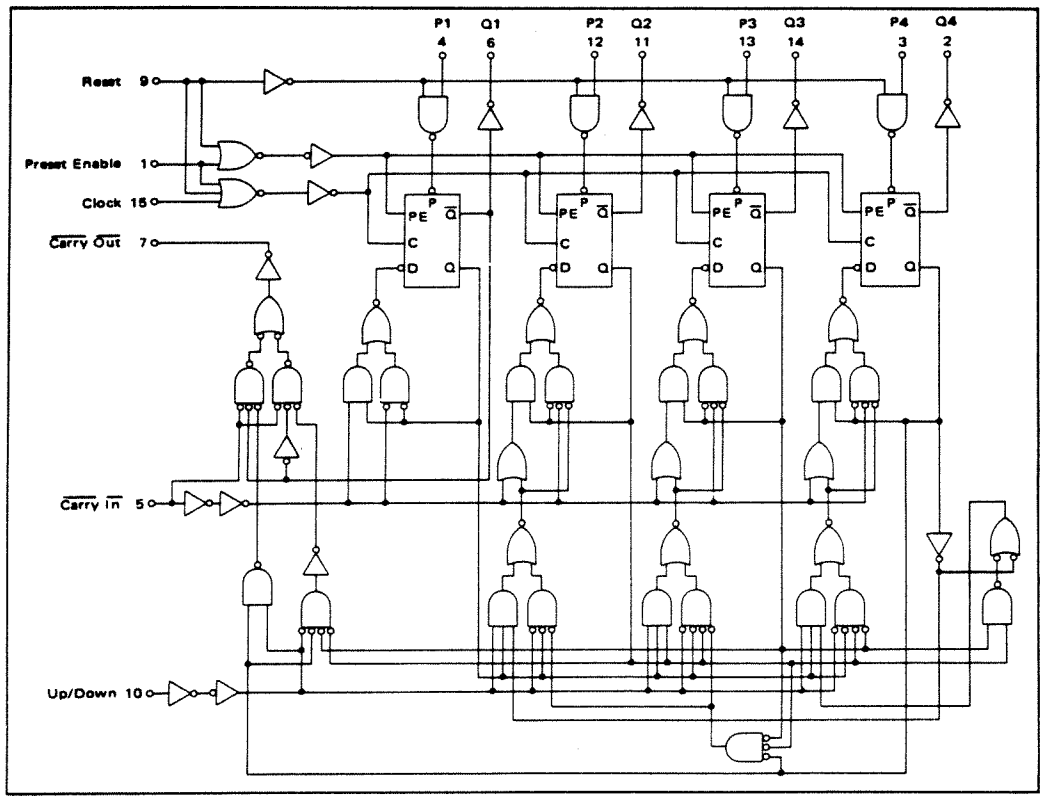


V_{DD} = Pin 16
V_{SS} = Pin 8

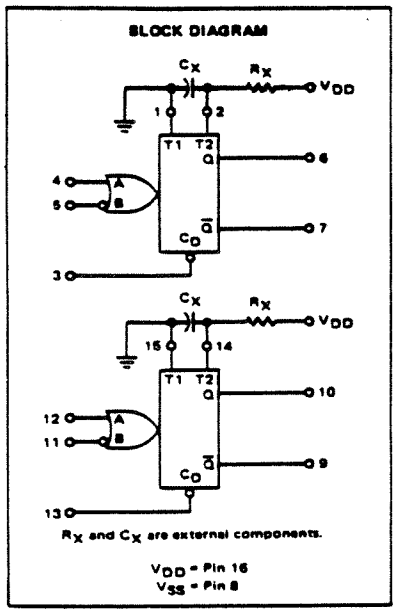
TIMING DIAGRAM

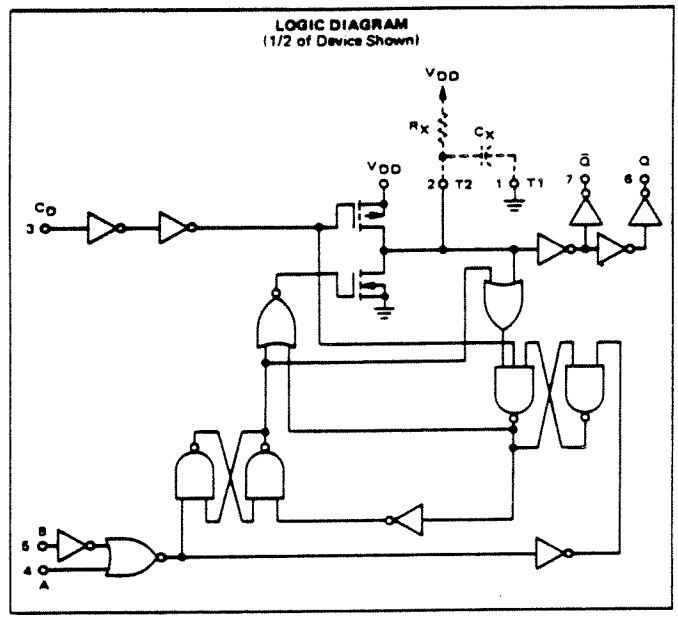


LOGIC DIAGRAM

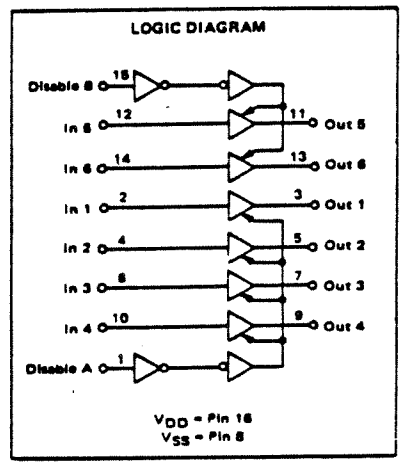


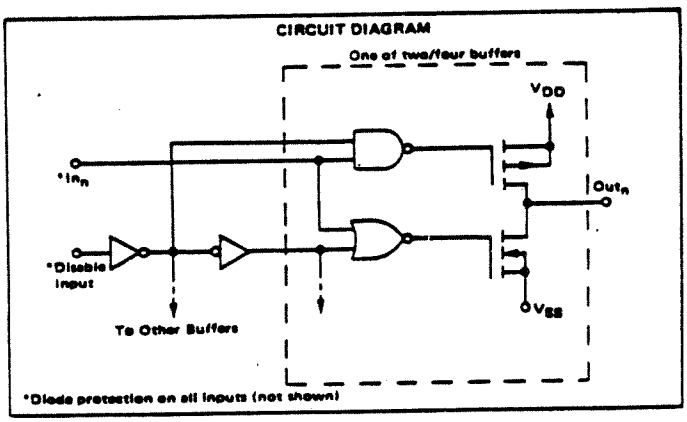
14528
DUAL MONOSTABLE MULTIVIBRATOR





14503
HEX 3-STATE BUFFER





TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

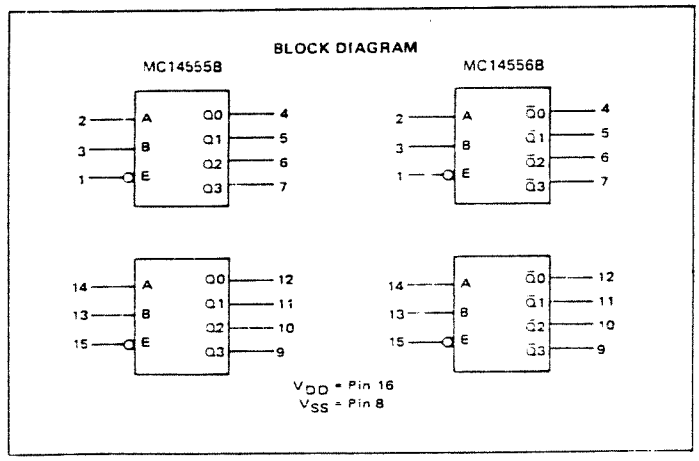
X = Don't Care

14555 14556
DUAL DECODER/DEMULTIPLEXER

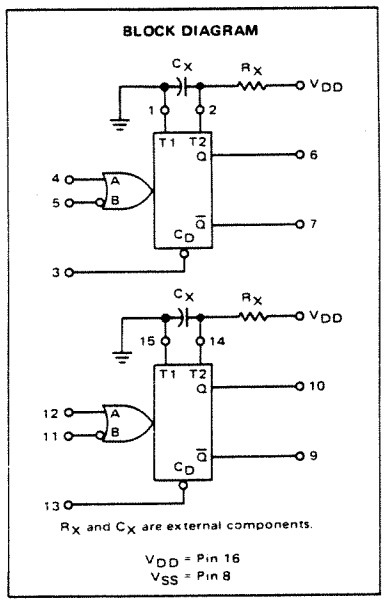
TRUTH TABLE

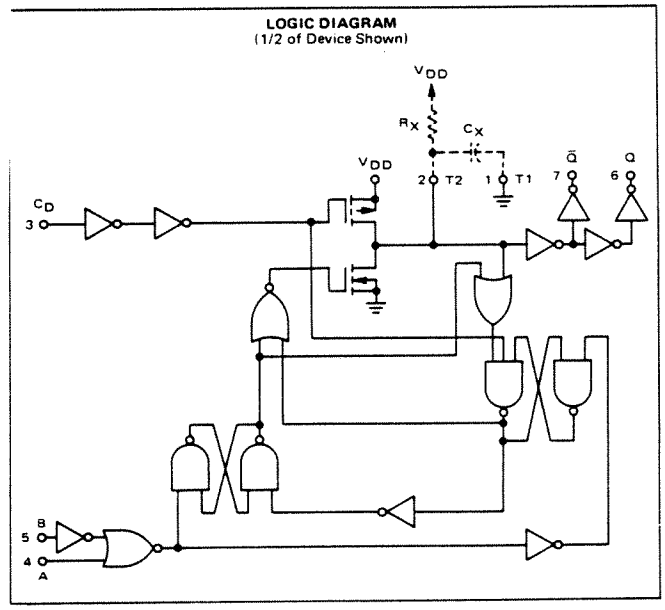
INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
$\bar{E}$	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

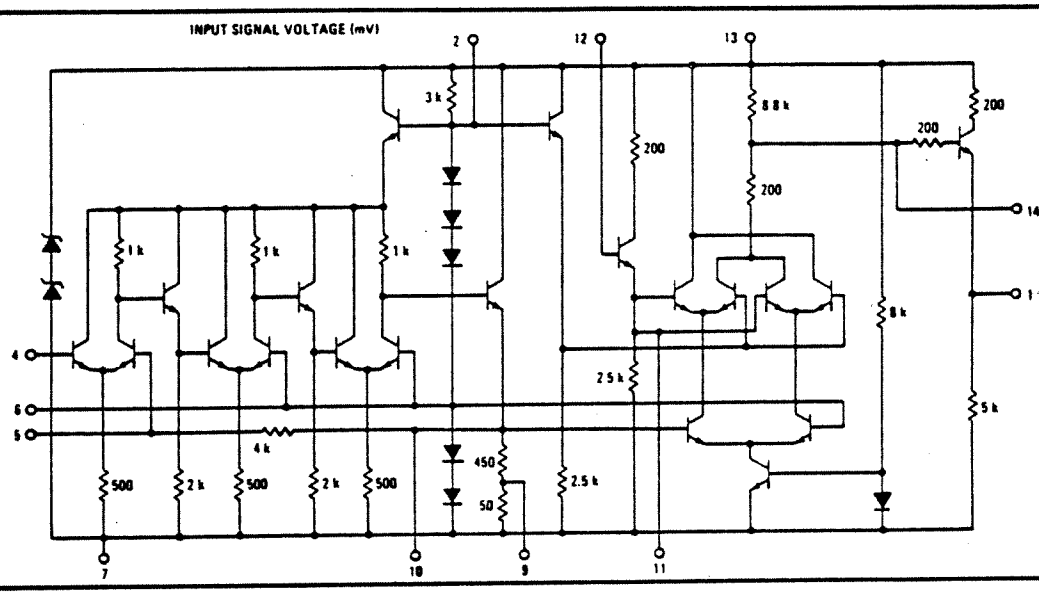


14528
RETRIGGERABLE/ RESETTABLE MONOSTABLE MULTIVIBRATOR

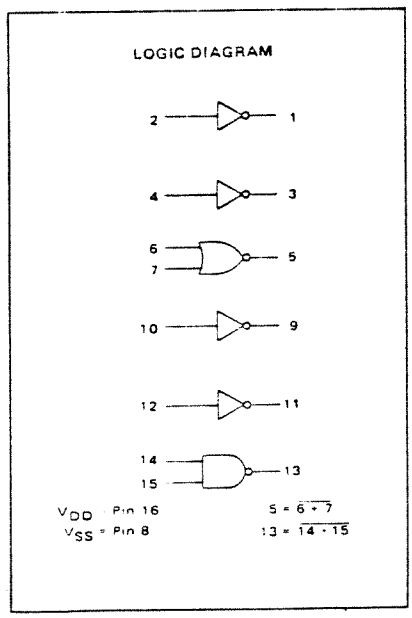




1375
IF AMPLIFIER AND QUADRATURE DETECTOR



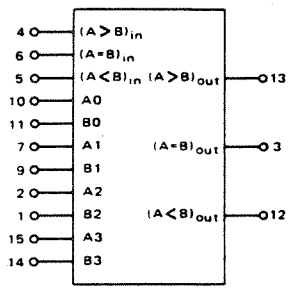
14572
HEXGATE



14585

4 BIT MAGNITUDE COMPARATOR

BLOCK DIAGRAM



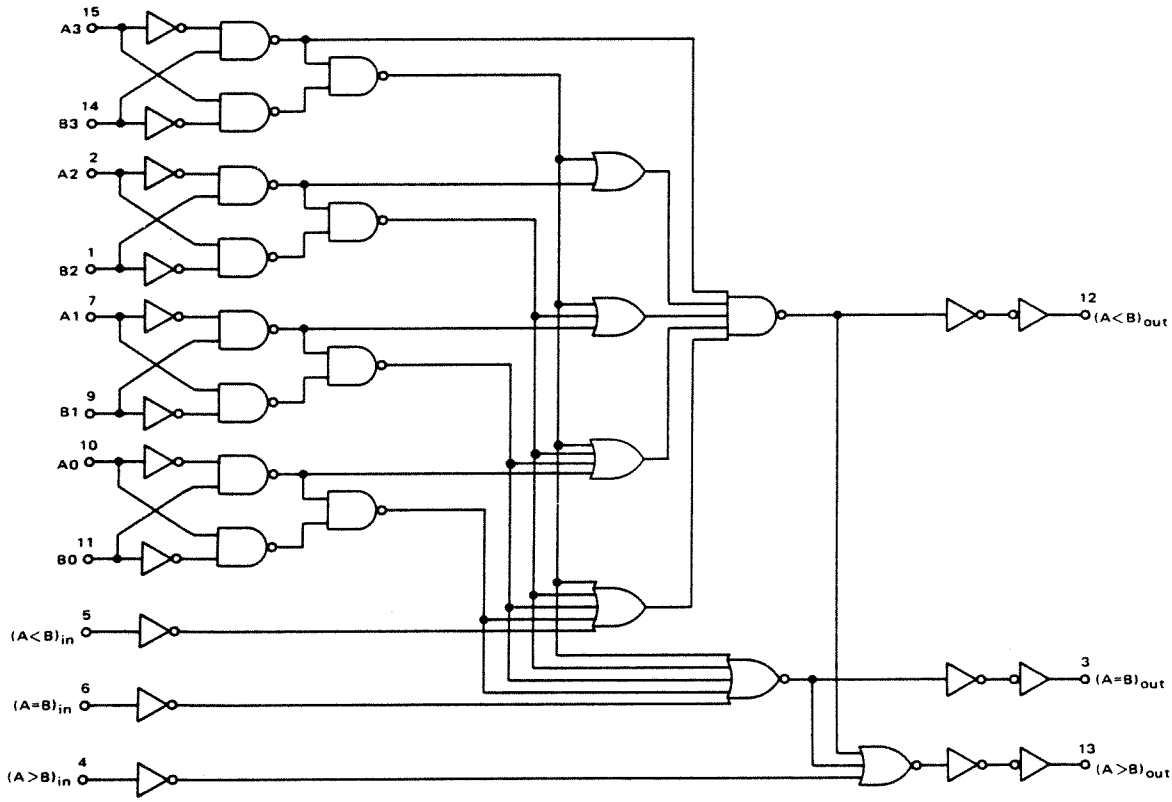
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

LOGIC DIAGRAM



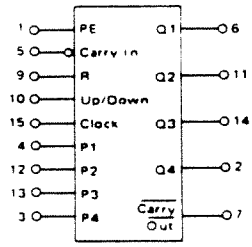
14516
BINARY UP-DOWN COUNTER

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

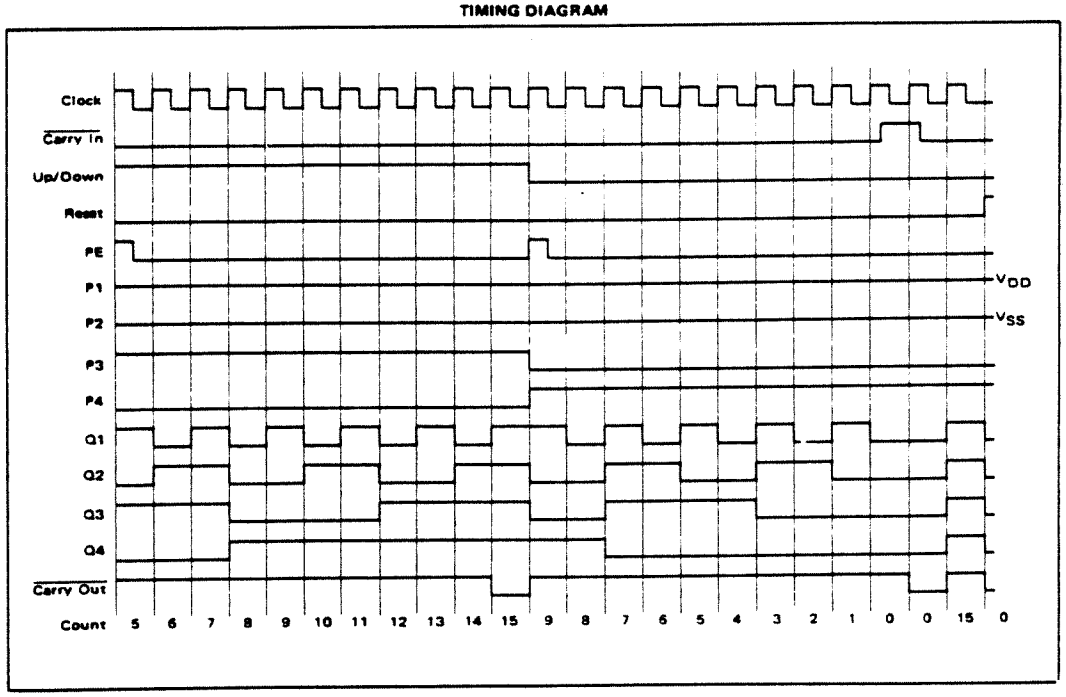
X = Don't Care

BLOCK DIAGRAM



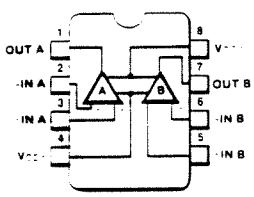
V_{DD} Pin 16
V_{SS} Pin 8

TIMING DIAGRAM



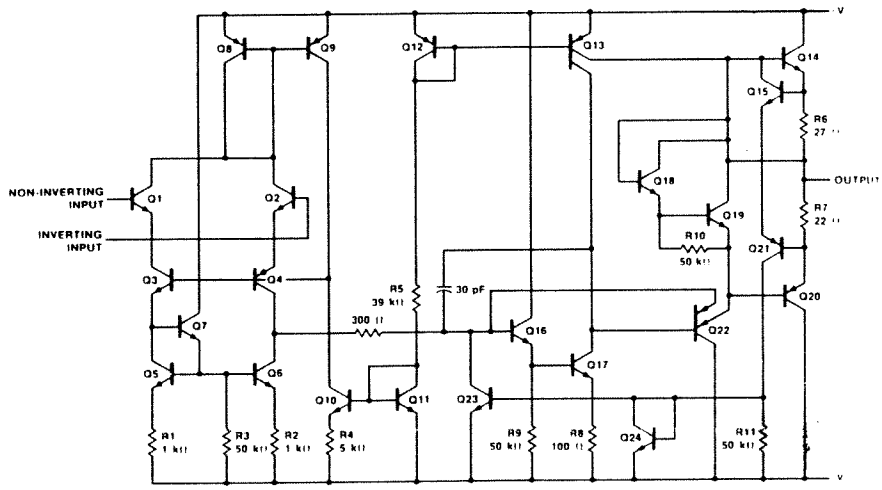
1458
DUAL OPERATIONAL AMPLIFIER

Connection Diagram
8-Pin DIP



(Top View)

Equivalent Circuit



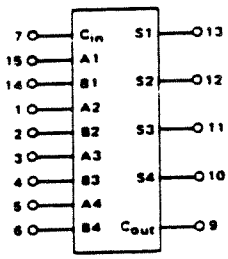
14560
NBCD ADDER (Natural Binary Coded Decimal)

TRUTH TABLE*

INPUT									* OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	0
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

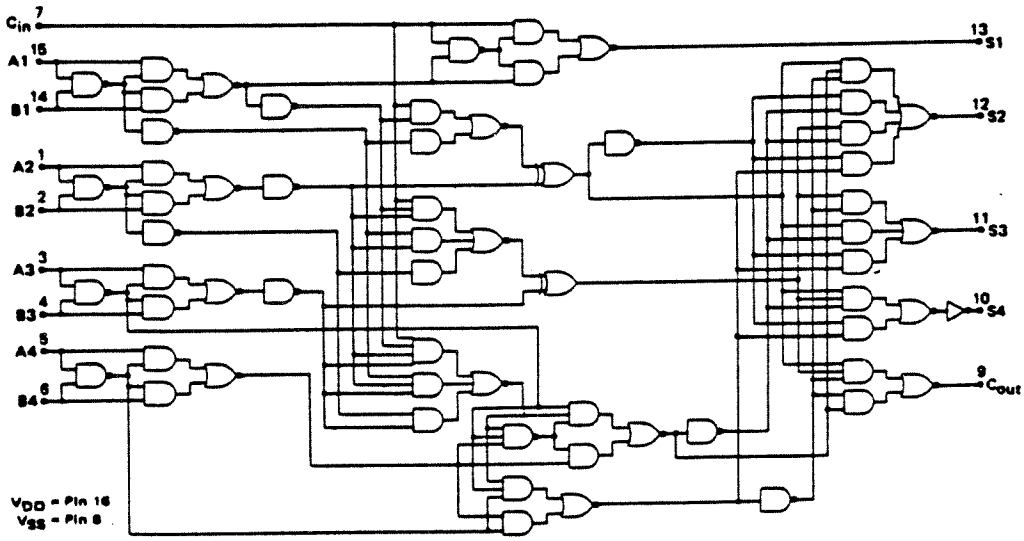
*Partial truth table to show logic operation for representative input values.

BLOCK DIAGRAM

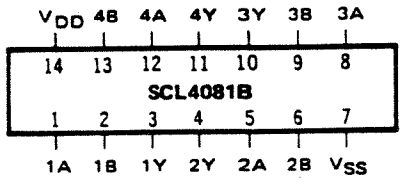


V_{DD} = Pin 16
V_{SS} = Pin 8

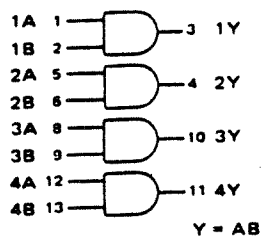
FUNCTIONAL EQUIVALENT LOGIC DIAGRAM



14081
QUAD 2-INPUT AND GATE

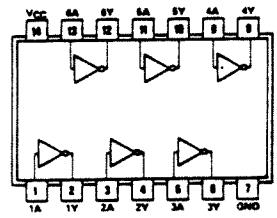


SCL4081B



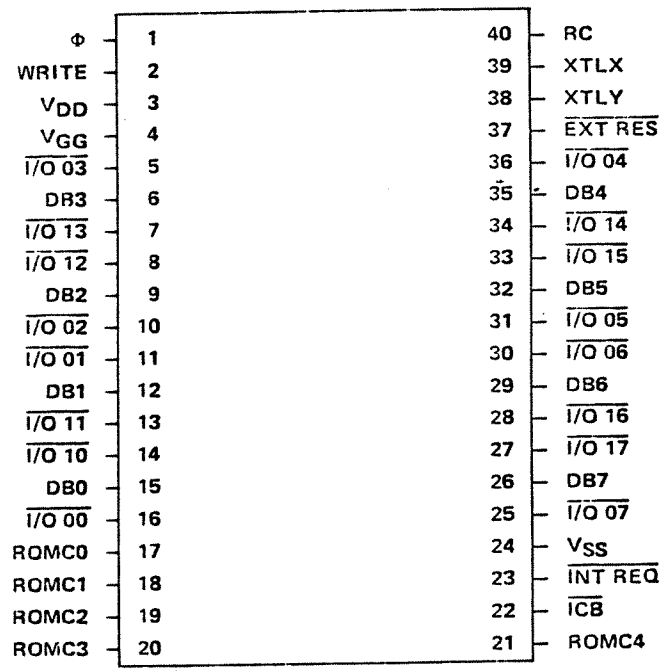
Y = AB

74 LS 04
HEX INVERTER



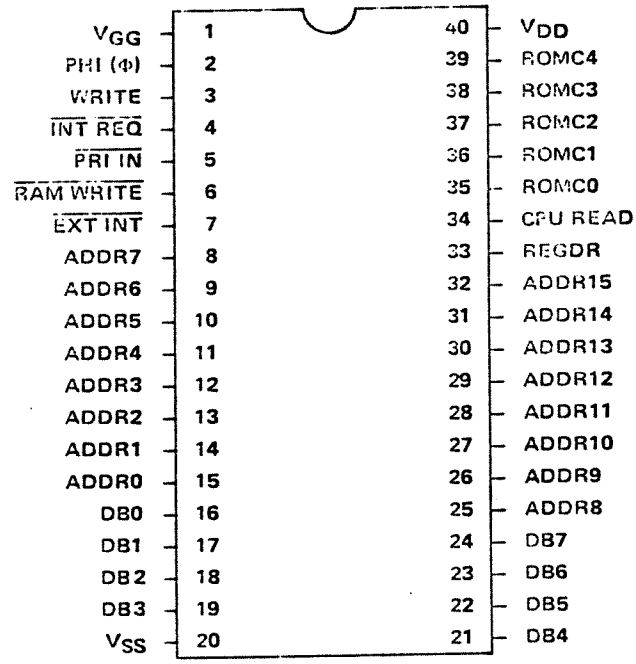
3850
CENTRAL PROCESSING UNIT

PIN NAME	DESCRIPTION	TYPE
DB0-DB7	Data Bus Lines	Bi-directional (3-State)
Φ, WRITE	Clock Lines	Output
$\overline{\text{I/O 00}}$-$\overline{\text{I/O 07}}$	I/O Port Zero	Input/Output
$\overline{\text{I/O 10}}$-$\overline{\text{I/O 17}}$	I/O Port One	Input/Output
RC	RC Network Pin	Input
ROMC0-ROMC4	Control Lines	Output
$\overline{\text{EXT RES}}$	External Reset	Input
$\overline{\text{INT REQ}}$	Interrupt Request	Input
$\overline{\text{ICB}}$	Interrupt Control Bit	Output
XTLX	Crystal Clock Line	Output
XTLY	External Clock Line	Input
V_{SS}, V_{DD}, V_{GG}	Power Lines	Input



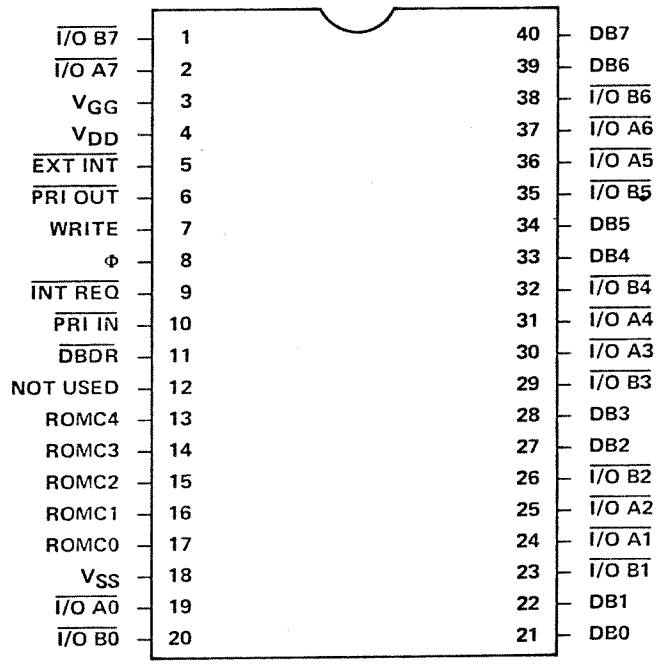
3853
STATIC MEMORY INTERFACE

PIN NAME	DESCRIPTION	TYPE
DB0-DB7	Data Bus Lines	Bi-directional
ADDR0-ADDR15	Address Lines	Output
Φ, WRITE	Clock Lines	Input
$\overline{\text{INT REQ}}$	Interrupt Request	Output
$\overline{\text{PRI IN}}$	Priority In Line	Input
$\overline{\text{RAM WRITE}}$	Write Line	Output
$\overline{\text{EXT INT}}$	External Interrupt Line	Input
REGDR	Register Drive Line	Input/Output
CPU READ	CPU Read Line	Output
ROMC0-ROMC4	Control Lines	Input
V_{SS}, V_{DD}, V_{SS}	Power Supply Lines	Input



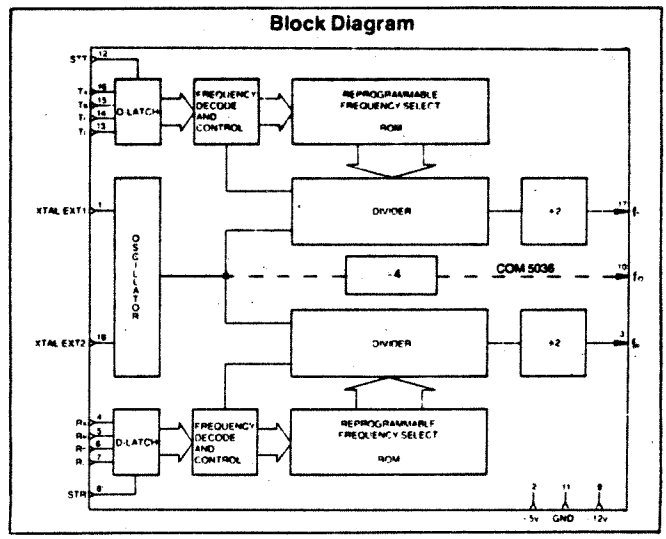
3861
PERIPHERAL INPUT/OUTPUT

PIN NAME	DESCRIPTION	TYPE
$\overline{\text{I/O A0}}$-$\overline{\text{I/O A7}}$	I/O Port A	Input/Output
$\overline{\text{I/O B0}}$-$\overline{\text{I/O B7}}$	I/O Port B	Input/Output
DB0-DB7	Data Bus	Bi-directional (3-State)
ROMC0-ROMC4	Control Lines	Input
Φ, WRITE	Clock Lines	Input
$\overline{\text{EXT INT}}$	External Interrupt	Input
$\overline{\text{PRI IN}}$	Priority In	Input
$\overline{\text{PRI OUT}}$	Priority Out	Output
$\overline{\text{INT REQ}}$	Interrupt Request	Output
$\overline{\text{DBDR}}$	Data Bus Drive	Output
V_{SS}, V_{DD}, V_{GG}	Power Supply Lines	Input



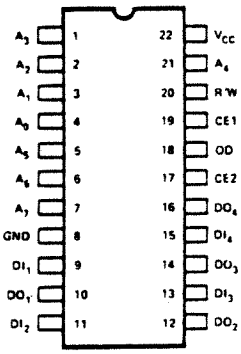
COM5016
DUAL BAUD RATE GENERATOR

Block Diagram

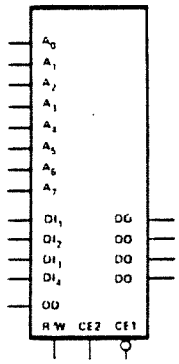


5101L
256X4 BIT STATIC RAM

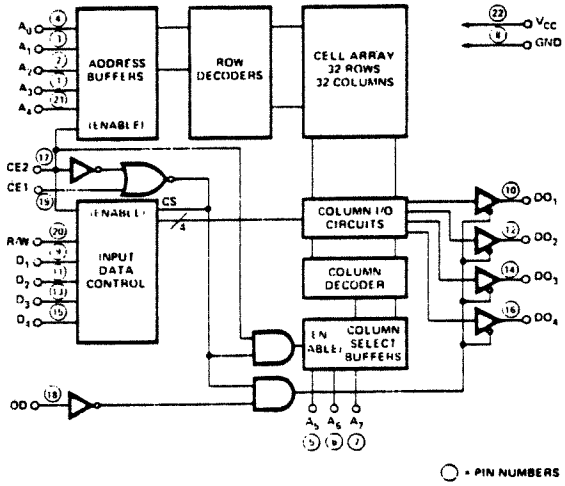
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM

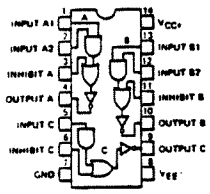


TRUTH TABLE

CE_1	CE_2	OD	R/W	D_{IN}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{IN}	Write
L	H	L	H	X	D_{OUT}	Read

9616
TRIPLE EIA/MIL LINE DRIVER

CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

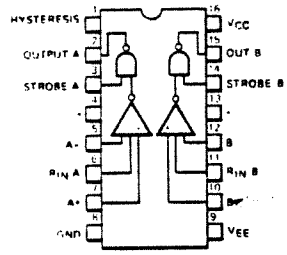
TYPE	PART NO.
9616	9616 DM
9616C	9616DC
9616E	9616 EDC

TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

(For Channel C, omit INPUT 2 Column)

9627
DUAL EIA/MIL LINE RECEIVER

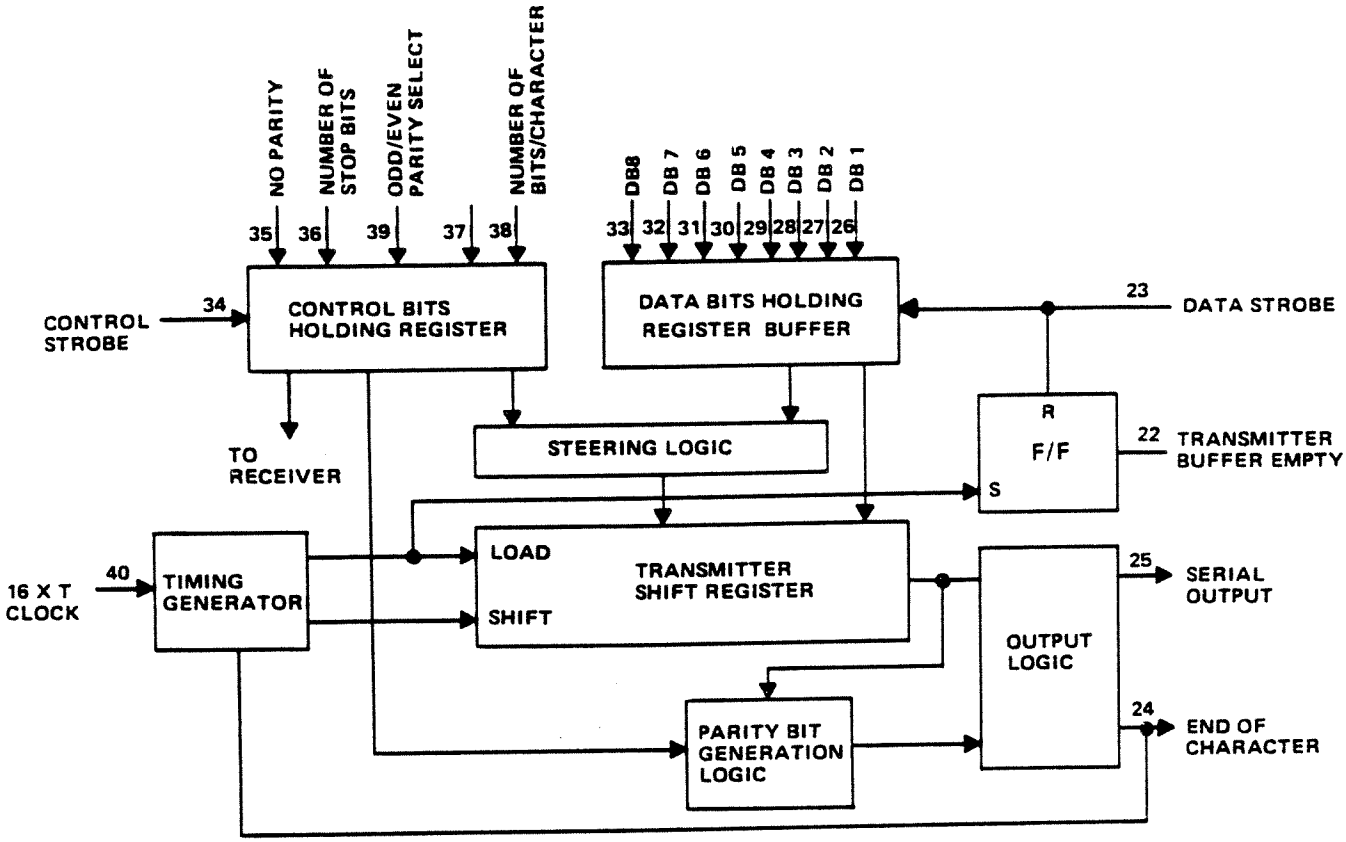


*Internal Connection

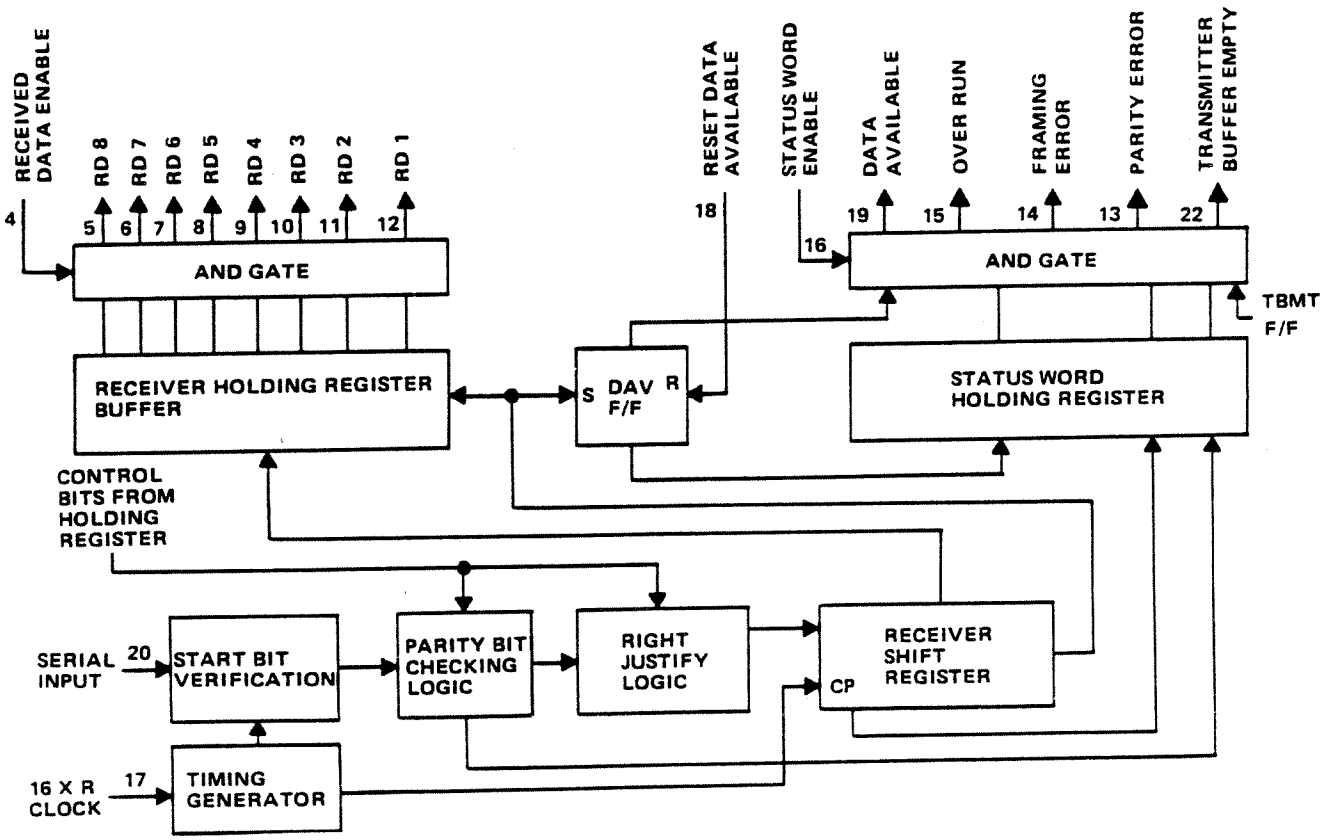
ORDERING INFORMATION

TYPE	PART NO.
9627	9627DM
9627C	9627DC

TRANSMIT CIRCUITS

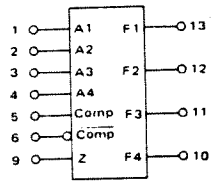


RECEIVE CIRCUITS



14561

BLOCK DIAGRAM



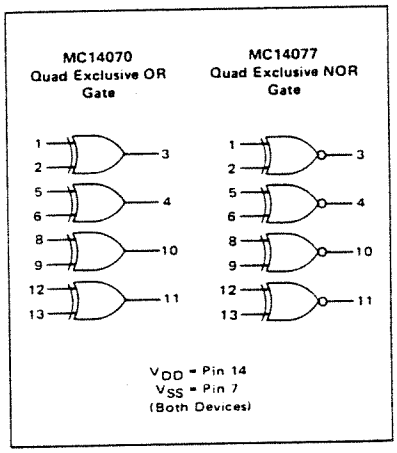
V_{DD} = Pin 14
V_{SS} = Pin 7

TRUTH TABLE

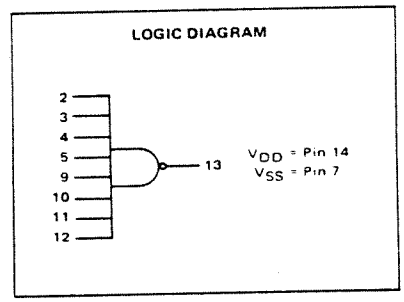
Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight through
0	0	1					
0	1	1					
0	1	0	$\bar{A}1$	A2	$A2\bar{A}3 + \bar{A}2A3$	$\bar{A}2\bar{A}3\bar{A}4$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care

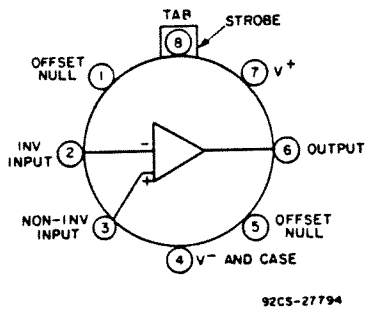
14070/14071
QUAD EXCLUSIVE OR/NOR



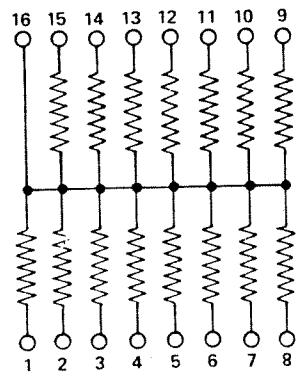
14068
8 INPUT NAND



3140



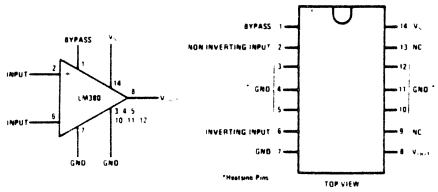
761-1-R22K



block and connection diagrams

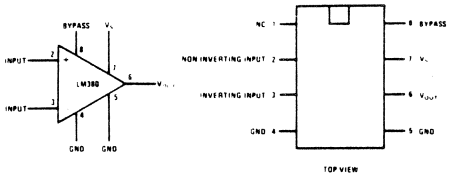
LM 380

Dual-In-Line Package



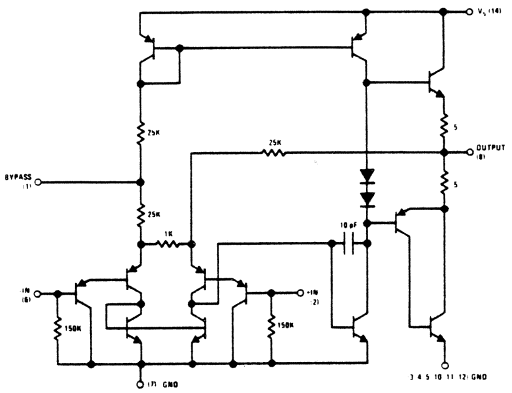
Order Number LM380N

Dual-In-Line Package

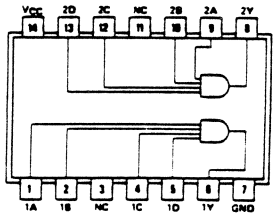


Order Number LM380N-8

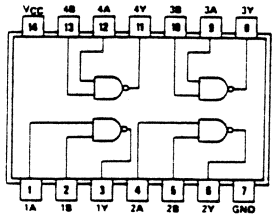
schematic diagram



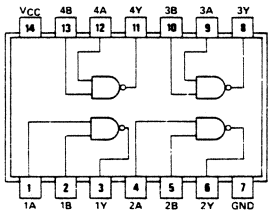
7421
DUAL 4-INPUT AND



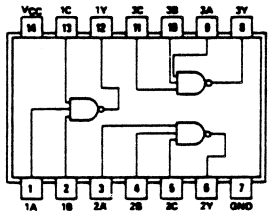
7438
QUAD 2-INPUT NAND



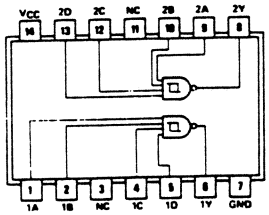
7400
QUAD 2 INPUT NAND



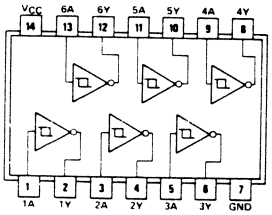
7410
TRIPLE 3 INPUT NAND



7413
DUAL 4 INPUT NAND SCHMITT TRIGGER

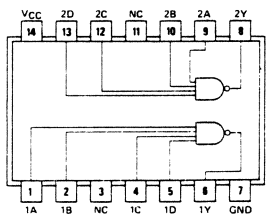


7414
HEX INVERTER

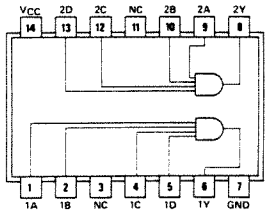


SN5414/SN7414(J, N, W)

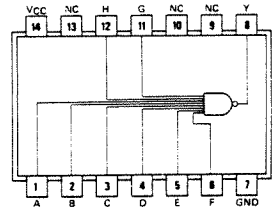
7420
DUAL 4 INPUT NAND



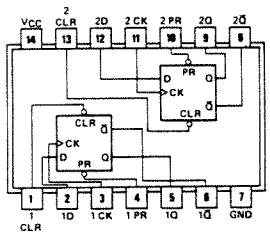
7421
DUAL 4 INPUT NAND



7430
8 INPUT NAND



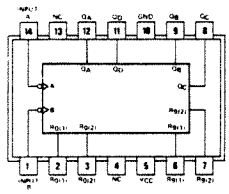
7474
DUAL D-TYPE FLIP-FLOP



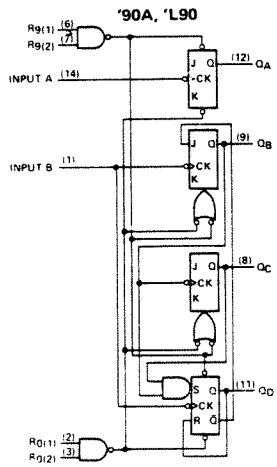
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

7490 DECADE COUNTER



'90A, 'L90



'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
BI-QUINARY (5-2)
(See Note B)

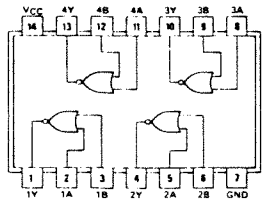
COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90
RESET/COUNT FUNCTION TABLE

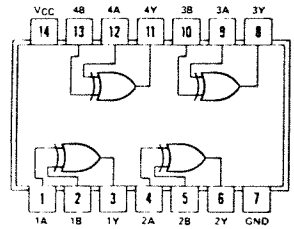
RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary

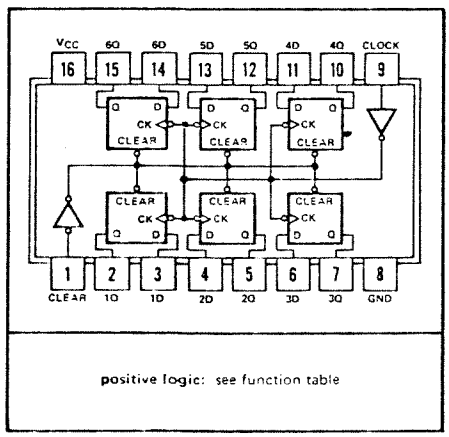
7402
QUAD 2 INPUT NOR

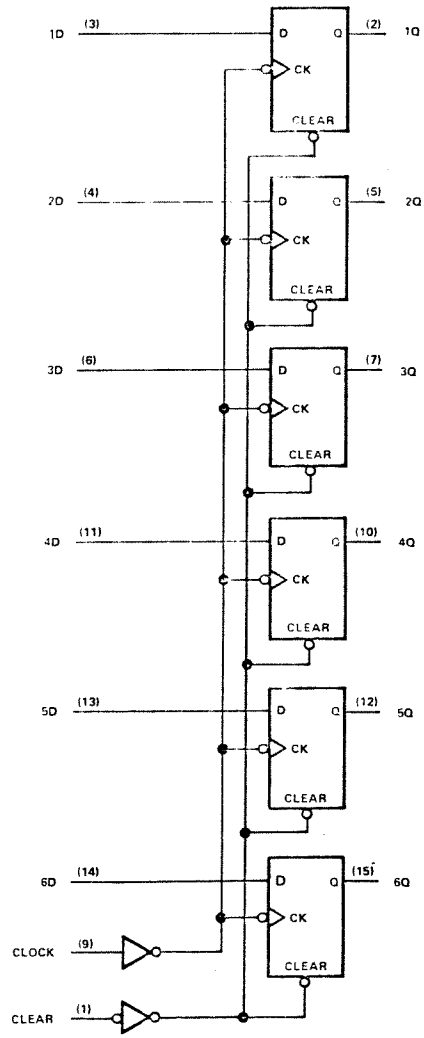


7486
QUAD EXCLUSIVE OR



74174 (F40174BDC)
HEX D-TYPE FLIP-FLOPS

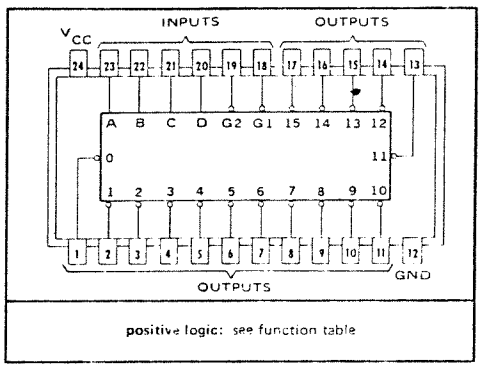


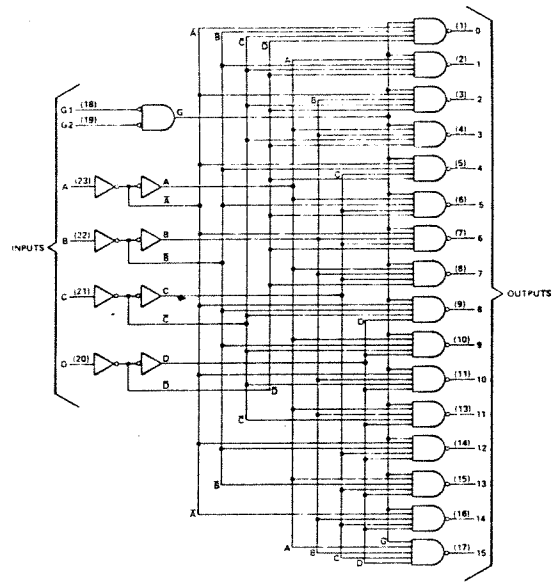


FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

74154
4 TO 16 LINE DECODER/DEMULTIPLEXER





FUNCTION TABLE

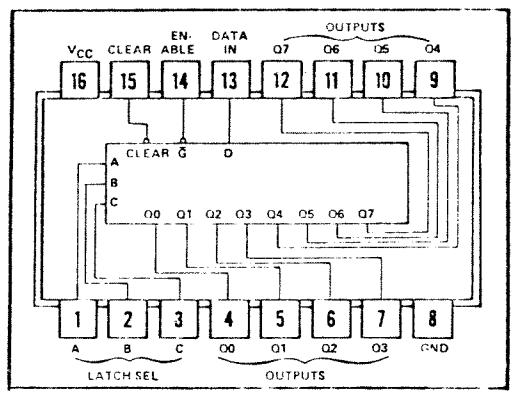
INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

74259
8 BIT ADDRESSABLE LATCHES

FUNCTION TABLE

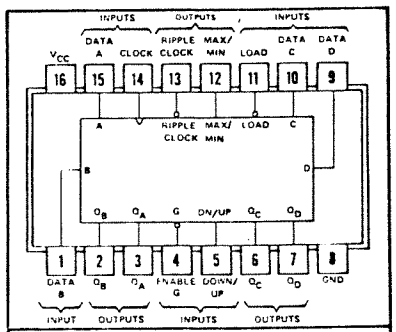
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	G			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear



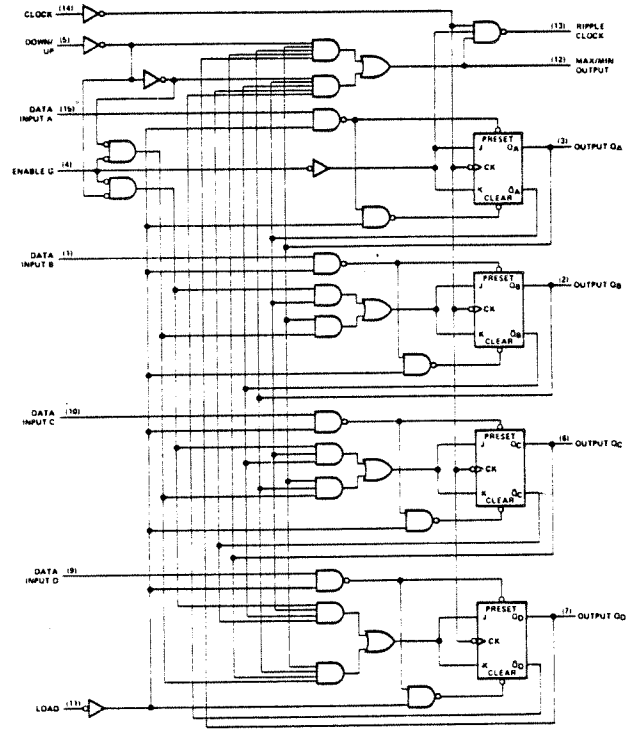
LATCH SELECTION TABLE

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

74191
SYNCHRONOUS UP/DOWN COUNTER



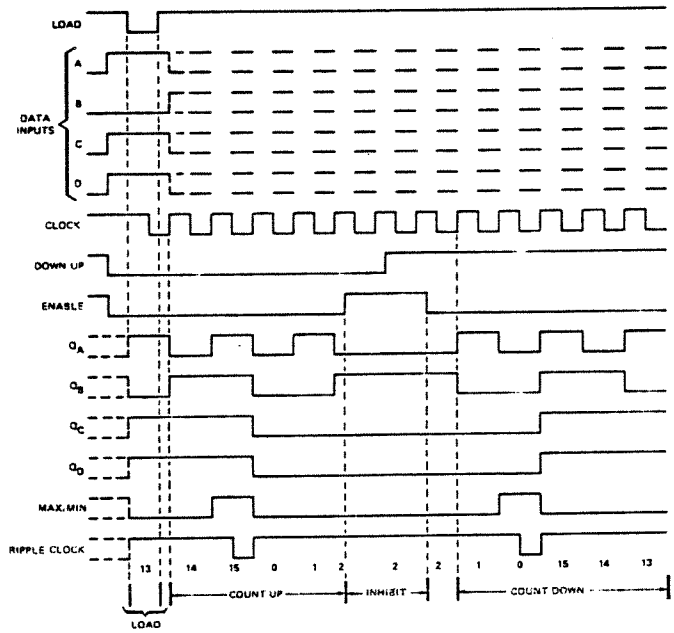
asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D



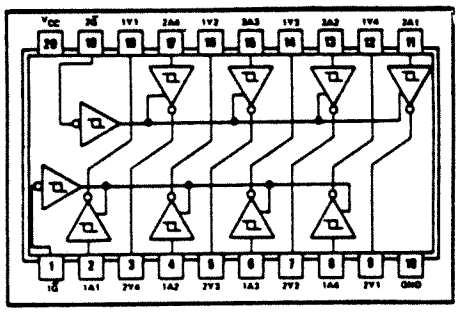
typical load, count, and inhibit sequences

Illustrated below is the following sequence:

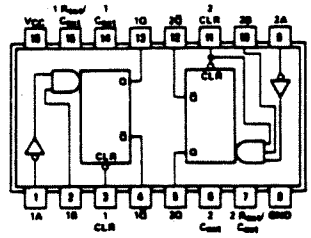
1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



74241
OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



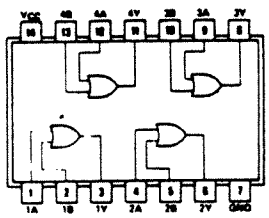
74123
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR



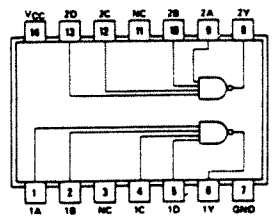
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

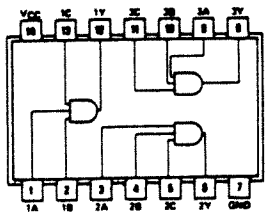
7432
QUAD 2 INPUT OR



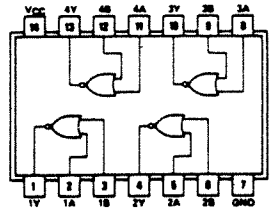
7440
DUAL 4 INPUT NAND



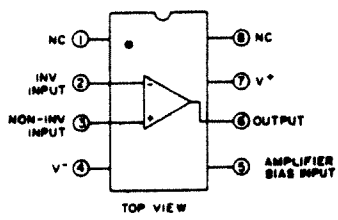
7411
TRIPLE 3 INPUT AND



7428
QUAD 2 INPUT NOR

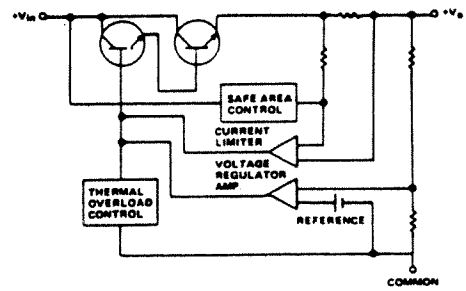


CA 3080S

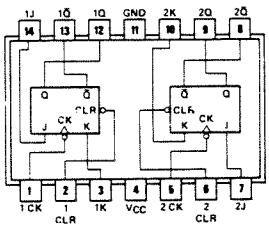


Plastic Package (CA3080E)

LA51520



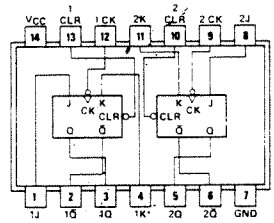
74103
DUAL J-K FLIP-FLOP



FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

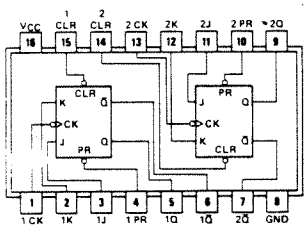
74107
DUAL J-K MASTER-SLAVE FLIP-FLOP



FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

74112
DUAL J-K FLIP-FLOP



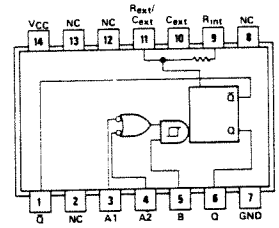
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

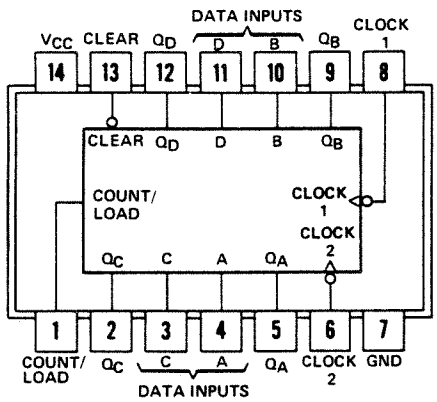
74121
MONOSTABLE MULTIVIBRATOR

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⊓	⊔
↓	H	H	⊓	⊔
↓	↓	H	⊓	⊔
L	X	↑	⊓	⊔
X	L	↑	⊓	⊔

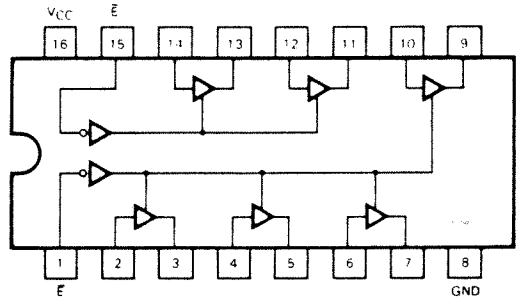


74196



74367

HEX 3-STATE BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS



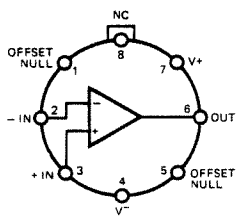
TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	L
L	H	H
H	X	(Z)

U5B1741393
FREQUENCY COMP OP AMPLIFIER

CONNECTION DIAGRAM

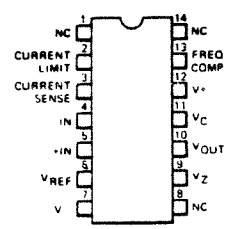
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B



Note: Pin 4 connected to case

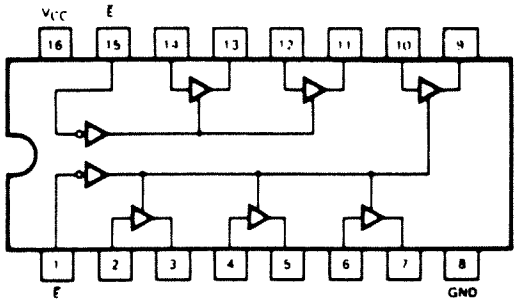
U5R7723393

14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



74367

HEX 3-STATE BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS

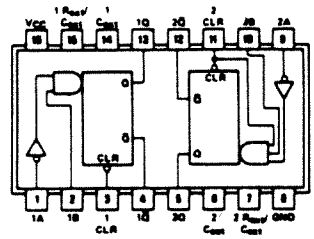


TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

74123

DUAL RETRIGGERABLE
MONOSTABLE MULTIVIBRATOR

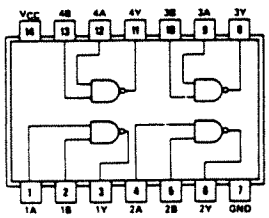


FUNCTION TABLE

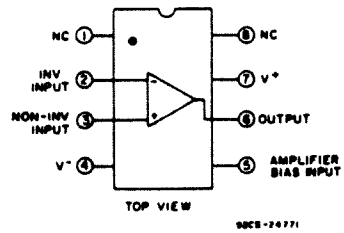
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

7400

QUAD 2 INPUT NAND

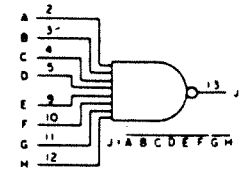


CA 3080S



Plastic Package (CA3080E)

CD 4068



V_{DD} = 14 1 = INTERNAL CONNECTION DO NOT USE
V_{SS} = 7 6, 8 = NO CONNECTION

74 LS 175

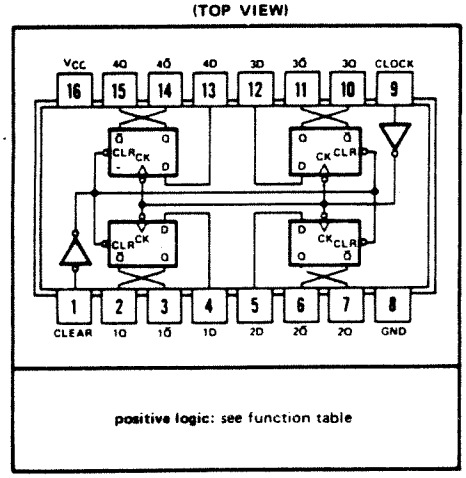
QUAD D-TYPE FLIP-FLOP

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$↑
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

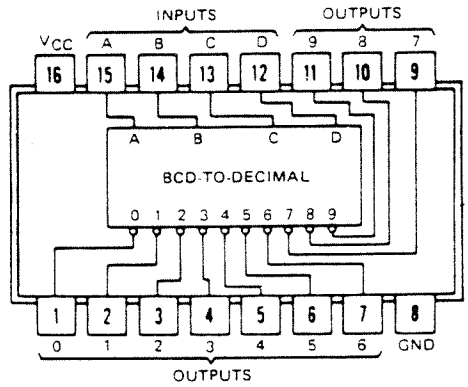
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

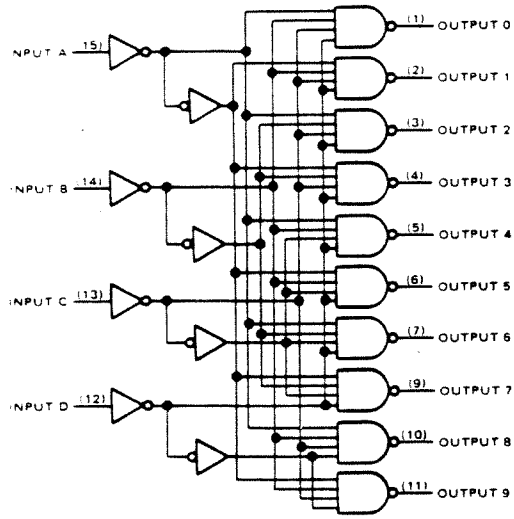
'175, 'LS175, 'S175 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see function table

74145
BCD/DECIMAL DECODER/DRIVER

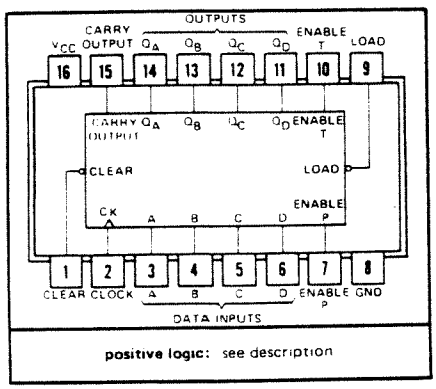


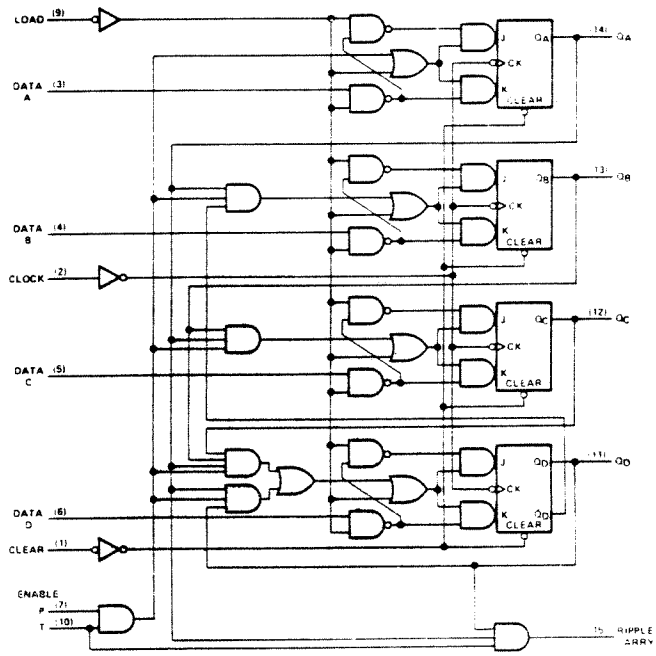


FUNCTION TABLE

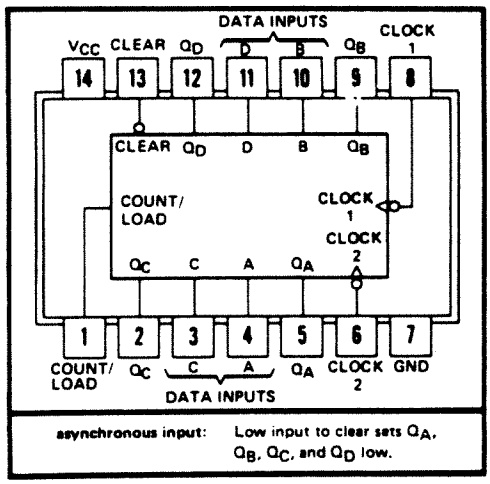
NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

74160
SYNCHRONOUS 4-BIT COUNTER





74176
PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

FUNCTION TABLES

DECADE (BCD) (See Note A)

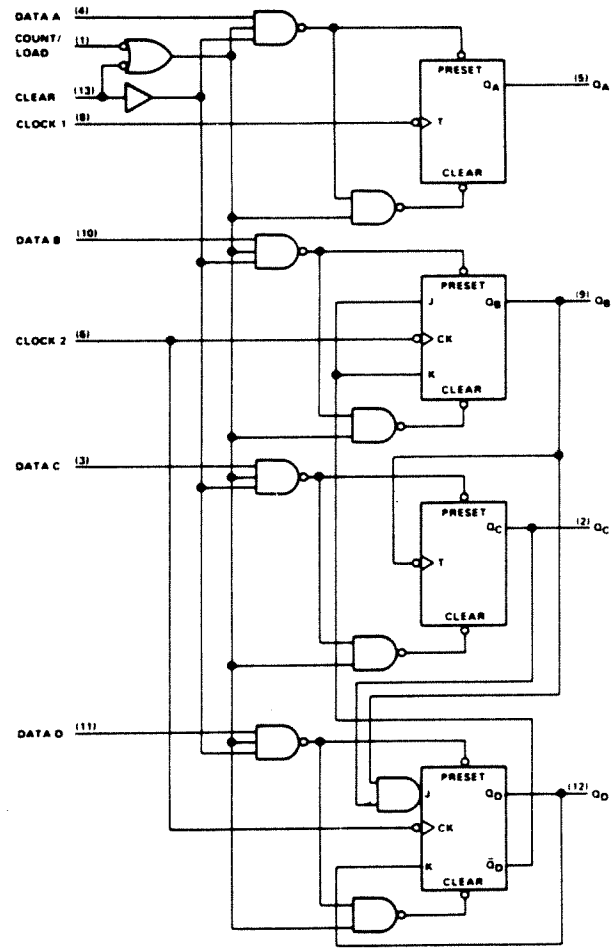
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

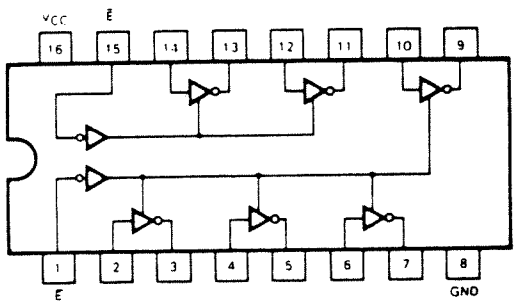
H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.



. . . dynamic input activated by transition from a high level to a low level

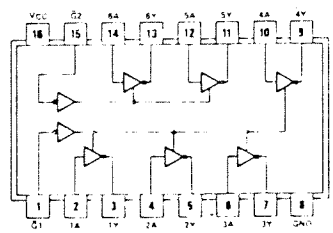
07420
HEX 3 STATE INVERTER BUFFER



TRUTH TABLE

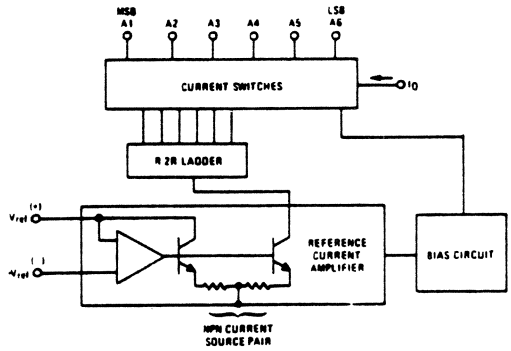
INPUTS		OUTPUT
$\bar{E}$	D	
L	L	H
L	H	L
H	X	(Z)

74368; F40098; 9LS368
HEX BUS DRIVER

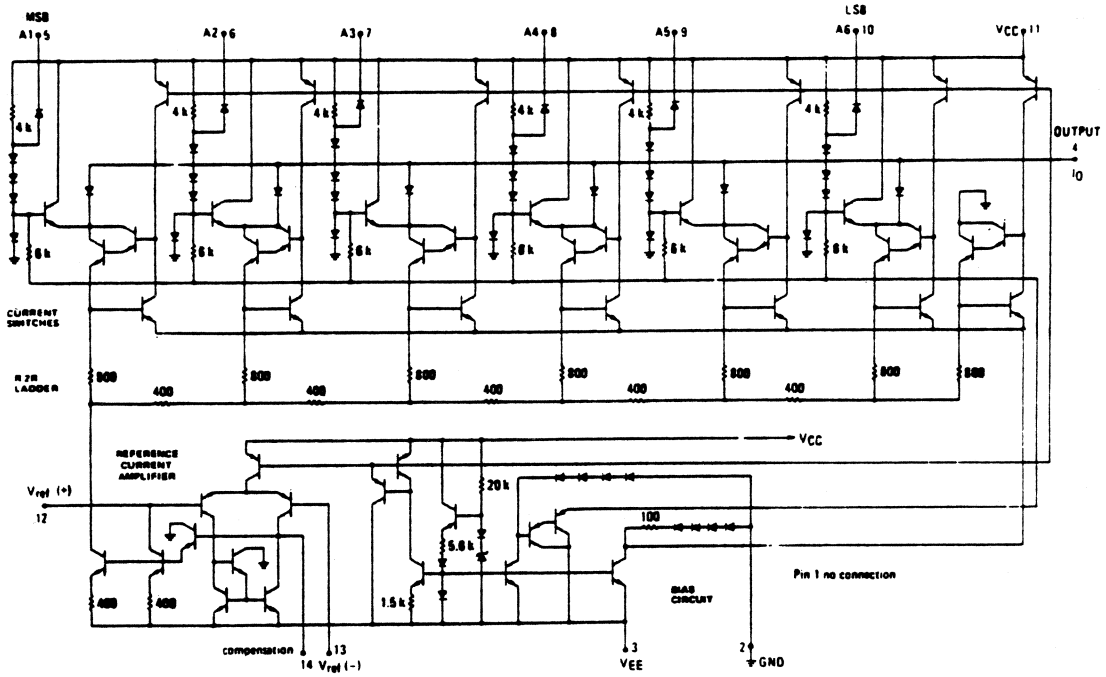


1406L
DIGITAL-TO-ANALOG CONVERTER

BLOCK DIAGRAM



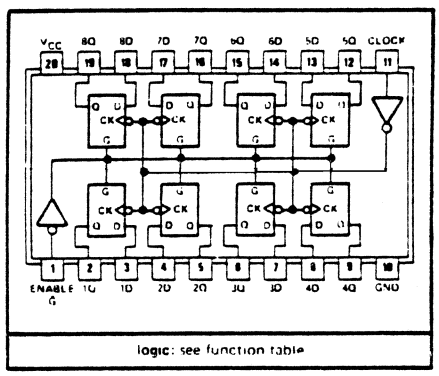
COMPLETE CIRCUIT SCHEMATIC
(Digital Inputs: pins 5,6,7,8,9,10)



74LS377
OCTAL D-TYPE FLIP-FLOP WITH ENABLE

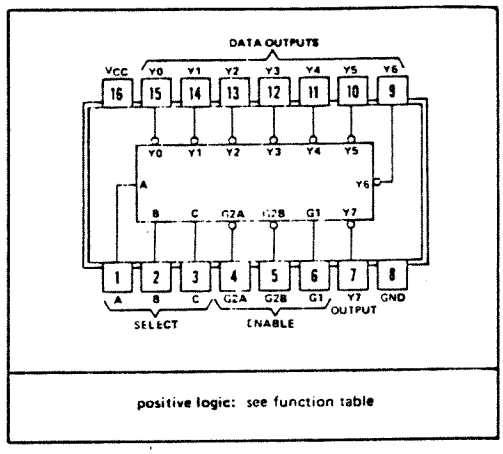
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

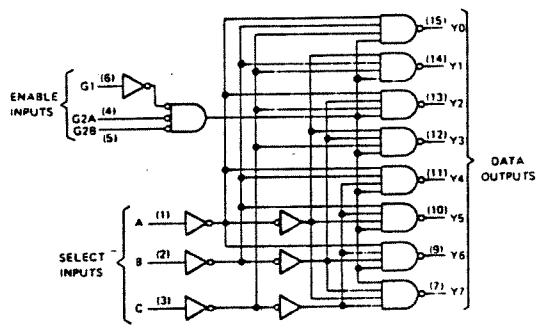


logic: see function table

74138; 9LS138
DECODER/DEMULTIPLEXER



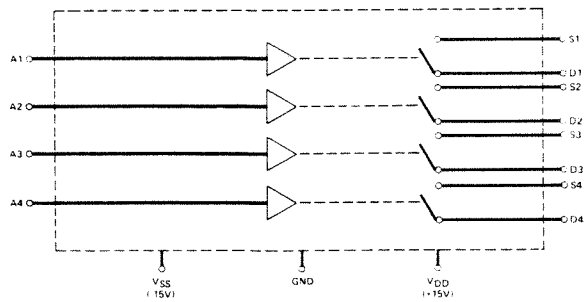
positive logic: see function table

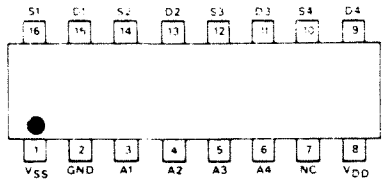


INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

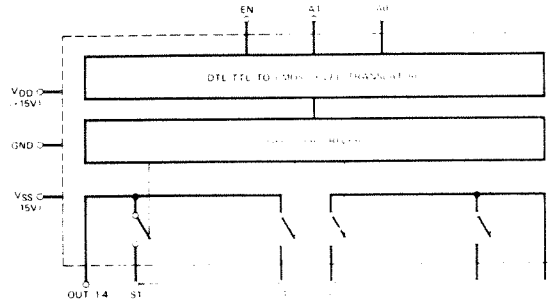
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

7510
QUAD SPST ANALOG SWITCH

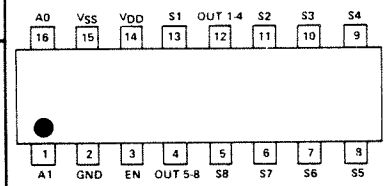




7502
4 CHANNEL DIFFERENTIAL ANALOG MULTIPLEXER

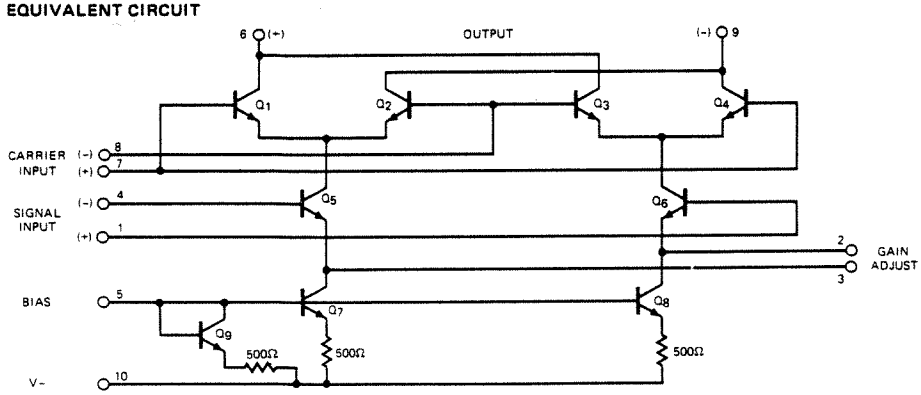


AD7502			
A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None



FU5E7796393
DOUBLE BALANCED MODULATOR/DEMODULATOR

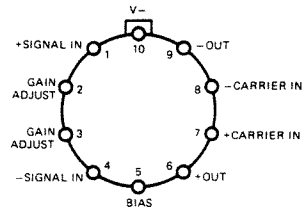
EQUIVALENT CIRCUIT



CONNECTION DIAGRAM

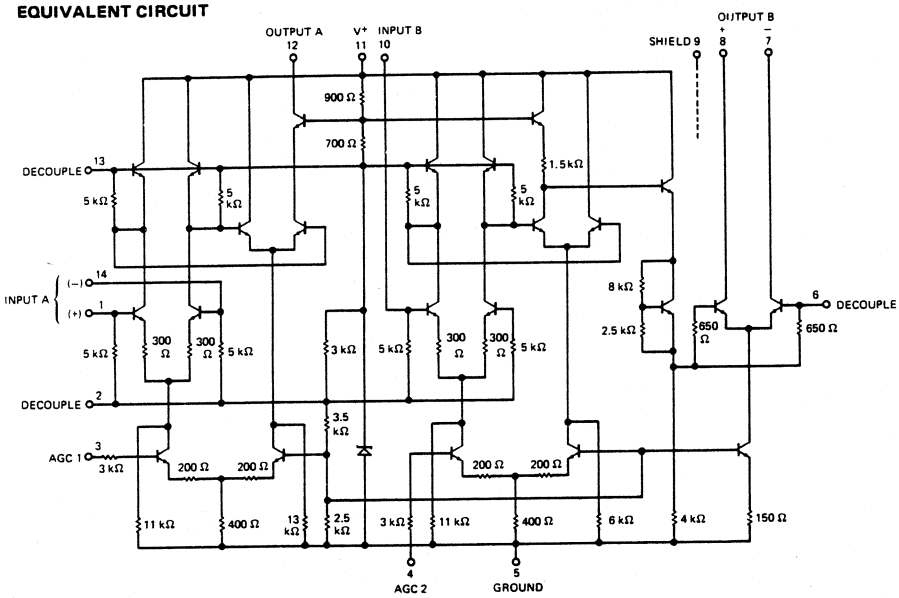
10-LEAD METAL CAN

(TOP VIEW)

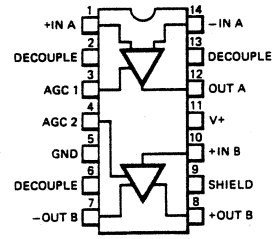


U6A7757393
GAIN CONTROLLED IF AMPLIFIER

EQUIVALENT CIRCUIT

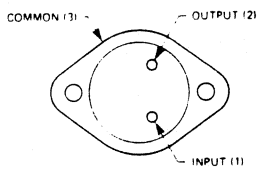


CONNECTION DIAGRAM
14-LEAD DIP
(TOP VIEW)



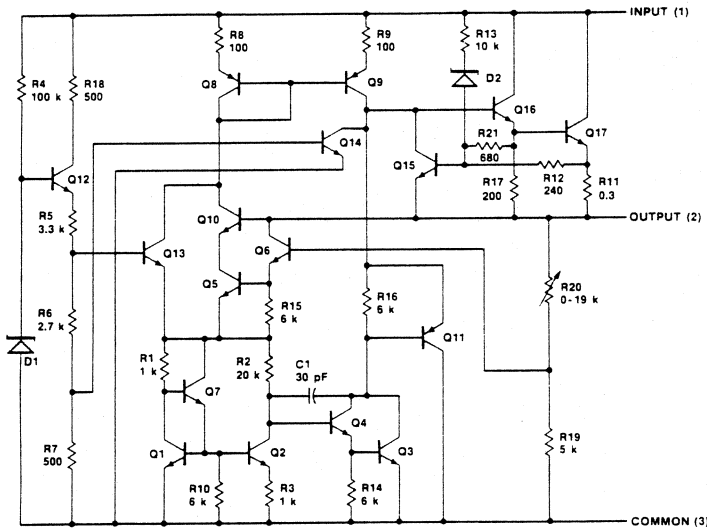
UA78H05KC

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K

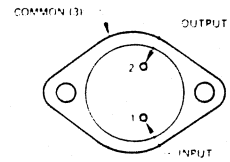


UA7812KC

EQUIVALENT CIRCUIT

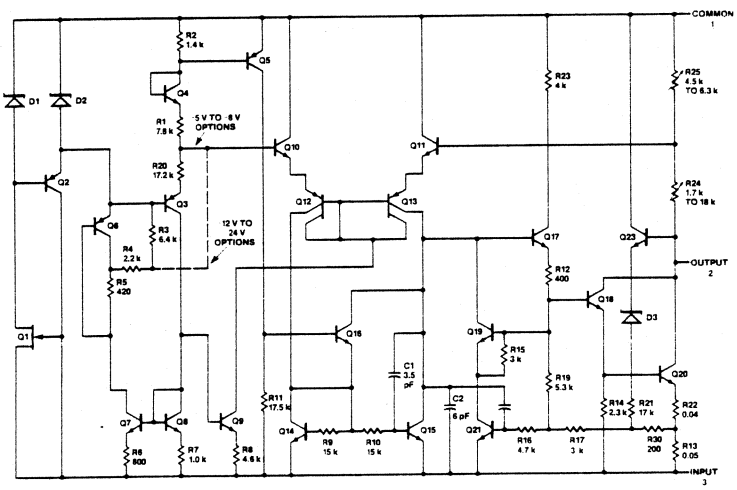


TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K

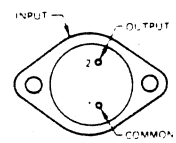


UA7912KC

EQUIVALENT CIRCUIT

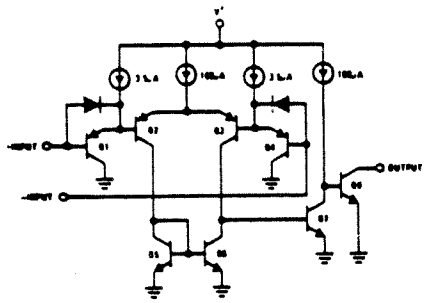


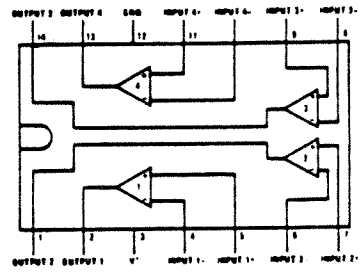
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



LM393J

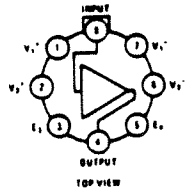
VOLTAGE COMPARATOR/BUFFER





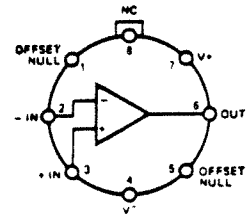
LH002CH

CURRENT AMPLIFIER



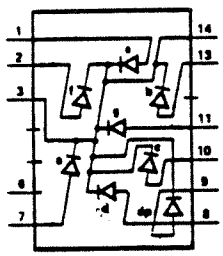
UA741

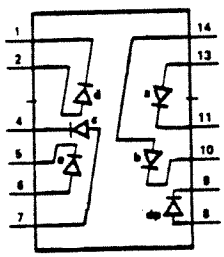
OPERATIONAL AMPLIFIER



7633/7636/7673

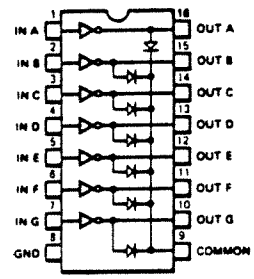
NUMERIC/SIGN LED DISPLAYS



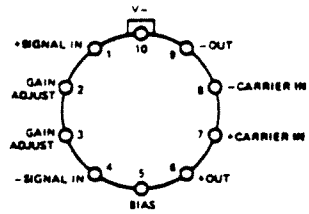


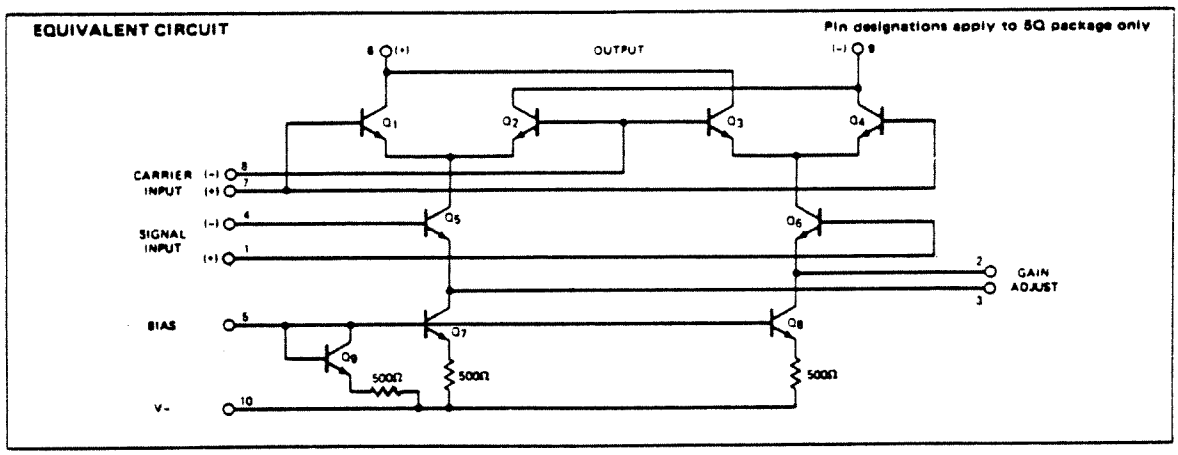
UA9667

DARLINGTON DRIVER

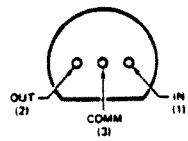


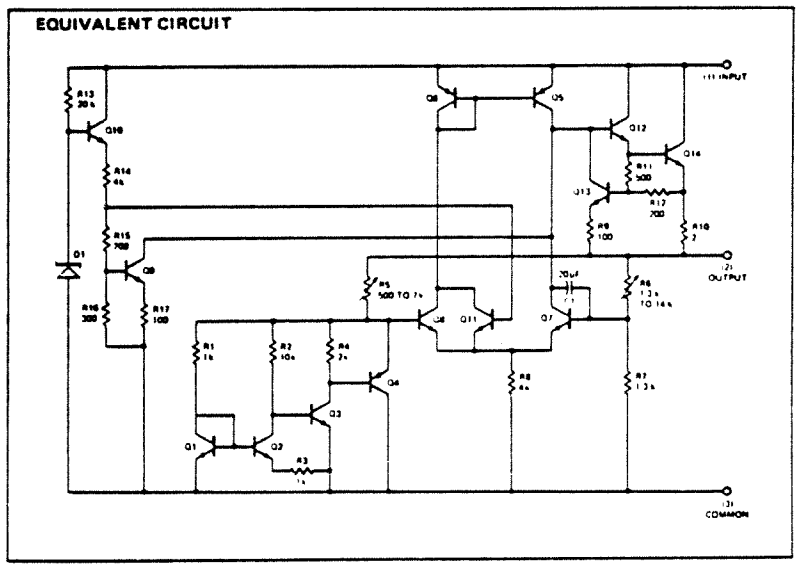
UA796HC
MODULATOR/DEMODULATOR



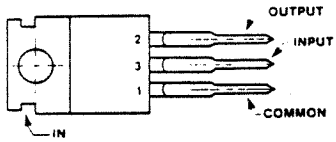


UA 78L82
POSITIVE VOLTAGE REGULATOR

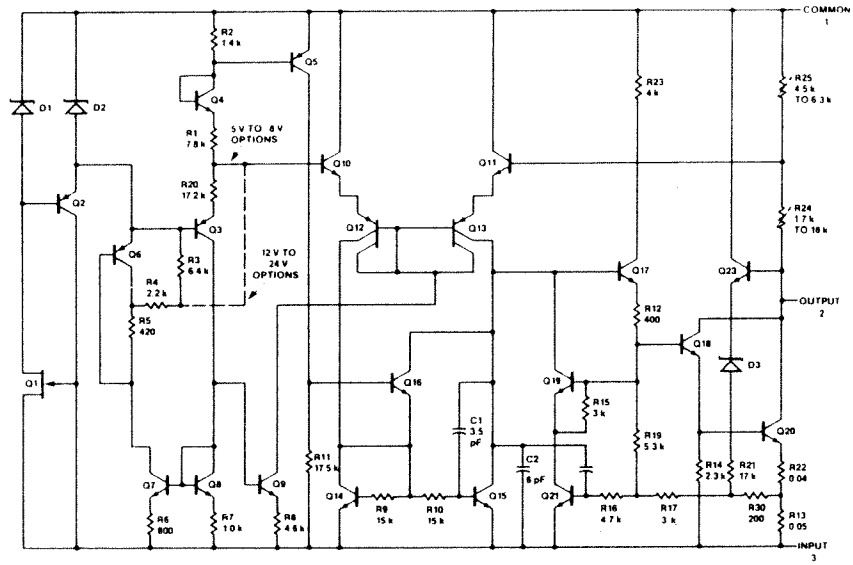




UA7905
–5V REGULATOR

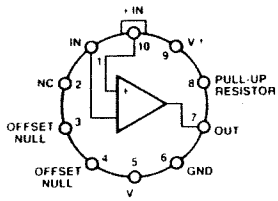


Equivalent Circuit



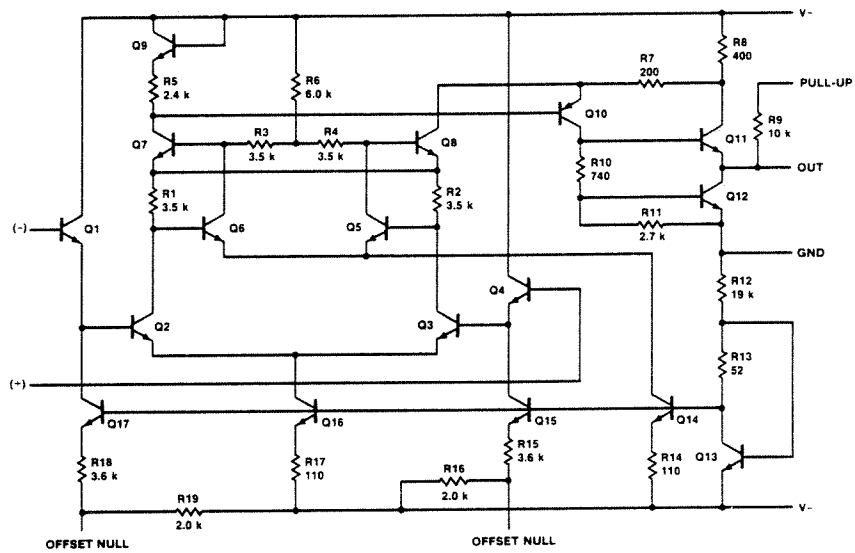
UA734
VOLTAGE COMPARATOR

Connection Diagram
10-Pin Metal Package



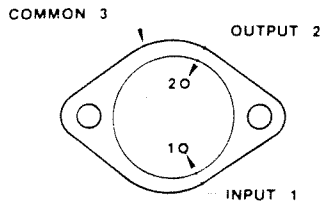
(Top View)

EQUIVALENT CIRCUIT



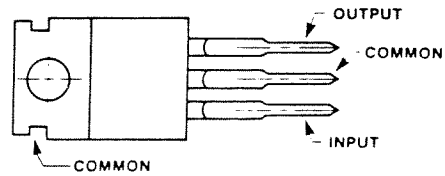
μA7800 Series
3-Terminal Positive Voltage Regulators

Connection Diagram
TO-3 Package



(Top View)

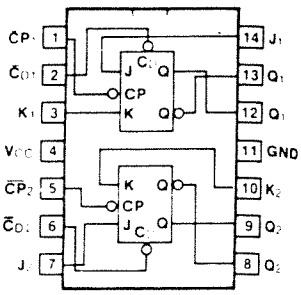
Connection Diagram
To-220 Package



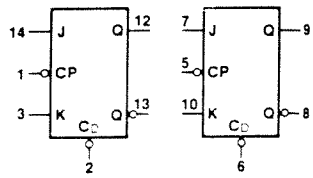
(Side View)

54/74H103
Dual JK Edge-Triggered Flip-Flop

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

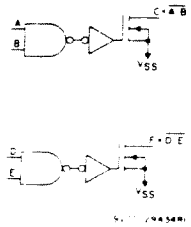
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

t_n = Bit time before clock pulse
t_{n+1} = Bit time after clock pulse
H = HIGH Voltage Level
L = LOW Voltage Level

CD40107B Types

COS/MOS Dual 2-Input NAND Buffer/Driver

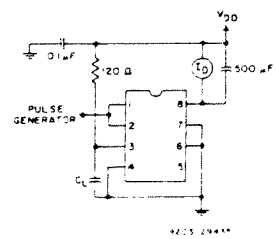
FUNCTIONAL DIAGRAM



TRUTH TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

*Requires external pull-up resistor (R_L to V_{DD})
#Without pull-up resistor (3-state)



Power dissipation test circuit for CD4010?BE.

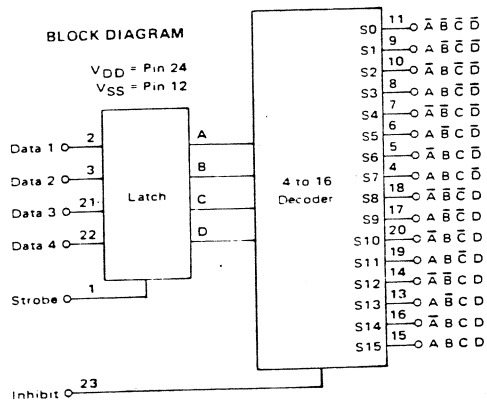
MC14514B
MC14515B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL, CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

V_{DD} = Pin 24
V_{SS} = Pin 12



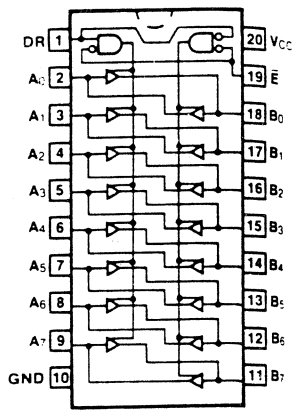
DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT (MC14514 Logic "1" / MC14515 Logic "0")
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

54LS/74LS245
Octal BUS Transceiver
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS Ē	INPUTS DR	OUTPUT
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

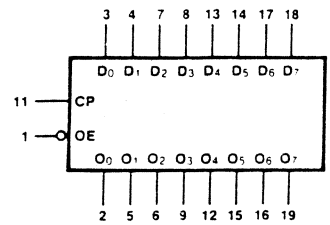
54LS/74LS374
Octal D-Type Flip-Flop
(With 3-State Outputs)

TRUTH TABLE

INPUTS Dn	CP	INPUTS OE	OUTPUTS On
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

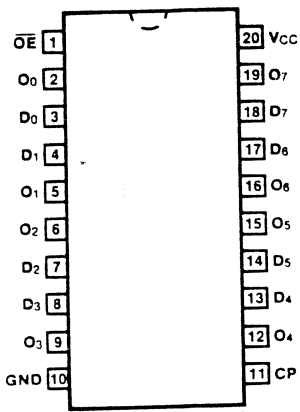
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC SYMBOL

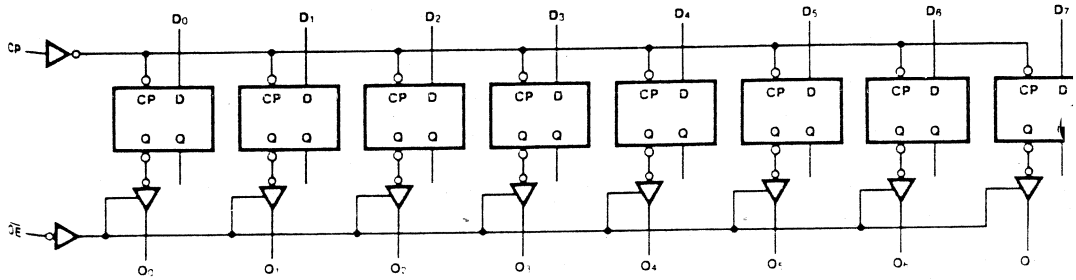


V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
PINOUT A

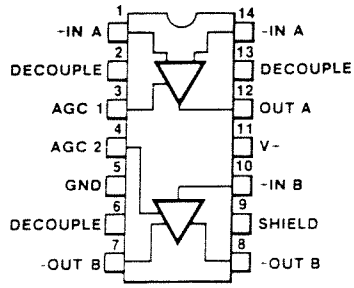


LOGIC DIAGRAM



μA757
Gain-Controlled IF Amplifier

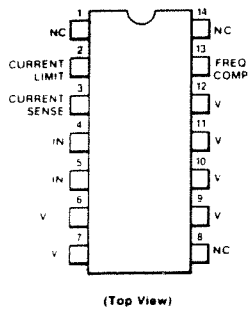
Connection Diagram
14-Pin DIP



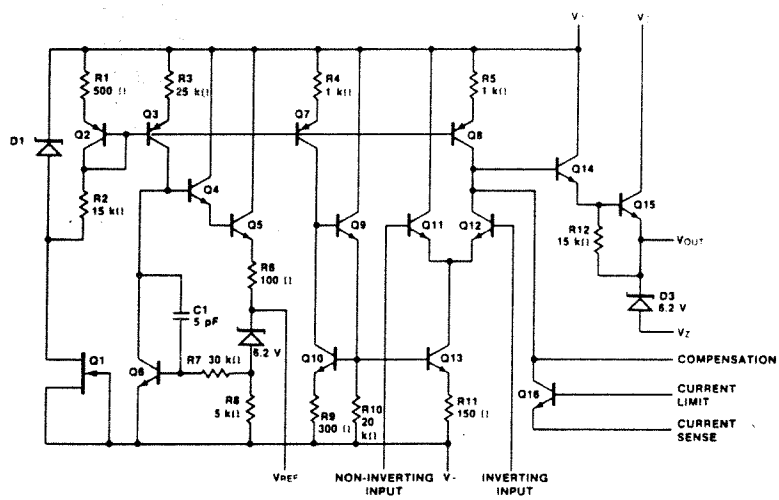
(Top View)

μA723
Precision Voltage Regulator

Equivalent Circuit

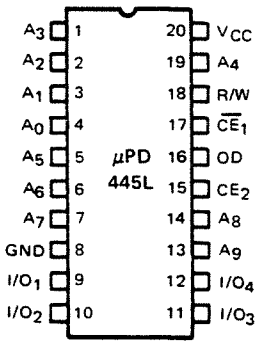


(Top View)



μPD445L
FULLY DECODED
4096 STATIC CMOS RAM

PIN CONFIGURATION



BLOCK DIAGRAM