Technical Manual

Model OAR3045

Automatic Direction Finding
and
Spectrum Monitoring Receivers

O.A.R. Corporation

a CompuDyne Company

Headquarters:
10447 Roselle Street
San Diego, CA 92121-1597
Telephone: (619) 453-4013
Telex: 697852
DDD: (619) 450-0414

Field Office:
1455 Research Boulevard
Rockville, MD 20850-3180
Telephone: (301) 424-0455
TWX: 7108289785

SECTION I

SYSTEM DESCRIPTION

1.1 GENERAL DESCRIPTION

The model OAR3045 receiver is a compact combined radio direction finding and communications receiver with a built-in spectrum monitor. The receiver is microprocessor controlled with synthesized tuning over the 20-520 MHz range. The receiver may be operated with the MA-396E Adcock antenna array over this range for mobile (vehicular and airborne) installations for direction finding, or with any 50 Ohm antenna for communications purposes. At fixed locations the equipment is operated with the larger AA-1301C stacked adcock array. Other optional DF antennas are available through OAR corporation for use at specific frequency ranges.

The basic OAR3045 receiver has a standard RS-232C I/O connector for use with a compass interface (MC1431-1), remote digital interface control equipment, a printer, or other peripheral devices. Other optional interface connectors are listed in Table 1-1.

Table 1-1 Interface Options

Model	I/O Connectors
OAR 3045/188	Bidirectional asynchronous control via MIL-STD-188C (low level) interface in lieu of RS-232C.
OAR 3045/488	Addition of bidirectional parallel General Purpose Interface Bus (GPIB) per IEEE-488 (with RS-232C).
OAR 3045/188-488	Addition of bidirectional parallel General Purpose Interface Bus (GPIB) per IEEE-488 and bidirectional asynchronous control via MIL-STD-188C (low level) interface in lieu of RS-232C.

The system has a Built-In Self Test (BITE) capability. On power-up the processor initiates a test sequence which checks the sensitivity at selected frequencies and the operation of the phase-locked synthesizer. Deviation from the standard values causes a flashing decimal to be displayed on the LCD. The system should then be serviced before operation. However, emergency operation is permissable if required.

The system (receiver and antenna) is powered via the receiver at a nominal +12Vdc (10.5-32 Vdc). An optional converter (OAR model EPS102-10) may be used for 115 or 230 Vac, 50 to 400 Hz sources.

1.2 SYSTEM PERFORMANCE

FREQUENCY COVERAGE: 20 to 520 MHz, dependant on antenna selected.

BEARING ACCURACY: 4 degrees rms typical for installations with sufficient ground plane using the monopole or ferrite loop antenna array. Specifications are for direct wave, vertically polarized signals only, under ideal site conditions with clear line-of sight, no adjacent reflective structures or RF interference, etc. Accuracy can be improved to 1 degree rms typical for given installation configurations using a processor controlled error correction table.

AZIMUTH COVERAGE: 360 degrees, in 1 degree increments.

SIGNAL INTERCEPT: Will intercept and display bearings on all signals of more than 85 milliseconds time duration or longer, at the tuned frequency. Model 3045 Receiver unit has built-in panoramic display for spectrum surveillance functions.

OVERALL DF SENSITIVITY:

FREQUENCY (MHz)	SENSITIVITY (uV/m)	
	MA396E	AA 1301C
20	15.0	1.5
50	5.0	0.5
110	2.0	0.3
250	3.0	0.3
360	5.5	1
520	12.0	15

NOTE: (1) System sensitivity is specified for an incident field strength in microvolts/meter for a 20dB S/N ratio at the video output (6 degrees RMS CRT bearing jitter) with an integration time of 200 msec and an IF bandwidth of 6.0 kHz.

(2) Improved sensitivities may be obtained using narrower band antennas. Consult the OAR sales representative.

POWER INPUT REQUIREMENTS: 11.5 to 32 Vdc standard: 115 or 230 Vac input at 50 to 400 Hz using optional external power supply unit.

POWER CONSUMPTION: 100 Watts maximum at 12 Vdc.

ENVIRONMENT:	Specifications are valid over a temperature range of 0 degrees to 45 degrees C. Typically, the system will function over the range of -20 degrees to +60 degrees C after a 30 minute warm-up Packaging and circuitry are designed to meet the intent of MIL-STD-810C.
MTBF RATING (Mean Time Between Failures):	3,000 hours
MTTR RATING (Mean Time To Repair):	1.5 hours

1.2.1 Receiver-Processor Unit

TYPE:	Single channel, triple conversion superhetrodyne, microprocessor-controlled.
TUNING RANGE:	20 to 520 MHz continuous.
CHANNEL SELECTION:	100 (0-99) Keypad programmable channels within receivers tuning range.

NOTE

Selected demodulation mode, DF bandwidth, track and hold and squelch threshold settings are stored in addition to frequency.

FREQUENCY TUNING:	Keypad entry to 10 Hz resolution. Key incremental tuning to 10 Hz resolution. Continuous dial tuning with selectable resolution to 10 Hz, 100 Hz, 1 kHz, or 10 kHz.
FREQUENCY SWEEP MODE:	Operator selected start and stop frequencies for sweeping throughout the tuning range. Sweep may be started, stopped or continued manually or automatically. In the automatic mode, threshold level and dwell time can be adjusted by the operator for automatic stop when a carrier is found. Found carriers may be transferred to the channel memory.
CHANNEL SCAN MODE:	Operator-controlled start and stop channel numbers for sequential scan of channels. Scan may be started, stopped or continued. Variable (0 to infinity) dwell time controls the time the scan pauses at a signal after the signal has dropped below the squelch threshold. Channels may be locked-out and omitted in the scanning sequence.
FREQUENCY REFERENCE	±2 ppm form 0 degrees to 45 degrees C. standard.

STABILITY: ±1 ppm optional.

PRESELECTOR BANDS:

20-32 MHz
32-51 MHz
51-83 MHz
83-125 MHz
125-175 MHz
175-280 MHz
280-400 MHz
400-520 MHz

DEMODULATION MODES:

AM Amplitude Modulation (A3)
FM Frequency Modulation (F3)
CW Continuous Wave (A1)
USB Upper Sideband Modulation (A3J)
LSB Lower Sideband Modulation (A3J)

IF BANDWIDTH: Standard, 200 kHz, 13 kHz, and 6 kHz.
Optional bandwidth filters available.

AUTOMATIC BANDWIDTH SELECTION:

DETECTION MODE	FREQUENCY RANGE (MHz)				
	20-30	30-80	80-115	115-225	255-520
FM	6 kHz	30 kHz	200 kHz	13 kHz	30 kHz
AM	6 kHz	6 kHz	13 kHz	13 kHz	13 kHz
CW	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz
USB/LSB	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz

IF SELECTIVITY:

FILTER	BANDWIDTH	
	-6dB points	-60 dB points
200 kHz	200 kHz	490 kHz
30 kHz	30 kHz	60 kHz
13 kHz	13 kHz	28 kHz
6 kHz	6 kHz	21 kHz

SENSITIVITY:

DETECTION MODE	IF BANDWIDTH SELECTED			
	200 KHz	30 KHz	13 KHz	6 KHz
FM	5 uV (-93 dBm)	1.5 uV (-103 dBm)	1.0 uV (-107 dBm)	0.5 uV (-113 dBm)
AM	not specified	1.0 uV (-106 dBm)	0.7 uV (-108 dBm)	0.5 uV (-110 dBm)
CW	not specified	not specified	not specified	0.35 uV (-110 dBm)
USB/LSB	not specified	not specified	not specified	0.35 uV (-115 dBm)

NOTES:

1. Sensitivity is specified terminated in 50 ohms at the receiver input.

2. Sensitivity is not specified for IF bandwidths not normally used for a particular demodulation mode.

3. FM sensitivity is defined as the minimum input signal required to produce a 10 dB SINAD ratio at the audio output. Measured with an FM signal with a peak deviation equal to 30% of the selected IF bandwidth and a modulation frequency of 1 KHz.

4. AM sensitivity is defined as the minimum input signal required to produce a 10 dB signal plus noise/to noise ratio [10 dB (S+N/N)] at the audio output. Measured with a 50% amplitude modulated signal at a modulation frequency of 400 Hz.

5. CW/SSB sensitivity is defined as the minimum input signal required to produce a 10 dB signal plus noise/to noise ratio [10dB (S+N/N)] at the audio output. Measured with a CW signal.

NOISE FIGURE: 10 dB typical

IMAGE REJECTION: 80 dB minimum

IF REJECTION: 80 dB minimum

INTERMODULATION DISTORTION:	Third-Order Intercept Point: +10 dBm, typical, referenced to receiver input.
	Second-Order Intercept Point: +30 dBm, typical, referenced to receiver input.
SINGLE TONE DYNAMIC RANGE:	AUDIO: 102 dB DF: 122 dB

NOTE

Single tone dynamic range is specified in dB from the noise floor to the 1.0 dB gain compression level with the specified noise figure and a 6 kHz IF bandwidth. Noise floor is defined as that level providing a minimum useable signal (10dB S+N/N). The DF noise floor is defined as a bearing with a jitter of 6 degree rms.

AGC FIGURE OF MERIT:	100 dB
AGC MODES:	NORMAL: Attack, 20 msec; release, 60 msec. SLOW: Attack, 20 msec; release, 5 sec. NOTE: Normal and slow refer to AGC decay time.
TRACK-AND-HOLD MODE:	Maintains bearing display for 25 seconds after signal has dropped below variable threshold level. Bearing data updated whenever signal exceeds threshold.
PLL MODE:	Signal lock obtained using tuning dial. Lock indicated by illuminated LED. Selectable wide or narrow noise-bandwidths. OPERATE/RESET switch activates the PLL track circuit or resets it to the center of the IF passband.

NOTE

If the receiver is used in the communication mode only, the receiver must be in the PLL RESET mode to achieve maximum sensitivity.

BEARING OFFSET (Antenna Zero):	Indicated relative bearings may be continuously offset by compass input. Keyboard fixed offsets may be entered for the following: 1. True North (variation from magnetic compass input). 2. True or relative bearings with offset programmed from keyboard. 3. Reciprocal bearings.
ANTENNA CONTROLS:	Phase, zero, and modulation adjustment possible from the front panel.

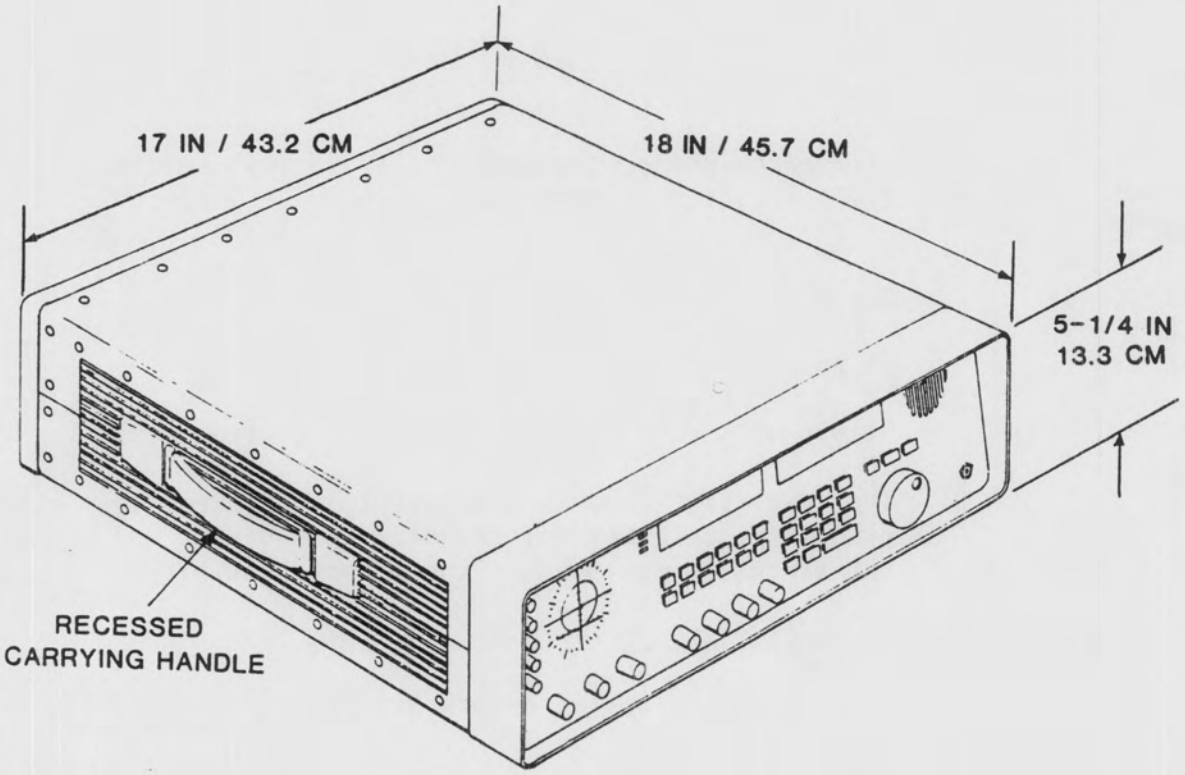
DISPLAYS AND CONTROLS:	See Section III.
CONNECTORS; (REAR PANEL)	See Section 2.3.1.
BITE (BUILT-IN TEST EQUIPMENT)	Microprocessor-controlled start up test sequence and fault location to the module level.
DIMENSIONS:	See Figure 1-1.
WEIGHT:	35 pounds (15.8 Kg)
CONSTRUCTION:	Aluminum case, drip and moisture protected. The chassis frame is cast aluminum construction with plug-in circuit boards. Modular arrangement and common bus wiring is employed to the extent possible.

1.2.2 MA-396E Antenna Specifications

TYPE:	Dual array, monopole, Adcock antenna; designed for car-top or aircraft mounting. Consists of a flat antenna housing containing; preamplifiers and RF signal processing circuit boards, nine removeable elements, and four car-top mounting straps. A 15 ft. (4.6 m) RF coaxial cable and power cable is connected from the receiver to the antenna base.
FREQUENCY RANGE:	20-520 MHz
DIMENSIONS:	See Figure 1-2
WEIGHT:	25 pounds (11.3 Kg)

NOTE

Specifications for other antennas compatible with the OAR 3045 are listed (where used) in the addendum to the technical manual.



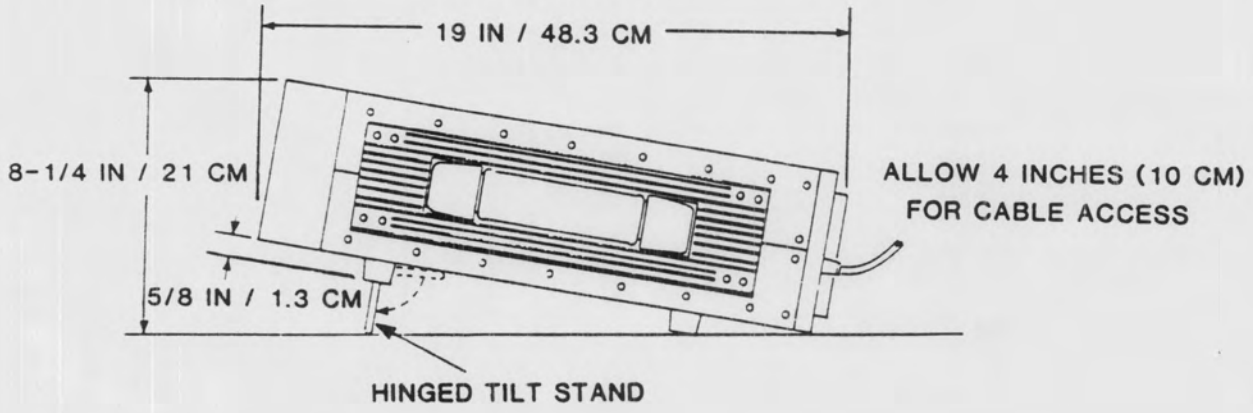


Figure 1-1. Chassis Dimensions, OAR 3045

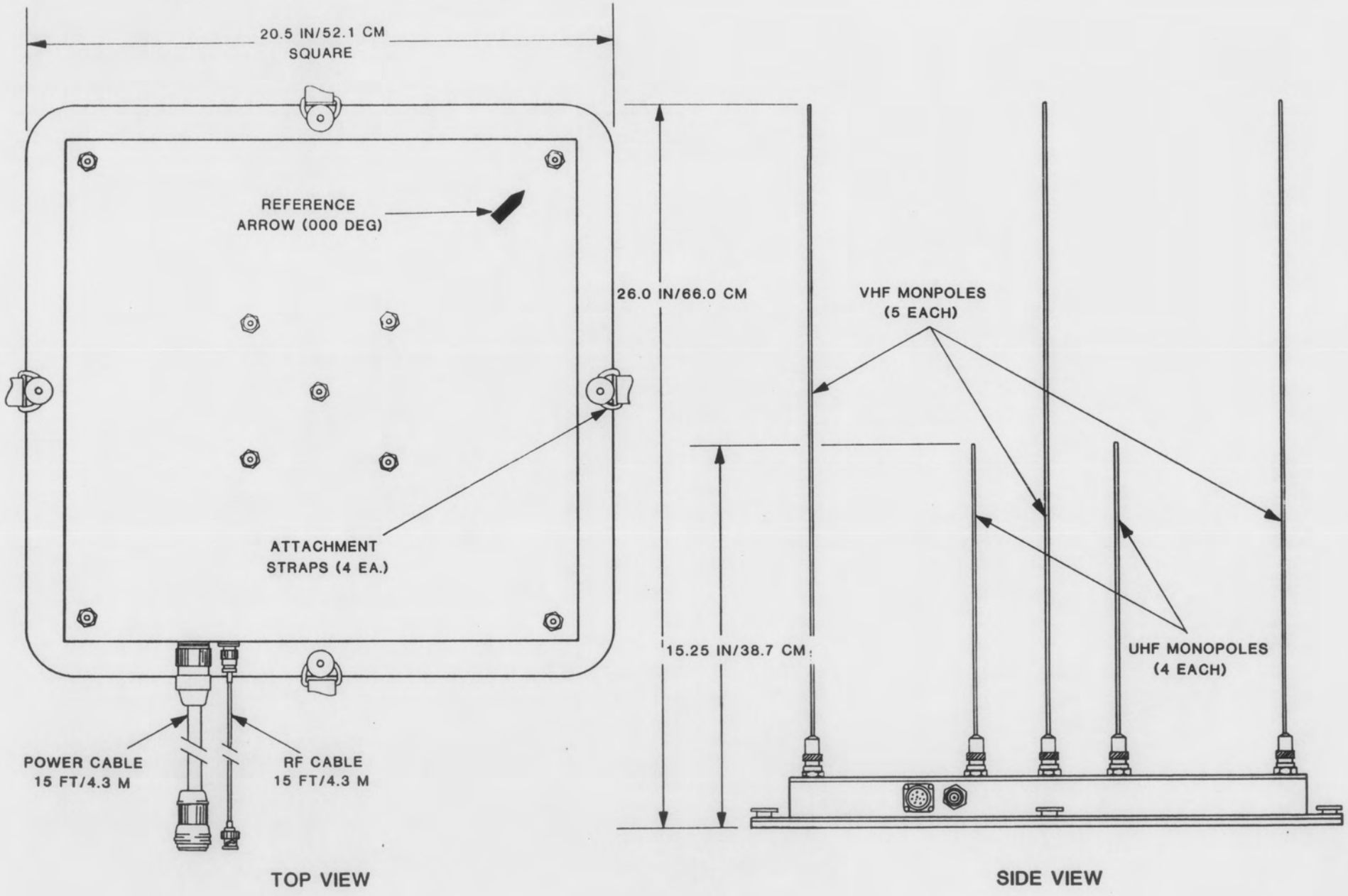


Figure 1-2. MA396E ANTENNA DIMENSIONS

SECTION II

SERVICE UPON RECEIPT AND INSTALLATION

2.1 SERVICE UPON RECEIPT

2.1.1. Unpacking and Inspection

A. Inspect the equipment for damage incurred during shipment. If the equipment has been damaged, retain the shipping cartons and packing materials for the carrier's inspection.

B. Check the equipment against the packing slip to see if the shipment is complete. Report any discrepancies to OAR, San Diego, or their authorized representative.

C. The system was thoroughly inspected and adjusted at the factory before shipment. If no shipping damage is found, the equipment is ready for use.

2.1.2. Storage. If the equipment is not to be installed immediately, or not to be used for a period, store it in the shipping carton using existing packing materials. Storage temperatures should not be lower than -4 degree F. (-20 degree C.) or higher then +140 degree F. (+71 degree C.). The storage area should be protected from the weather, especially from the adverse effect of moisture.

2.2 INSTALLATION PLANNING

The locations of the receiver and antenna, and the routing of interunit cables are of primary concern in planning the installation of the system. In general, a location should be selected that offers ease of access for operation and maintenance. The relative locations of the receiver and antenna also depend on interunit cable lengths. Only the 10 ft. (304 cm), 12 Vdc power input cable is furnished with the receiver. The RF and power cables furnished with the mobile antennas are 15 ft. (4.6 M) long.

Special cable lengths may be ordered; however, antenna cables in excess of 50 feet (15.24 m) are not recommended due to voltage drop and signal losses.

2.3 INSTALLATION

2.3.1. Receiver Installation. The receiver is normally shelf-mounted with a tilt-stand or in a standard EIA equipment rack. One of the most important items to consider when mounting the receiver in a confined area is heat dissipation. The receiver generates heat and adequate air circulation must be provided. Since all signal and power connections are made in the rear of the receiver, ease of access and adequate space must be planned. Provisions should be made for shock mounting. Prolonged exposure to shock and vibration can only lead to an earlier failure if such additional protection is not provided. The receiver should be located so the operator can observe the scope and adjust the controls if required. Areas with low ambient light for

good scope contrast are preferred.

Chassis outline dimensions are shown in Figure 1-1. Connect the receiver to its power source. The standard unit operates on 12 VDC (60 Watts).

2.3.2 Interconnections. All connectors are located on the rear of the receiver except for a 4 Ohm, 4 Watt phone jack on the front panel. Rear panel connectors are shown in Figure 2-1. Descriptions of each connector with paragraph letter related to the callouts in the illustration.

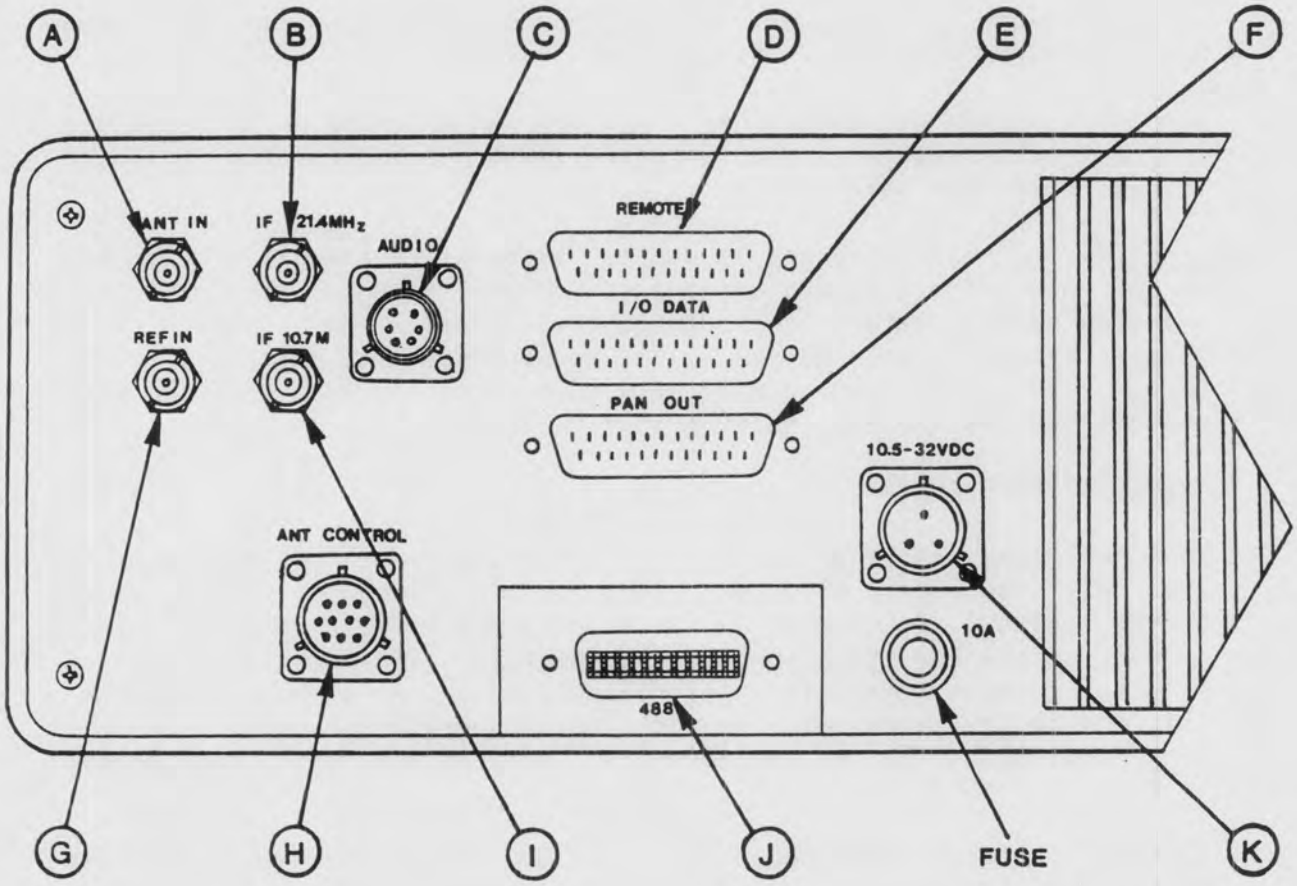


FIGURE 2-1. REAR PANEL CONNECTORS, OAR 3045 RECEIVER

A. RF input from antenna (J1); BNC, 50 Ohm connector.

B. Wide-band, IF output connector (J2) for input to a 21.4 MHz signal monitor or recorder, BNC 50 Ohm connector.

C. Remote audio connector (J6) is used for external audio recording. In addition to the audio output, there is a carrier operated relay (COR) circuit to turn on/off the recorder. The COR switching level is adjusted by the SQUELCH threshold control. The connector also has

provision for receiver muting by external grounding. This is a PT02E-10-6-SW connector with the following pins.

PIN	CIRCUIT FUNCTION
A	External Mute. Receiver is muted when this pin is grounded through the audio return (pin C).
B	Audio output. Audio level is internally adjustable to 1.5 Vp-p into 600 Ohms.
C.	Audio return (ground).
D.	COR Relay common.
E.	COR Relay NC (normally closed)
F.	COR Relay NO (normally open).

NOTE: COR lines should be limited to 100 V, referenced to ground, and 1 Amp maximum current or the relay may be damaged.

D. Remote control connector (J7) is used for remote control and monitoring of the receiver, and is designed to connect to a modem or a computer. The 25 pin connector (IEC-625-1, male) is configured as a DTE (data terminal equipment) with pins conforming to RS-232C standards except the audio lines as listed below.

PIN	CIRCUIT FUNCTION
1	Chassis (protective ground)
2	TXD, transmitted data output
3	RXD, received data input
4	RTS, request to send output
5	CTS, clear to send input
6	DSR, data set ready input
7	Signal Ground (common return)
8-10	No Connection
11	Audio return
12-19	No Connection
20	DTR, data terminal ready output
21-24	No connection
25	Audio (-9 dBm, 600 Ohms)

E. Input/Output data connector (J8) conforms to RS-232C standards and is an IEC 625-1, 25 pin female connector. Pin circuit functions are the same as in D (above) except that pins 11 and 25 are not connected. Configured as a DCE (Data Communications Equipment). All lines listed as output are input and vice-versa. This connector can also be used as an input for a digital output compass (optional).

F. Panoramic output connector (J9) is also an IEC 625-1, 25 pin female, and is the digital data bus output for the PAN display. Connector J9 also contains the X, Y, and Z remote CRT analog outputs.

G. Reference frequency (1 MHz) input connector (J3) is a BNC, 50 Ohm connector.

H. Antenna Control (J5) is a 19 pin output to the antenna with the following pin functions.

PIN	CIRCUIT FUNCTION
A	+15 Vdc
B	Chassis ground
C	Horizontal tone
D	Vertical tone
E	Direction (DIR)
F	Modulation
G	Antenna data
H	-15 Vdc
J	Data 0
K	Data 1
L	Data 2
M	Data 3
N	Data 4
P	Data 5
R	Data 6
S	Address 0
T	Address 1
U	Address 2
V	Write (WRT)

I. Narrow Bandwidth IF output connector (J4) is for input to special purpose detector or recorder, BNC, 50 Ohm connector.

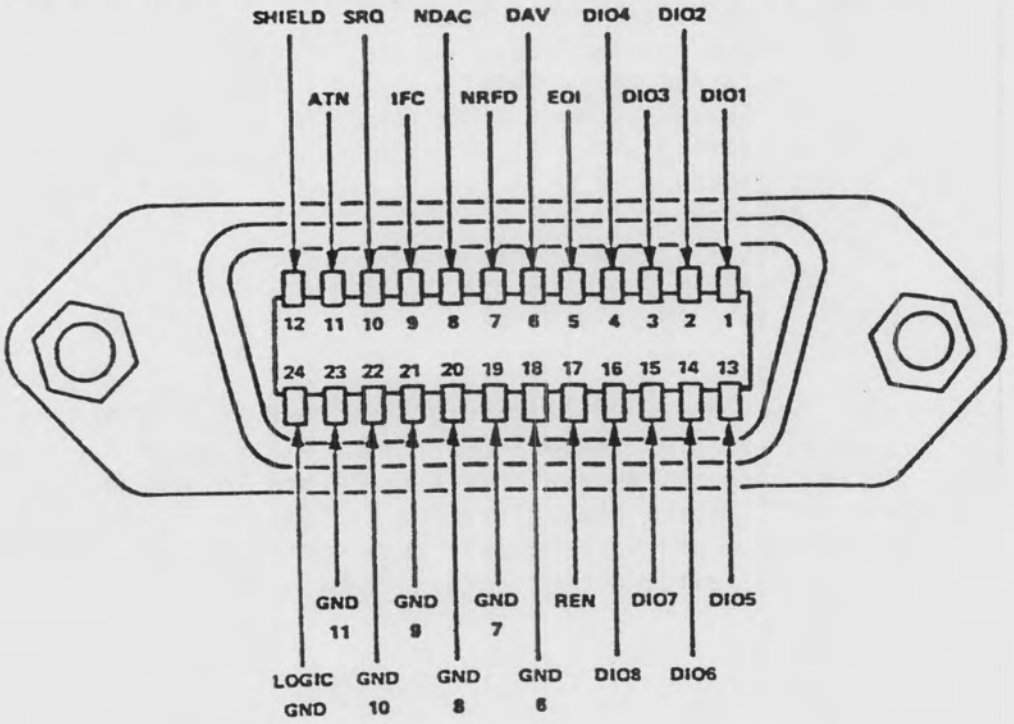


FIGURE 2-2. IEEE-488 STANDARD CONNECTOR

J. Optional IEEE-488 General Purpose Interface Bus (GBIB) connector (J14), type IEEE-488/ANSI MC1.1, with connections as showing in Figure 2-2.

K. Input power connector (J13), a three-pin Cannon connector, type DBSP-B25P with the following pins.

PIN	FUNCTION
A	+12 Vdc (10.5-32 Vdc), fused for 10 Amp.
B	+12 Vdc return.
C	Chassis ground.

2.3.3. Antenna Installation. The proper location of the antenna is paramount for optimum system performance. Generally, the location should be as far away as possible from sources of signal reflection or reradiation. If more than one site is available, each location should be tested for best results before installation is made.

The antenna may require initial alignment and realignment after the system is operational to improve system accuracy. The system is electrically aligned by O.A.R. so that with the red arrow on the antenna pointed in the direction of a received signal, the CRT trace will be at 0 degrees. What is chosen for the 0 degree reference depends upon the operational use of the ADF system. Normally, landbased installations align the antenna with the red arrow pointing to True or Magnetic north so that True or Magnetic bearings of radio signals may be read directly from the CRT. Ship, automobile and aircraft installations normally have the antenna mounted with the arrow pointing forward or dead ahead so that the CRT trace indicates in degrees relative to the heading or course.

The antenna must be mounted on a metal ground plane (such as the roof-top of an automobile or the fuselage of an aircraft). The MA396E monopole antenna is shipped with the nine elements removed. Before operation, these elements must be installed on the housing. The elements are attached with the TNC connectors. Improved bearing accuracy may be possible by removing the elements for an unused frequency range. For example; if operating frequencies are restricted to the VHF band (20-120 MHz), remove the four, short UHF elements. Outline dimensions of the antenna is shown in Figure 1-2.

2.3.3.1. Aircraft Installations. For optimum results, the monopole antenna should be installed on the underside of the aircraft on a flat surface as far away as possible from obstructions such as other antenna and landing gear. Its location must not interfere with the safe operation of the craft and should not be exposed to excessive amounts of gas, oil or engine exhaust. A sheltered route must exist for inter-unit cables. Recommended antenna locations for typical aircraft are as shown in Figure 2-2. The antenna is capable of operation up to air speeds of 1/4 Knots (200 mph, 322 Km/hr) when securely mounted on a structure capable of withstanding the

aerodynamic forces on the antenna base. The plate is hinged at the base to existing pads and the supporting arms fastened to pads with quick-release toggle pins. The support plate on helicopters should be tilted approximately 7 degrees to the axis of the airframe so that the dipoles are vertical when the helicopter is in flight and tilted 5-10 degrees to the horizontal plane.

Follow the steps below to install the antenna:

A. Note the forward part of the antenna that is marked with the red tape arrow. Position the antenna on the underside of the fuselage (figure 2-3) so the forward part points toward the desired reference point, usually the front of the craft.

B. Attach the elements to the antenna housing.

C. Determine where the straps and antenna will be placed. Clean an area at least 4 inches around the edge of the area where the antenna and straps will be placed. The surface must be clean and dry. If available, use a solvent to remove grease and film. In lieu of solvent use clean rags.

NOTE

On a small fixed-wing aircraft the best installation is typically in back of the cockpit where the fuselage is smaller. Cartop straps can be put around the whole fuselage.

D. While holding the antenna against the fuselage, attach the cartop straps and pull tight. Cartop straps can be extended by connecting an extension strap. Align the antenna so it is "square" with the fuselage. This alignment will affect 000 degrees bearing indications.

E. Tape around the edge of the antenna leaving the connectors clear. Tape down the cartop straps. Use two or three layers overlapping about 3/4 in 1 inch. Place the first strip of tape along the edge of the antenna towards the rear of the plane.

F. Make sure that there are no loose pieces of tape or strap. Cover any area that looks questionable with more tape.

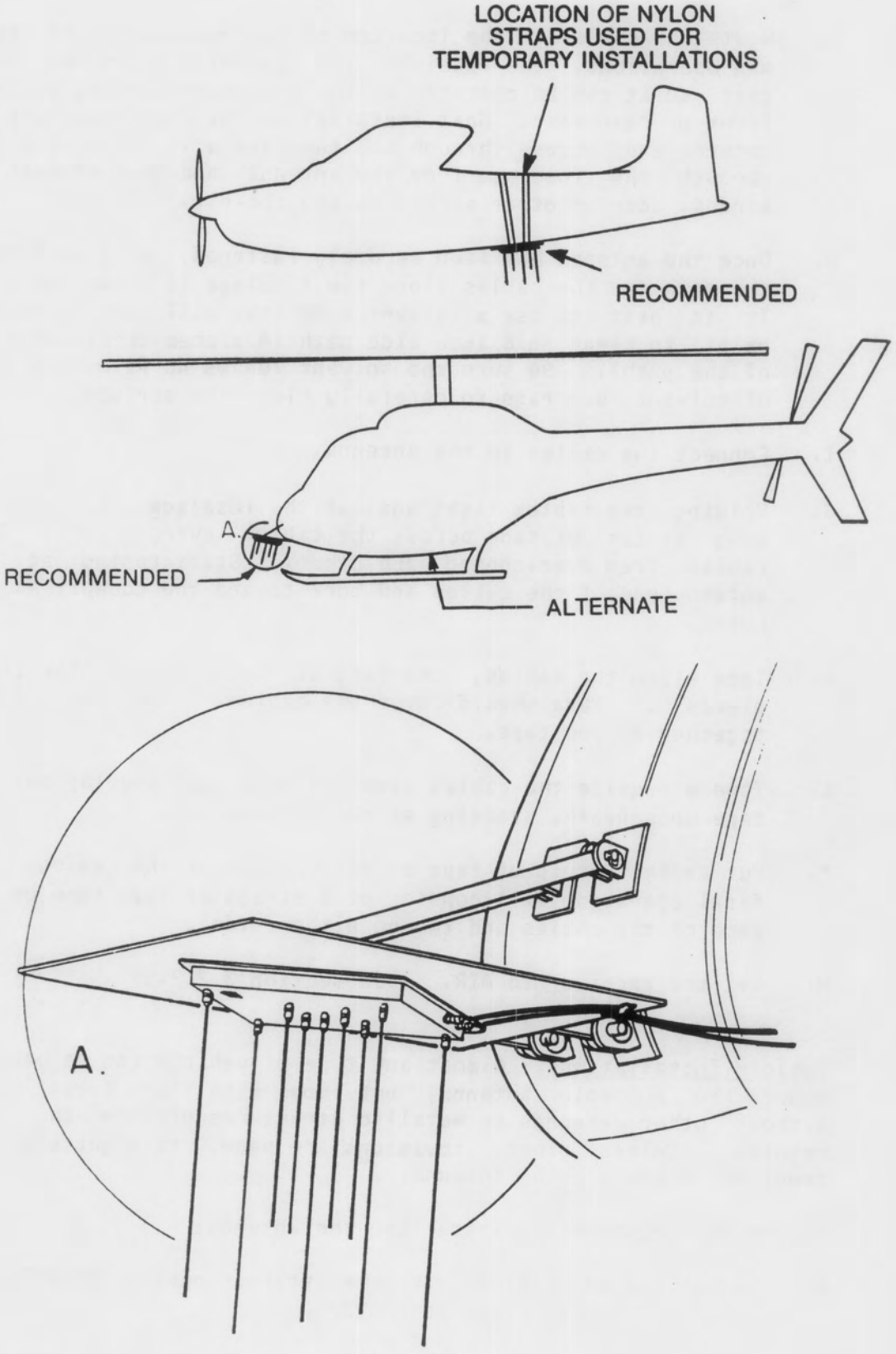


Figure 2-3. Recommended MA396E Antenna Locations On Aircraft.

G. Route the cables to the location of the receiver. For two-man operations, the receiver will typically be on the back seat so it can be operated by the passenger sitting in the front or rear seat. Most installations will be temporary in nature and access through the fuselage will typically be through the fuselage from the antenna and then through a window, door or other access to the cockpit.

H. Once the antenna has been securely fastened, make sure that the path for the cables along the fuselage is clean and dry. It is best to use a solvent (one that will not dissolve paint) to clean an 8 inch wide path (4 inches on either side of the path). Be sure the solvent leaves no film. In lieu of solvent, use rags to carefully clean the surface.

I. Connect the cables to the antenna.

J. Holding the cables tight against the fuselage, use 6 inch long strips of tape across the cables every foot. Keep cables from overlapping each other. Start taping at the antenna end of the cables and work toward the cockpit access hole.

K. Tape along the cables, starting at the antenna. The first pieces of tape should cover the cables. Push the cables together as you tape.

L. Tape alongside the cables with 3/4 to 1 inch overlap on the tape underneath, starting at the antenna end.

M. Put another strip of tape on either side of the cables. The final operation will consist of 5 strips of tape (one on top each of the cables and two on either side).

N. Set the receiver to AIR. (see section 3.2.7.2)

2.3.3.2. Vehicle Installations. Almost any type of vehicle can be used to mount the monopole antenna, but those with flat metal roofs without other antennas or metallic structures provide the best results. Unless other provisions are made, rain gutters are required to install the antenna.

Following the steps for installing the antenna:

A. Attach the sense element to the antenna housing (AFL285E) or the four tubular elements (MA287).

B. Place the antenna on the vehicle roof and align the red arrow toward the front as shown in Figure 2-4.

C. Hook the O-ring of each of the four straps over the base-plate post, and route the clamp ends of the straps to the gutter.

D. Hook the clamps onto the gutters, and tighten the straps until the antenna is firm against the roof; maintaining forward element alignment.

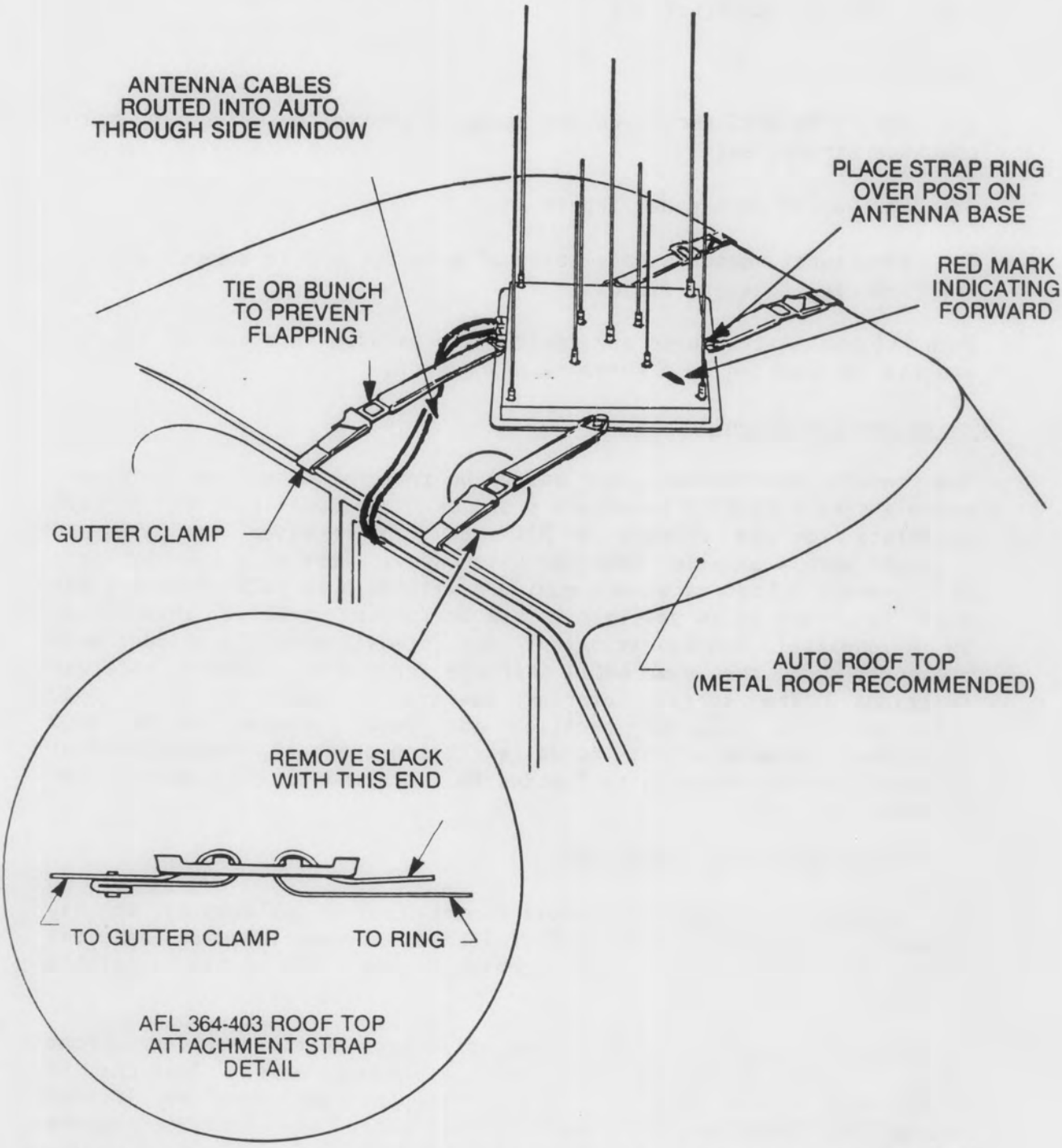


Figure 2-5. Strap-Mounted MA396E Antenna, Typical Cartop Installation

E. Tie off any loose strap ends to prevent flapping in the wind.

F. Route the two integral cables that exit the housing into the vehicle through a passenger-side window. These cables mate with the receiver.

G. Set the receiver on AUTO. (see section 3.2.7.2)

2.4 REMOTE CONTROL INSTALLATIONS

2.4.1 General

The OAR 2040/3045 receivers are remotely controlled using two basic commands structures:

A. Equivalent from panel inputs or,

B. Structural commands consisting of a leader and in some cases, a numeric arguement field.

Both command structures are designed to be used in a remote control program implemented by a software programmer.

2.4.2 Design Considerations

The remote control equipment has to be interfaced to the receivers using a serial RS-232C interface protocol. Optionally, the RS-232C interface can be changed to MIL-188. The receiver can also be supplied with a parallel IEEE-488 interface if fast data transfer is a requirement. For receivers equipped with both an IEEE-488 and a RS-232C interface it is possible to use serial and parallel interfacing in a parallel configuration(but not simultaneously), since both protocols use the same ASCII character groups to address receiver functions. The serial interface operates at speeds of up to 9600 bytes/sec. The IEEE-488 parallel interface operates up to 8000 bytes/sec. However, the actual execution speed of remote control commands by the receiver is limited to approximately 10 commands per second.

The Remote Controller (Computer)

The protocol selected for remote control can be implemented on any computer compatible with RS-232C or IEEE-488 in any language that uses ASCII characters. This incorporates at least 99% of all available computers.

Due to the limited number of operating keys on the receiver front panel, certain functions require multiple key strokes. This can be troublesome to the operator. An external processor (computer) located beside the receiver can simplify operation and increase system capability.

A. Complicated key sequences can be reduced to simple operator entries using an interactive question-and-answer type operator/processor interface. This interface can be written in any language that uses the Roman alphabet.

B. Measurement and status information can be requested from the receiver, stored in the computer and/or processed immediately for operator analysis.

C. In the scan mode, the computer can generate an RF-spectrum display in parallel with the receiver scanning. This eliminates the need for a separate RF spectrum display.

D. While the receiver can be connected to an OAR furnished line printer, all types of printers, plotters, disk and tape medium can be attached through a processor.

E. The processor can be used for network control (see figure 2-7).

OAR offers such a processor (computer) for use in spectrum monitoring and automatic direction finding systems. The programming language is PASCAL and a RS-232C interface is used where only one receiver needs to be controlled. Remote control using RS-232C is limited to the one receiver, one processor configuration. Where there are long distances between the receiver and processor, a modem on both sides and a connecting medium (telephone, microwave) is required for remote control.

Real network control (more than one local receiver and/or more than one remote site) requires the use of the parallel IEEE-488 interface. Although many receivers, controllers and peripherals can be connected in daisy-chain fashion at the local (control) site; those using a processor, an OAR 2040, OAR 3045, and a printer require full remote control capability and the receivers must have the optional IEEE-488 interface installed. Therefore, the extension to include remote sites does not really change the configuration (just more receivers and antennas), but only the interconnect medium changes.

Each remote site will be set up like the local site with all receivers daisy-chained to the IEEE-488 controller which is connected to a modem, the interconnect medium (Telephone, RF or Microwave) and on the master (local) site, through a modem, back to a 488 controller. A typical network consisting of a master (local) site and two remote sites with one 2040/3045 combination at each site would look like figure 2-7. The audio part of the network is not shown. If only one

line is available per site, data and audio can be combined in one channel, using a sub-audio tone to tell the receiving side if data or audio is being sent over the line (figure 2-8).

The display of the remote IF-panoramic presentation requires a high speed data channel through a microwave link as shown in figure 2-9. The data rate should be at least 4800 baud for the panoramic line. A less expensive alternative is to display the real RF spectrum when the receivers are in the scanning mode. Any detected carrier will be reported to the master controller together with the signal level. This information can be used for a spectrum display at the master site. This could be accomplished with a small programming effort. The build-up time of a spectrum display will be relatively slow, depending on the speed of the interface link.

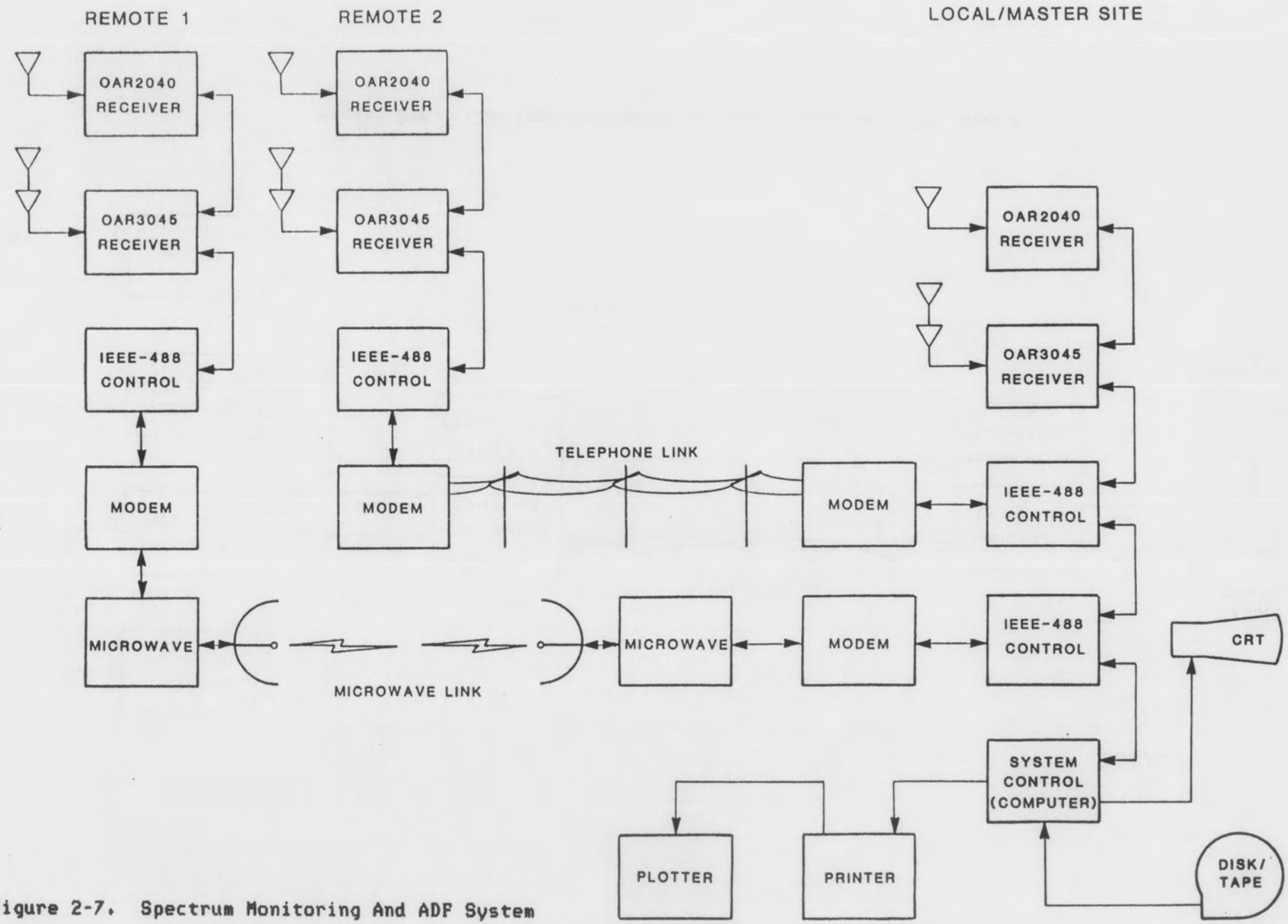


Figure 2-7. Spectrum Monitoring And ADF System

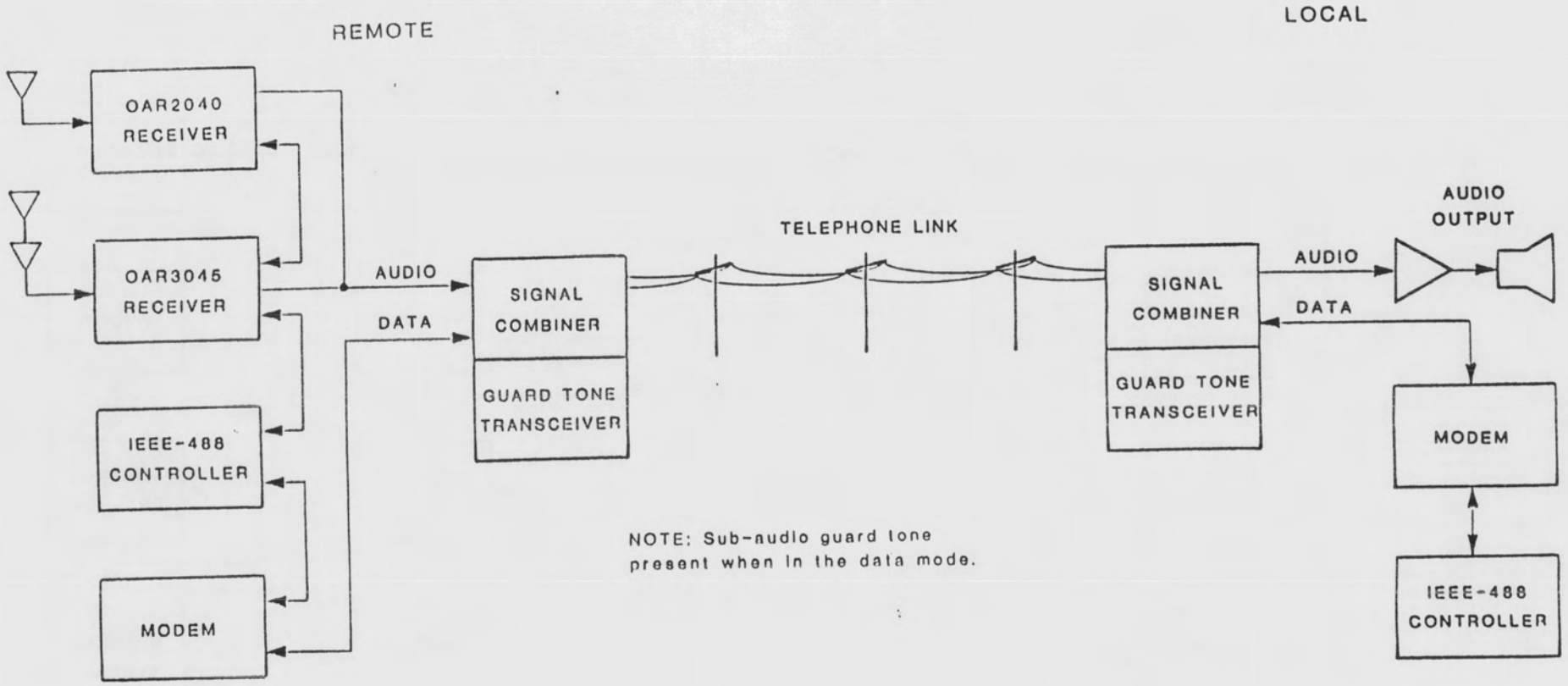


Figure 2-8. Combined Audio/Data Transmission Over One Channel

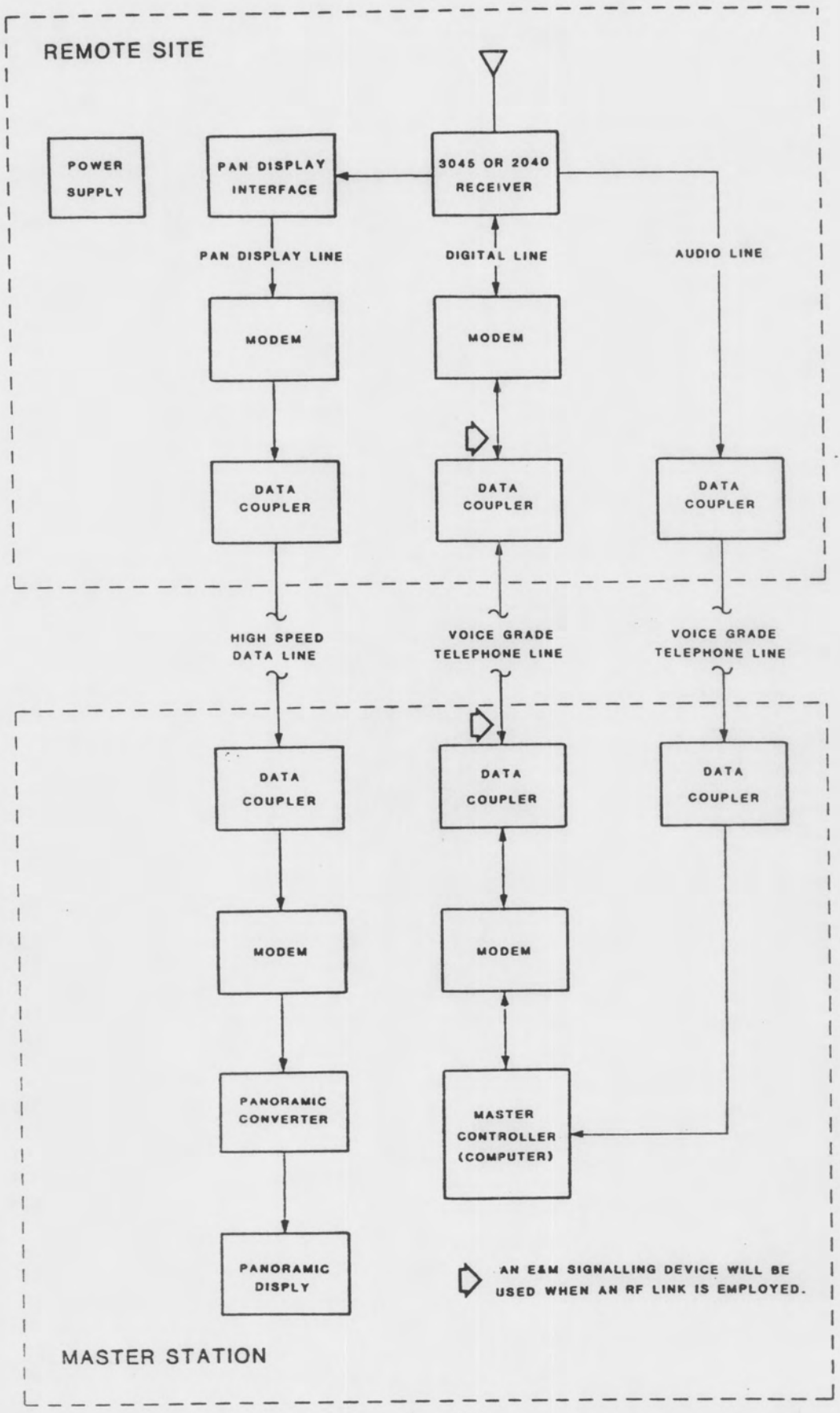


Figure 2-9. Remote Control System Using Separate Control, Audio, And Panoramic Links

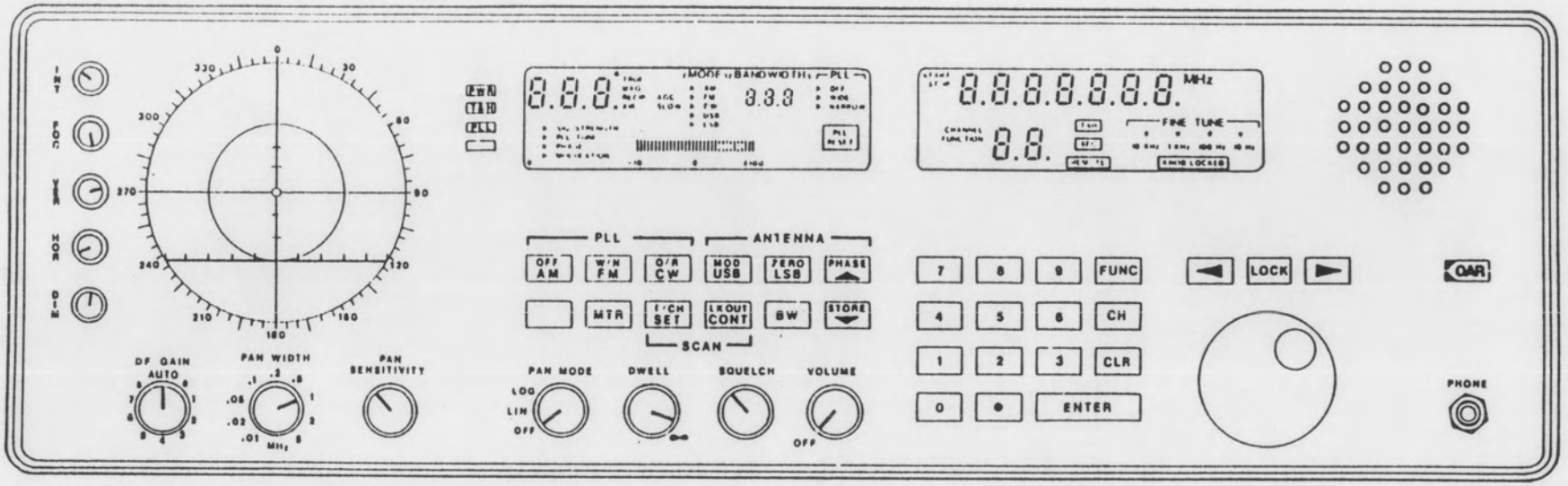


Figure 3-1. OPERATING CONTROLS AND DISPLAYS, OAR 3045

OPERATING INSTRUCTIONS

CAUTION

Read the operating instructions completely before attempting to operate the equipment.

3.1 OPERATING CONTROLS AND INDICATORS

All controls and indicators are identified in Figure 3-1 and listed below. The controls, pictorially represented, and their basic functions are described below. All the basic operating controls are located on the front panel.

NOTE

Model OAR240 and OAR345 receivers do not have a panoramic display. Paragraphs of Section III referring to the panoramic controls and display do not apply to the OAR240 or OAR345 receivers.

3.1.1 Controls

A. VOLUME CONTROL/ON-OFF SWITCH

This control operates both as an ON/OFF switch for the ADF system, and as the audio volume control. Turning the switch clockwise will turn system power on. There will be a slight time delay (approximately one second) before system power will come on. Do not attempt to restart during this period, wait for the system to power up. Once power is up, the system will self-test as per paragraph 4.5.2.

Once the system is on, the audio volume may be increased by turning the switch clockwise. Turning the switch fully counterclockwise will turn the system off.

A LED (light emitting diode) to the right of the CRT will light up to indicate that power is on.

B. CRT CONTROLS

These controls are used for adjusting the CRT display under static conditions.

INTENSITY

This control establishes the brightness of the CRT trace. Rotate the intensity control clockwise just far enough to provide minimum visible brightness to present

adjustment of this control may be necessary once a signal trace is established. Always rotate this control fully counterclockwise prior to turning the equipment OFF.

CAUTION

Never leave this control at a high intensity position. When a constant dot or trace appears on the screen over an extended period of time, CRT damage can result.

FOCUS

This control should be used to establish a sharp, well-defined dot or trace on the CRT. The intensity and focus controls will interact to some extent, but once set to the desired position these two controls should require no further adjustment while the equipment is operating.

VERTICAL

The vertical control is used to move the dot up or down. Adjust this control to center the dot vertically with no signal present or at the zero gain setting.

HORIZONTAL

The horizontal control is used to move the dot left or right. Adjust this control to center the dot horizontally with no signal present or at the zero gain position of the gain control.

C. DIMMER

This single control varies the background illumination for the LCD displays and the front panel controls. The DIMMER control also varies the illumination of the LED's and keypads. Adjust the control so displays and controls are clearly visible under the existing operating conditions.

D. DF GAIN

This control varies the trace length when a bearing is displayed on the CRT. The DF gain control is a 10 position switch. The 0 position represents zero gain (no trace) positions 1 through 8 will increase gain a step at a time. The switch controls a variable attenuator in the scope video amplifier, and has no effect on the receiver gain.

Adjust the DF gain control to establish a bearing trace extending almost to the edge of the CRT. This is the best trace length for

reading bearings. Use the maximum gain position (8) when searching for a signal. Once the system has locked onto a signal, the gain control can be adjusted to the desired length. Optionally, the switch may be set to the automatic gain control (AGC) position. In this case the equipment selects the best optimum gain setting automatically.

The DF gain control has no effect using panoramic display.

E. PAN WIDTH

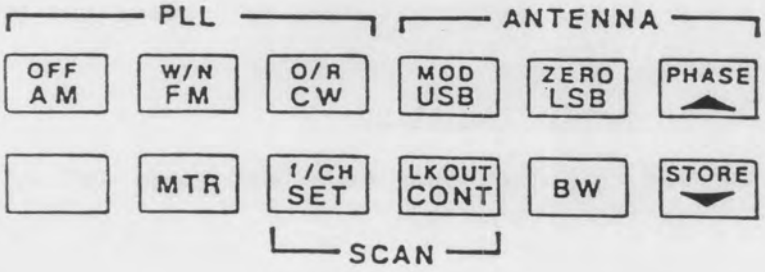
This is a nine position switch used to adjust the horizontal presentation when the system is in the panoramic mode of operation. When panoramic display is utilized, the CRT will sweep a frequency band centered at the frequency the receiver is set to. The PAN WIDTH controls the bandwidth of frequencies that will be swept. In panoramic display a number of signals may be observed at once. Decreasing the pan width will increase the resolution between signals.

NOTE

Pan width is variable between 20 kHz and 2.5 MHz in the OAR 3045 receiver. The lowest and highest positions of the switch are unused.

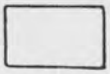
F. PAN SENSITIVITY

This control is used to vary the sensitivity of the vertical panoramic presentation. The control should be adjusted to give adequate sensitivity to weak signals without driving the stronger signals off the face of the scope. The graticule markings on the vertical center line allow comparison of relative signal strength between signals. Vertical deflection is determined by relative signal strength and the setting of the pan sensitivity control.



G. MULTIFUNCTION KEYPAD

This Keypad consists of a series of receiver controls with dual function capabilities. The bottom key labels are the effective controls until the SHIFT KEY is pressed. When the SHIFT KEY (lower left, unlabeled) is pressed the shift LED to the right of the CRT will illuminate, and the upper set of controls will be enabled. Pressing a key initiates a control sequence of one step, or multiple steps. In either case, when the control sequence is complete, the SHIFT KEY will automatically deactivate, and the bottom key labels will again be in control. The dual function control keys are labeled with black letters on the bottom functions, and green letters on the top. The green letters serve as a visual indication of SHIFT initiated functions.



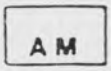
SHIFT

This is the light green unlabeled key in the bottom left corner of the key pad. If the SHIFT key is depressed prior to depressing one of the dual function keys, an upper control sequence is initiated. Control is automatically restored to the lower functions once the control sequence is completed. When pressed once, the SHIFT key initiates upper function control. If no other button is pressed, upper level control will be maintained indefinitely. Depressing the SHIFT key a second time will restore lower level control. The green SHIFT LED serves as an indicator of shift status, and a dot will appear in the lower left corner of LCD1 when upper level control is active.

DEMODULATION MODE CONTROLS

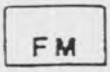
With lower level control (shift deactivated), the first five keys across the top of the key pad set the demodulation mode for the ADF system.

Demodulation modes are as follows:



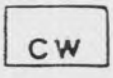
Amplitude Modulation

For carriers that have been modulated by varying the amplitude.



Frequency Modulation

For carriers that have been modulated by varying the carrier frequency.



Continuous Wave

For pulsed CW, when the carrier has been turned on and off. Adjust the fine tuning for best reception.

[USB]

Upper Sideband

For single sideband transmission when the carrier is suppressed and information is in the upper sideband. Activating USB will disconnect the audio filter. Fine tune for best reception.

[LSB]

Lower Sideband

For single sideband when the carrier is suppressed and information is in the lower sideband. Adjust fine tuning for best reception.

The remaining lower level control functions are as follows:

[▲]

INCREMENT

Facilitates an increase in the active function.

[▼]

DECREMENT

Facilitates a decrease in the active function.

These two controls are used in adjusting various receiver functions in the following manner.

FREQUENCY:

Tunes the receiver frequency at the selected tuning step size.

CHANNEL:

Dependent on current status will set the next higher or lower channel.

MODULATION

Increase or decrease antenna modulation.

PHASE

Shifts antenna phase by one increment.

ZERO HEADING:

Offsets antenna zero heading by one increment.

[SET]

SET

Is used to display the stop and start frequency/or channel. SET acts as a toggle for reviewing scan capabilities. When the key is initially toggled it will remove the receiver from its current status and display the start

frequency/channel. The second toggle will display the STOP frequency/channel. Depressing the SET key again will return the receiver to its current status.

CONT

CONTINUE

Initiates SCAN function. Initially pressing this key will cause the receiver to scan. If the scan was previously set to a frequency it will scan frequencies. If the scan was previously set to a channel it will scan channels. The frequencies or channels scanned will depend on the initial setup of the SCAN function. Depressing the key again will stop the scan and the system will dwell indefinitely at the current scan point. Pressing CLR will return the receiver to its current status.

MTR

METER

Toggles the bar graph section of the LCD1 display. Each time this key is depressed it will display one of the four metered functions (signal strength, PLL tune, antenna phase, antenna modulation) and an arrow on the LCD will point to the active function. With PLL tune selected and the PLL OFF, AFC voltage is displayed.

BW

BANDWIDTH

This key is used for manual selection of IF bandwidth. To manually select bandwidth, depress the BW key and the appropriate bandwidth will be selected in ascending order. There are four selectable bandwidths (6 KHz, 13 KHz, 30 KHz 200 KHz). The selected bandwidth in KHz will be displayed in the three digit section of LCD1.

The following are upper level controls and are active when the SHIFT key has been depressed and the LED is illuminated:

PLL CONTROLS

These three keys control receiver PLL (Phase-Locked Loop) operation. See Paragraph 3.2.3.4. for further explanation.

W/N

WIDE/NARROW (PLL ON)

Depressing this key when the PLL is OFF will turn the PLL ON in the wide position. Depressing the key with the PLL ON and wide will toggle to the narrow position.

OFF

PLL OFF

Depressing this key will unconditionally turn PLL OFF.

O/R

OPERATE/RESET

Depressing this key with the PLL operating will trigger a PLL RESET condition. The error voltage will drop to zero and the PLL oscillator will return to 455 KHz. RESET will also turn off the sub-audio antenna modulation tones. Depressing this key in a RESET condition will trigger a PLL OPERATE condition.

NOTE

When using the receiver as a communications receiver only, the PLL should always be put in the RESET condition. This shuts down the DF circuits in the antenna.

ZERO

ANTENNA ZERO

Initiates antenna zeroing control sequence.

PHASE

ANTENNA PHASE

Initiates antenna phase setting control sequence for AFL285 and other specified ferrite antennas only.

MOD

ANTENNA MODULATION

Initiates a control sequence to manually set antenna modulation.

SCAN CONTROLS

The following two Keys are scan control sequence switches, and are used in conjunction with the SET and CONT controls (lower level, same key).

F/C

FREQUENCY/CHANNEL

When displaying SCAN STOP/START capabilities this Key is used to switch between frequency and channel displays.

LKOUT

LOCK OUT

This key will lock-out either the current channel, or a selected channel from the scan sequence. It is also used to restore a locked out channel.

STORE

STORE

This control stores the current receiver status as a channel. If a numeric entry was made, that channel number

is utilized. If a channel already exists under that number, it is replaced by the new entry. If not a valid channel number, an error code is flashed.

H. PAN MODE

This control is a three position switch used to initiate the panoramic display function.

LOG

Turns on the logarithmic section of the AM amplifiers in the panoramic receiver, allowing presentation of a logarithmic display of signal strength.

LIN

Turns on the same display as LOG.

OFF

Turns the panoramic section of the receiver and displays the bearing on the CRT.

I. DWELL

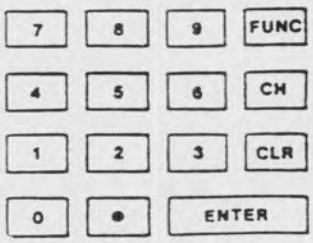
This control is used in scan function. When the receiver detects an active frequency it will stop at that frequency for operator observation. DWELL control determines how long the system will pause at this frequency before continuing scan. Infinity means it will dwell until the CONT key is pressed.

J. SQUELCH

Sets the system squelch, T+H, and COR threshold levels. Mutes audio noise when a signal is not present. Counterclockwise is minimum squelch, clockwise is maximum. To adjust the squelch threshold, turn the control fully counterclockwise and tune the receiver to noise. Adjust the control clockwise till the noise just disappears. Tune to a known weak signal and adjust, if necessary, to attain that signal. Repeat the process as necessary to achieve the desired level.

K. NUMERIC ENTRY KEYPAD

This Keypad consists of keys for entering the numbers 0-9 and the control keys associated with numerical entries. All numerical entries appear in the seven digit display area of LCD2.



NUMERIC ENTRY

The keys labeled zero thru nine and the decimal point, are used for making numeric entries.

Numeric entries are used to set frequency, to review or

store a channel, to set scan parameters, and to enter coded functions.

When a numeric entry is made it will clear the display, and the first entry will appear to the extreme left of the seven digit display. A flashing prompt will appear to the right of the first number entered until the complete entry is terminated by a command. Subsequent numbers will appear from left to right, with the display moving one step to the right with each number entered.

If the first entry is decimal then [0.] will be displayed. Otherwise, the decimal is used when required as an entry.

If a terminated numeric entry is invalid for the desired function, an improper entry error code is displayed in the seven digit display. Depressing CLR clears the error code and restores the display to its current status. The numeric entry process can now be restarted.

In subsequent paragraphs of this chapter, a series of numerals to constitute a numeric entry will be designated by "(numeric entry)" in a bracket.

CLR

CLEAR

Operates as a system reset; pushing this key will update the controls and displays and return the receiver to its current status. During a multi-step control procedure, pressing CLR will return to the previous step, and pressing CLR a second time will return the receiver to its current status. During a multiple step control procedure, most other keys are deactivated and will have no effect. When in channel mode, pressing CLR will return the receiver to frequency mode.

ENTER

ENTER

This key acts as terminator in a control sequence,. It is used in setting frequency, setting channel, setting antenna functions, setting sweep parameters, etc. Depressing the ENTER key updates the receiver with numerical entries which set the frequency, change the channel, or alter other functions as designated by the preceding command sequence.

CH

CHANNEL

This key is used in a control sequence when reviewing or selecting a channel. If preceded by a numerical entry, depressing CH will cause the receiver to tune to that channel. If not preceded by a numerical entry, the receiver will display status of the last channel selected since power on; if no channel was selected, any active channel is displayed. Depressing CH a second time will set the receiver to that channel.

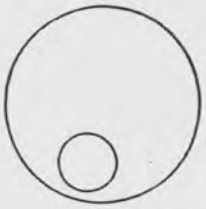
FUNC

FUNCTION

This Key is utilized in a control sequence to display a numbered function. If a numeric entry was made prior to the FUNC Key being depressed, and if that entry represents a valid function, that function will be executed, and the receiver returned to its current status. For multi-step functions see Paragraph 3.2.7.2. If not a valid function, the receiver returns to its current status. Numbered functions are listed in Paragraph 3.2.7.2.

L. FINE TUNING CONTROLS

The fine tuning controls consist of a tuning Knob and three Keys mounted above the tuning Knob. Fine tuning controls consist of the following:



TUNING KNOB

The Tuning Knob is a continuously variable control Knob, which will change frequency at a rate determined by its associated Keys, and as shown on the fine tune section of LCD2. Each turn of the tuning Knob consists of 500 increments on an optical encoder which sends pulsed information to the data processor, which in turn will output commands to tune the ADF system to the desired frequency. Each segment will tune at the current fine tune resolution rate.

Tuning clockwise will increase the frequency. Tuning counterclockwise will decrease the frequency. If the tuning Knob setting exceeds the frequency limits of the receiver, the data processor will no longer accept the information and the display will stop changing, but no error code will be flashed. The tuning Knob may be used during scanning to stop scan.

◄ ►

TUNING RESOLUTION

These two Keys will alter the tuning resolution. The arrows indicate SHIFT LEFT and SHIFT RIGHT as observed on the tuning area of LCD2. Tuning rates are selectable (10KHz, 1kHz, 100Hz, 10Hz) as indicated on the display. Depressing the SHIFT LEFT (arrow) Key will increase the tuning rate. Depressing the SHIFT RIGHT (arrow) Key will decrease the tuning rate. When at the 10 KHz limit the SHIFT LEFT (arrow) will not function; when at the 10 Hz limit the SHIFT RIGHT (arrow) will not function.

LOCK

LOCK

Depressing this Key will lock the system to its displayed frequency and electrically disconnect the tuning Knob. "KNOB LOCKED" will appear under the tuning section of LCD2. Locking the Knob ensures that the system will remain tuned

to the desired frequency. Accidental bumping of the Knob, or mechanical vibration of a vehicle will have no effect on the tuning as long as the knob is locked. Depress the LOCK key again to remove lock.

M. PHONE JACK

PHONE

This is a standard tip-ring connected phone jack. It is used for connecting a low impedance (4 ohm) audio headset to the front panel, so signal inputs may be heard. Connecting the headset will disconnect the internal speaker.

WARNING

Before connecting the headset ensure that the SQUELCH control is turned fully clockwise and the VOLUME control is turned counterclockwise to its lowest position. Failure to do this could result in ear damage to the operator.

After the headset is connected the SQUELCH should be set to just above the level where noise is heard, and then the VOLUME increased gradually until a desirable level is attained. Some interaction may necessitate retuning the squelch.

N. SPEAKER

The speaker is flush mounted to the front panel and will give an audio output when a signal is attained by the system. Audio level is set by the VOLUME control as previously described. There will be no output from the speaker if the headset is plugged in.

3.1.2 INDICATORS

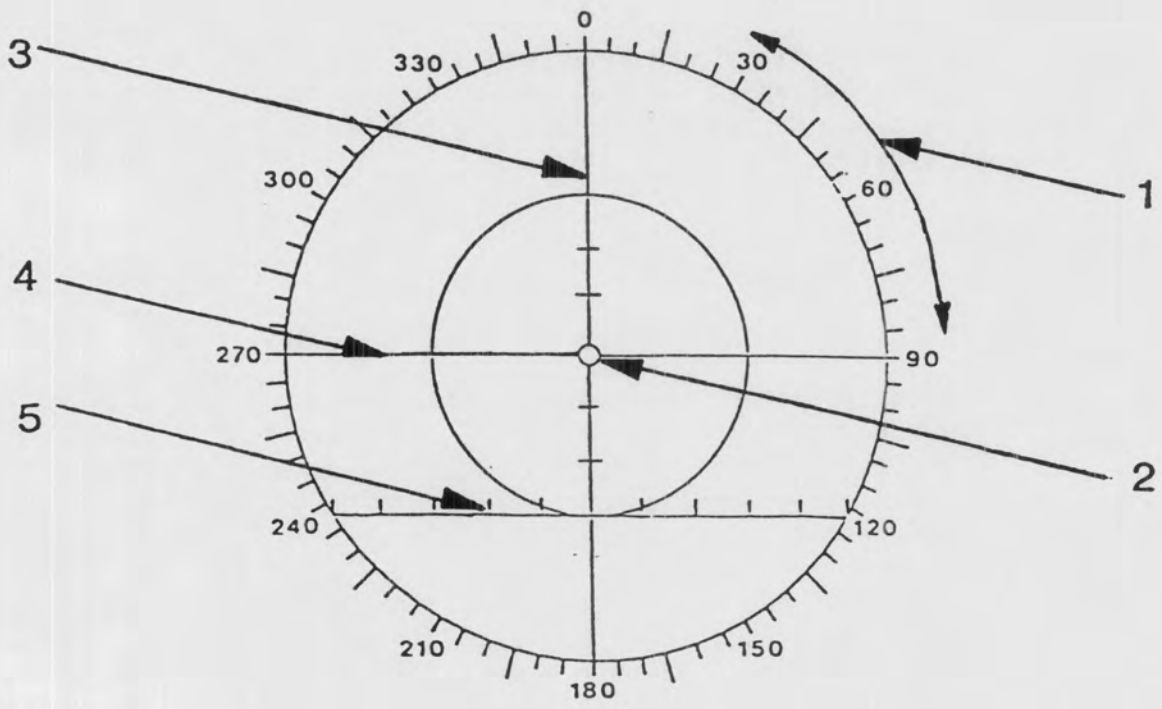


FIGURE 3-2 CRT DISPLAY

D. CATHODE RAY TUBE (CRT)

The cathode ray tube is a three inch (7.6 cm) diameter tube with a plastic overlay on which lines are etched to interpret various facets of the signal presentation. If the system is in DF operation the received signal will appear as a trace running from the center to the edge of the CRT scope. If the system is in PAN (panoramic) operation, the trace will appear across the bottom of the scope as a horizontal sweep, with a vertical deflection for each frequency received within the selected band.

The main CRT markings are identified by number in Figure 3-2 and appear as listed below:

(1) BEARING MARKINGS

Bearing readings are numericaly designated around the edge of the scope, with numerical designations at each 30 degree interval. Graticule markings at 5 degree interval permit

easy reading of the bearing, and interpolation allows bearings to be read to the closest degree. Bearing information also appears on LCD1 (three digit display).

(2) CENTER DOT

Providing a visible center dot marking provides an aid to centering the CRT dot with no signal present.

(3) VERTICAL CENTER LINE

This line corresponds to N-S (0 degrees - 180 degrees) representation on the scope. When in panoramic position, graticule markings allow comparison of relative signal strength.

(4) HORIZONTAL CENTER LINE

This line corresponds to E-W (90 degrees - 270 degrees) on the scope.

(5) PANORAMIC BASE LINE

The horizontal (sweep) trace should appear along this line when in panoramic position. The baseline may be centered by lining up the CRT trace with the panoramic baseline. The frequency the receiver is tuned to appears at the center, and graticule markings allow interpolation to determine the frequency of other signals in the display.

F. LED DISPLAY

The LED display consists of four LED's listed below which give visual indicators of the following conditions:

PWR POWER (BLUE LIGHT)

Indicates that power is up and the system is operational.

T&H TRACK AND HOLD (GREEN LIGHT)

Indicates that the system is holding a received signal.

PLL PHASE-LOCKED LOOP (YELLOW LIGHT)

Indicates that the phase-locked loop function is operational.

SHIFT (GREEN LIGHT)

Indicates that shift key is activated and the upper level controls of the multifunctional keyboard are active.

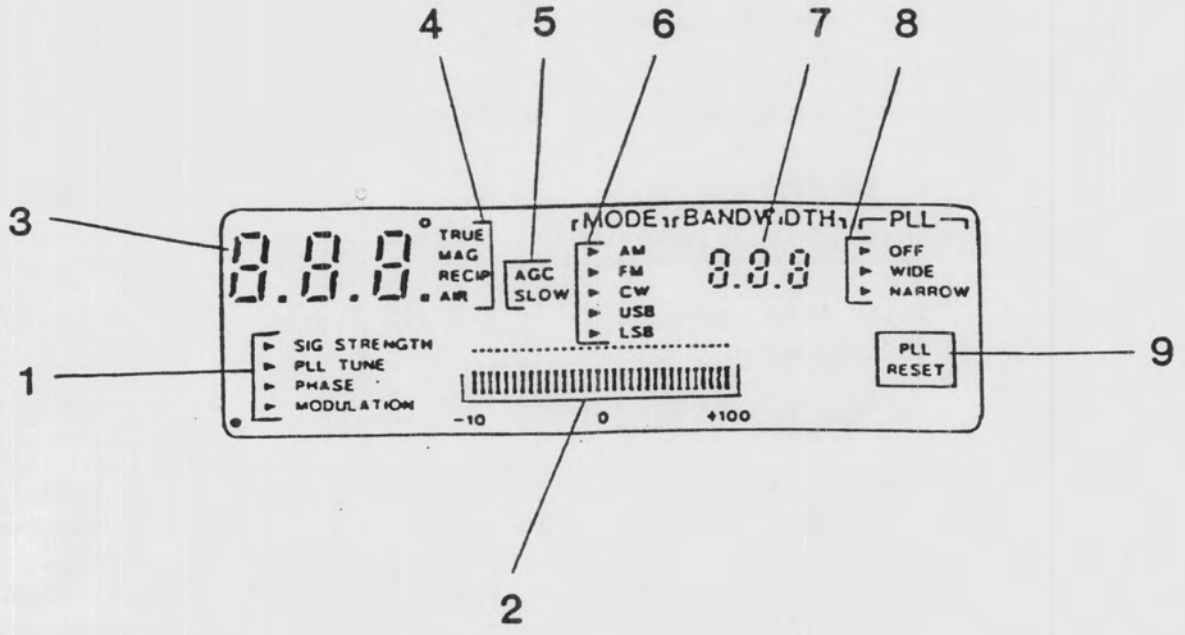


FIGURE 3-3 LCD 1 DISPLAY

Q. LCD 1 DISPLAY (LEFT SIDE LCD)

This display presents various indications of antenna and system operational modes. Main sections of the display are numerically designated in Figure 3-3, and listed below. Display lettering is black, with a reflective background.

(1) BAR GRAPH INDICATOR

The arrow will indicate which of the following sources of data is on the bar.

(2) BAR GRAPH

Displays visually the following data.

SIGNAL STRENGTH

Displays relative signal strength across the face of the graph.

PLL

Indicates if the PLL is tuned above or below the center frequency (preset) of 455 KHz.

AFC

Indicates if the AFC is tuned above or below the center frequency (on PLL display with PLL off).

ANTENNA PHASE

Indicated across the face of the graph. See section 3.2.4.1 for a more detailed explanation.

ANTENNA MODULATION

0 to 100% across the face of the graph. See section 3.2.4.2 for further explanation.

(3) 3 DIGIT BEARING DISPLAY

Numeric indication of bearing (0-359 degrees) of a received signal. Bearing is displayed to the closest degree. A decimal behind the bearing indicates that offsets are present. Display also provides indications when setting antenna zero heading.

(4) BEARING DISPLAY INDICATOR

Indicates the type of bearing the system is referenced to. Indications as shown below:

NO INDICATION

If there is no visual indication, the bearing is RELATIVE. Usually, this means bearing is referenced to the heading of the vehicle or ship the ADF system is installed on. Tentatively it could be referenced to anything. For instance: The direction of a street or a fixed sight.

TRUE

Bearings are referenced to True North.

MAGNETIC

Bearings are referenced to Magnetic North. (Compass variation will vary according to the region of the earth).

RECIP

Bearing displayed is reciprocal. This is used for situations such as guiding a mobile unit to a station. The bearing will reflect the direction the unit must go to arrive at the station.

AIR

Indicates that the antenna has been mounted on the bottom of an aircraft so that the 90 degree and 270 degree (E-W) segments of bearing are reversed. The system, therefore, has electrically displaced the E-W signal 180 degrees to attain proper bearing information.

(5) AGC SLOW

Indication is present when slow AGC is being utilized by the system. Slow AGC is used for tracking quick pulsing transmitters.

(6) MODE INDICATOR

Indicates the selected demodulation mode of the receiver (AM, FM, CW, USB, or LSB). The arrow will point to the current mode of operation.

(7) 3-DIGIT BANDWIDTH DISPLAY

Numerical display of system IF bandwidth. Manual selection of four IF bandwidths is available, or automatic bandwidth selection is available. In either case, current IF bandwidth is displayed.

(8) PLL INDICATOR

Indicates whether PLL is OFF, or in the WIDE or NARROW mode of operation.

(9) PLL RESET INDICATOR

This indicator is present when PLL is in a RESET. condition, absent when PLL is in operating condition. (Reset drops error voltage to zero and sets oscillator output to 455 kHz, and turns off the antenna modulation tones).

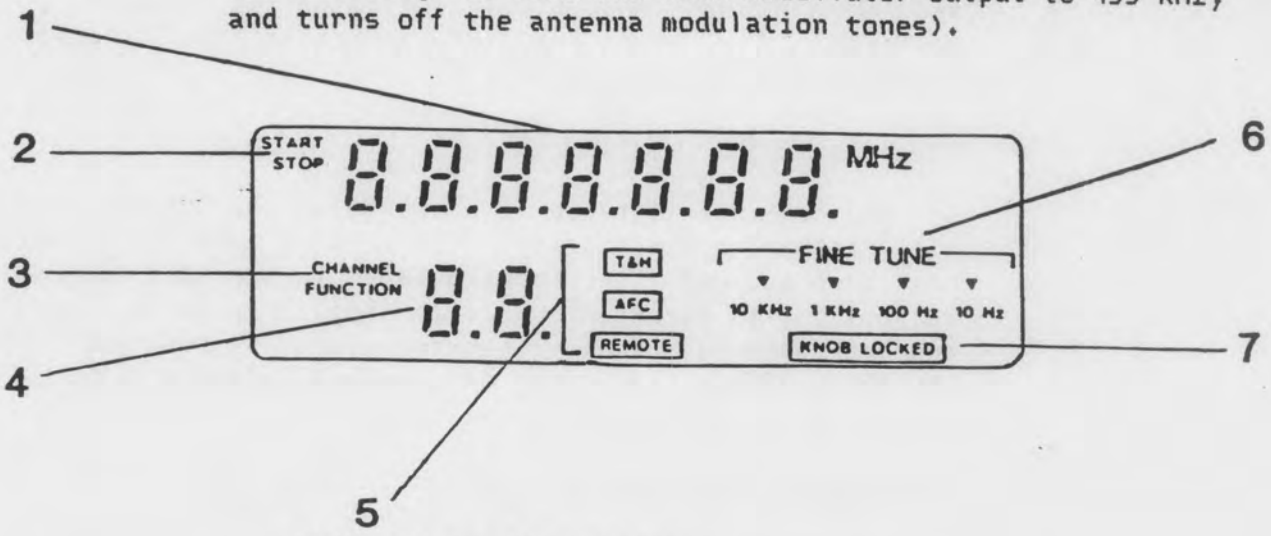


FIGURE 3-4 LCD2 Display

R. LCD2 DISPLAY (RIGHT SIDE LCD)

This presents channel and frequency indications, fine tuning information, and indication of active system functions. Various types of numeric entries will appear here while changes are being implemented. Main sections of the display are numerically designated in Figure 3-4, and listed below. Display lettering is black with a reflective background.

(1) 7-DIGIT DISPLAY

This display gives a seven digit fixed decimal point representation of any number as entered by the numeric keyboard. During entry a flashing prompt appears to alert the operator that the entry is not complete. All numerical entries initially appear here.

When the system is currently operating on a frequency, the operating frequency in MHz is displayed. Frequency information is erased when any numeric entry is begun, but reappears when current receiver status is restored. If frequency has been changed the display will update and the new frequency will appear.

(2) START/STOP INDICATOR

When setting up or reviewing the START/STOP scan frequencies, the flash word "START" will appear to indicate a start frequency, and the flashing word "STOP" will appear to indicate a stop frequency.

(3) CHANNEL/FUNCTION INDICATOR

The word "CHANNEL" indicates that the Channel Display is showing the channel number the system is tuned to. If the word "CHANNEL" is flashing the channels are being reviewed, and the channel number only indicates the channel being reviewed. The word "FUNCTION" indicates that a numbered function code is being displayed.

(4) 2-DIGIT CHANNEL/FUNCTION DISPLAY

If the receiver is tuned to a channel, the channel number will appear on the display. If a valid numbered function has been entered, the function will be executed (unless it is multi-step function). If an invalid numbered function has been entered, receiver current status is restored. (The CHANNEL/FUNCTION indicator references whether display is a channel or a function).

(5) OPERATIONAL INDICATOR

Any of three operational indicators will be present when active in system operation.

T&H

Indicates that the track-and-hold capability of the system is active. This allows the system to hold the bearing of a fading or intermittent signal for up to approximately 25 seconds when it has dropped below AGC threshold level.

AFC

Indicates that automatic frequency control is being utilized by the system.

REMOTE

Indicates that the system is being controlled by a remote unit.

(6) TUNING INDICATOR

The arrow indicates which frequency resolution the fine tuning control is set at.

(7) KNOB LOCKED INDICATOR

Appears when the tuning knob is electrically locked.

(8) ERROR

The word "ERROR" and a code number will appear in the 7-digit display. The error codes are as follows:

ERROR 0: A numerical entry is out of range.

Example: 90 MHz in a Model 2040, since range is 0.2 to 80 MHz.

ERROR 1: A general channel memory error has occured. Possible causes:

(a) Frequency stored in selected channel is out of the receiver's frequency range.

(b) Channel memory is not installed.

(c) A failure in the channel memory hardware.

ERROR 2: No channels exist between the selected START/STOP channel parameters.

ERROR 3: Channel Memory Full

(9) FAULT

A fault indication consists of a flashing 7-digit display. If a fault occurs, consult the maintenance procedures in Section IV (para. 4-5). The flashing will persist as long as the fault occurs.

A flashing decimal point in the 7-digit display warns the opertor of a power on BITE failure.

(10) 'no ant'

This indication indicates that either an antenna is not installed. Or a failure is indicating to the system that no antenna is installed.

(11) DATA WINDOW

Through the use of numbered functions, selected information is displayed in the 7-digit area of LCD2 for a period of two seconds. (See paragraph 3.2.7.2, Functions 40, 41, 49 and 71).

3.2 OPERATION UNDER NORMAL CONDITIONS

In general, operating an installed system consists of energizing the equipment, and selecting the desired frequency or channel. Bearing to a source of transmission at the frequency is automatically displayed

by a trace on the CRT scope, and registered in the bearing display area of LCD 1.

The available alternative methods of antenna zero orientations for the ADF system are as follows:

RELATIVE BEARING. The most common method of antenna orientation. When a 0 degree bearing is present on the CRT, the source of transmission is in line with the forward antenna element. This element is normally designated by a red arrow, or marked "FORWARD". Mobile installations using the system for homing on a received signal commonly orient the antenna so this direction represents forward motion of the vehicle or craft. Fixed stations using relative bearing can orient their antennas to True or Magnetic North, in the direction of a street, or landmark.

TRUE BEARING. When the forward antenna element is aligned with True North. This is done by aligning the antenna a fixed number of degrees out of line with a compass reading, to allow for the variation from True North, for the area of the site.

MAGNETIC BEARING. When the forward antenna element is physically aligned with Magnetic North.

RECIPROCAL BEARING. Electronic switching within the system allows reading of reciprocal bearing on the scope (Bearing from transmitting unit to receiving station). By use of this method a mobile unit can be guided to a station.

AIR. This method is used to reverse the E-W indications electronically when an antenna is mounted on the bottom of an aircraft and consequently E-W orientation (90 degree - 270 degree) has been mechanically reversed.

LOCAL OFFSET. In addition, antenna zero may be electronically offset by the operator to compensate for a constant error caused by local conditions. Once setup, the offset remains in effect until the operator cancels or changes it. In specific cases a bearing correction table may be pre-programmed into the system. Otherwise, the operator may desire to record the offsets for various frequencies on a card for reference (See paragraph 3.3.1.2).

In any case, the operator should be familiar with the method of orientation before operating the system.

3.2.1 Starting Procedures. A sequence of control settings for starting the equipment and bringing it up operationally is provided in Table 3-1. First, check the initial control settings. With the controls set in accordance with the table, the operator should be able to observe bearings on the CRT display. Other adjustments can be made as necessary, or as desired, in accordance with the following paragraphs of this section.

NOTE

The receiver contains battery back-up for some of the processor memory functions. When switching off the equipment or when losing power through malfunctions the receiver settings will be transferred to memory and retained there until power is restored. The receiver is then automaticallyset to the same front panel status for continued operation.

Power on BITE

When the equipment is initially turned on, the built-in test equipement (BITE) will perform a series of tests to determine whether the equipment is working properly. During this test all LCD segments are on. It is up to the opertor to verify that all segments are on. Test measurements may be output through the I/O data part, and numbered function 86 enables or disables this capability. Pass/fail codes are stored in a buffer and are available through Function 88. The test can be run with power on by enabling function 87. For further information consult Section IV of this manual.

3.2.2 ADF Operating Procedures. Once the system is operational, a received signal is displayed as a bearing on the CRT, and in the 3-digit bearing display section of LCD1. Bearing may be read directly from the display, or observed on the CRT. Bearing markings on the CRT bezel allow easy interpretation to the closest degree.

OPERATION AS COMMUNICATIONS RECEIVER. If the receiver is used as a monitoring receiver only (no DF), the antenna modulation tones must be switched off by selecting the PLL-RESET mode. This will increase monitoring sensitivity and provide better audio quality.

NOTE

For monitoring purposes, the DF antenna can be replaced by any 50 Ohm terminated antenna. This will allow use of directive antenna systems for extended range coverage.

The following paragraphs deal with ADF channel and frequency adjustments.

TABLE 3-1. STARTING PROCEDURES.

OPERATIONAL CONTROL	INITIAL SETTING	CONTROL SETTING OR ACTION REQUIRED
ON/OFF-VOLUME	OFF (FULLY CCW	SWITCH SYSTEM ON BY TURNING SLIGHTLY CLOCKWISE. POWER LED SHOULD LIGHT AFTER SLIGHT DELAY.
DIM	FULLY CCW	ADJUST CW FOR EASY VIEWING OF CONTROLS AND DISPLAYS
INTENSITY	FULLY CCW	TURN CLOCKWISE JUST ENOUGH TO OBSERVE DOT. IF NO DOT APPEARS CHECK VERT. AND HORIZ. ADJUSTMENT.
VERTICAL	MID RANGE	ADJUST TO CENTER DOT VERTICALLY.
HORIZONTAL	MID RANGE	ADJUST TO CENTER DOT HORIZONTALLY.
FOCUS	MID RANGE	ADJUST FOR SHARP DISPLAY (FOCUS AND INTENSITY MAY REQUIRE SOME ADJUSTMENT ONCE SIGNAL IS PRESENT).
DF	ZERO	SET TO AUTO, OR TO HIGHEST MANUAL POSITION (8). GAIN MAY BE READJUSTED WHEN SIGNAL IS PRESENT.
CHANNEL/FREQUENCY	LAST	SELECT DESIRED CHANNEL OR FREQUENCY (AS PER PARAGRAPH 3.2.1 OR 3.2.2.2).
VOLUME	ON	ADJUST SPEAKER VOLUME TO DESIRED AUDIO LEVEL BY TURNING CLOCKWISE.
MODE	LAST	SET TO MATCH TYPE OF SIGNAL BEING RECEIVED. (AM, FM, CW, LSB, USB).
ANTENNA	LAST	ADJUST ANTENNA PHASE, ZERO AND MODULATION (IF NECESSARY) TO ATTAIN PROPER BEARING DISPLAY. (SEE PAR. 3.2.3.1, 3.2.3.2, AND 3.2.3.3).

GENERAL: FURTHER ADJUSTMENTS MAY BE DESIRED TO CORRESPOND TO A PARTICULAR METHOD OF OPERATION. (i.e. PANORAMIC, PLL, SCAN, NUMBERED FUNCTIONS) FOR THESE CONTROL SETTINGS REFER TO THE SPECIFIC PARAGRAPH.

3.2.2.1 Setting the ADF to a Frequency.

.1 SET FREQUENCY: (NUMERIC ENTRY) [ENTER]

If the numeric entry is within the tuning range of the receiver, the receiver is set to the selected frequency. The seven digit display is updated with the fixed decimal point representation of the number just entered.

EXAMPLE: [2] [1] [8] [•] [7] [ENTER]

Will tune the receiver to 218.7 MHz.

If the receiver is turned off, the last frequency is retained in memory and the receiver will tune to that frequency an power up.

.2 INCREMENTAL TUNING: [△] [▽]

The increment decrement keys can be used to tune the frequency at the current frequency step size. The 7-digit area is updated with the current frquency as the receiver is tuned. Tuning beyond the receiver range is prevented, but no error message is displayed.

.3 SET INCREMENT/DECREMENT FREQUENCY STEP SIZE:

(NUMERIC ENTRY) [△] [▽]

The increment/decrement frequency step size is determined by the operator. A (NUMERIC ENTRY) followed by increment or decrement, will set the current frequency step size, and the [△] [▽] keys will change frequency tuning by the selected amount. Step size is variable in the 0-10 MHz range. When set to 0 the step size will reset to 1 MHz.

EXAMPLE: [•] [6] [4] [0] [△]

The increment/decrement keys will now alter the frequency .640 MHz at each step.

The current frequency step size may be observed by pressing the sequence [4] [0] [FUNC].

.4 FINE TUNING: [◁] [LOCK] [▷]

The tuning resolution keys will set the tuning resolution. Turning the knob will tune at the current rate. The LOCK key will electrically disconnect the knob once frequency is set. Tuning beyond the range of the receiver is prevented, but no error message is displayed.

3.2.2.2. Setting the ADF to a Channel.

SET TO A CHANNEL: (NUMERIC ENTRY) [CH]

If the channel selected is an active channel, the ADF is set to that channel. The channel number is displayed in the two-digit channel display area of LCD2 and the work "CHANNEL" is displayed. The CHANNEL DATA is also displayed. CHANNEL DATA consists of frequency, demodulation mode, and bandwidth. If the channel selected is not an active (stored) channel an improper entry error code is displayed, press [CLR] to remove the error, and reselect the channel. The system has a channel capability of 0-99, however, the number of channels actually used is arbitrary.

EXAMPLE: [3] [6] [CH]

Will tune the receiver to channel 36 and lock it. CHANNEL DATA will be displayed.

SET TO LAST CHANNEL SELECTED [CH] [CH]

Recalls the last channel selected and sets the receiver to that channel, even if power was previously shut off. The last selection is retained in memory and channel recall can be repeated indefinitely.

CLEAR CHANNEL MODE: [CLR] [CH]

Pressing this sequence will clear channel mode, and return the receiver to its current status.

3.2.2.3. Reviewing Stored Channels.

REVIEW ANY CHANNEL: [CH]

If the channel select key is pressed with no (NUMERIC ENTRY) the receiver will display for review the last channel that was selected. The cannel number is displayed and the word channel will flash. The increment/decrement [△] [▽] keys can be used to cycle through the active channels. If it is desirable to tune to a reviewed channel push [CH] a second time.

3.2.2.4. Storing Current Receiver Status as a Channel.

.1 STORE CURRENT STATUS AS A SELECTED CHANNEL:

(NUMERIC ENTRY) [ ] [STORE]

If the numeric entry designates a valid channel number, the current receiver status is stored under the channel. If the channel designated is an active (previously stored) channel, the previous channel data is erased and replaced by the new entry. An update

occurs, and the new channel data is displayed. If the channel number is invalid, no entry is made and an error code is displayed.

.2 STORE CURRENT STATUS AUTOMATICALLY AS A CHANNEL: [ ] [STORE]

If in frequency mode (not set to a channel), the current status will be stored under the first available number in the channel memory, and an update is performed. If in channel mode, the current channel is updated with any changes made in frequency, bandwidth, or mode. If a numeric entry is pressed (as in the previous sequence) and a channel stored under a specific number, each time the sequence [ ] [STORE] is pressed the next available channel above that number will be programmed.

3.2.2.5. Tuning Through Active Channels.

INCREMENT/DECREMENT: [△] [▽]

If the receiver is currently tuned to a channel, the increment/decrement keys can be used to tune to the next higher or lower active channel, or to tune through active channels.

3.2.3. Operating Mode Adjustments.

3.2.3.1. Selecting Demodulation Mode.

SET MODE: [AM] [FM] [CW] [USB] [LSB]

Pressing any one of these keys when the system is up and operating sets the demodulation mode. The entered mode is set. An update occurs and the current receiver status is displayed. If the auto select bandwidth function is active, the demodulation mode is compared with the current frequency and the proper IF bandwidth is selected. In upper sideband mode the audio filter is disconnected.

3.2.3.2. Manually Selecting Bandwidth.

CHANGE BANDWIDTH SELECTION: [BW]

Pushing bandwidth will set the IF bandwidth to the next choice in a selection of four possible bandwidths in ascending order. The bandwidth key can be used to rotate thru the bandwidth selections.

3.2.3.2. Manually Selecting Bar Graph Display Data.

SELECT BAR GRAPH DISPLAY: [MTR]

Pressing the meter key will set the bar graph display to the next in a series of displayed data. An arrow will indicate which of the data displays (SIGNAL STRENGTH, PLL TUNING, ANTENNA PHASE OR ANTENNA MODULATIONS) is being displayed on the bar graph. The bar graph is similar to a meter, with mid range being the center. When the bar graph is in the PLL tune position and the PLL is off, the AFC voltage is displayed.

3.2.3.3. Selecting the PLL Operating Mode.

Phase-locked loop operation allows the system to lock on a weak signal that would otherwise be lost in the noise background. A signal may be lost due to decreased signal strength, increased noise, or change in frequency. The PLL adjusts receiver frequency to compensate for frequency drift of the received signal in the selected bandwidth.

The narrower the noise bandwidth the better a signal may be tracked. Because of acquisition difficulty, an operator will normally adjust the fine tune for best lock indication with track and hold off. As lock is neared the trace length will be increased and steadier, and the lock indicator will illuminate for longer periods. When lock is neared, adjust the fine tuning for best indication in the wide position, then switch to narrow and re-adjust for best indication.

.1 TURN PLL ON/OR SELECT WIDE/NARROW: [ ] [W/N]

If the PLL is OFF, pressing the wide/narrow key will turn it ON in the wide bandwidth position. If the PLL is ON and in the wide bandwidth position, pressing the wide/narrow key will set the PLL to the narrow position.

.2 RESET THE PLL: [ ] [O/R]

When the key is depressed with the PLL ON, a "RESET" condition is initiated. The error voltage will drop to 0V, the PLL oscillator will reset to 455 kHz. The "PLL RESET" display will appear in the lower right corner of LCD1, and the tones will be turned off.

Initiate the same sequence to return the PLL to "OPERATE" condition. The PLL will now lock on the received signal and the "PLL RESET" display will shut off.

.3 TURN PLL OFF: [ ] [OFF]

Unconditionally turns the PLL off.

3.2.4. Antenna Adjustments.

Antenna adjustments are set very close to optimum at the factory and further adjustments may not be necessary. Such adjustments may become necessary when operating under less than ideal conditions, or may be desirable to optimize for a particular site, vehicle, or locale.

These adjustments are normally made once, and then left alone. Phase zero and modulation adjustments remain as a power-on constant even if the system is shut off.

The phase is adjusted for specified ferrite antennas only. It consists of adjusting the phase of the vertical (Y) and horizontal (X) signals in relationship to the omnidirectional (Z) signal. The phase is adjusted for maximum trace length with no variation.

Modulation is normally adjusted to about 50%. Since the signal modulation and the antenna modulation are added, overmodulation can result in a garbled audio signal. Some adjustments may be necessary to correct for this condition.

Antenna zero heading is normally adjusted physically by the antenna orientation when it is installed. If antenna orientation is known to be correct, but a constant bearing error exists, some local condition may be responsible for the error. Or, space requirements (as on board ship) may require that the antenna zero heading may need to be electronically adjusted to compensate for the inbred inaccuracy. This is done by adjusting the offsets in the bearing processor.

3.2.4.1. Setting Antenna Phase. (For AFL-285 and other specified ferrite antennas only).

SET ANTENNA PHASE: [ ] [PHASE]

The current power-on calibration constant phase level is set and displayed. The increment/decrement [△] [▽] keys can now be used to adjust the phase. The phase is adjusted for maximum trace length on the CRT without variations in the length. [CLR] will return the receiver to its current status.

3.2.4.2. Setting Antenna Modulation.

SET ANTENNA MODULATION: [ ] [MOD USB]

The current power-on calibration constant modulation level is set and displayed. The increment/decrement [△] [▽] keys can be used to adjust modulation. The modulation may need occasional adjustment since overmodulation can result in a garbled audio signal. There will also be some interaction between the phase and modulation as both affect the length of the trace. [CLR] will return the receiver to its current status.

3.2.4.3. Setting Antenna Zero Heading.

SET ANTENNA ZERO: [ ] [ZERO LSB]

The current zero heading offset is set and displayed.

NOTE:

The result of bearing + zero heading offset + other offsets is displayed during this procedure in the bearing display area of LCD1

INCREMENT/DECREMENT

The increment/decrement [△] [▽] keys can be used to adjust the zero heading, zero heading is adjusted to compensate for a local variation or physical displacement. [CLR] will return the receiver to its current status.

NOTE

In cases where bearing jitter is present due to reflected inputs, the jitter can sometimes be adjusted out by increasing the bearing integration rate. (consult paragraph 3.2.7.2 numbered function 10.)

3.2.5. Scan Method of Operation.

Scan method of operation allows the operator to initiate an automatic search mode, where a selected band of frequencies, or a selected group of channels are swept. When a signal that exceeds a set threshold is received, the system will pause for a predetermined time so the operator can observe the signal. If the operator desires, scan may be terminated to allow continuous observation of that input, or Scan will automatically reinitiate if no operator action is taken.

For scan operation a START and STOP frequency/or channel is programmed into the system by the operator, and the system will sweep this set of frequencies or channels once scan is initiated. Scan method of operation is initiated and controlled in accordance with the following.

3.2.5.1. Initial Set Up of Scan Frequencies or Channels.

Normally, scan sequence will be preset at the factory to sweep the entire operational range of frequencies or channels. To set the scan to a selected range of frequencies or channels, use the procedures in the following paragraphs.

Note that the scan will sweep up if the start frequency or channel selected is lower than the stop frequency or channel. If the start frequency or channel is higher than the stop frequency or channel, the scan will sweep down. If the preset start and stop frequencies or channels are the same, the scan will continually check the same frequency or channel.

.1 SETTING UP SCAN FREQUENCIES

(a) Depress [SET] which will call up the initial START frequency if a frequency scan capability was last initiated. If the word "CHANNEL" and a channel number appears prior to the 2-digit display of LCD2 the channel scan capability has been initiated, and the operator should proceed to step (b), otherwise proceed to step (c).

(b) To call up the frequency scan capability depress [ ] [f/CH] this will switch the system from channel scan to frequency scan.

(c) A frequency will appear in the 7-digit display area of LCD2. The word "START" will appear prior to the 7-digit display. The word "CHANNEL" should not appear.

(d) A (NUMERICAL ENTRY) of the desired frequency can now be put in, and will be shown on the 7-digit display.

(e) [ENTER] can now be depressed to enter the START frequency. The display will be updated and the entry retained in

memory. If an error is made pressing [CLR] will return to the last step.

(f) [SET] key can now be used to switch to the STOP frequency. The desired STOP frequency can be entered using steps (d) and (e) above.

(g) Scan step size is set automatically at half the IF bandwidth. If it is desirable to manually adjust the scan step size, consult paragraph 3.2.7.2 in regard to function 70.

.2 SETTING UP SCAN CHANNELS:

Follow the step by step procedure below to set up the scan START/STOP channels:

(a) Depress the [SET] which will call up the initial START channel provided channel scan capability was last initiated. If the word "CHANNEL" appears along with a channel number it indicates channel scan has been initiated and the operator should proceed to step (c), otherwise the frequency scan capability has been initiated and the operator should proceed to step (b).

(b) To call up the channel scan capability press [ ] [f/CH] this will switch the system from frequency scan to channel scan.

(c) The frequency of the START CHANNEL should appear in the 7-digit display area of LCD2 and the word "START" will appear prior to the 7-digit display. The channel number should appear in the 2-digit display preceded by the word "CHANNEL".

(d) A (NUMERICAL ENTRY) representing the desired "START" channel (0-99) can now be put in and will be shown on the 7-digit display. Alternatively, the increment/decrement keys may be used to cycle through channels while setting the channel scan START/STOP parameters.

(e) [ENTER] is pressed and if the entered channel number is valid the channel number will be entered as the "START" channel. An update will occur and the new "START" channel frequency will be displayed. If the channel chosen is locked out or not programmed, the receiver will search for and select the nearest programmed and unlocked channel. (It will do this for both the START and STOP parameters. If an error code is displayed consult paragraph 3.1.1 R(8)) Press [CLR] to return to the last step.

(f) Once start channel is entered press [SET] to switch to the STOP channel. The stop channel can be reset using the procedures in steps (d) and (e) above.

(g) Once channel scan is setup [ ] [LK OUT] can be used to remove any channel from the scan sequence by tuning to that channel and depressing [ ] [LK OUT]. To remove lockout

tune to that channel and press [ ] [LK OUT] again.

3.2.5.2 Review or Change Preset Scan Frequencies or Channels.

Basic command sequences to review and/or change scan stop/start frequencies or channels are as follows.

.1 DISPLAY STOP/START FREQUENCY OR CHANNEL:

[SET] The first time the SET key is pushed it will initiate the SCAN display sequence and the START frequency or channel will be displayed. Whether a frequency or channel will be displayed depends on whether a frquency or a channel scan sequence was last initiated.

If a frequency scan sequence was last initiated the START frequency will be displayed. When the [SET] Key is pushed again the STOP frequency will be displayed. Pressing [SET] again will return the receiver to its current status.

.2 CHANGE FREQUENCY TO CHANNEL: [ ] [f/CH]

or CHANGE CHANNEL TO FREQUENCY: [ ] [f/CH]

This command sequence can be used to the above case to switch from frequency to channel display, after which channel display can be cycled using the same method as above. This command sequence will switch from channel to frequency/or from frequency to channel unconditionally once scan capability has been actuated. This sequence may also be used to switch from a different operational mode to the scan setup state. The current

frequency channel mode status may be noted by the type of display presented.

.3 ENTER NEW START/STOP FREQUENCY OR CHANNEL:

(NUMERICAL ENTRY) [ENTER]

This command sequence may be used during a scan display sequence to change a frequency or channel START/STOP entry. [The sequence (NUMERICAL ENTRY) [CH] may also be used in channel scan mode.]

3.2.5.3 Scan Operation

To scan frequencies or channels the following operational procedures are used. Simply depressing the [CONT] key will initiate scan operation, but only if the other operational controls are properly set up. Therefore, review the entire paragraph before initiating scan operation.

.1 SQUELCH

The squelch control sets the threshold for scan operation. To ensure proper opeation, tune the receiver to noise, and set the squelch control to the point where the noise just disappears. Then, tune to a known weak signal within the scan range and adjust to just pick up the signal. Interaction may require several adjustments until the desired level is attained. If noise level is not excessive, the operator may choose to adjust the squelch control to minimum (fully counter-clockwise).

.2 START/CONTINUE SCAN: [CONT]

Press the continue key to initiate the scan sequence. Pressing [CONT] again (or turning the tuning knob) will stop the scan. Scan can be toggled on or off at any time by pressing [CONT]. Pressing [CLR] will interrupt the scan sequence and return the receiver to the start of the scan sequence.

Pressing the sequence [SET] [CONT] will start the scan at its preset START frequency or channel. Pressing [CONT] only will start at the current operating frequency or channel, providing it is within the scan limits.

During frequency scanning the last digit of the frequency will not appear till the STOP parameter or a dwell point is reached. To obtain a current frequency readout press the [ENTER] key. Pressing the [ENTER] key will not stop the scan. During dwell, pressing the [CONT] button will continue the SCAN sequence.

.3 CHANGE FREQUENCY TO CHANNEL: [ ] [f/CH]

or CHANGE CHANNEL TO FREQUENCY: [ ] [F/CH]

This command sequence can be used in the above case to switch from frequency to channel scan, or from channel to frequency scan. This command sequence will switch from channel to frequency/or from frequency to channel unconditionally once scan capability has been actuated. (In the frequency scan setup mode

[CH] Key can also be used to switch to the channel mode.)

.4 DWELL: 

The dwell control is a variable potentiometer which sets a dwell (pause) time during the scan sequence. When the system is scanning and attains an input signal that exceeds a set threshold on any frequency (or channel) it will dwell at that frequency for an interval determined by the dwell control. During the dwell time the current status will be displayed with a bearing on the received signal. If no action is taken scan will reinitiate automatically and continue at the end of the dwell interval. To store the observed frequency on any available channel during dwell, depress [ ] [STORE]

The dwell interval is set by the dwell control. Fully counter-clockwise is zero dwell and scan will not pause. As the control is turned clockwise the dwell time will increase. Fully clockwise is infinite, and the system will stop and dwell indefinitely at an input frequency until a command sequence is initiated or [CONT] is pushed.

.5 SET SCAN FREQUENCY STEP SIZE [7] [0] [FUNC]

Normally, scan intervals are set at half the IF bandwidth. The above sequence allows the scan interval to be set by the operator. Steps may be set at any intervals in the range of 0-10 MHz, and [0] will default to half the IF bandwidth. The assumed purpose of this mode is to locate transmitters based at known intervals.

The sequence [7] [0] [FUNC] will activate the mode. [△] [▽] may then be used to set the scan interval as desired. Setting this mode to [0] will deactivate the mode.

.6 DISPLAY SCAN STEP SIZE [7] [1] [FUNC]

This sequence will display the current scan step size.

.7 CHANNEL OCCUPANCY MODE ON [7] [2] [FUNC]

When initiated, the above function causes scanning without dwell. When a signal is detected it is recorded with a message output to a teleprinter via the I/O data part. A bearing conversion is not made in this mode. The sequence [7] [2] [FUNC] initiates scan without dwell. The sequence [7] [3] [FUNC] turns the scan without dwell function off.

.8 SCAN WITHOUT AFC: [7] [4] FUNC

It may be desirable to scan without using the AFC, as there is some interaction between scan and AFC. The sequence [7] [4] [FUNC] allows scanning without AFC. The sequence [7] [5] [FUNC] returns to scan with AFC. (Refer to paragraph 3.2.7.2 for details).

.9 SCAN DEFAULT RESET [7] [6] [FUNC]

When this function is initiated scan is reset to its initial parameters as follows:

START FREQUENCY = MINIMUM

STOP FREQUENCY = MAXIMUM

START CHANNEL = 0

STOP CHANNEL = 99

STEP SIZE = 1/2 IF BANDWIDTH

NORMAL FREQUENCY SCAN WITH AFC ENABLED

3.2.6 Panoramic Method of Operation.

In the panoramic method of operation a horizontal sweep is actuated along the baseline near the bottom of the CRT. The band of frequencies swept is determined by the frequency the ADF receiver is set at, and the setting of the PAN WIDTH control. The frequency the ADF receiver is set to will correspond to the center of the band swept.

Frequencies will appear as vertical deflections forming a pattern similar to the one shown in Figure 3-5.

The amount of vertical displacement is proportional to the relative signal strength of the received signal. No bearing information is presented, but by use of this method a band of freuencies can be observed and compared.

A particular frequency can be isolated, and tuned to, and once desired observations are made, the receiver can be returned to DF operation. To utilize panoramic method of operation refer to TABLE 3-2.

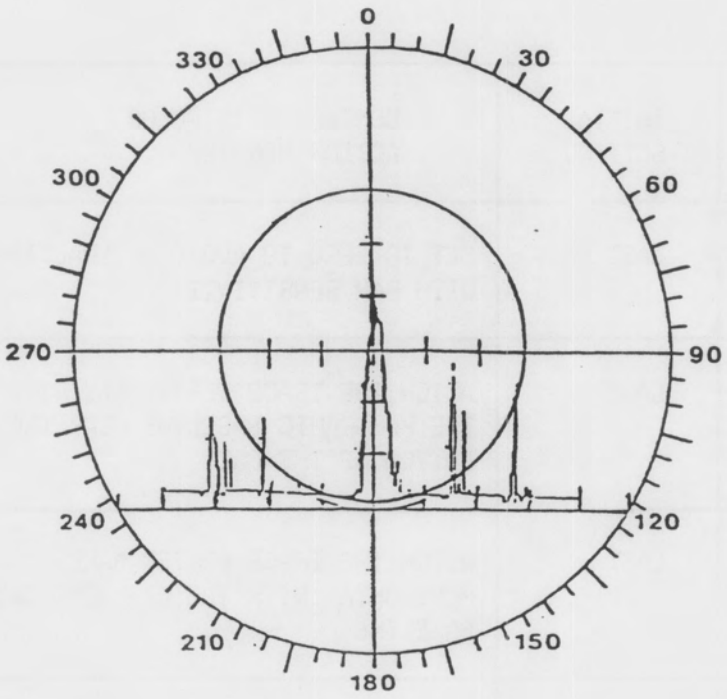


FIGURE 3-5 Panoramic Frequency Display

TABLE 3-2. Operational Procedures for Panoramic Display

OPERATIONAL CONTROL	INITIAL SETTING	CONTROL SETTING OR ACTION REQUIRED
DF GAIN	LAST	SET TO ZERO TO AVOID INTERACTION WITH PAN SENSITIVITY
VERTICAL	LAST	ALIGN THE TRACE VERTICALLY WITH THE PANORAMIC BASELINE NEAR THE BOTTOM OF THE CRT
HORIZONTAL	LAST	ALIGN THE TRACE CENTER MARKER HORIZONTAL WITH THE CRT VERTICAL BASELINE
PAN MODE	OFF	TURN TO LOG
PAN WIDTH	LAST	SET TO DESIRED BANDWIDTH
PAN SENSITIVITY	LAST	ADJUST TO MAXIMUM SENSITIVITY AND OBSERVE INCOMING SIGNALS. ADJUST TO KEEP LARGEST SIGNAL WITHIN LIMITS OF SCOPE

NOTE

Once the signal of interest is found, the tuning knob may be used to bring the signal to the center of the screen. When the signal is centered the ADF receiver is tuned to the frequency of interest. The PAN width control may be used to increase resolution between frequencies.

3.2.7 Numbered Functions.

Numbered functions consist of those functions not covered through use of

the other front panel controls. Numbered functions are made available to increase the capabilities of the system without the use of additional front panel controls. Use of numbered functions and a listing of numbered functions within the scope of this manual is contained in the following paragraphs.

3.2.7.1 Use of Numbered Functions.

.1 INITIATE CURRENT FUNCTIONS: [FUNC] [FUNC]

The first time the key is depressed, if there is a valid function (previously initiated) in memory, the receiver displays the function number in the two digit display area of LCD2 prefixed by the flashing word "FUNCTION". The second time the key is depressed the function is initiated.

.2 INITIATE NUMBERED FUNCTIONS: (NUMERIC ENTRY) [FUNC]

If the number entered is an active function, that function is initiated, and the function number is displayed in the 2-digit display area of LCD2 prefixed by the word "FUNCTION". If the number is invalid an error code will be displayed. Pressing [CLR] will return the receiver to its current status. [CLR] may be used to remove an error, or to return to current status from a numbered function. If the numbered function is a multi-step function the word "FUNCTION" will flash until the command sequence is completed. The command sequence for a multi-step numbered function is as listed under that number in paragraph 3.2.7.2.

3.2.7.2. List of numbered functions.

NUMBERED FUNCTIONS:

00 TURN ON ALL LCD SEGMENTS (Tests LCD)

01 AFC ON/OFF

02 AGC NORM/SLOW

03 AUTO SELECT BANDWIDTH ON

04 AUTO SELECT BANDWIDTH OFF

05 AUDIO FILTER ON

06 AUDIO FILTER OFF

07 CRT ON

08 CRT OFF

09 TRACK & HOLD ON/OFF

10 SET BEARING AVERAGING TIME

(Determines number of samples taken for each scan)

MULTI-STEP PROCEDURE:

(1) [1] [0] [FUNC]

The current bearing integration rate is displayed.

(2) [△] [▽]

Increment/decrement keys can be used to cycle through the available bearing integration rates, (0.25, 0.5, 1,2,4 Seconds) until the desired rate is established. Integration may be increased to counteract jitter due to reflected inputs.

12 DISPLAY AUTO/AIR BEARING

13 DISPLAY NORM/RECIPROCAL BEARING

14 DISPLAY BEARING CORRECTION ON
(Adds correction table factor into displayed bearing).

15 DISPLAY BEARING CORRECTION OFF
(Removes correction table factor from displayed bearing).

20 ERASE A CHANNEL
(Only active when the receiver is tuned to a channel).

21 ERASE ALL CHANNELS

MULTI-STEP PROCEDURE:

(1) [2] [1] [FUNC]

Enables the erase function.

[9] [9] [9] [9] [9] [9] [9] [ENTER]

Will erase all channel memory. The front panel keys will lock for approximately 15 seconds while EEPROM memory is erased. (The long sequence prevents accidental erasure).

30 SEND STATUS MESSAGE

(Activating this function sends a fixed format message of receiver status in ASCII, and allows for printout of the message. The message format, and an example, are found in the pages following this table).

40 DISPLAY FREQUENCY INCREMENT/DECREMENT STEP SIZE

41 DISPLAY SIGNAL STRENGTH VALUE

49 DISPLAY SOFTWARE VERSION NUMBER. THE NUMBER IS A MAINTENANCE REFERENCE USED BY THE MANUFACTURER.

70 SET SCAN STEP SIZE

MULTI-STEP PROCEDURE:

(1) [7] [0] [FUNC]

Scan steps are normally set at half the IF bandwidth automatically. This function allows

manually setting the scan step size.

(2) (NUMERIC ENTRY) [ENTER]

Enters the desired step rate. Rates of 0.001 MHz to 0.1 MHz are available. Entering 0 returns the step to one-half the IF bandwidth.

71 DISPLAY SCAN STEP SIZE

72 SCAN WITHOUT DWELL ON

73 SCAN WITHOUT DWELL OFF

74 SCAN WITHOUT AFC

75 SCAN WITH AFC

76 SCAN DEFAULT RESET

Sets scan up in accordance with the following parameters:

Start frequency = minimum

Stop frequency = maximum

Start channel = 0

Stop channel = 99

Step size = 1/2 IF bandwidth

Normal frequency scan with AFC enabled

78 SET IEEE-488 ADDRESS

MULTI-STEP PROCEDURE:

(1) [7] [8] [FUNC]

The current address is displayed.

(2) [△] [▽]

Increment/decrement keys can be used to cycle

through the addresses (00-30), until the desired IEEE-488 address is established. The address will be displayed (as activated) on the 7 digit display area of LCD2.

79 SET REMOTE DATA PORT BAUD RATE

MULTI-STEP PROCEDURE:

(1) [7] [9] [FUNC]

The current baud rate is displayed.

(2) [△] [▽]

Increment/decrement keys can be used to cycle through the available baud rates until the desired rate is established. The baud rates will be displayed (as activated) on the 7 digit display area of LCD2.

80 SET BAUD RATE OF I/O DATAPORT

MULTI-STEP PROCEDURE:

(1) [8] [0] [FUNC]

The current baud rate is displayed.

(2) [△] [▽]

The increment/decrement keys can be used to cycle through the available baud rates until the desired rate is established. The baud rates will be

displayed (as activated) on the 7-digit display area of LCD2.

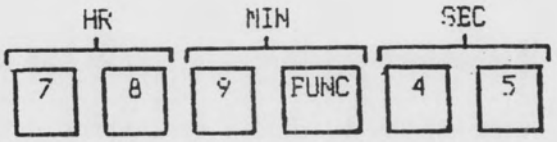
81 SET/DISPLAY REAL TIME CLOCK

MULTI-STEP PROCEDURE:

(1) [8] [1] [FUNC]

Will initiate the real time clock display. The time may now be observed. The hours and minutes of the 24 hour clock appear on the 7-digit display of the LCD2. The seconds appear in the two-digit display.

(2)



The top four buttons of the numerical keyboard and the next two buttons below, may now be used to set the corresponding digits of the clock. Pressing any of these buttons freezes the display, and the clock can now be set.

EXAMPLE: [7] [PHASE] [STORE]

Once [7] is pressed the INCREMENT/DECREMENT keys can be used to change the first digit on the display.

(3)

By pressing any of the top six keys as desired, and using the INCREMENT/DECREMENT keys, each digit

may be set individually.

(4) [ENTER]

Once the display has been changed to reflect the real time, pressing [ENTER] will set the clock to the desired time.

(5) [.]

Pressing the decimal key will restore the clock display. Pressing [CLR] will return the receiver to its current status.

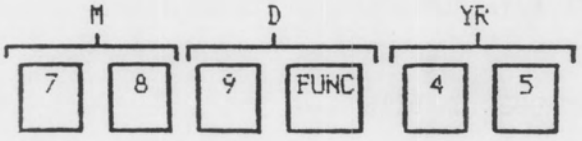
82 SET/DISPLAY DATE

MULTI-STEP PROCEDURE:

(1) [8] [2] [FUNC]

Will initiate the real time clock date display. The month, date, and year will appear as four digits on the 7-digit display of LCD2 and the year as two digits on the two digit display of LCD2.

(2)



The top four digits of the numerical keyboard and the next two digits below may now be used to set the date in the same manner the real time clock (function 81) was set.

EXAMPLE:

Once [7] is pressed the INCREMENT/DECREMENT keys can be used to change the first digit of the display.

(3) By pressing any of the top six keys as desired, and using the INCREMENT/DECREMENT keys, each digit may be set individually.

(4) [ENTER]

Once the display has been changed to reflect the actual date, pressing [ENTER] will set the real time clock to the desired date.

(5) [.]

Pressing the decimal key will restore the date display to its normal function. Pressing [CLR] will return the receiver to its current status.

83 ENABLE EXTERNAL SENSE ELEMENT

84 DISABLE EXTERNAL SENSE ELEMENT

86 POWER ON BITE MEASUREMENTS PRINTOUT ON/OFF

87 EXECUTE POWER ON BITE

88 DISPLAY POWER ON BITE FAULT CODES

MULTI-STEP PROCEDURE:

(1) [8] [8] [FUNC]

Will display one of the fault codes which are stored for each power-on BITE test that failed. The list will be displayed one item at a time in the 7-digit area of LCD2. A blank display indicates there were no fault codes. See table 4-1 and 4-2 for the listing of fault codes.

(2) Four keys can now be used to cycle between fault codes.

(a) [◁] Displays the fault code at the start of the list.

(b) [▷] Displays the fault code at the end of the list.

(c) [△] Displays the next fault code on the list. (Wraps from the end to the beginning)

(d) [▽] Displays the previous fault code on the list. (Wraps from the beginning to the end)

[CLR] Clears out of this function.

92 ENABLE MGC

93 DISABLE MGC

94 ANTENNA BITE GENERATOR ON

95 ANTENNA BITE GENERATOR OFF

96 RECEIVER BITE GENERATOR ON

97 RECEIVER BITE GENERATOR OFF

NOTE

The selected information in steps 40, 41, 49 and 71 is displayed for two seconds in the 7-digit area of LCD2. This is referred to as the data window.

STATUS MESSAGE OUTPUT DESCRIPTION

(FUNCTION 30)

The following ASCII encoded status message is sent through the DCE RS-232 port marked I/O DATA:

(1.) Automatically, each time a signal is detected while scanning

(2.) Manually, each time numbered FUNCTION 30 is executed

```
08/12/84 07:59:02 002.89700 045 03 AM 2.5K(cr/lf)
-------- -------- --------- --- -- -- ----
  ¦        ¦        ¦       ¦   ¦  ¦   ¦
  ¦        ¦        ¦       ¦   ¦  ¦   `- Bandwidth
  ¦        ¦        ¦       ¦   ¦  `- Demodulation Mode
  ¦        ¦        ¦       ¦   `- Signal Strength (0..99)
  ¦        ¦        ¦       `- Bearing (0..99)
  ¦        ¦        `- Frequency (MHz)
  ¦        `- Time (HHMMSS)
  `- Date (MMDDYY)
```

NOTE

(1) (cr/lf) = carriage return/line feed

(2) Bearing field is sent blank if signal strength is below bearing measurement threshold.

(3) Channel field is sent blank if the audio is not set to a channel.

(4) The record length is fixed. Leading zeros are not suppressed. A space is used as a delimiter between fields.

SAMPLE PRINTOUT

```
10/15/84 09:36:14 100.70792M 079 43 FM 200K
10/15/84 09:36:19 103.70028M 030 45 FM 200K
10/15/84 09:36:23 105.30194M 251 32 FM 200K
10/15/84 09:36:27 107.90094M 204 21 FM 200K
10/15/84 09:36:32 096.49370M 066 34 FM 200K
10/15/84 09:36:35 098.10597M 077 31 FM 200K
10/15/84 09:36:41 100.70262M 080 43 FM 200K
10/15/84 09:36:46 103.70558M 030 46 FM 200K
10/15/84 09:36:50 105.29310M 199 32 FM 200K
10/15/84 09:36:54 107.79310M     00 FM 200K
```

3.2.8 Remote Control Programming

3.2.8.1 General

The OAR 2040 or OAR 3045 receivers are remotely controlled using a parallel IEEE-488 interface or a serial RS-232C interface (as described in Section II of this manual).

The details of remote command and response messages are presented here. An outline and description of message syntax and types, with examples, and a complete collection of tables listing all command and response messages follows.

Since familiarity with remote programming devices via IEEE-488 and/or RS-232 interfaces is assumed in this manual, a tutorial on these topics is not included. However, implementation notes are given near the end of the functional description. It is strongly recommended that you read these notes, since they discuss important technical details of the remote control software.

3.2.8.2 Functional Description

3.2.8.2.1 Overview

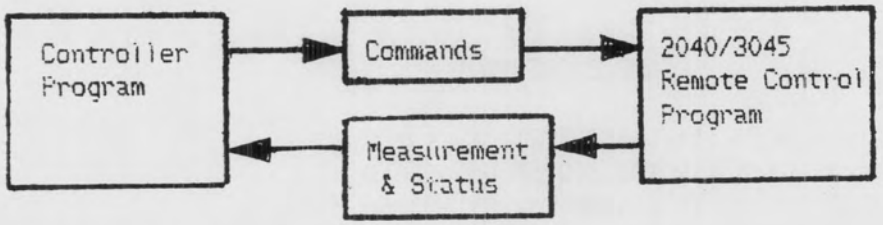


Figure 3-6. Overview Diagram

Remote programming involves two basic activities:

(1) Sending command messages to alter device or remote interface status, and requesting messages containing device status and measurement data.

(2) Receiving messages in response to requests for measurement data and/or device status.

3.2.8.2.2 Command Messages

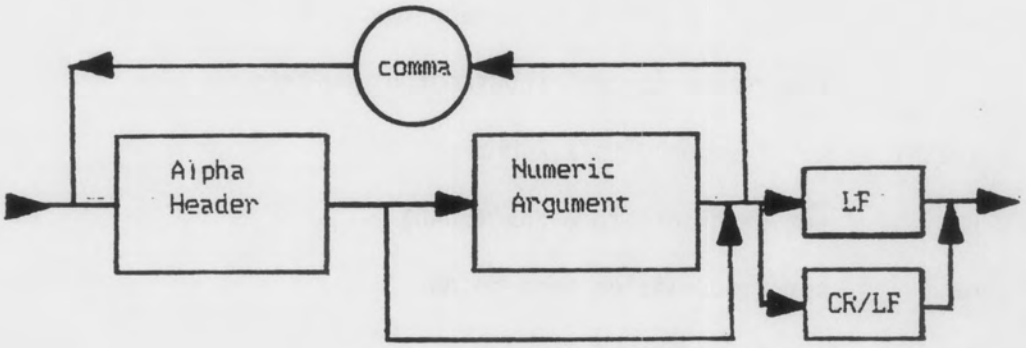


Figure 3-7. Command Syntax Diagram

NOTE

(1) Numeric arguments must be in fixed point notation. Leading zeros are permitted.

(2) (lf) = The ASCII line feed character

(3) (cr/lf) = the ASCII carriage return/line feed character combination

All command messages are comprised of ASCII character strings, and are sent singly or in groups separated by a comma. A COMMA MUST BE USED TO SEPARATE COMMANDS.

The command input buffer will accept a string up to 200 characters long. Lower case characters are translated to upper case before commands are interpreted. A (lf) MUST terminate every command string. Furthermore, command processing will not proceed until the (lf) terminator is detected (or the input buffer overflows). (A (cr/lf) combination is also a legal terminator.)

Example of several commands sent at one time:

DCLR,1.2ENT,BWB,AM,SQ0(lf)

Sending this string of commands will:

DCLR	cancel any active functions (such as scan), reset the remote control input/output buffers
1.2ENT	set Frequency to 1.2 MHz
BWB	set Bandwidth to 6 Khz (2040)
AM	set Demodulation Mode to AM
SQ0	set Squelch to 0 (minimum)

A. Key Commands

A Key command is a string of ASCII characters that is equivalent to depressing one of the front panel keys. To use these commands the programmer determines which key sequences will generate the desired function. The equivalent key commands are sent in the same order, and the front panel responds just as if the keys were depressed locally.

Table 3-3 contains a list of all Key Commands.

Examples:

12.34567ENT(lf)

Sets the radio to 12.34567MHz, the same as pushing

the equivalent front panel keys.

70FUNC,0.001ENT(lf)

Sets the scanning step size to 1KHz.

B. State Commands

It is possible to invoke all front panel key initiated functions by using key commands, but some keys are pushed repeatedly to select one state from a set of options.

For example, the BW key cycles through the four possible I.F. bandwidth options. Also, some numbered functions toggle between two possible states. The local display provides feedback in these cases so the operator knows which state is selected.

State Commands are provided to select a state absolutely.

Table 3-4 contains a list of all State Commands.

Examples:

PLLWID(lf)

Sets the PLL to On and Wide

AFCON(lf)

Turns on the AFC

AFCOFF(lf)

Turns off the AFC

C. Value Commands

The other front panel controls: potentiometers, rotary switches, and the optically encoded tuning knob; are emulated with commands that, in every case except one, require a numeric argument.

Table 3-5 contains a list of all Value Commands.

Examples:

PSENS127(if)

Sets the Pan Sensitivity to half scale

FT-45(if)

Decrements the current operating frequency by 45 increments, (Increment magnitude = current tuning resolution...the same as tuning from the front panel).

D. Interface Commands

Several of the IEEE-488 interface bus commands are repeated as device dependent commands so these conditions can be set when remote control is via the RS-232 remote port. (See also remote/local description in the Implementation Notes section.)

Table 3-6 contains a list of all Interface Commands.

E. Measurement and Status Commands

Measurements, such as bearing and signal strength, and status information, such as freqeuncy, are requested with these commands from the device under control. Each command is a request for a particular type of message.

Table 3-7 contains a list of all Measurement and Status Commands and their responses.

Example:

OMB(1f)

A message is returned containing the following information:

Date, Time, Frequency/Channel Flag, Channel Number, Frequency, Bearing, Signal Strength, Demodulation Mode, Bandwidth.

F. Message and Format and Status Mask Commands

These commands are used to set the format of the ASC II message. The commands permit selection of field separators and message terminators and similar ASC II functions. These commands make interface with the standard character oriented input procedures of high level languages less complicated.

Table 3-8 contains a list of all Message Format and Status Mask Commands.

3.2.8.2.3 Response Messages

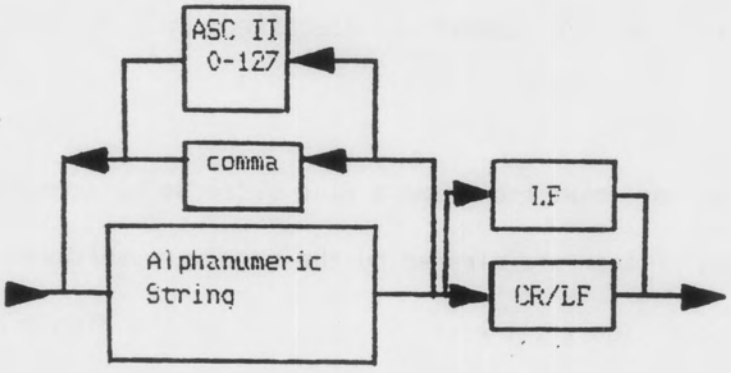


Figure 3-8. Response Syntax Diagram

Note

(1) Numeric strings are sent in fixed point notation. Leading zeros are not suppressed.

(2) (lf) = the ASC II line feed character

(3) (cr/lf) = the ASCII carriage return/line feed character combination

The minimum response message is comprised of an ASCII character string with a data field terminated by lf or (cr/lf).

If the message has more than one data field, then a comma is used as a delimiter between fields. Alternatively data fields may be separated with the ASC II value represented by the ASC II decimal digit string ddd, where ddd = 0..127 (default = 44 = comma).

A. Flag Response

Flags are indicators of the presence or absence of some predefined conditon. Flags are sent as a 3 digit number in the range 0..255, and it is assumed this number will be translated to an internal 8-bit byte representation by the controller software. The 8 bits then are decoded as flags indicating the condition specified in the response description.

It is important to note that each time a flag response is sent to the controller, those flags are cleared by the receiver software. Of course, if the condition still exists, the appropriate flag will be set once again.

B. Status Response

Status data includes the current settings used to control the device

hardware and records of system parameters. The nature of status data is such that it normally remains static unless changed through either remote or local commands.

Examples of status data are: current operating frequency, demodulation mode, and bandwidth.

Status can be used to verify command execution.

C. Measurement Response

Measurements are self-explanatory with one exception: they are periodic, which can be significant to the correct interpretation of this type of data.

For example, the fact that bearing measurements are only taken every 250 milliseconds is important in the collection and display of a bearing histogram. The sampling rate for a particular measurement is part of its field description.

COMMAND	KEY	COMMAND	KEY
AM	AM	MTR	MTR
FM	FM	SHFT	
CW	CW	0 to 9 or .	0 .. 9 ●
USB	USB	FUNC	FUNC
LSB	LSB	CH	CH
UP	△	CLR	CLR
DWN	▽	ENT	ENTER
BW	BW	MORE	◁
CONT	CONT	LOCK	LOCK
SET	SET	LESS	▷

Table 3-3 Key Commands

COMMAND	FUNCTION
PLLOFF	PLL OFF
PLLWID	PLL ON AND WIDE
PLLNAR	PLL ON AND NARROW
PLLOPR	PLL OPERATE
PLLRES	PLL RESET
BWA	BANDWIDTH 6 KHz
BWB	BANDWIDTH 13 KHz
BWC	BANDWIDTH 30 KHz
BWD	BANDWIDTH 200 KHz
SIGMTR	SIGNAL STRENGTH METER
PLLMTR	PLL TUNE METER
PHSMTR	ANTENNA PHASE METER
MODMTR	ANTENNA MODULATION METER
TENHZ	10 HZ TUNING RESOLUTION
HUNHZ	100 HZ TUNING RESOLUTION
ONEKHZ	1 KHZ TUNING RESOLUTION
TENKHZ	10 KHZ TUNING RESOLUTION
UNLCK	FINE TUNE KNOB UNLOCK
LCK	FINE TUNE KNOB LOCK
SCFRQ	SET SCAN FREQUENCIES (SWEEP) MODE
SCHAN	SET SCAN CHANNELS (STEP) MODE
AFCOFF	AFC OFF
AFCON	AFC ON
AGCNRM	AGC NORMAL
AGCSLW	AGC SLOW
TAHON	TRACK & HOLD ON
TAHOFF	TRACK & HOLD OFF
AUTO	AUTO BEARING DISPLAY
AIR	AIR BEARING DISPLAY
NORM	NORMAL BEARING DISPLAY
RECIP	RECIPROCAL BEARING DISPLAY

Table 3-4 State Commands

COMMAND	FUNCTION
	NOTE: d = the equivalent of a decimal number
BAVGd	BEARING AVERAGING TIME, d = 0..4 0 = 0.25 sec 1 = 0.5 2 = 1 3 = 2 4 = 4
DFGd	DF GAIN, d = 0..9
PWIDd	PAN WIDTH, d = 0..8 0 = .01 MHz 1 = .02 2 = .05 3 = .1 4 = .2 5 = .5 6 = 1 7 = 2 8 = 5
PSENSd	PAN SENSITIVITY, d = 0..255
PMODEd	PAN MODE, d = 0..2 0 = Off 1 = LIN 2 = LOG
DWLTd	DWELL TIME, d = 0..255 (Time = d x 0.1 sec)
DWION	DWELL INFINITY SWITCH ON
DWIOFF	DWELL INFINITY SWITCH OFF
SQd	SQUELCH, d = 0..255
FTd	FINE TUNE, d = +/- 0..255 (increments) increment = fine tune resolution see table 3-4

Table 3-5 Value Commands

COMMAND	FUNCTION
LCLO	LOCAL LOCKOUT
LCL	GO TO LOCAL
RENB	REMOTE ENABLE
DCLR	DEVICE CLEAR

Table 3-6 Interface Commands.

COMMAND	RESPONSE
OMA	STATUS FLAGS - One decimal ASCII encoded number (000..255) representing one byte comprised of bit flags (0 = false, 1 = true)

x = not used

Bit 7 6 5 4 3 2 1 0

```
- - - - - - - -
| | | | | | | |
| | | | | | | `- error condition exists
| | | | | | |
| | | | | | `- fault condition exists
| | | | | `- Scan mode active
| | | | `_ Scan hit
| | | `- X
| | `- Service Request
`- No antenna connected
```

OMAE	ERROR DETAIL FLAGS - Error number composed of four bit binary number, and four bit flags (0=false, 1-true)

x = not used

Bit 7 6 5 4 3 2 1 0

```
- - - - - - - -
| | | | | | | |
| | | | | | | `- Error number (valid only if bit 6 is
| | | | | | |    set)
| | | | | | `-  4 bit binary number
| | | | | `-
| | | | `-
| | | `- X
| | `- X
| `- Error message displayed on front panel
`- Remote command error
```

Table 3-7. Commands Requesting Measurement and Status Information

(Table 3-7 Continued)

COMMAND	RESPONSE
OMAF	FAULT DETAIL FLAGS - Format same as OMA

x = not used

```
Bit 7  6  5  4  3  2  1  0
    -  -  -  -  -  -  -  -
    |  |  |  |  |  |  |  |
    |  |  |  |  |  |  |  `- Hardware fault line low
    |  |  |  |  |  |  `- Power-on BITE test failure
    |  |  |  |  |  `- X
    |  |  |  |  `- X
    |  |  |  `- X
    |  |  `- X
    |  `- X
    `- X
```

OMB	DATE, TIME, FREQUENCY/CHANNEL FLAG, CHANNEL NUMBER, FREQUENCY, BEARING, SIGNAL STRENGTH, DEMODULATION MODE, BANDWIDTH

```
841208,075902,0,00,002.89700,045,03,AM,2.5K(cr/lf)
------ ------ - -- --------- --- -- -- ----
  |      |    |  |     |      |   |  |   |
  |      |    |  |     |      |   |  |   `- Bandwidth
  |      |    |  |     |      |   |  `- Demodulation Mode
  |      |    |  |     |      |   `- Signal Strength (0..99)
  |      |    |  |     |      |      200 millisecond sample
  |      |    |  |     |      `- Bearing (0..359, 360 = no bearing
  |      |    |  |     |         250 millisecond sample
  |      |    |  |     `- Frequency (MHz)
  |      |    |  `- Channel Number (0..99)
  |      |    `- Frequency/Channel flag (0 = freq, 1 = chan)
  |      `- Time (HHMMSS)
  `- Date (YYMMDD)
```

OMBSC	Same as OMB except data is sampled when a carrier is detected while scanning. This data is stored in a buffer, and it is the contents of this buffer that is sent when the OMBSC command is received.

(Table 3-7 Continued)

COMMAND	RESPONSE
OMC	SQUELCH OPEN/CLOSED, SQUELCH THRESHOLD, DWELL INFINITY ON/OFF, DWELL TIME, D.F. GAIN, PAN WIDTH, PAN SENSITIVITY

```
0,012,1,034,5,1,5,123(cr/lf
- --- - --- - - - ---
|  |  |  |  | | | |
|  |  |  |  | | | `- Pan Sensitivity (d=0..255)
|  |  |  |  | | `- Pan Width (d=0..8)(see Table 3-5)
|  |  |  |  | `- Pan Mode (d=0..2)(see Table 3-5)
|  |  |  |  `- D.F. Gain (d=0..9)
|  |  |  `- Dwell Time (d=0..255)
|  |  `- Dwell Infinity (1 = on)
|  `- Squelch Threshold (d=0..255)
`- Squelch open/closed (1 = open)
```

OMD	BEARING, SIGNAL STRENGTH Same as the decription for these data fields in OMB, except only the bearing and signal strength fields are sent.
OME	SCAN FREQUENCY/CHANNEL MODE, SCAN START FREQUENCY, SCAN STOP FREQUENCY, SCAN FREQUENCY STEP SIZE, SCAN START CHANNEL, SCAN STOP CHANNEL, SCAN FREQUENCIES WITH/WITHOUT AFC, SCAN WITH/WITHOUT THRESHOLD DETECTION, DWELL INIFINITY ON/OFF, DWELL TIME

```
1,000.20000,080.00000,000.00100,00,99,0,0,1,255(cr/lf)
- -------- -------- -------- -- -- - - - ---
|     |        |        |     |  | | | | |  |
|     |        |        |     |  | | | | |  |
|     |        |        |     |  | | | | |  `- Dwell Time (0..255)
|     |        |        |     |  | | | `- Dwell Infinity on/off(1=on)
|     |        |        |     |  | | `- Scan with/without Threshold
|     |        |        |     |  | |    (1 = without)
|     |        |        |     |  | `- Scan frequencies with/without
|     |        |        |     |  |    AFC (1 = without)
|     |        |        |     |  `- Scan Stop Channel (0..99)
|     |        |        |     `- Scan Start Channel (0..99)
|     |        |        `- Scan Frequency Step Size
|     |        |           (0.00010..0.100000 MHz, 0 = 1/2 I.F.BW)
|     |        `- Scan Stop Frequency (MHz)
|     `- Scan Start Frequency (MHz)
`- Scan Frequency/Channel mode flag (1 = freq, 0 = chan)
```

(Table 3-7 Continued.)

COMMAND	RESPONSE
OMF	FREQUENCY/CHANNEL FLAG, CHANNEL NUMBER, FREQUENCY, FINE TUNING RESOLUTION, KNOB LOCK

```
0,00,020.00000,3,1(cr/lf)
- -- --------- - -
¦  ¦     ¦     ¦ ¦
¦  ¦     ¦     ¦ `- Knob Lock (1 = locked)
¦  ¦     ¦     `- Fine Tune Resolution
¦  ¦     ¦        (0 = 10 Hz, 1 = 100 Hz, 2 = 1 KHz, 3 = 10 KHz)
¦  ¦     `- Frequency (MHz)
¦  `- Channel Number (0..99)
`- Frequency/Channel Flag (0 = Freq, 1 = Chan)
```

OMG	PLL, PLL OPERATE/RESET, AFC, AGC, METER

```
2,1,0,1,3,(cr/lf)
- - - - -
¦ ¦ ¦ ¦ ¦
¦ ¦ ¦ ¦ `- Meter (0..3)  (0 = Signal Strength, 1 = PLL Tune,
¦ ¦ ¦ ¦    3 = Phase, 4 = Modulation)
¦ ¦ ¦ `-AGC (0 = Normal, 1 = Slow)
¦ ¦ `- AFC (0 = Off, 1 = On)
¦ `- PLL Operate/Reset (0 = operate, 1 = Reset)
`- PLL (0..2)
   (0 = PLL Off, 1 = On and Wide, 2 = On and Narrow)
```

OMH	TRACK AND HOLD ON/OFF, MAGNETIC BEARING, TRUE BEARING, AUTO/AIR, NORMAL/RECIPROCAL, BEARING CORRECTION TABLE ON/OFF

```
1,0,1,0,1,0,(cr/lf)
- - - - - -
¦ ¦ ¦ ¦ ¦ ¦
¦ ¦ ¦ ¦ ¦ `- Bearing Correction Table On/Off (0 = On)
¦ ¦ ¦ ¦ `- Normal/Reciprocal  (1 = Reciprocal)
¦ ¦ ¦ `- Auto/Air  (1 = Air)
¦ ¦ `- True Bearing (1 = On)
¦ `- Magnetic Bearing (1 = On)
`- Track and Hold On/Off (1 = On)
```

(Table 3-7 Continued.)

COMMAND	RESPONSE
OMI	AUTO SELECT BANDWIDTH ON/OFF, CW AUDIO FILTER ON/OFF, CRT ON/OFF, MGC ON/OFF, RECEIVER BITE GENERATOR ON/OFF, ANTENNA BITE GENERATOR ON/OFF, EXTERNAL/INTERNAL SENSE ELEMENT

```
1,0,1,0,1,0,1(cr/lf)
- - - - - - -
¦ ¦ ¦ ¦ ¦ ¦ ¦
¦ ¦ ¦ ¦ ¦ ¦ `-External/Internal Sense Element (1 = External)
¦ ¦ ¦ ¦ ¦ `- Antenna Bite Generator On/Off (1 = On)
¦ ¦ ¦ ¦ `- Receiver Bite Generator On/Off (1 = On)
¦ ¦ ¦ `- MGC On/Off (1 = On)
¦ ¦ `- CRT On/Off (1 = Off)
¦ `- CW Audio Filter On/Off (1 = On)
`- Auto Select Bandwidth On/Off (1 = Off)
```

OMJ	REMOTE PORT BAUD RATE, I/O DATA PORT BUD RATE, IEEE-488 ADDRESS

```
4800,0300,30(cr/lf)
---- ---- --
  ¦    ¦    ¦
  ¦    ¦    `- IEEE-488 Address (0..30)
  ¦    `- I/O Data Port Baud Rate
  `- Remote Port Baud Rate
```

OMK	ANTENNA ZERO HEADING OFFSET, ANTENNA MODULATION, ANTENNA PHASE

```
000,99,16(cr/lf)
--- -- --
 ¦   ¦  ¦
 ¦   ¦  `- Antenna Phase (0..32)
 ¦   `- Antenna Modulation (0..99)
 `- Antenna Zero Heading Offset (0..359)
```

OMZA	I.F. FILTER COMPENSATION FOR FL1,FL2,FL3,FL4

```
012,340,346,358(cr/lf)
--- --- --- ---
 ¦   ¦   ¦   ¦
 ¦   ¦   ¦   `- FL4 (0..359)
 ¦   ¦   `- FL3 (0..359)
 ¦   `- FL2 (0..359)
 `- FL1 (0..359)
```

COMMAND	FUNCTION
CRLF	Terminate messages with the ASCII carriage return/ line feed combination
LF	Terminate messages with the ASCII line feed character only
COMMA	Separate data fields with a comma.
SEP ddd	Separate data fields with the ASCII value represented by the ASCII data string "ddd", where "ddd" = 0..127 (default = 44 = comma)
SMSKddd	The summary status flag mask is set to the unsigned binary number ddd, where ddd is an ASCII decimal string 0..255. The service request bit will be set if the corresponding summary status condition is true.

TABLE 3-8 MESSAGE FORMAT COMMANDS

STATUS MASK

The status mask is used to set the condition under which a service request bit will be set (see OMA message response, Table 3-7). Through use of this command the seervice request bit will be set when the status summary mask of the OMA message equals the corresponding binary (or decimal) valus indicated by the command.

Example: If the SMSK command is sent and the mask value is 004, the service request bit (D6) is set when the FAULT CONDITION (D2) bit of the OMA message is 1. All other bits are masked and will be 0.

	D7	D6	D5	D4	D3	D2	D1	D0
STATUS SUMMARY MASK =	0	X	0	0	0	1	0	0

Under these conditions if D2 (FAULT) = 1, then when OMA is sent both D2 and D6 (SERVICE REQUEST) are set. The controller is then alerted that a fault condition exists and can use the OMAF command to receive a fault detail flag response. It follows logically then, that through use of the status mask, the service request can be set when any, part, or all of the bits (D0-D4, and D7) are set, dependant on the mask value.

3.2.8.2.4 Response/Command Dictionary

RESPONSE	COMMAND
AFC	OMG
AGC	OMG
ANTENNA BITE GENERATOR ON/OFF	OMI
ANTENNA MODULATION	OMK
ANTENNA PHASE	OMK
ANTENNA ZERO HEADING OFFSET	OMK
AUTO SELECT BANDWIDTH ON/OFF	OMI
AUTO/AIR	OMH
BANDWIDTH	OMB,OMBSC
BEARING	OMB,OMBSC,OMD
BEARING CORRECTION ON/OFF	OMH
CHANNEL	OMB,OMBSC,OMF
CW AUDIO FILTER ON/OFF	OMI
D.F. GAIN	OMC
DATE	OMB,OMBSC
DEMODULATION MODE	OMB,OMBSC
DWELL INFINITY ON/OFF	OMC,OME
DWELL TIME	OMC,OME
ERROR CONDITION	OMA
ERROR NUMBER	OMAE
ERROR MESSAGE DISPLAYED ON FRONT PANEL	OMAE
EXTERNAL/INTERNAL SENSE ELEM.	OMI
FAULT CONDITION	OMA
FINE TUNING RESOLUTION	OMF

3.2.8.2.4 Continued

RESPONSE	COMMAND
FREQUENCY	OMB, OMBSC, OMF
FREQUENCY/CHANNEL MODE	OMB, OMBSC, OMF
HARDWARE FAULT LINE LOW	OMAF
I.F. FILTER COMPENSATION	OMZA
I/O DATA PORT BAUD RATE	OMJ
IEEE488 ADDRESS	OMJ
KNOB LOCK	OMF
MAGNETIC BEARING	OMH
METER	OMC
MGC ON/OFF	OMI
NORMAL/RECIPROCAL	OMH
NO ANTENNA CONNECTED	OMA
PAN SENSITIVITY	OMC
PAN WIDTH	OMC
PLL	OMG
PLL OPERATE/RESET	OMG
POWER ON BITE TEST FAILURE	OMAF
RECEIVER BITE GENERATOR ON/OFF	OMI
REMOTE COMMAND ERROR	OMAF
REMOTE PORT BAUD RATE	OMJ
SCAN FREQUENCIES WITH/WO AFC	OME
SCAN FREQUENCY STEP SIZE	OME
SCAN FREQUENCY/CHANNEL MODE	OME
SCAN HIT	OMA

3.2.8.2.4 Continued

RESPONSE	COMMAND
SCAN MODE ACTIVE	OMA
SCAN START CHANNEL	OME
SCAN START FREQUENCY	OME
SCAN WITH/WO THRESHOLD DETECT	OME
SERVICE REQUEST	OMA
SIGNAL STRENGTH	OMB, OMBSC, OMD
SQUELCH OPEN/CLOSED	OMC
SQUELCH THRESHOLD	OMC
TIME	OMB,OMBSC
TRACK AND HOLD ON/OFF	OMH
TRUE BEARING	OMH

3.2.8.2.5 Implementation Notes

A. IEEE-488 FUNCTIONS IMPLEMENTED

(1)	SH1	Source Handshake
(2)	AH1	Acceptor Handshake
(3)	T4	Basic Talker (subset 4)
(4)	L2	Basic Listener (subset 2)
(5)	RL1	Remote/Local (complete capability)
(6)	DC1	Device Clear (complete capability)

NOTE

Refer to IEEE-488-1978 Standard for details.

B. IEEE-488 REMOTE/LOCAL FUNCTION

The IEEE-488-1978 Standard decribes the remote/local function for subset RL1. In addition, the following options were selected when implementing the standard:

(1) In LWLS (Local with Lockout State) remote commands are ignored and are not stored.

(2) When going from LOCAL TO REMOTE the local control settings are used until overidden by remote input data.

(3) When going from REMOTE TO LOCAL the current local settings become active immediately.

C. IEEE488 vs. RS-232 REMOTE CONTROL PROGRAMMING

Although the syntax and content of device dependent commands are the same for both IEEE-488 and RS-232 remote control, they require a distinctly differant programming approach.

The IEEE-488 protocol prevents any device from transmitting unless it is addressed as a Talker. Also, handshaking assures that devices with different transmission speeds can Talk and Listen, since the data transmission slows to match the slowest active Listener on the bus. The RS-232 interface in the 2040/3045 remote control software does not provide for addressing or handshaking.

A 200 byte input command buffer in the receiver will accept any combination of commands. But when the controller requests measurement or status data it must be ready to receive a response message immediately following the command requesting this data. The receiver will not wait to respond.

Either the controller must poll his RS-232 input device until the full message is received, or an interrupt driven buffer must be used to store the message until the controller is ready to process it.

One possible procedural implementation is presented below.

```
Procedure GetMeasurementOrStatus
    Send command to request measurement or status
    Repeat
       Wait until RS-232 input ready
```

```
        Add new character to buffer
    Until character received = ASCII line feed (end of message)
```

Note that as a result of the method used for RS-232 remote control, a group of commands sent with a request for measurement or status information in the middle or with multiple requests will result in incomplete or missed messages. Make your request individually or only at the end of a multiple command string and read one message before requesting another. Adhering to this method will prevent any loss of data.

D. A METHOD FOR REMOTE SCANNING

The correct method for scanning may not be immediately obvious. Assuming the controller is not dedicated to continuously monitoring the status of one device, it is necessary to sample the status of the scanning function until a signal is detected. Then, the measurement and status data taken when the signal was detected is read from the device. A command to continue scanning is sent and the controller returns to monitoring the signal detect flag.

The procedure has two major sections: setup and scanning. An outline of tasks would look like:

```
Procedure ScanSetup
    Clear device
    Set scan frequency/channel mode
    Set scan stop frequency/channel
    Set dwell infinity on
    Set signal detection threshold squelch
    Start Scanning
```

```
Function ScanCheck
    Read status flags
    If signal detected then
        Read scan measurement and status data
        Continue Scanning
        ScanCheck = true
        else ScanCheck = false
```

After setup, calls to ScanCheck will return true if a signal was detected while scanning and false if not. Note that the dwell time was set to infinity during setup. Otherwise, the device will not wait until the controller sends a command to continue scanning. This guarantees that measurement and status data taken when signals are detected are not missed if the controller is not ready to read in the data. To clear the scanning function, a device clear command is issued.

3.3 PRELIMINARY CALIBRATION AND ADJUSTMENT

3.3.1 Calibration of System Bearing Accuracy.

A calibration of the system's bearing accuracy should be performed when the installed equipment is operational. As stated before, bearings indicate the direction of arrival of signals. This direction may not be toward the transmitter due to reflections, re-radiation, or changes in polarization of the signal caused by the local environment or antenna installation. Bearing error will change with frequency and bearing calibration conditions data at the low end of the receiver band may not be the same as the upper end. Undesirable bearing error may occur if the incoming signal is modulated at 165 Hz. Calibration determines the effect of the antenna installation and allows the operator to use the system with greater accuracy at a given frequency.

3.3.1.1 Antenna Zeroing.

Prior to calibration the system may be realigned so that a signal received from 0 degrees is displayed as such on the CRT. Normally the fixed station antenna will remain zeroed to true North as described in paragraph 2.3.2.2(B). Where high bearing accuracy is desired on only one frequency the antenna can be electrically zeroed at that frequency. Zeroing is accomplished with a low power transmitter located visually at 0 degrees, and by manually rotating the antenna until the CRT trace is 0 degrees. The antenna should be zeroed at the frequency of primary use or alternately at a midband frequency. Zeroing should also be done is a "trial-and-adjust" procedure, as the presence of a technician adjusting the antenna will distort the antenna's field

and its directional capability. When 0 degrees is obtained on the CRT in an unobstructed environment, secure the antenna mountings. If antenna cannot be secured in a 0 degrees position due to obstructions, consult paragraph 3.2.3.

3.3.1.2 Calibration.

360 degree calibration is a calibration of the bearings through a full circle and is performed after the 0 degrees calibration is complete. The purpose is to measure the differences between visual and indicated bearings and record the information for future use. For shipboard or land-based stations, the data may be taken every 5, 10 or 15 degrees as desired. The data is normally taken only at the cardinal (every 90 degrees) or semi-cardinal (every 45 degrees) points for auto or aircraft installation. At least one complete calibration should be accomplished at the middle of each receiver band. All calibrations for other than the land-based stations should be conducted with the transmitter stationary. The ship, auto or aircraft is then slowly rotated to allow the CRT and actual bearings to be measured and recorded.

A. Depending on the application, set up or establish the position of a transmitter as follows (transmitter power should be less than 10 Watts):

(1) Land-based installation. A transmitter at street level (or in the air if used with aircraft) approximately 0.25 to 1.0 mile (0.4 to 1.6 Km) away. Operate in

a clear open area, if possible, away from tall buildings, mountains or other causes or bearing errors.

(2) Shipboard installation. A transmitter on the water surface or on another ship approximately 0.5 to 2 miles (0.8 to 3.2 km) away. Operate offshore or in clear open harbor area away from bridges, large vessels, large dockside equipment, etc. Note that a harbor area is normally a poor area to conduct a calibration due to the presence of signal reflections.

(3) Automobile installations. A transmitter at approximately 0.25 to 1 mile (0.4 to 1.6 km) away. Operate in as open an area as possible away from downtown, multi-level buildings, overhead wired, etc. The best location is an open field.

(4) Aircraft installation. A transmitter at approximately 1 to 3 miles (1.6 to 4.8 km) away while flying as low as possible. Operate over relatively flat and open terrain.

B. After readings have been taken, prepare an error/correction chart if required. An example of this type chart, with bearings recorded ever 45 degrees, appears in the table 3-9:

CRT Bearing (Requiring correction)	Known Bearing Error (Correction applied to CRT bearings)	To Obtain Actual Bearing (Visual)
0 degree	0 degree	0 degree
45	+4 degree	49
90	+6 degree	96
135	+4 degree	139
180	0 degree	180
225	-4 degree	221
270	-6 degree	264
315	-4 degree	311

TABLE 3-9. Typical Error/Correction Chart

C. To use the table, apply the known bearing error to the CRT bearing. For example, while operating the system, a bearing of 225 degrees is noted on the CRT. From the chart above the bearing correction to be applied is -4 degrees. Therefore, the actual bearing to the signal is 225 degrees minus 4 degrees, or 221 degrees.

To ensure consistent bearings, note those conditions which might be influential during the calibration. For example, the tuned frequency on other antennas, the rigging of booms, cranes, davits, etc.

3.3.2 Adjustment for Noise.

Signal reception can be improved significantly by reducing the amount of radio frequency interference (RFI) within the operating band of the equipment. RFI can be introduced into the receiver by radiation picked up at the antenna or the cables, or by

conduction (usually via the power supply). The particular source of noise can sometimes be identified by listening to the speaker; for example: radar pulse repetition rates, power hum, 60 Hz, etc. In any event, the amount of interference from various sources should be examined and reduced as much as possible to assure the best reception for the ADF system. This can be accomplished by conducting the following test during periods when there is minimal radio traffic and minimal electrical equipment usage.

A. Preparation.

(1) Disconnect the receiver from its normal power source and connect it to a temporary source. For standard DC, this can be a 12 VDC battery with short leads and alligator clips. Fasten the clips to pins B and C of the power connector J13 [(see Figure 2-1(K)]. Units with optional power supplies can rig similar hookups.

(2) Disable the automatic gain control (AGC).

(3) Connect an audio power meter across the speaker terminals or to a telephone jack at the rear panel of the receiver.

(4) Turn the receiver on and locate the three frequencies (preferable high, midband, and low) where there are no apparent signals. Record the exact frequency and audio power for each selected frequency. Do not change any controls (except frequency selection) for the remainder of the tests.

B. Radiated Noise Test.

(1) Disconnect the antenna input and connect a 50-Ohm dummy load to the audio output, on the receiver's rear panel.

(2) Record the audio power output for each of the three frequencies selected in step A (4). The difference in power levels at each frequency is the measure of RF picked up in the antenna and its coaxial cable.

C. Conduction Noise Test.

(1) Disconnect the battery and reconnect the receiver to its normal power source.

(2) Disconnect or open all nonessential station circuit breakers.

(3) Record the audio power output for each frequency selected in step A (4). The difference between these outputs and those in B (2) is the conducted noise from essential circuits.

(4) Energize remaining circuits and machinery noting any significant increase in audio noise levels as each is energized.

(5) Restore the system to its normal operating mode.

3.3.2.1 Radiated RFI Reduction.

An excellent way to determine the source of radiated interference

is by observing the display. Since local radiation normally requires a local power source, turning on and off individual equipment while observing the display is usually the easiest method. If the interference is insufficient to pinpoint using the scope, a portable (small loop) RFI detector can be used.

When the source is identified, the easiest cure is to make sure it is not energized when the ADF is in use. If the source is vital to other operations, then the radiation should be minimized. Any source of radiation has to have an antenna, and a signal generator. Eliminating the generator is the best approach, as you may also be stopping conducted interference. When this is not possible, the effective antenna must be shielded or bonded. Shielding is covering the source with a metal (conducting) surface that has a good ground contact. Bonding is providing a good contact to ground at every quarter-wavelength in floating conductors such as lifelines, guys cables, etc. A quarter-wave length ($\lambda/4$) for any frequency (f) can be determined from the formula.

$$4 = \frac{75 \text{ meters}}{f \text{ (in megaHertz)}} = \frac{246 \text{ feet}}{f \text{ (in megaHertz)}}$$

In the marine FM band, 148-174 MHz, the mid band quarter-wavelength would be 1.5 feet (.46 m), the best bond or ground straps are solid copper strips approximately one-inch wide with both ends bolted to bright metal surfaces. The strap should be as short as possible. Good bonding will not only reduce noise sources, but decrease the re-radiation of received signals that causes ADF bearing errors.

3.3.2.2 Conducted RFI Reduction.

Interference sources are generally electric generators, motors, inverters or rectifiers that emit broad-band noise. Noise from these sources can often be decreased by good maintenance such as cleaning commutators or reseating the brushes. Sometimes it is necessary to install suppression filters (large capacitors that conduct the interfering frequency(s) to ground). RFI can also be generated in purely mechanical devices, particularly where corroded surfaces are in contact at different electrical potentials. On a ship or boat almost any metallic interface is a potential source of RFI.

3.4 OPERATION UNDER UNUSUAL CONDITIONS

3.4.1 Emergency Operation.

The design of the equipment eliminates the need for any emergency operating procedures.

3.4.2 Operation Under Extreme Climatic Conditions.

It may become necessary to operate the equipment under abnormal conditions where extreme cold, heat, humidity, moisture or sand conditions prevail.

In subzero temperatures handle the equipment carefully. The parts, especially plastics and wire insulation, become brittle. If possible, keep the equipment operating so it remains warm and dry.

In tropical climates, moisture conditions are acute. Poor ventilation

and high relative humidity may cause condensation. Dry the equipment thoroughly at the first signs of moisture.

The main problem in desert operation is large amounts of sand, dust and dirt entering the equipment. Do not remove panels or expose internal components unless absolutely necessary. Clean assemblies thoroughly before replacing them. Make frequent preventive maintenance checks.

3.4.3 Operating Conditions Causing Bearing Errors.

Certain physical, environmental or technical conditions can cause false or misleading signals that result in bearing errors. Signal reflection is probably the most common source, but simultaneous signals and polarization variations can also cause errors. When the operator becomes familiar with the equipment and the area of operation, careful observation of bearing data can usually detect misleading signals.

Signals reflections in the VHF band can be caused by nearly any object--people, vehicles, trees, buildings, antennas, etc. As an example, signals reflected off of a low-flying aircraft can oscillate 5 to 10 degrees around a center bearing. This oscillation, known as bearing jitter, can sometimes be removed by increasing the bearing integration rate through the use of numbered function 10.

Since the system points to where the signal is coming from, this may or may not be toward the transmitter due to these reflections. For fixed land or shipboard stations, reflections are typically caused by structures near or in the path of the signal on the ground.

Reflections from structures are more significant than from aircraft, since reception is line-of-sight to the signal source.

In mobile land applications, it is usually best to keep moving and visually time average the bearings to integrate out reflected signals. If there is little or no bearing change on the display as you move, the indicated bearing is probably the correct one. But if the bearing moves widely, the operator must interpret the display. In such cases, try to identify a 45 degree or 90 degree sector on the display where the bearing is present most of the time. If this can be done, proceed in that general direction. Otherwise, continue driving until the bearings are more repeatable. When operating in the area of multilevel buildings, which typically cause significant reflections, it is sometimes necessary to wait for a clear intersection to determine the correct direction to proceed.

The antennas for this system are designed to receive vertically polarized signals, the type most transmitting stations emit. When these signals are reflected, they sometimes arrive from different directions causing bearing errors. Some reflected signals change to horizontal polarization. When bearing error is caused by polarization (in mobile applications), the recommended procedure is to keep moving and visually time average the bearings received. The longest and steadiest displays are typically the ones to vertically polarized signals, which are in the correct direction to the signal source.

There is another condition that can cause bearing errors for mobile situations. The displayed bearing to a signal may change if the auto, boat, or plane rocks back and forth. At times this error could be in

excess of 10 to 15 degrees. To obtain the most accurate bearings it is best to take them when the airplane is in level flight, the boat is straight up (between rolls), or the auto is level on flat ground.

3.5 PREPARATION FOR MOVEMENT

This section contains instructions for removal and repacking the equipment prior to reshipment. These instructions are also used to repack the equipment for storage for a limited period.

3.5.1 Disassembly of Equipment.

In general, the only disassembly required to move the equipment is to dismount the receiver and remove all connections, to dismount the antenna and disconnect cabling and to disengage the antenna coax and power cables from their route.

To ready the receiver for movement, disconnect the power cable, the antenna coax and power cables, any optional equipment attachments (such as headphones), and remove the unit from its mounting (as required).

To remove the fixed site antenna, disconnect the cables, and disassemble the element as necessary to remove the antenna from its mounting.

Power and coaxial cables between the receiver and the antenna are typically 50 feet in length. Disengage these cables carefully from their route and coil separately for storage.

To prepare the mobile antenna for movement, disconnect the two cables

and dismount the unit from its installation. Monopole elements may be removed from their connectors and packaged separately. Attachment straps may be also removed from the antenna and packaged separately.

3.5.2 Repacking for Shipment for Storage.

A. The exact procedure for repackaging depends on the material available and the conditions under which the equipment is to be shipped or stored. If the original shipping carton is still available and in good condition, consider using it. Normally the direction finder system will be shipped or stored complete with all interconnecting cables.

B. Pack to withstand harsh treatment.

C. Identify the contents of the carton by use of appropriate labels. Mark the outer carton FRAGILE - ELECTRONIC EQUIPMENT INSIDE and clearly indicate the shipping destination of the equipment.

SECTION IV
MAINTENANCE

4.1 GENERAL

The OAR3045 Spectrum Monitoring and Automatic Direction Finding Receiver is a combination radio direction finding and communications receiver with a built-in spectrum monitor. The receiver is microprocessor controlled, single channel, triple-conversion superhetrodyne type using synthesized tuning over the 20 MHz to 520 MHz range.

4.2 Theory of Operation

Consider an H-Adcock array mechanically rotating at a constant rate in a uniform electromagnetic field as shown in Figure 4-1.

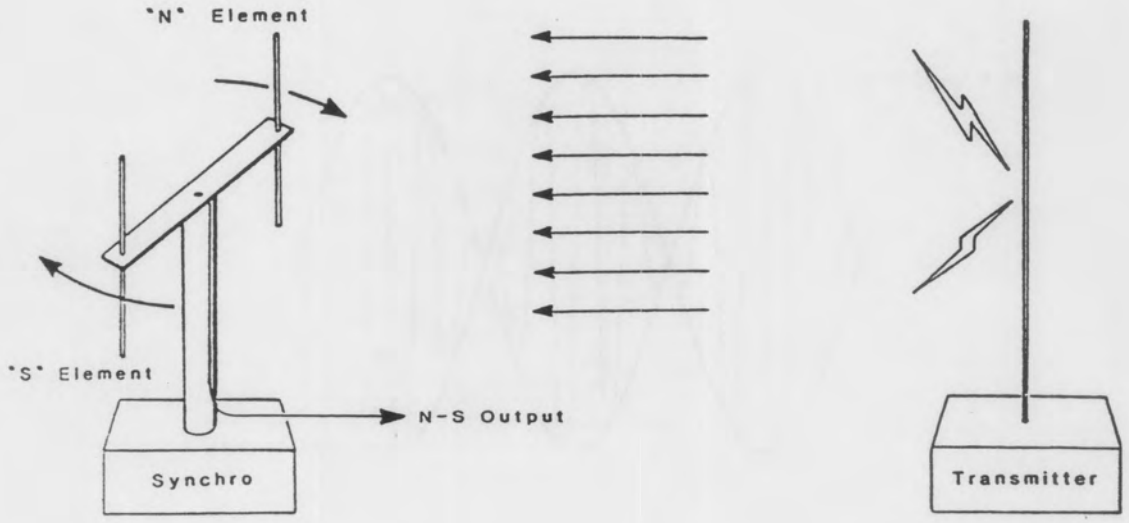


Figure 4-1. ROTATING H-ADCOCK

If the outputs of the two opposing elements are differenced, a rotating figure-of-eight pattern will occur in the horizontal plane as shown in Figure 4-2 with the output maximum when the opposing elements are aligned

toward the signal source and minimum when the opposing elements form a line perpendicular to the direction of the wavefront. This difference (N-S) output will be amplitude modulated at a rate equal to twice the rotational rate of the H-Adcock.

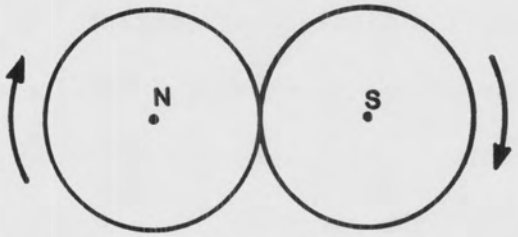


Figure 4-2. ROTATING FIGURE-OF-EIGHT PATTERN

Figure 4-3 illustrates the output waveform under such circumstances.

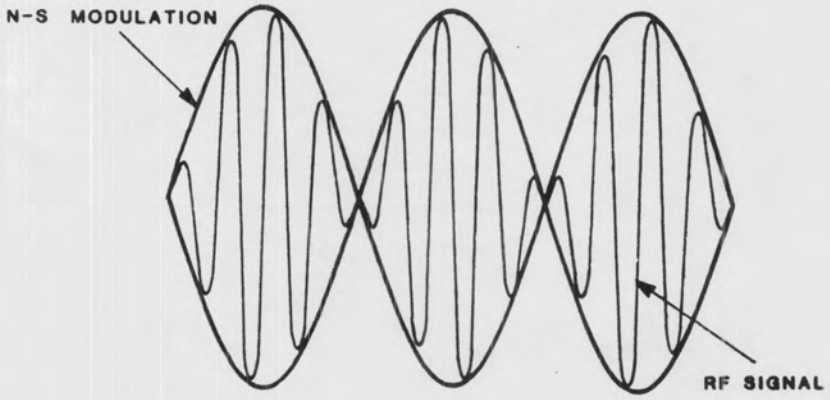


Figure 4-3. ROTATING H-ADCOCK RF OUTPUT

Note the RF phase reversal that occurs at each minimum in Figure 3. This effect is most easily explained by the vector diagrams in Figure 4-4.

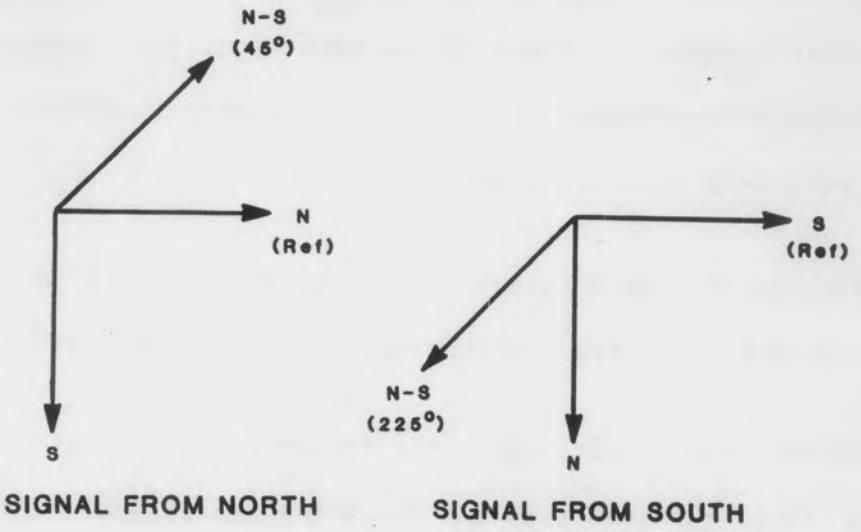


Figure 4-4. VECTOR RELATIONSHIP WHEN SIGNAL IS FROM NORTH OR SOUTH

Figure 4-4 assumes the elements are in line with the signal source, the "north" element closest to the signal source, and with a quarter-wavelength spacing between the two elements. In this instance, the N-S difference component leads the north vector by 45 degrees. If the H-Adcock now rotates 180 degrees so that the "south" element is closest to the signal source, the vector diagram changes. In this case, the N-S vector now leads the reference vector (the south vector in this case) by 225 degrees, and is therefore 180 degrees out of phase with the N-S vector. This accounts for the RF phase reversal at each minimum as shown in Figure 4-3. This phase reversal is very important, as it ultimately permits resolution of any 180 degree bearing ambiguity.

Examination of the waveform of Figure 4-3 reveals that it is actually a double sideband (DSB) suppressed carrier, amplitude modulated signal, identical to that which would be obtained in a balanced modulator with the carrier modulated at a rate equal to the rotational frequency of the H-Adcock. Given this fact, we can then say that the RF carrier from the

signal source is being multiplied by an audio sinusoid (assuming a circular figure-of-eight antenna difference pattern) equal in frequency to the rotational rate of the H-Adcock. If the RF carrier is A x sin Wct and the rotational rate is B x sin Wmt, then

$$\text{Rotating H-Adcock output} = (A \times \sin Wct)(B \times \sin Wmt)$$
$$= (A \times B)\,((1/2 \cos (Wct-Wmt) - 1/2 \cos (Wct+Wmt)) \quad (1)$$

which indicates the existence in the frequency domain of two distinct frequencies (the carrier plus and minus the rotational rate). The A coefficient in expression (1) represents the magnitude of the RF carrier. The physical significance of B is less clear, but probably relates to the antenna gain.

Next, if we add a vertical omnidirectional sense element at a point midway between the opposing H-Adcock elements, another vector (representing the output of this element) is created that is mid-phase between the N and S vectors of Figure 4-4. See Figure 4-5.

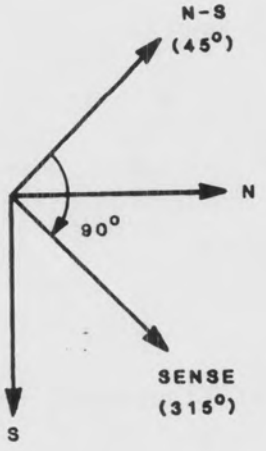


Figure 4-5. VECTOR RELATIONSHIPS WITH ADDITION OF SENSE ELEMENT

Note that this sense signal phase lags the N-S difference vector by 90

degrees. In fact, it can be shown by trigonometry that a quadrature phase relationship will always exist between the N-S and sense signals, regardless of the azimuth of the signal source.

In order to use the RF outputs of the H-Adcock plus central sense antenna in a single-channel ADF, the sense and difference signals must be integrated in such a manner that the resultant signal can be demodulated by a subsequent receiver that will permit recovery of the directional and sense information in a useable form. The most convenient technique is to recombine the N-S and sense signals to form a synthetic AM signal with carrier. This can be accomplished by retarding or advancing the phase of the sense signal by 90 degrees and then combining this phase shifted sense signal with the N-S signal in a linear summing junction as shown in Figure 4-6.

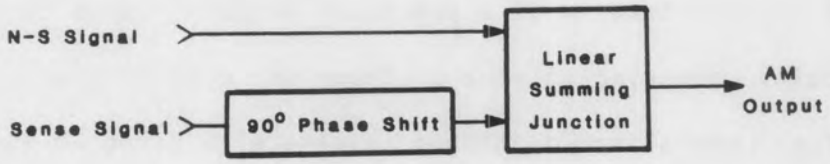


Figure 4-6. SYNTHESIS OF AM SIGNAL

This AM synthesis process can also be considered mathematically. First, consider the sense signal prior to 90 degrees phase retardation in its time domain form:

$$\text{sense signal} = C \times \cos \omega t \qquad (2)$$

where C is the peak amplitude of the sense signal. That this sense signal is a cosine function may be seen by the 90 degrees offset between the sense and N-S signals in Figure 4-5. Next, if we retard the sense signal by 90 degrees (using a phasing line as is done in existing OAR single-channel

ADFs), (2) above becomes a minus sine function:

$$\text{sense signal } -90 \text{ degrees} = -C \times \sin Wct \qquad (3)$$

Now, by linearly summing expressions (1) and (3) we obtain the following expression:

$$\text{summing junction output} = -C \times \sin Wct + \frac{AB}{2} \cos (Wct-Wmt) - \frac{AB}{2} \cos (Wct+Wmt) \qquad (4)$$

This summing junction output as expressed in (4) above will be recognized as a standard AM signal with carrier, the modulation depth being established by the magnitude of the coefficients of A, B, and C. This AM signal is then applied to an AM receiver.

Figure 4-7 is a block diagram of a practical antenna system that eliminates the mechanically rotating antenna in favor of electronically commutated elements. The central sense antenna is also eliminated in favor of sense derivation from all elements.

Assume the AM signal of (4) is now processed by the receiver and applied to an AM demodulator. For simplicity, we will disregard the receiver frequency conversions. If the AM demodulator is of the carrier recovery type; the incoming signal divides into two paths, strips the modulation off of the signal through one of the paths via hard limiting, then multiplies this recovered carrier by the signal from the other path. The limited signal is expressed as

$$\text{recovered carrier} = C \times \sin Wct \qquad (5)$$

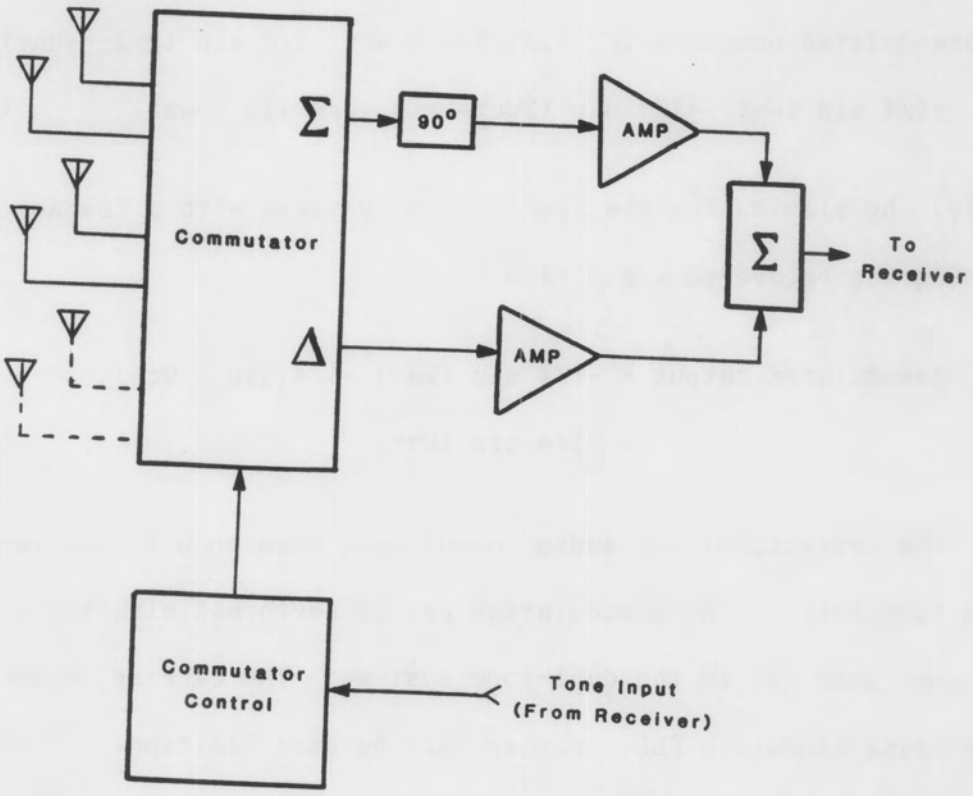


Figure 4-7. FUNCTIONAL BLOCK DIAGRAM OF COMMUTATING ANTENNA SYSTEM.

Multiplying this recovered carrier by the AM signal of (4) gives us

$$\text{demodulated output} = -C \times \sin Wct \left((-C \times \sin Wct + \frac{AB}{2} \cos (Wct-Wmt) - \frac{AB}{2} \cos (Wct+Wmt)\right) \quad (6)$$

Setting coefficients A, B and C equal to unity for simplicity and expanding:

$$\text{demodulated output} = \sin Wct - 1/2 \sin Wct \times \cos (Wct-Wmt) + 1/4 \sin Wct \times \cos (Wct+Wmt) \quad (7)$$

Next, employing the appropriate trigonometric identities:

$$\text{demodulated output} = 1/2 - 1/2 \cos 2\,Wct - 1/4 \sin (2\,Wct - Wmt) - 1/4 \sin (Wmt) + 1/4 \sin (2Wct + Wmt) + 1/4 \sin (-Wmt) \qquad (8)$$

Finally, by eliminating the high frequency terms with a lowpass filter and combining the recovered audio terms:

$$\text{demodulated output} = -1/4 \sin (Wmt) + 1/4 \sin (-Wct) = -1/4 \sin (Wmt) \qquad (9)$$

Thus, the rotational or audio commutating frequency is recovered phase-locked loop (PLL). AM demodulation can be performed with the single tone technique just as in the dual-tone system. The carrier is derived by a narrow noise bandwidth PLL, rather than by hard limiting. This recovered carrier (the PLL VCO output) is then quadrature phase shifted and multiplied by the incoming IF signal. Equations (6) and (9) are still valid.

Suppose now that the azimuth of the received signal (or the antenna orientation) changes by 180 degrees. This results in a phase reversal of the N-S output as was shown in the vector diagrams of figure 4-4, while the phase of the sense signal remains unchanged. This N-S phase reversal is accommodated mathematically by changing the sign of (1) which results in a sign change (phase reversal) of the sidebands in the summing junction output (synthetic AM) signal of (4). Carrying this through the receiver, the new expression for the output of the AM demodulator becomes:

$$\text{demodulated output} = -C \times \sin Wct \,((-C \times \sin Wct - \tfrac{AB}{2} \cos (Wct - Wmt) + \tfrac{AB}{2} \cos (Wct + Wmt)) \qquad (10)$$

By employing the same expansions, trigonometric identities, lowpass filtering, and term combining as in (7) - (9), we obtain

$$\text{demodulated output} = 1/4 \sin \omega mt \qquad (11)$$

Note that the recovered audio tone of expression (11) is identical in magnitude but 180 degrees out of phase with the recovered audio tone of expression (9), thus proving that the single-tone single-channel ADF can resolve the 180 degrees ambiguity of the received signal.

If the received signal is from the East or West, the cosine terms in (1) change to sine terms. By performing the same mathematical operations as described above, an audio term is again recovered, but this audio term is now a cosine function (+ or - depending upon whether the received signal is from the east or west). If the received signal is from an intercardinal point (45 degrees for example), the recovered audio tone will then contain both sine and cosine components.

Figure 4-8 is a block diagram of a signal processor that handles the recovered audio tone. A 165 Hz oscillator generates a "sine" output that is used to commutate the antenna elements as well as to provide a multiplying signal to the "N-S" synchronous detector. A "cosine" output is also generated to drive the "E-W" synchronous detector. Figure 4-9 illustrates the synchronous detector outputs with signals received from due "north" or due "south".

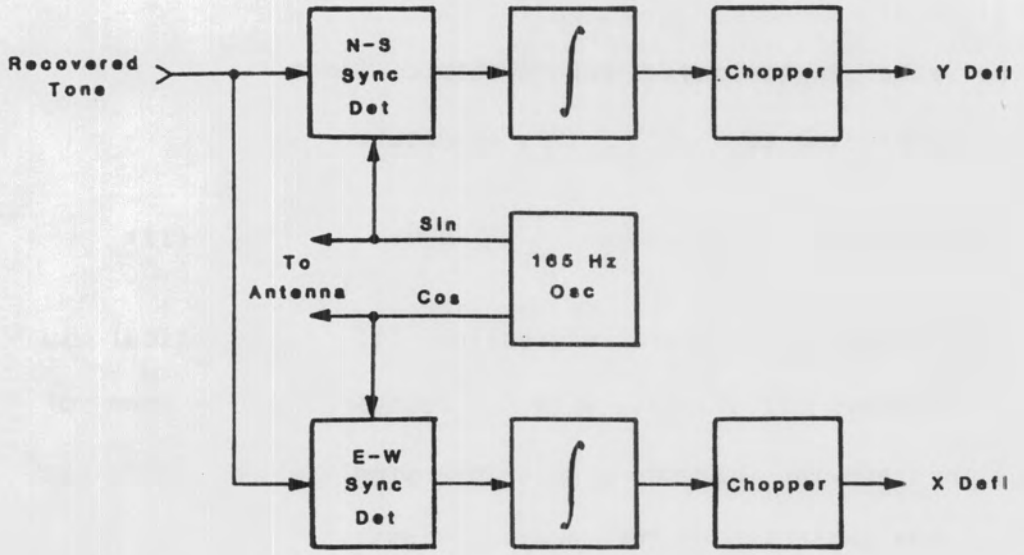


Figure 4-8. SINGLE TONE SIGNAL PROCESSOR

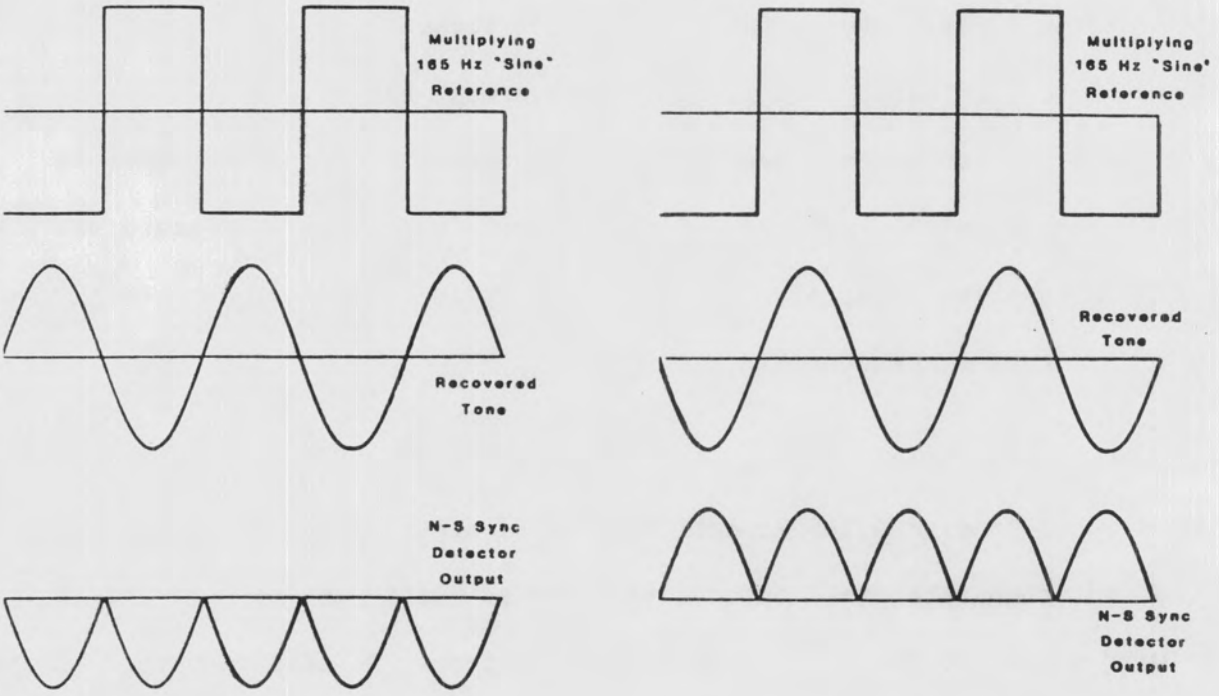


Figure 4-9. N-S SYNCHRONOUS DETECTOR WAVEFORMS

Note how the recovered audio tone is synchronously full-wave rectified with the appropriate polarity change. Figure 4-10 illustrates the E-W synchronous demodulator outputs under identical circumstances.

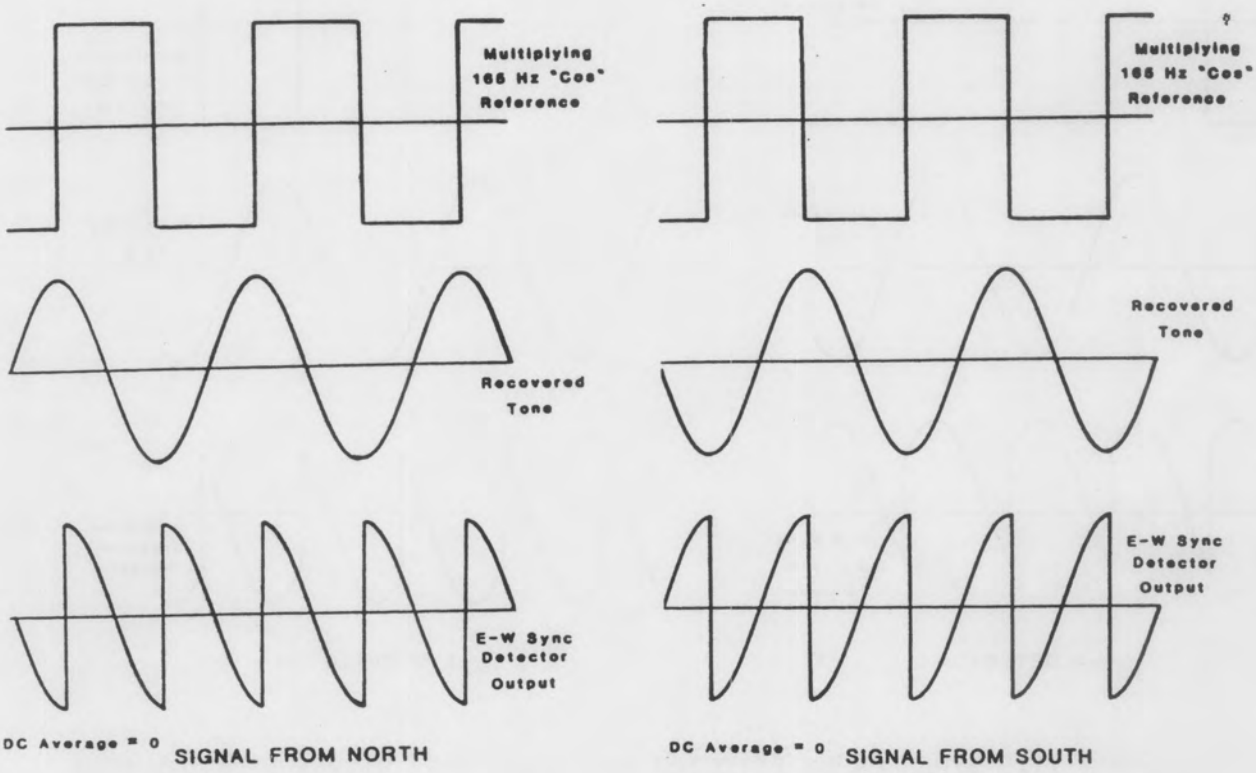


Figure 4-10. E-W SYNCHRONOUS DETECTOR WAVEFORMS

Note how these outputs average to zero. If the azimuth of the signal source changes to 90 degrees or 270 degrees (East or West), then the full wave rectified signal will be recovered from the E-W synchronous detector, with the N-S synchronous detector averaging zero. A signal source at 45 degrees results in partial dc outputs from both synchronous detectors as shown in Figure 4-11. The synchronous detector outputs are next integrated, chopped, and then applied to the CRT.

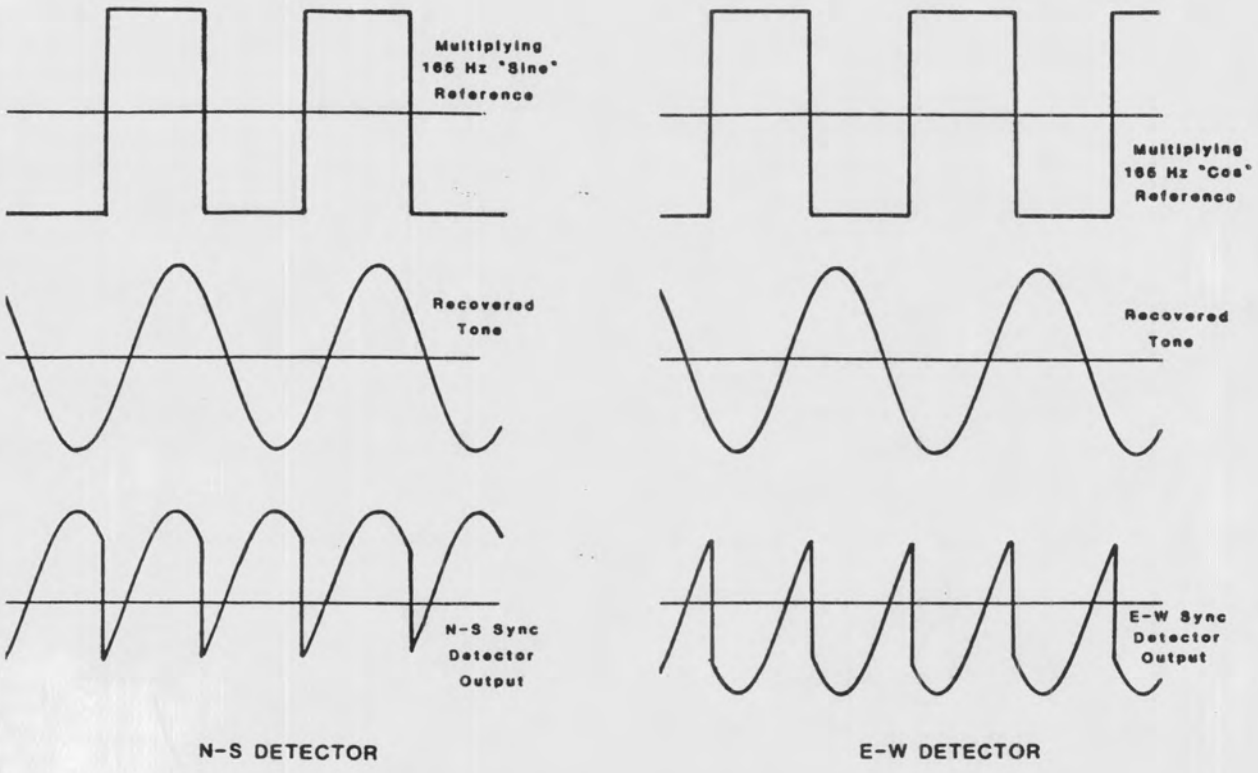


Figure 4-11. SYNCHRONOUS DETECTOR WAVEFORMS WITH SIGNAL RECEIVED FROM 45 DEGREES.

4.3 Electrical Description

See figure 4-12 for the following description. The RF signal (20 MHz to 520 MHz) is input to the RF Module (A1) from the antenna. The RF is a double sideband, suppressed carrier signal containing noise and any modulation imposed by the transmitter. The signal passes through one of eight preselector filters first, to decrease the noise-bandwidth. The filter is automatically selected in response to logic on the signal and power bus. This bus provides the control of functions in A1 and other receiver assemblies by the Data Processor, A7.

4.4 Mechanical Description

4.4.1 Chassis. For the most part, the assemblies consist of boards (A1-A7 and A14) that are plugged into the Power and Signal Bus Board (A8) on the bottom of the receiver chassis. The Video Amplifier Board (A12) is next to A8. Boards A9-A11 and A14 are mounted vertically and the Power Supply Board (A13) is mounted inside of a shielded module. The Panoramic Oscillator (A15) is mounted above A12. The assemblies are shown in figure 4-13.

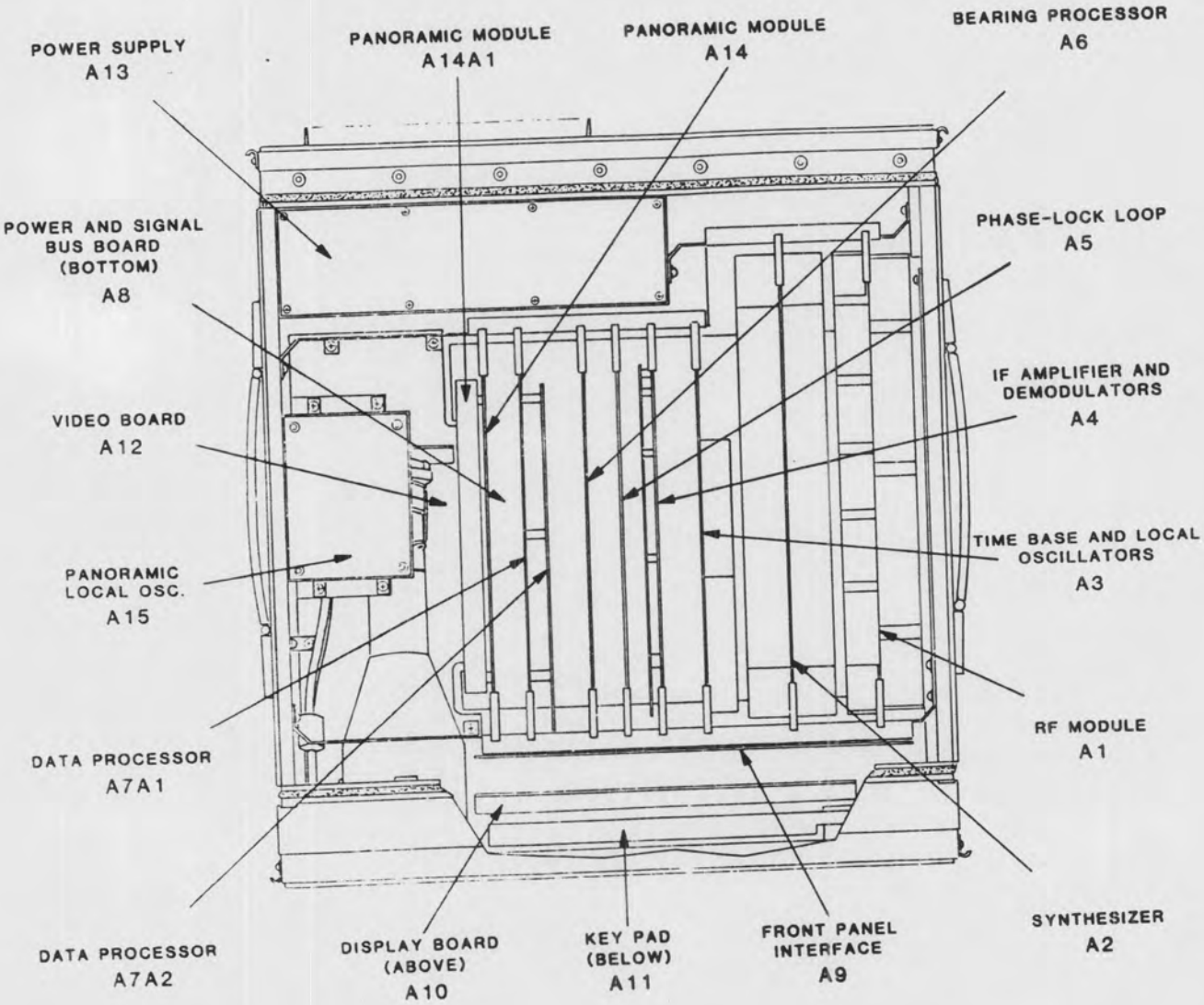


Figure 4-13. Assembly Location, Receiver

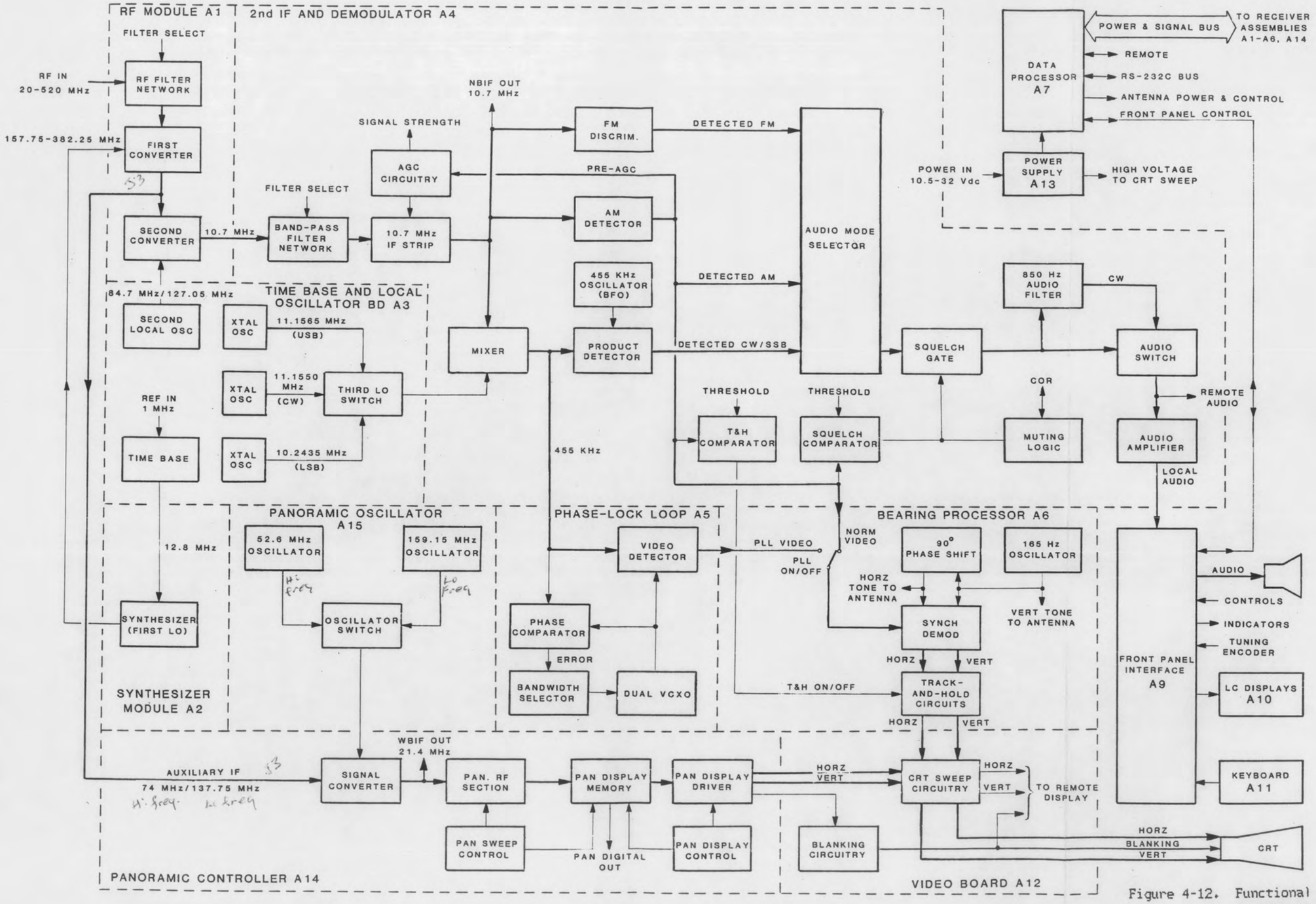


Figure 4-12. Functional Block Diagram, OAR3045 Receiver.

The filtered RF signal in A1 is next mixed with the first local oscillator (LO) signal, 157.75-382.25 MHz, from the Synthesizer A2, to obtain a 74 MHz or 137.75 MHz intermediate frequency (IF) output to the second converter. The converter switches from low injection to high injection mixing and back at each band in the toning range. The second LO output (84.7 MHz to 127.05 MHz) from the Time Base and Local Oscillator board, A3 is then mixed with the IF output to obtain a 10.7 MHz output to the IF Amplifier and Demodulator, A4.

The 10.7 MHz IF is filtered by one of four manually or automatically selected band-pass filters in A4. The bandwidth selected depends on the demodulation mode used. After IF amplification and output of the external 10.7 MHz narrowband IF (NBIF) signal; the signal is demodulated. One of six demodulation/bandwidth combinations below is automatically selected unless manually changed by the operator.

DETECTION MODE	FREQUENCY RANGE (MHz)				
	20-30	30-80	80-115	115-225	225-520
FM	6 kHz	30 kHz	200 kHz	13 kHz	30 kHz
AM	6 kHz	6 kHz	13 kHz	13 kHz	13 kHz
CW	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz
USB/LSB	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz

One of the four detected audio outputs is selected for input to the squelch gate, which opens or closes depending on several conditions. The gate opens, passing the audio when detected AM audio level exceeds an operator-controlled threshold level or by external mute or the carrier-operated relay (COR).

The detected audio for the selected mode is output to the remote audio jack for external devices. COR and remote muting are possible through this jack. Audio for the local speaker and headset jack are output to the front panel via the Signal and Power Bus, Data Processor (A7), and Front Panel Interface (A9). The detected AM audio includes the two antenna modulating tones (reference 165 Hz and phase-shifted 165 Hz) which are used for the video output. The same detected AM audio to the front panel is notch-filtered to remove these tones.

The 10.7 MHz IF from the IF strip output is also mixed with the third local oscillator frequency (approximately 11.155 MHz) to obtain a 455 kHz IF output to the Phase-Lock Loop (PLL), A5 and to the CW, USB, and LSB product detector. The third LO is automatically offset, approximately +1500 Hz for USB and LSB modes by control inputs from A7.

The Phase-Lock Loop is used to extend the AM threshold into the noise level in order to pick out weak signals in a high noise background. This is done by multiplying the 455 kHz input signal from A4 with another 455 kHz signal generated by one of two voltage controlled crystal oscillators (VCXO) to detect the AM video signal. To synchronize the 455 kHz L.O. to the received signal, the VCXO phase is compared with that of the signal in the receiver IF. An error voltage is developed that is proportional to the phase difference between the two signals. This error voltage increases or decreases the frequency of the VCXO so that the two remain in a phase-locked state. With the phase-locked loop locked, the VCXO frequency is continually changing to match any drift in the received frequency. One of two loop noise-bandwidths may be selected by the operator.

Either the direct video from A4 or the PLL video from A5 is selected in the

Bearing Processor (A6) for processing to provide horizontal (X) and vertical (Y) deflection outputs to the CRT. The horizontal and vertical output to the antenna consists of two 165 Hz tones 90 degrees out of phase. These tones are locked to a fixed reference vector (true north for example), and may be thought of as representing the SINE (horizontal) and COSINE (vertical) of this angle (0 degrees). These tones modulate the RF input in the antenna circuitry, and the X and Y tones are now shifted in phase to represent the SINE and COSINE of angle 0, the vectorial angle of the input bearing contained in the video input. The same tones are used to synchronously detect the bearing information as dc horizontal and vertical deflection voltages proportional to the inputs at the axial (N-S) and transverse (E-W) pairs of antenna elements. The deflection voltages may be sustained by the track-and-hold circuitry when the detected AM drops below the threshold level set in the T8H comparator on A4.

The Video Board (A12) uses the inputs to develop sweep voltages for the horizontal (90 degrees, 270 degrees) and vertical (0 degrees, 180 degrees) CRT deflection plates. The high voltage deflection outputs are zeroed (offset) by the front panel HORIZONTAL and VERTICAL controls.

The Antenna Interface circuitry (not shown) converts TTL logic (0 or +5V) to CMOS (0 or +10V) levels and vice-versa to permit communication between the antenna and the Data Processor (A7). In early models of the OAR3045 the antenna interface circuits were on a separate board. In later models they are located on the bearing processor board. The data processor board A7, controls most of the ADF receiving system functions using a central microprocessor. This is done by routinely monitoring all operator controls and displays. When any changes occur, the data processor determines and implements any internal changes, and updates the front panel display

accordingly.

The data processor provides interface to RTI, RS-232C and IEEE-488 systems. Serial data, and analog inputs and outputs interface with the receiver assemblies via the signal and power bus located on the Signal and Power Bus Board, A8. The bus also distributes low voltages (+15 Vdc, -15 Vdc and +8 Vdc) to each receiver assembly where they are regulated for use by individual circuits.

The Auxiliary IF input to the Panoramic (PAN) section is a wide-band, 74 MHz or 137.75 MHz signal from A1. The input to the PAN converter is mixed with 52.6 MHz or 159.15 MHz to obtain a 21.4 MHz IF for an external output and for input to the PAN receiver. In the PAN receiver the IF signal is converted to 10.7 MHz which is swept over one of nine selectable ranges by the PAN sweep control. The start of the frequency sweep is synchronized with the horizontal sweep of the CRT so that lower frequencies are displayed on the left of the CRT and higher frequencies on the right. The tuned or center frequency is centered on the CRT. The 10.7 MHz signal is next mixed with 10.245 MHz to obtain a 455 KHz signal which is then detected to output a quantized signal that is proportional to signal strength.

The signal level is stored in memory and output to the driver for vertical deflection of the CRT. During resweep, the center (tuned) frequency is zeroed by a pulse from a marker oscillator. Both the sweep and display controllers provide internal control of the panoramic display in response to commands from the data processor, A7.

The Front Panel Interface, A9 interfaces the Data Processor to the optical

tuning encoder, Keypad (A11), Liquid Crystal Display (LCD), (A10), and other front panel controls and indicators.

A detailed electrical description of all circuits is included in each tabbed section (A1-A15) of the 3045 Maintenance Manual. Receiver interconnections are shown in drawing 345-810.

Interconnection Diagram

345-810

to be furnished when completed.

Assembly drawings with component or sub-assemblylocations and the parts list are included in each tabbed section (A1-A14).

4.4.2 Interconnections. Receiver plugs and jacks are identified in figures 4-14 through 4-16. The companion tables list the coaxial (RF) and multi-conductor interconnections.

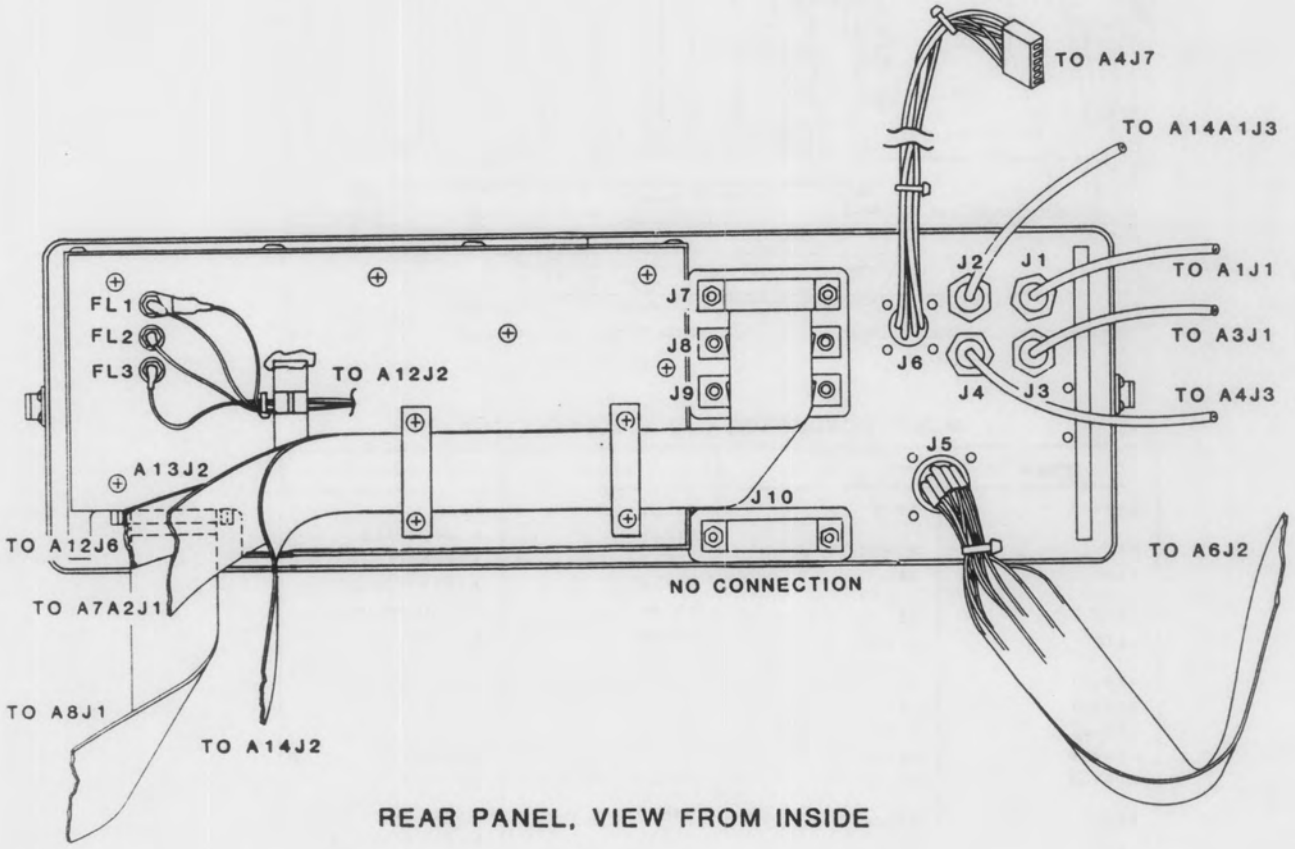
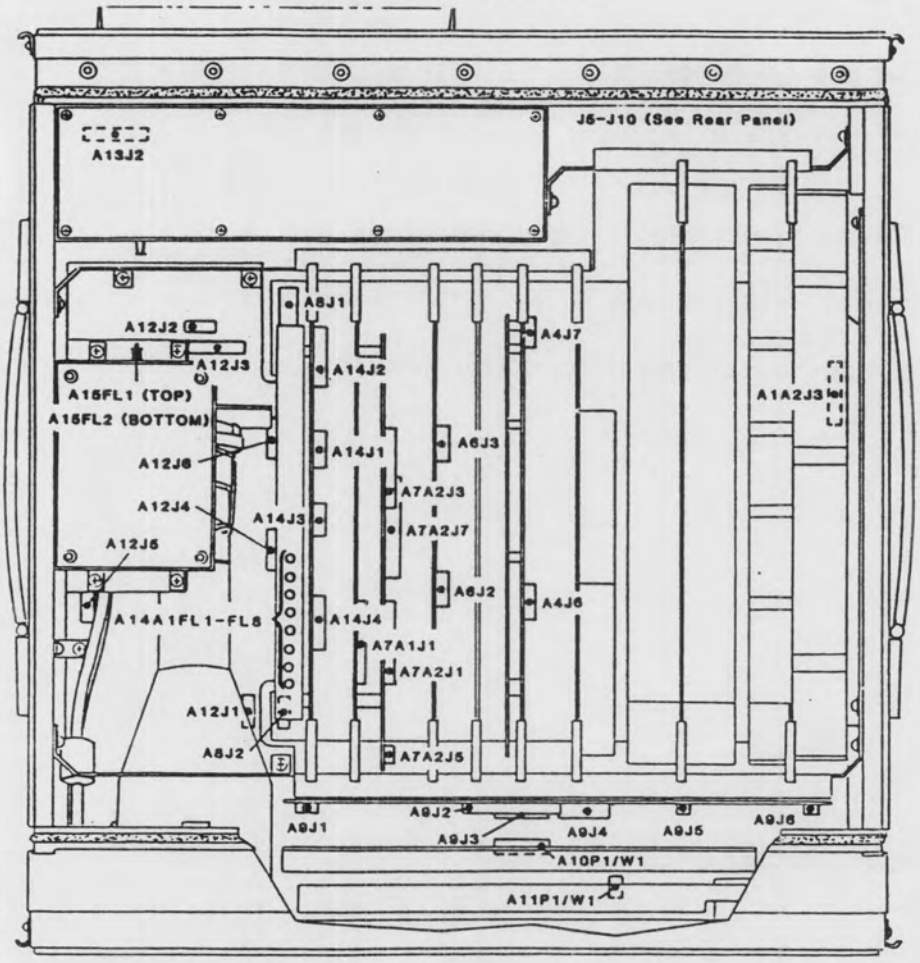


Figure 4-14. Rear Panel Connections

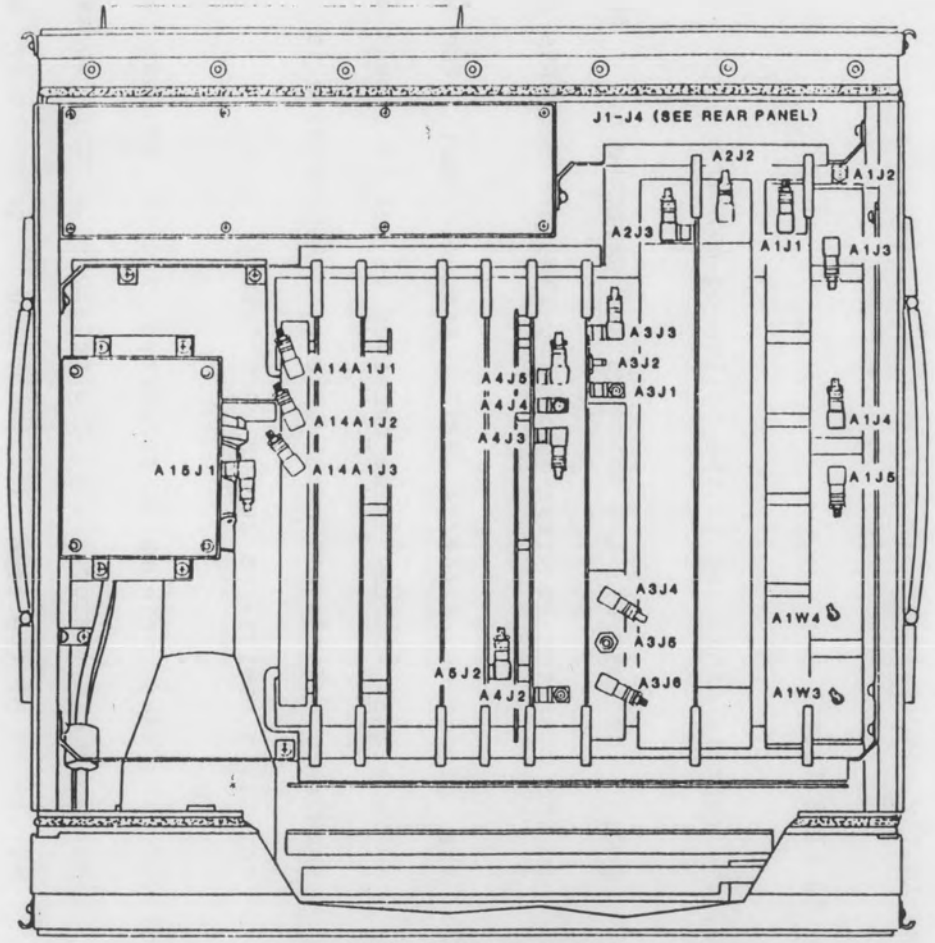
TOP VIEW, COVER REMOVED



MULTI-CONDUCTOR CABLE CONNECTIONS

FROM	TO	FROM	TO
A1A2J3	A4J6	A12J1	A8J2
A4J6	A1A2J3	A12J2	A13FL1-FL3
A4J7	J6	A12J3	A12A1W1
A6J2	J5	A12J4	A14J3
A6J3	A7A2J5	A12J5	F.P. HORIZ/VERT
A7A1J1	J7	A12J6	A14J1
A7A2J1	J8	A13J2	A8J1
A7A2J3	N/C	A13FL1-FL3	A12J2
A7A2J5	A6J3	A14J1	A12J6
A7A2J7	A9J1	A14J2	J9
A8J1	A13J2	A14J3	A12J4
A8J2	A12J1	A14J4	A14A1FL1-FL8
A9J1	A7A2J7	A14A1FL1-FL8	A14J4
A9J2	F.P. CONTROLS	A15FL1	A14A1FL1
A9J3	F.P. AUDIO	A15FL2	A14A1FL2
A9J4	A11J1/W1	J5	A6J2
A9J5	TUNING ENCODER	J6	A4J7
A9J6	A10P1/W1	J7	A7A1J1
A10P1/W1	A9J6	J8	A7A2J1
A11J1/W1	A9J4	J9	A14J2
		J10	NO CONNECTION

Figure 4-15. Multi-Conductor Connections.



TOP VIEW, COVER REMOVED

COAXIAL CABLE CONNECTIONS

FROM	TO	SIGNAL
A1J1	J1	ANTENNA RF IN
A1J2	A1W3	CONDITIONED FIRST LO
A1J3	A14A1J1	AUXILIARY IF
A1J4	A3J6	SECOND LO
A1J5	A4J2	10.7 MHz IF
A1W3	A1J2	CONDITIONED FIRST LO
A1W4	A2J2	FIRST LO
A2J2	A1W4	FIRST LO
A2J3	A3J3	12.8 MHz
A3J1	J3	REF IN (1 MHz)
A3J2	N/C	
A3J3	A2J3	12.8 MHz
A3J4	A4J4	THIRD LO
A3J5	N/C	
A3J6	A1J4	SECOND LO
A4J2	A1J5	10.7 MHz IF
A4J3	J4	NBIF (10.7 MHz)
A4J4	A3J4	THIRD LO
A4J5	A5J2	455 KHz IF
A5J2	A4J5	455 KHz IF
A14A1J1	A1J3	AUXILIARY IF
A14A1J2	A15J1	PAN LO
A14A1J3	J2	WBIF (21.4 MHz)
A15J1	A14A1J2	PAN LO
J1	A1J1	ANTENNA RF IN
J2	A14A1J3	WBIF (21.4 MHz)
J3	A3J1	REF IN (1 MHz)
J4	A4J3	NBIF (10.7 MHz)

Figure 4-16. Coaxial Cable Connections.

4.5 Troubleshooting

4.5.1 General

TROUBLESHOOTING AT THE OPERATOR LEVEL IS LIMITED TO LOCATING AND CORRECTING MALFUNCTIONS TO THE REMOVABLE BOARD LEVEL. The system has a built in test equipment (BITE) capability which executes tests automatically whenever power is initially turned on. The power-up BITE test determines whether the direction finder system main assemblies; the receiver, bearing processor, and antenna are functional. Failures (FAULTS) that appear on the BITE test list may be used as a guide in troubleshooting. However, BITE measurements are made at the ends of signal paths, and will not necessaily isolate failures to the module level.

4.5.2 Power On BITE Test

Briefly, the test is conducted in the following manner:

(1) During the test all LCD segments are switched on. It is up to the operator to visually verify that all segments are on.

(2) The direction finder's BITE harmonic oscillator is used as a signal source. The receiver is set to a sequence of frequency, bandwidth combinations. AGC voltage is tested against a nominal value for each case.

(3) If an OAR antenna is connected, and if it has a BITE harmonic oscillator, then the receiver is tuned to selected harmonics of the test oscillator and three tests are made at

each point - AGC, bearing, and x, y voltage magnitude (trace length).

Each measurement is associated with a unique failure code. While the test is running, the codes of any measurements that fail to meet the predicted nominal range are recorded, but the test is not interrupted.

After the test has terminated, if any failures were detected, a flashing decimal point in the 7-digit frequency display will flash, and warn the operator of a power-on BITE failure. This will persist, but in no way interferes with equipment operation. Fault codes are displayed using numbered function 88. A table keyed to the codes is used to look up the associated measurement information, which can be used as a troubleshooting aid.

Frequency (MHz)	IF Filter Bandwith (KHz)	Preselector Filter Range (MHz)	AGC Nominal Value (minimum)	Fault Code
20	6	20-32	5	1
20	13	20-32	5	2
20	30	20-32	5	3
20	200	20-32	5	4
40	200	32-51	5	5
70	200	51-83	5	6
110	200	83-115	5	7
140	6	115-175	5	8
140	13	115-175	5	9
140	30	115-175	5	10
140	200	115-175	5	11
230	200	175-279	5	12

Table 4-1. OAR3045 RECEIVER SENSITIVITY TEST

RECEIVER SENSITIVITY TEST. The BITE harmonic oscillator, located in the preselector, is switched on, which injects a test signal directly

ahead of the bandpass filters. A software controlled measurement sequence is executed, which tests the preselector and IF filters at the two IF frequencies (74 MHz and 137.95 MHz) the sequence is listed in Table 4-1, along with the FAULT codes.

ANTENNA TEST The BITE antenna test is only run if a 285E antenna containing a BITE oscillator is connected to the equipment.

A 0.640 MHz BITE harmonic oscillator is switched on in the antenna and three measurements are made at each test frequency: AGC, X, Y voltage magnitude, and bearing.

The AGC measurement verifies the R.F. signal path from the input of the sense element to the receiver. During this test the encoding tones are switched off.

The X, Y voltage magnitude is measured at the output of the bearing processor with the encoding tones switched on. Either X and Y is selected for comparison (whichever is greater). The encoding tones modulate the test oscillator signal; X, Y voltages are a function of the percent modulation. This tests the antenna and receiver signal processing circuitry.

The bearing test verifies that BOTH X and Y signal paths in the antenna and bearing processor are functional.

The antenna test sequences are as listed in Table 4-2. The FAULT codes are listed in the order they appear in the test sequence.

EXAMPLE: AGC VALUE (16), BEARING RANGE (17), X/Y VOLTAGE (18).

Frequency (MHz)	Min. AGC Value	Bearing Range	X, Y Voltage Magnitude	Fault Codes
1.28	122	25..65	25	16,17,18
3.84	105	25..65	48	19,20,21
7.04	94	102..250	40	22,23,24
16.0	76	220..260	34	25,26,27
26.24	68	230..290	26	28,29,30

Table 4-2. AFL 285E ANTENNA TEST

4.5.3 BITE Related Numbered Functions

Additional BITE related capabilities are programmed into the equipment through the use of numbered functions. These functions are listed below to provide an aid to troubleshooting the equipment:

(1) POWER ON BITE MEASUREMENTS PRINTOUT ON/OFF (Function 86)

Power on BITE information is available through the I/O data part through use of an external printer. If this feature is enabled, every BITE test measurement is reported. Numbered function 86 toggles the printout option on or off. The selected state of this switch will persist until changed again with function 86.

Since the BITE measurement interval is relatively brief compared to the time required to send a character oriented message, and no more than one message is buffered in the output stream, a device with an effective throughput of 4800 baud is required to receive these messages. Practically, this means your receiving device must be capable of buffering at least 1000 characters of data at 4800 baud.

Two ASCII message types are currently sent:

(a) Receiver Sensitivity Test Message

DATE, TIME, FREQUENCY, AGC, DEMODULATION MODE, BANDWIDTH

(B) Antenna Test Message

DATE, TIME, FREQUENCY, AGC, BEARING, X,Y VOLTAGE MAGNITUDE, DEMODULATION MODE, BANDWIDTH

The format and range specifications for data fields are as follows:

Date: YYMMDD

Time: HHMMSS

Frequency: MHz, 10 Hz resolution, leading zeros not supressed

AGC: 0..255

Bearing: 0..359, padded with spaces if no bearing

X,Y Voltage Magnitude: 0..511

Demodulation Mode: AM, FM, CW, USB, LSB

Bandwidth: 2.5K, 6K, 13K, 30K, 200K

Data fields are delimited with a comma and messages are terminated with a carriage return/line feed combination.

(2) EXECUTE POWER ON BITE (FUNCTION 87)

Function 87 allows the operator to conduct a power on BITE test without turning the equipment power off and on. When function 87 is activated it immediately causes execution of the power-on BITE test. This will clear any fault codes stored from a previous test. Fault codes resulting from the current test will be stored. Measurements will be printed out if this feature is

enabled.

(3) DISPLAY POWER ON BITE CODES (FUNCTION 88)

Numbered FAULT codes are stored on a list during power-on BITE for each test that failed. When function 88 is invoked, this list can be displayed one item at a time on LCD2. Four keys are used to move through the list. A blank display means there are no fault codes.

Displays the failure code at the beginning of the list.

Displays the failure code at the end of the list.

Displays the next failure code on the list (wraps at end to the beginning).

Displays the previous failure code on the list (wraps at the beginning to the end).

Pressing the CLR Key clears out of this function.

(4) ANTENNA BITE GENERATOR ON/OFF (Function 94, 95)
RECEIVER BITE GENERATOR ON/OFF (Function 96, 97)

The BITE generator ON/OFF functions may be used to provide a test signal for system troubleshooting. The receiver BITE generator can be turned ON by activating function 96, and OFF by activating function 97. If an AFL285 antenna with a BITE generator is attached function 94 turns the antenna BITE generator ON, and

function 95 turns it OFF. These functions operate independantly of and are unrelated to the power on BITE test.

4.5.4 Board Level Replacement

To replace boards in the receiver, the twenty-three 1/8 inch screws in the top cover must be loosened, and the cover removed. The boards in the receiver are identified in figure 4-13.

The synthesizer (A2) and time base (A3) boards have LED fault indicators located at the top of each board. If either LED is illuminated, the board is probably defective and may be replaced. To replace any receiver board, follow the procedures below:

(a) Turn off the receiver

(b) Unplug all connectors on the defective board.

(c) Lift the latches at each end of the board and remove the board by lifting, straight-up.

(d) Install replacement board by following the above steps in reverse order.

CAUTION

When installing boards, care should be taken to ensure the board is properly aligned, and insertion should not be forced. Improper alignment can cause pin damage.

Repairs beyond this level should be accomplished by a trained technician.

WARNING

Dangerous voltages exist in the equipment, and may be fatal if contacted. Do not reach into the equipment if the power is on and the top cover removed.

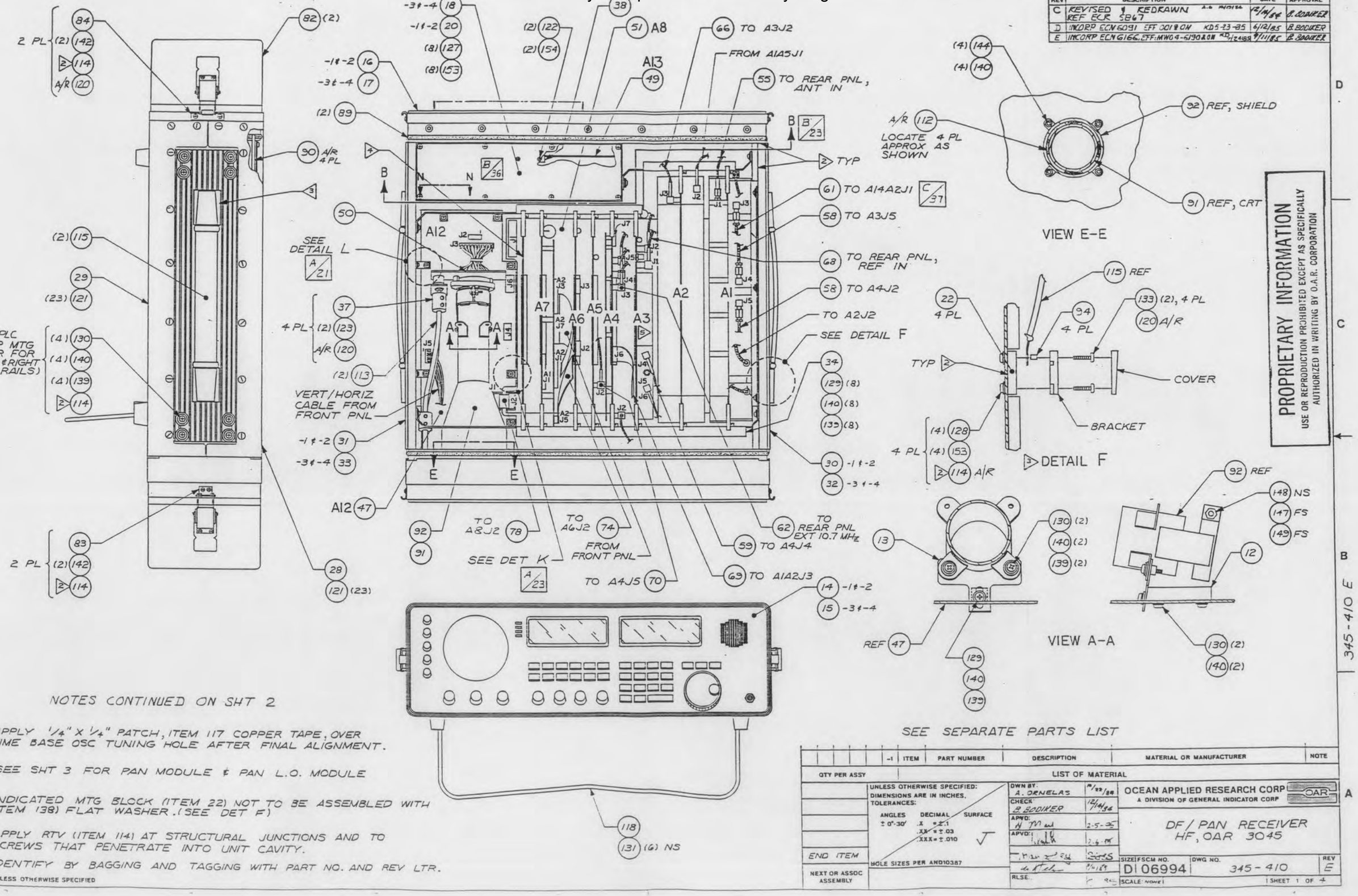
APPLICABLE DRAWINGS

REF DESIG	ASSEMBLY	ASSY DRAWING AND PARTS LIST	SCHEMATIC DRAWING
	3045 Receiver	345-410-4	
	Interconnect Diagram		345-810
A1	RF Module	7100422-1	7100822-1
	Second Converter	7100327-1	7100527-1
	First Converter	7100328-1	7100528-1
	Data Receiver	7100329-1	7100529-1
	RF Filter Network	7100330-1	7100530-1
	Synthesizer Filter	7100343-1	7100543-1
A2	Synthesizer Module	7100418-1	7100818-1
	Synthesizer Sub Loop	7100304-1	7100504-1
	Synthesizer Main Loop	7100305-1	7100505-1
	Carrier Board, Synthesizer	7100306-1	7100818-1
	Main Loop VCO/ Low Band	7100308-1	7100819-1
	Main Loop VCO/ High Band	7100308-2	7100819-2
	VCO Module / Switched Range	7100309-1	7100805-1
	VCO Module / Low Band	7100419-1	7100819-1
	VCO Module / High Band	7100419-2	7100819-2
	Voltage Regulator	7100421-1	
A3	Time Base Module	7100429-2	7100829-2
	Time Base Circuit Board	7100307-1	7100507-1
	Third Local Oscillator	7100311-2	7100511-2
	Second Local Oscillator	7100320-1	7100520-1
A4	IF Amplifier & Demodulator	7100316-2	7100516-2
	Filter Board, 200KHz	7100319-1	7100519-1
A5	Phase Lock Loop	7100346-1	7100546-1
A6	Bearing Processor	7100344-1	7100544-1
A7	Data Processor Module	7100406-1	7100806-1
	Data Processor Board A	7100312-1	7100512-1
	Data Processor Board B	7100313-1	7100513-1
	Channel Memory Module	7100432-1	7100832-1
	Channel Memory Circuit Board	7100342-1	7100832-1
A8	Power and Signal Bus Board	7100324-1	7100524-1
A9	Front Panel Interface	7100400-1	7100800-4
	Circuit Board	7100315-1	7100515-1
	Analog Cable	7100464-1	7100522-1
A10	Front Panel Display	7100314-1	7100514-1

APPLICABLE DRAWINGS

REF DESIG	ASSEMBLY	ASSY DRAWING AND PARTS LIST	SCHEMATIC DRAWING
A11	Key Pad	7100403-1	
A12	Video Amplifier	7100303-1	7100503-1
	CRT Cable	7100323-1	7100523-1
A13	Power Supply DC to DC Converter	7100301-1	7100501-1
A14	Panoramic Display Module	7100440-2	7100840-2
	Controller Board	7100347-1	7100547-1
	RF Module	7100449-1	7100849-1
	Converter Board	7100353-1	7100553-1
	RF Board	7100350-1	7100550-1
A15	Panoramic Local Oscillator	7100448-1	7100848-1
	Pan LO Circuit Board	7100349-1	7100549-1
	MA 396E Monopole Antenna Interconnect Diagram	396-400-2	396-552
A1	VHF Antenna Board	396-302-1	396-502-1
A2	UHF Antenna	386-301-4	386-501-4
A3	Antenna Controller Board	285-306-2	285-506-2
A4	RF And Power Switch Board	396-300-1	396-500-1
A5	BYTE Generator Board	396-307-1	396-507-1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
C	REVISED & REDRAWN A.O. PHOTOS REF ECR 5867	12/14/84	R. BOOKER
D	INCORP ECN 6091 EFF 3018 ON KDS-23-85	6/12/85	R. BOOKER
E	INCORP ECN 6166. EFF: MW04-6190 & ON KD/12489	9/11/85	R. BOOKER



NOTES CONTINUED ON SHT 2

5. APPLY 1/4" X 1/4" PATCH, ITEM 117 COPPER TAPE, OVER TIME BASE OSC TUNING HOLE AFTER FINAL ALIGNMENT.

4. SEE SHT 3 FOR PAN MODULE & PAN L.O. MODULE

3. INDICATED MTG BLOCK (ITEM 22) NOT TO BE ASSEMBLED WITH (ITEM 138) FLAT WASHER. (SEE DET F)

2. APPLY RTV (ITEM 114) AT STRUCTURAL JUNCTIONS AND TO SCREWS THAT PENETRATE INTO UNIT CAVITY.

1. IDENTIFY BY BAGGING AND TAGGING WITH PART NO. AND REV LTR.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X ±.1, .XX ±.03, .XXX ±.010 SURFACE √

HOLE SIZES PER AND10387

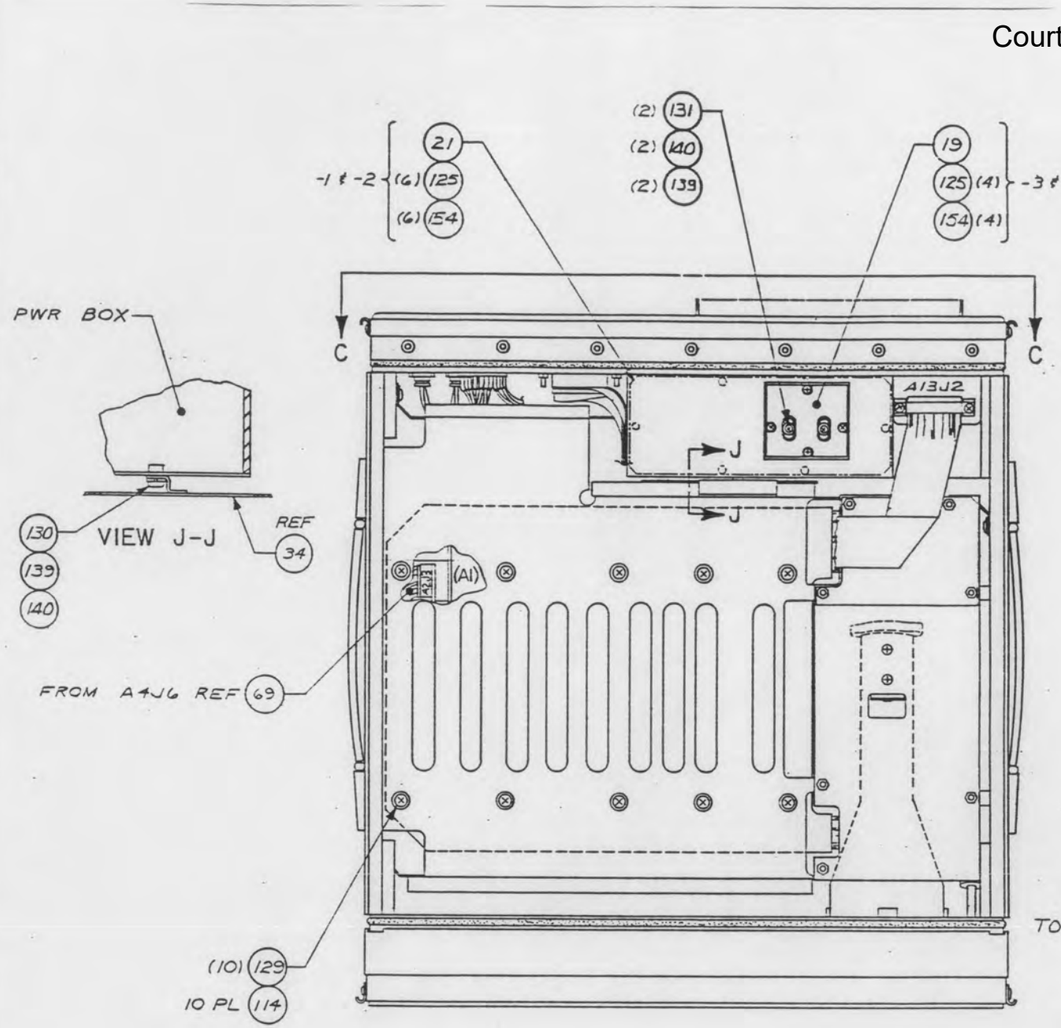
END ITEM

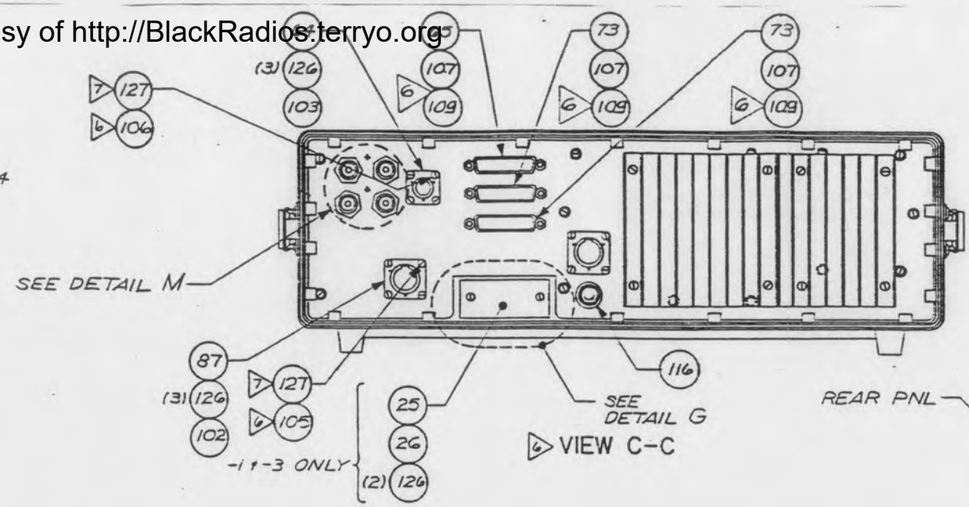
NEXT OR ASSOC ASSEMBLY

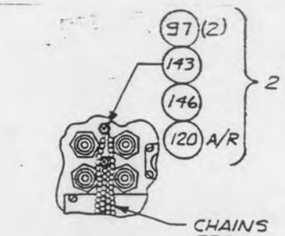
DWN BY: A. ORNELAS	11/22/84	OCEAN APPLIED RESEARCH CORP (OAR) A DIVISION OF GENERAL INDICATOR CORP
CHECK: B. BOOKER	12/14/84	DF / PAN RECEIVER HF, OAR 3045
APVD: N. [illegible]	2-5-85	
APVD: [illegible]	2-6-85	
[illegible]	2-6-85	SIZE D | FSCM NO. 06994 | DWG NO. 345-410 | REV E
[illegible]	3/4/85	SCALE: NONE | SHEET 1 OF 4
RLSE	[illegible]	

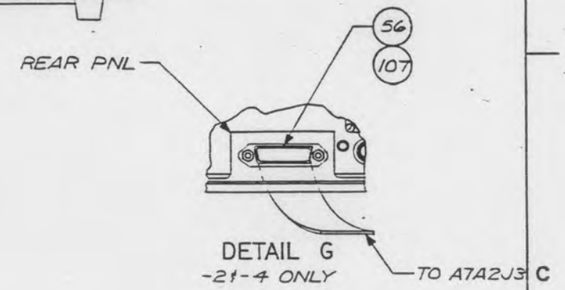
PROPRIETARY INFORMATION
USE OR REPRODUCTION PROHIBITED EXCEPT AS SPECIFICALLY AUTHORIZED IN WRITING BY O.A.R. CORPORATION

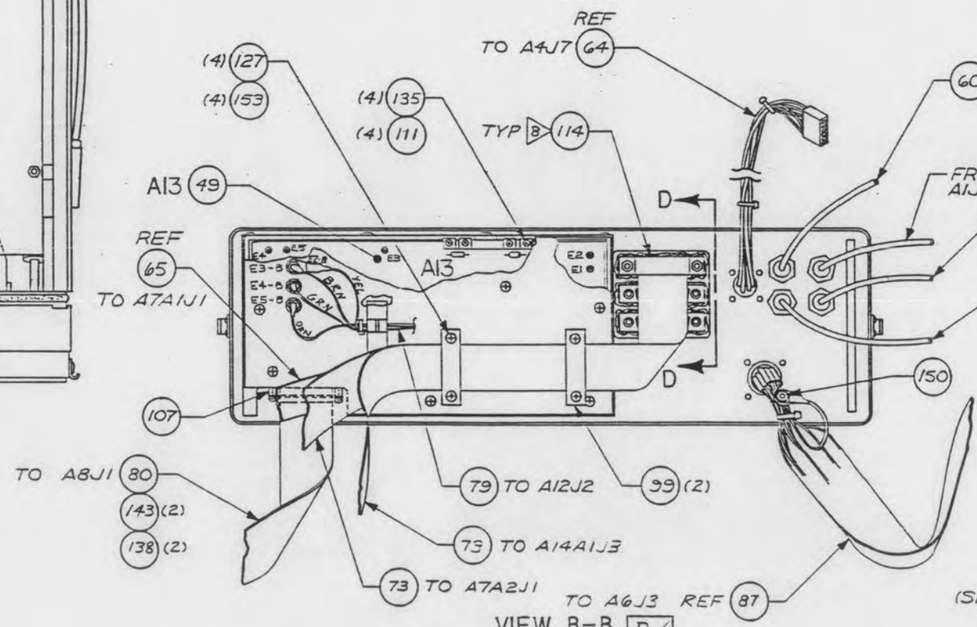
345-410 E

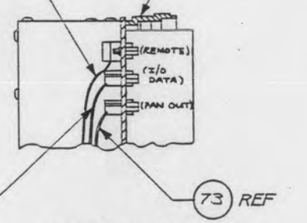


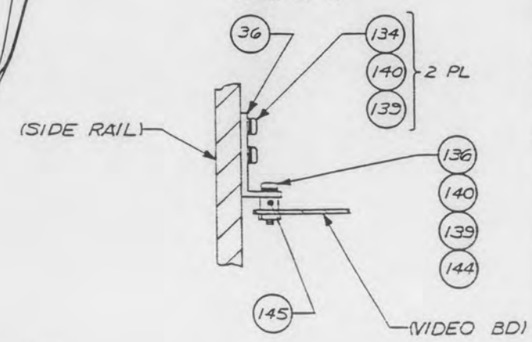


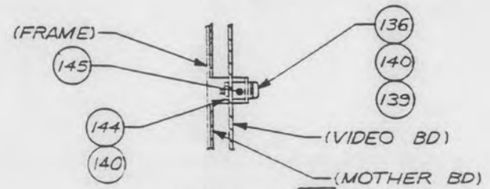












DETAIL K C/5

TYP MTG OF VIDEO BD TO FRAME - 5 PL

DETAIL L C/6

TYP 2 PL

8 USE (ITEM 114) RTV TO SEAL INDICATED AREA.

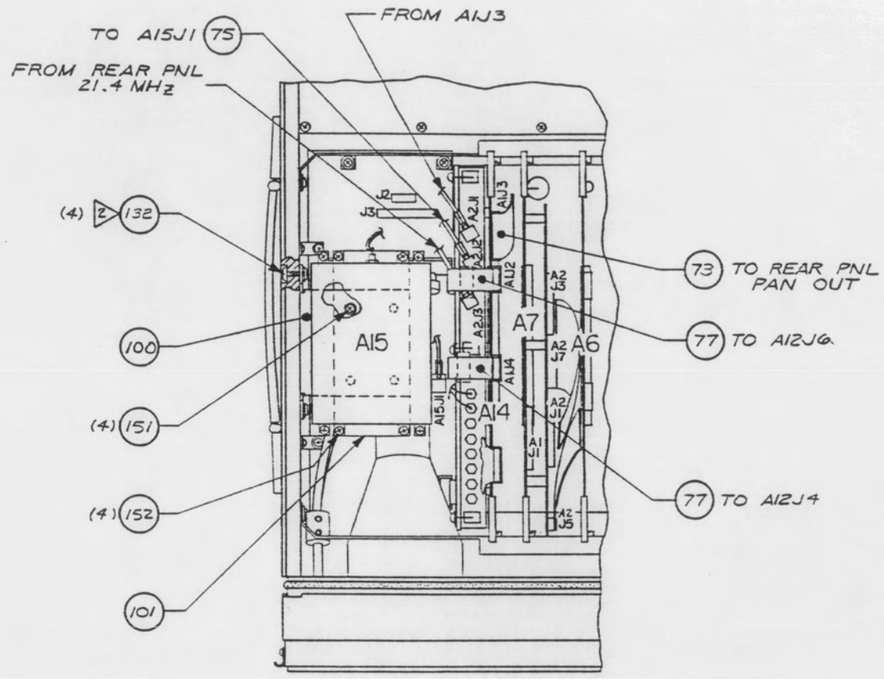
7 USE INDICATED SCREW TO ATTACH CONNECTOR COVER CHAIN. APPLY RTV (ITEM 114) TO SCREW THREADS PRIOR TO ASSY.

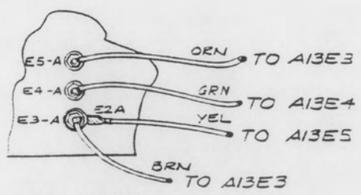
6 AT VIEW C-C, ITEM 105 AND 106 CAP PTCZ; ITEM 97 CAP BNC; ITEM 81 PWR CORD; ITEM 109 CAP ARE NOT SHOWN FOR CLARITY.

NOTES: (CONTINUED FROM SH 1 A/6)

SIZE	FSCM NO.	DWG NO.	REV
D	06994	345-410	E
SCALE: NONE		SHEET 2	

345-410 E

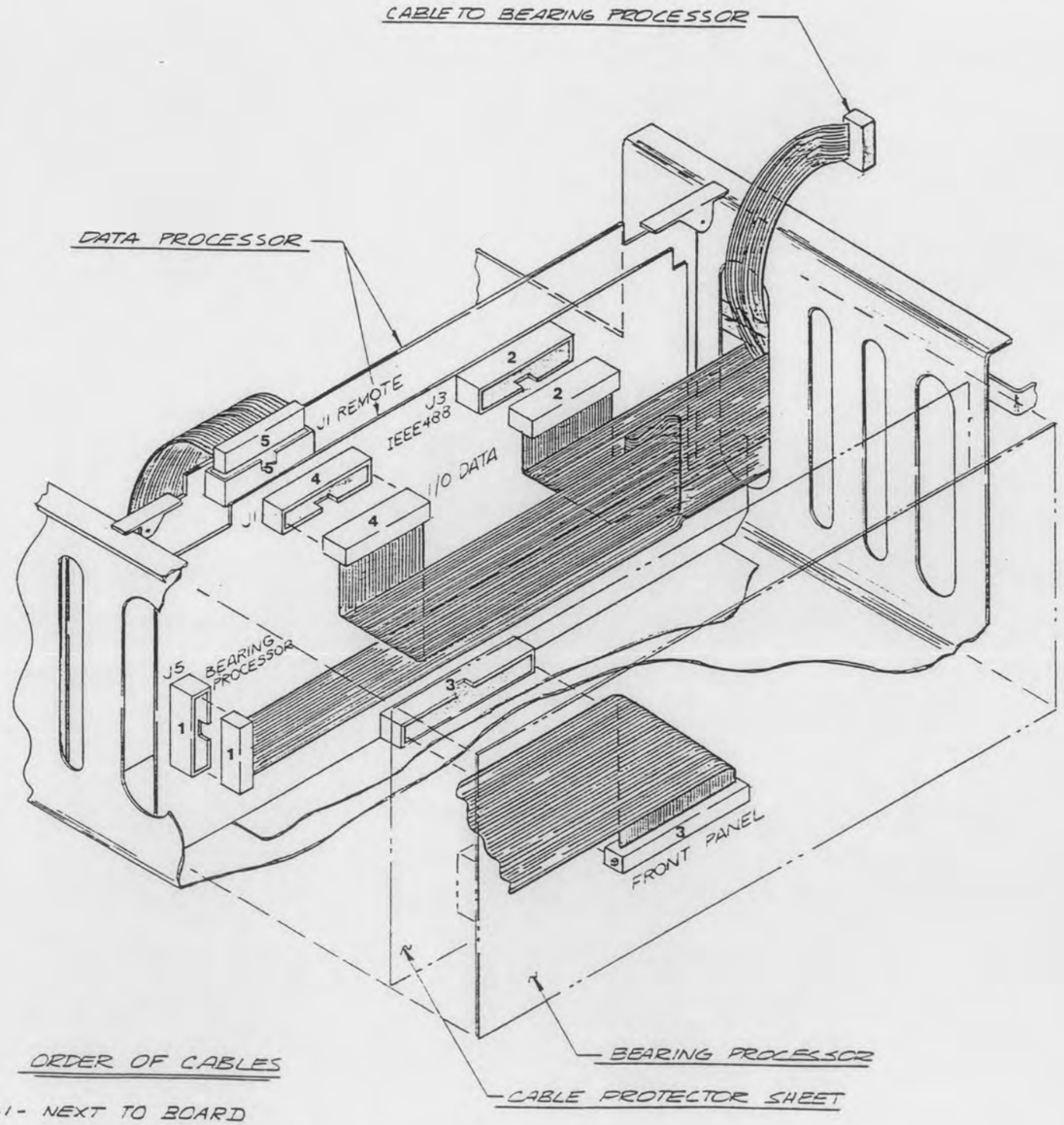




VIEW N-N

SIZE	FSCM NO.	DWG NO.	REV
D	06994	345-410	E
SCALE: NONE		SHEET 3	

345-410 E



ORDER OF CABLES

#1 - NEXT TO BOARD
#2 BETWEEN CABLE #1 & #3
#3 BETWEEN CABLE #3 & #4
#4 - OUTSIDE

REMOVE DATA PROCESSOR:

1. REMOVE BEARING PROCESSOR AS FOLLOWS:
   A. EJECT BEARING PROCESSOR APPROX 1.0".
   B. DISCONNECT CABLE FROM BEARING PROCESSOR & ROUTE IT STRAIGHT UP TO CLEAR BEARING PROCESSOR.
   C. REMOVE BEARING PROCESSOR WHILE CABLE PROTECTOR REMAINS IN PLACE.
2. REMOVE CABLE PROTECTOR:
3. REMOVE DATA PROCESSOR AS FOLLOWS:
   A. DISCONNECT CABLES #2, #4, & #5 FROM CONNECTORS
   B. EJECT DATA PROCESSOR FAR ENOUGH TO GET TO CONNECTOR FROM CABLE #1 & DISCONNECT IT.
   C. EJECT DATA PROCESSOR FAR ENOUGH TO GET TO CONNECTOR FOR CABLE #3 & DISCONNECT IT.
   D. REMOVE DATA PROCESSOR FROM CHASSIS.

IN BOTH OF THESE STEPS PULL THE CABLES AWAY FROM THE BOARD WHERE THEY ARE ROUTED THRU THE CARD CAGE TO AVOID SNAGGING THEM ON THE COMPONENTS ON THE DATA PROC.

NOTE: DO NOT LAY DATA PROCESSOR ON A METAL SURFACE DUE TO BATTERY MAY BE SHORTED OUT, CAUSING LOSS OF CALIBRATION CONSTANTS & POSSIBLY BATTERY OVERHEATING.

DATA PROCESSOR INSTALLATION

1. MAKE SURE BEARING PROCESSOR & CABLE PROTECTOR SHEET ARE REMOVED FROM RADIO.
2. START REAR DATA PROCESSOR BOARD INTO CARD GUIDE.
3. MAKE SURE CABLES EXITING FROM CARD CAGE CLEAR THE COMPONENTS, OR THE DATA PROCESSOR, IN ALL STEPS TO FOLLOW.
4. INSERT DATA PROCESSOR INTO CARD CAGE FAR ENOUGH TO CONNECT CABLE #3, THEN CONNECT CABLE #3.
5. INSERT DATA PROCESSOR FAR ENOUGH TO CONNECT CABLE #1.
6. ROUTE CABLE #1 BETWEEN THE BOARD & CABLE #3, THEN CONNECT CABLE #1.
7. FINISH INSERTING DATA PROCESSOR WHILE MAKING SURE CABLES DO NOT SNAG ON COMPONENTS.
8. IF THIS RADIO CONTAINS CABLE #2 (IEEE-488 INTERFACE CABLE) MATE ITS CONNECTOR & ROUTE IT OUTSIDE CABLE #1 WITH FOLD APPROX WHERE SHOWN.
9. ROUTE CABLE #4 OUTSIDE CABLE #3 & MATE ITS CONNECTOR WITH THE BOARD CONNECTOR. FOLD CABLE #4 APPROX WHERE SHOWN SO IT LAYS FLAT.
10. ARRANGE THE CABLES SO THEY LAY AS FLAT AS POSSIBLE AGAINST THE DATA PROCESSOR. CABLE #1 MAY NEED A 5.0" BEND APPROX WHERE SHOWN TO TAKE UP ITS EXTRA LENGTH.
11. LAY THE CABLE PROTECTOR SHEET AGAINST THE CABLES WITH ITS BOTTOM EDGE ON THE DATA PROCESSOR SIDE OF THE BEARING PROCESSOR CONNECTOR, THEN WHILE HOLDING ITS TOP EDGE AGAINST THE CABLES, INSTALL THE BEAR PROCESSOR UNTIL IT IS APPROX 1.0" FROM BEING SEATED.
12. CONNECT THE BEARING PROCESSOR CABLE TO THE BEARING PROCESSOR & SEAT THE BEARING PROCESSOR IN ITS CONNECTOR.

INSTALLATION IS COMPLETED

SIZE	FSCM NO.	DWG NO.	REV
D	06994	345-410	E
SCALE: NONE		SHEET 1	

345-410 E

OCEAN APPLIED
ESEARCH CORPORATION
San Diego, Cal. 92121

REL	
APPVD D. May	DATE 2-5-84
CHECK B. BODIKER	DATE 12/11/84
DRAWN A. ORNELAS	DATE 10/27/84

DF/PAN RCVR
VHF/UHF
OAR 3045

345-[illegible]10
SHEET 1 OF 8 REV E
MWO

NUFACTURING WORK ORDER NO.	NEXT ASSY	FINAL			
Y REQUIRED THIS RELEASE	FINAL ASSY				
LEASE DATE MTL REQD					
TAL PARTS COST THIS RELEASE					

	DESCRIPTION		APPVD	DATE
	D.D.C. : ADDED PAN MODULES AND ASSOC HARDWARE, NEW BRG PROC. (UPDATED TO MOST CURRENT CONFIG.)	A.O. 10/22/84	B. BODIKER	12/11/84
	INCORP ECN 6091, EFF: 001 & ON	KD 5-23-85	B. BODIKER	6/12/85
	INCORP ECN 6166, EFF: MWO 4-6190 & ON	KD 7-24-85	B. BODIKER	9/11/85
	TITLE WAS DF/PAN RCVR HF, OAR 3045 ECR 6259	9-1-85	L. CHAVEZ	11/1/85

345-410
SH 3 OF E

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
7101019-1	PLATE IEEE 488 PATTERN		1	-	1	-						
7101021-1	GASKET IEEE PATTERN		1	-	1	-						
7100007-1	COVER, TOP		1	1	1	1						
7100007-2	COVER, BOT		1	1	1	1						
7101003-1	SIDE RAIL		1	1	-	-						
7101003-2	SIDE RAIL		1	1	-	-						
7101004-1	SIDE RAIL		-	-	1	1						
7101004-2	SIDE RAIL		-	-	1	1						
7100024-1	FRAME		1	1	1	1						
7101012-1	BRACKET		2	2	2	2						
7101005-1	COUPLER		4	4	4	4						
7101030-1	CLIP		1	1	1	1						
7100422-1	RF MODULE		1	1	1	1						A1
7100418-1	SYNTHESIZER		1	1	1	1						A2
7100429-2	TIME BASE		1	1	1	1						A3
7100316-2	IF AMPL & DEMODULATOR		1	1	1	1						A4
7100346-1	PLL		1	1	1	1						A5
7100344-1	BRG PROC II		1	1	1	1						A6

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
-1	RCVR		X									PROD STD
-2	RCVR			X								PROD IEEE-488
-3	RCVR				X							PRE-PROD STD
-4	RCVR					X						PRE-PROD IEEE-488
345-810	DIAGRAM		REF	REF	REF	REF						
345-600	WIRE/CABLE LIST		REF	REF	REF	REF						
345-900	ACCEPTANCE TEST PROCEDURE		REF	REF	REF	REF						
345-901	PRE-ACCEPTANCE TEST PROCEDURE		REF	REF	REF	REF						
7100084-1	BLOCK, CRT MTG		1	1	1	1						
7100085-1	BRKT, CRT MTG		1	1	1	1						
7100400-3	FRONT PNL		1	1	-	-						
7100400-4	FRONT PNL		-	-	1	1						
7100095-1	REAR PNL		1	1	-	-						
7100083-1	REAR PNL		-	-	1	1						
7100099-1	COVER, TOP - PWR SUPPLY		-	-	1	1						
7101001-1	COVER, HEATSINK PWR SUPPLY		-	-	1	1						
7100008-1	COVER, TOP PWR SUPPLY		1	1	-	-						
7100009-1	COVER, BOTTOM PWR SUPPLY		1	1	-	-						
7100056-1	MTG BLOCK, HANDLE		4	4	4	4						

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
7100406-1	DATA PROC		1	1	1	1						A7
7100448-1	PAN L.O. ASSY		1	1	1	1						A15
7100303-1	VIDEO BD		1	1	1	1						A12
7100440-2	PAN MODULE		1	1	1	1						A14
7100301-1	PWM / DC-DC CONVERTER		1	1	1	1						A13
7100323-1	CRT CABLE BD		1	1	1	1						
7100324-1	MOTHER BD		1	1	1	1						A8
7100413-4	CABLE (RF INPUT)		1	1	1	1						
7100411-1	CABLE (IEEE-488)		-	1	-	1						
7100414-2	CABLE (2ND L.O.)		2	2	2	2						
7100414-3	CABLE (3RD L.O.)		1	1	1	1						
7100413-1	CABLE (EXT WB IF)		1	1	1	1						
7100414-4	CABLE (PAN RF)		1	1	1	1						
7100413-2	CABLE (EXT I.F. 10.7 MHz)		1	1	1	1						
7100410-1	CABLE (EXT AUDIO)		1	1	1	1						
7100407-3	CABLE (REMOTE)		1	1	1	1						
7100414-6	CABLE (SYNTH TIME BASE)		1	1	1	1						

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
7100413-3	CABLE (EXT REF)		1	1	1	1						
7100409-1	CABLE (RF CONTROL)		1	1	1	1						
7100414-8	CABLE (455 KHz)		1	1	1	1						
7100408-4	CABLE (IO/DATA, PAN OUT)		2	2	2	2						
7100455-1	CABLE, SEMI-RIGID COAX (PAN L.O.)		1	1	1	1						
7100409-5	CABLE DATA (PAN PROC DATA)		1	1	1	1						
7100409-3	CABLE (PAN VIDEO DATA)		2	2	2	2						
7100409-4	CABLE (VIDEO PWR)		1	1	1	1						
7100415-1	CABLE (HI VOLTAGE)		1	1	1	1						
7100408-1	CABLE (POWER SUPPLY)		1	1	1	1						
7100442-1	DC PWR CORD		1	1	1	1						
7100446-1	COVER, TRNST		2	2	2	2						
7101038-2	STRIKER, LATCH		2	2	2	2						
7101039-1	STRIKER, LATCH		2	2	2	2						
7100456-1	IDC TO CIRCULAR (ANT CONT)		1	1	1	1						

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SH 6 OF E

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
2-279-C557-70	O-RING	PARKER	2	2	2	2						
.139 CROSS SECTION C557-70	MOLDED CORD STOCK	PARKER	A/R	A/R	A/R	A/R						
S208P1	CRT	B-SCAN	1	1	1	1						
C-270-B-C	SHIELD	AMUNEAL.	1	1	1	1						
1457A	SPACER	KEYSTONE	4	4	4	4						
M39012/25-0015 31-3027	CAP, BNC	QPL OR AMPHENOL	4	4	4	4						
7101065-1	STRIP, RETAINER	M/F .060 FIBERGLASS	2	2	2	2						
7101057-1	MTG BKT PAN LOCAL OSC		1	1	1	1						
7101058-1	MTG PLATE PAN LOCAL OSC		1	1	1	1						
10-40450-14	GASKET	BENDIX	1	1	1	1						
10-40450-10	GASKET	BENDIX	1	1	1	1						
10-101960-14-3	CAP, PTOZ	BENDIX	1	1	1	1						
10-101960-10-3	CAP, PTOZ	BENDIX	1	1	1	1						
D ZD418-2	SET OF 2 JACKPOSTS	CANNON	4	4	4	4						MIL NO. MZ4308/26-1
DB60-	CAP	CANNON	3	3	3	3						

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
60-11-8302-1674	INSULATOR	CHOMERICS	4	4	4	4						
1/8 THK	SHIM	NEOPRENE	A/R	A/R	A/R	A/R						
152	FLEX SHAFT	H.H. SMITH	2	2	2	2						
RTV121	ADHESIVE	G.E.	A/R	A/R	A/R	A/R						
300010	HANDLE	ASM	2	2	2	2						
314010	FUSE, 10A	LITTEFUSE	1	1	1	1						
	1/4" x 1/4 PATCH	COPPER TAPE	A/R	A/R	A/R	A/R						
BC-14215	BAIL	BUD INDUSTRIES	1	1	1	1						
T18S	TY-RAP	TYTON	A/R	A/R	A/R	A/R						
#495	RTNG CMPD	LOCTITE	A/R	A/R	A/R	A/R						
8-32 x 1/4	SCREW	BLK OXIDE BINDER HD SLOTTED	46	46	46	46						
NO.2 TYPE BP. x 1/4	SCREW SELF TAP	PAN HD PHILLIPS	2	2	2	2						
4-40 x 1/8	SET SCREW		8	8	8	8						
2-56 x 1/4	SCREW	PAN HD PHILLIPS	6	6	4	4						
S4-40 x 1/4	SEELSKREW	APM - HEXSEAL	8	6	8	6						
4-40 x 1/4	SCREW	PAN HD PHILLIPS	14	14	14	14						
4-40 x 3/8	SCREW		16	16	16	16						
6-32 x 1/4	SCREW		19	19	19	19						
6-32 x 5/16	SCREW		21	21	21	21						
6-32 x 7/16	SCREW	PAN HD PHILLIPS	8	8	8	8						
S4-40 x 5/16	SEELSKREW	APM - HEXSEAL	4	4	4	4						

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SH & OF | E

PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
6-32 x 5/8	SCREW	PAN HD PHILLIPS	8	8	8	8						
6-32 x 3/8	SCREW	PAN HD PHILLIPS	4	4	4	4						
4-40 x 3/16	SCREW, NYLON	RD HD SLOT	4	4	4	4						
6-32 x 1/2	SCREW	PAN HD PHILLIPS	7	7	7	7						
NO. 4	FLAT WASH		2	2	2	2						
NO. 6	FLAT WASH		41	41	41	41						
NO. 6	LOCK WASH,	INT STAR	52	52	52	52						
4-40 x 1/4	SCREW	BLACK OXIDE BINDER HD SLOTTED	8	8	8	8						
4-40 x 3/16	SCREW	PAN HD PHILLIPS	4	4	4	4						
NO. 6	NUT, HEX		11	11	11	11						
8821	SPACER	H.H. SMITH	7	7	7	7						
B1535-1/4	SPACER	USECO	2	2	2	2						
8-32 x 1/2	SCREW	PAN HD PHILLIPS	1	1	1	1						
NO. 8	NUT, HEX		1	1	1	1						
NO. 8	LOCK WASH,	INT STAR	1	1	1	1						
NO. 4	NUT, HEX -	SM PATTERN	1	1	1	1						
4-40 x 3/16	SCREW	FL HD PHILLIPS	4	4	4	4						
4-40 x 5/16	SCREW	PAN HD PHILLIPS	4	4	4	4						
NO. 4	LOCK WASH,	INT STAR	28	28	28	28						
NO. 2	LOCK WASH	INT STAR	8	8	6	6						

RF MODULE

ASSEMBLY: 7100422

SCHEMATIC: 7100822
7199527
7100528
7100529
7100530
7100543

SECTION I

DESCRIPTION

1.1 General

The RF module consists of five boards mounted as one unit. All five boards are mounted on standoffs and attached to a base board. External connection to the power and signal bus is made by a plug on the data receiver board. The first and second converter boards, and the synthesizer filter board are enclosed in separate cavities of a common housing, and covered by a metallic plate, providing RF shielding. External connections are made via feed thru connectors mounted on the housing. The filter network is mounted to the opposite side of the base board, and housed in the same fashion.

1.2 Circuit Description

Refer to the simplified block diagram of the RF module (Figure 1), and the interconnect diagram (7100822) during the following discussion.

The J1 input to the RF filter network from the antenna circuits is 20 to 520 MHz tone modulated RF (unmodulated when used for communications purposes). The RF is sent through one of eight filters in the filter network as determined by the PIN diode switches. Switching inputs from the data receiver determine which of the eight receiver ranges has been activated by the data processor. The selected bandpass filter output is then sent from the RF filter network to the first converter (via J2). The built-in test equipment (BITE) generator of the filter network is activated by a data receiver control input. When selected, the BITE generator provides test signal inputs at 10 MHz intervals across the range of the receiver. The test signal is modulated by a vertical tone input, to

pn2

closely resemble an actual RF antenna input. When the test signal is switched into the filters, the antenna is switched out to prevent interference.

The 20 to 520 MHz RF input (at J1) to the first converter is mixed with the first local oscillator frequency of 157.75 to 382.25 MHz (input at E2/E3 via J2) to provide an IF output of 74 MHz or 137.75 MHz (dependant on range) to the second converter at J2, and an auxiliary IF output to the spectrum monitor converter at J3 (when used).

The second converter input at E1/E2 is 74 MHz or 137.75 MHz switched IF from the first converter. The IF input is mixed with an input of 84.7 MHz or 127.05 MHz (as selected by the data processor) from the second local oscillator at E3/E4 (via J4). The difference frequency resultant of 10.7 MHz IF at E5/E6 is output to the IF/demodulator at J5. Delayed AGC provides up to 40 db of second converter gain reduction.

The synthesizer filter board is used to clean up the synthesizer (first local oscillator) output by removing spurious outputs. The synthesizer output enters the filter at J1. The conditioned local oscillator output occurs at J2, and is fed (via W3) to the first converter input (J2).

The data receiver board accepts serial data from the data processor (via P1), and uses it to provide control switching outputs to the filter network (via P4). Eight of the P4 switching outputs to the filter network determine which bandpass filter will be activated. The data processor selects a bandpass filter with a range corresponding to the frequency the receiver is tuned to. A ninth switching output is to the built-in test equipment (BITE) generator, and is used to turn the BITE generator on and off.

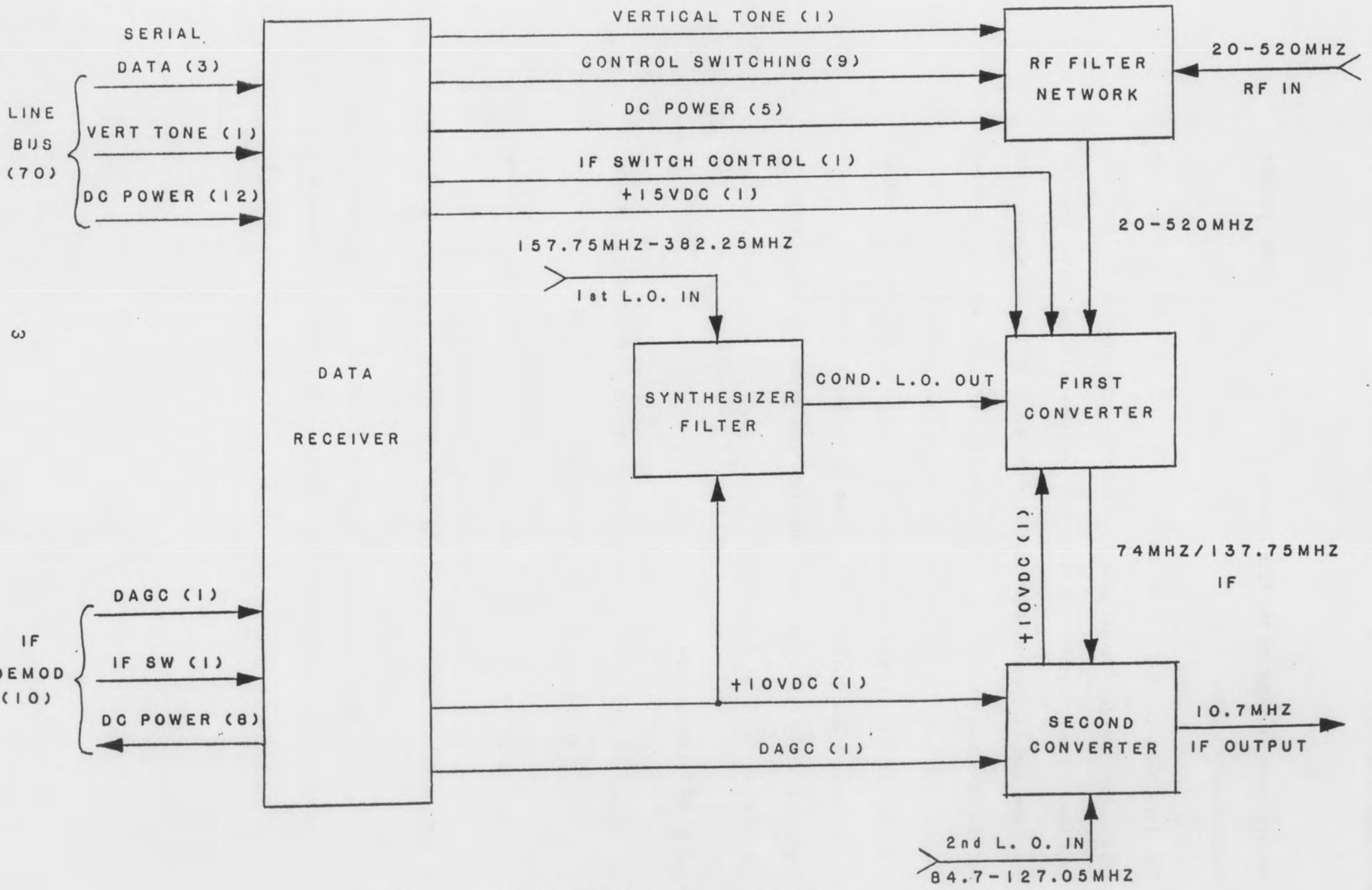


Figure 1. Simplified Block Diagram, RF Module

Vertical tone is input to the BITE generator from P4, via a cross connect to the line bus (P1).

The line bus connector (P1) of the data receiver plugs into the power and signal bus board. Serial data is input via this connector to the data receiver. Power supply inputs to four regulators on the data receiver board are used to provide power to the other boards of the RF module, and to the IF demodulator via J3. An additional +10V line (W5) is connected from the E9 output of the second converter to supply +10V dc to the first converter at E7. Delayed AGC from receiver connector J3 is cross connected to provide a DAGC output to the second converter at J2 (pin 3). An IF switching signal is also cross connected from J3 to provide an output to the first converter at J2 (pin 4).

1.2.1 RF Filter Network

Refer to the block diagram (Figure 2) and the schematic drawing 7100530 during the following discussion.

The 20-520 MHz tone modulated (or unmodulated) RF input from the antenna at J1 is connected to the input of eight filters (FL1-FL8).

PIN diode switching determines which of the eight filters are selected. The selected filter determines which of the eight ranges of RF inputs will be processed through to the receiver in accordance with Table 1.

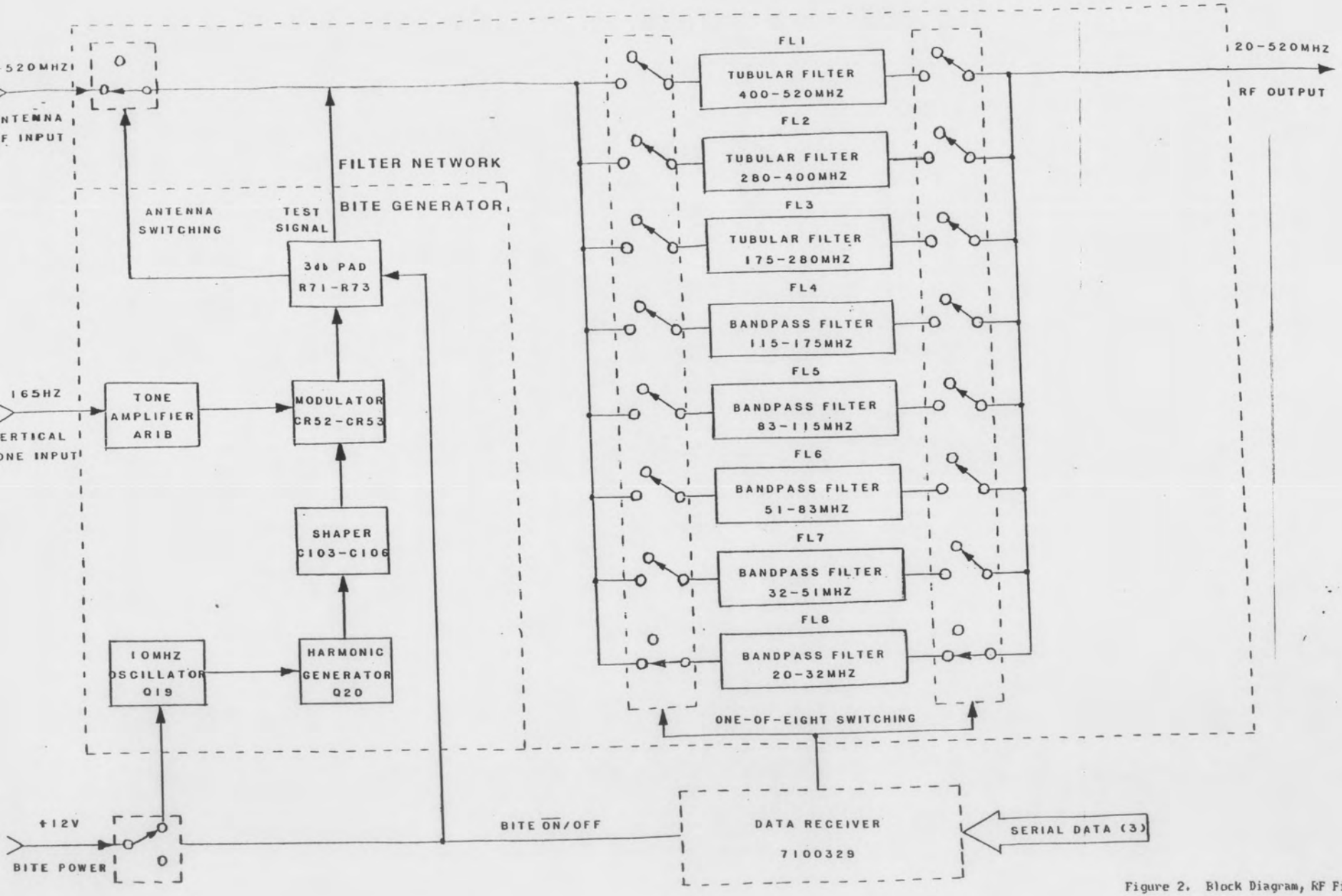


Figure 2. Block Diagram, RF Filter Network

5/6 BLANK

FILTER	INPUT DESIGNATOR	SWITCHES	RANGE
FL1	H	CR3, CR10	400 TO 520 MHz
FL2	G	CR4, CR9	280 TO 400 MHz
FL3	F	CR13, CR17	175 TO 280 MHz
FL4	E	CR27, CR30	115 TO 175 MHz
FL5	D	CR23, CR26	83 TO 115 MHz
FL6	C	CR14, CR18	51 TO 83 MHz
FL7	B	CR31, CR34	32 TO 51 MHz
FL8	A	CR35, CR38	20 TO 32 MHz

Table 1. RF Filter Selection

The selected filter determines which one of the eight ranges of RF inputs will be processed thru to the IF/demodulator. Five of the filters are conventional bandpass (in the 20-32MHz, 32-51MHz,51-83MHz, 83-125MHz and 125-175MHz ranges), but the other three (175-280MHz), 280-400 MHz, and 400-520 MHz) are tubular filters for better high frequency response. The selected output RF is fed to J2, where it is sent to the first converter.

The PIN diode switches are controlled by the eight data receiver inputs at J3. Serial data from the data processor is sent to the data receiver. A high output from the data receiver on one of the eight J3 inputs to the filters will determine which filter will activate.

Assume that the 20-32 MHz range has been selected by the data processor. A high input (+5V) at J3 (pin 4) will forward bias

transistors Q1 and Q2, providing a negative input (-12V) to the 20-32 MHz filter input. This will forward bias PIN diode switches CR35 and CR38 in the signal path, and reverse bias PIN diodes CR36 and CR37, which otherwise ground the filter when it is not in use. The negative input also forward biases PIN diodes CR20 in the input path and CR39 in the output path. The RF input can now be fed thru the filter (FL-8) and out J2 to the first converter. Operation of the other select filters is basically the same.

The BITE generator is disconnected during normal operation, but can be used for testing when the BITE function is activated at the front panel (or by remote). When BITE is selected the data processor outputs a low from the data receiver to J3 (pin 6) input of the filter network. The low input turns AR1A off, providing a -12V output at pin 1. The negative output of AR1A removes forward bias from Q18, turning it off; and provides forward bias to Q17, turning it on. With Q17 on, +12 V input is provided to the 10 MHz oscillator (Q19) turning it on. With Q18 off, +12V is provided as an input to the 3 db pad (R71-R73), this forward biases PIN diodes CR53 and CR52 in the oscillator signal path, allowing BITE output. The positive input at point K, and the negative input at point I, reverse biases PIN diode CR1, disabling the antenna input during testing.

The 10 MHz oscillator (Q19) is a Colpitts oscillator with crystal control in the feedback path. The oscillator output is to a class "C" amplifier (Q20). The amplifier output, which is rich in harmonics, is shaped and attenuated to provide an RF testing signal to the modulator (CR52, CR53). Due to the harmonic content of the output, a test signal is input at 10 MHz intervals throughout the range of the ADF

system.

The vertical tone input from the bearing processor at J3 (pin 7) is used to modulate the test signal so that it closely resembles an antenna input. The 1 Vpp tone input is amplified to 4 Vpp by the tone amplifier (AR1B). This signal is input via point J to the two PIN diodes (CR52, CR53) of the modulator. As the voltage across the PIN diodes varies, their resistance will vary proportionally, controlling the current output, and amplitude modulating the RF test signal at a 165 Hz rate. The modulated RF test signal is then sent thru a 3 db pad (R71-R73) to the input of the RF filters in place of the disconnected antenna input. The BITE signal will now be present thru each range of the receiver as the filters are switched.

1.2.2 First Converter

Refer to the block diagram (Figure 3) and schematic drawing 7100528 during the following discussion.

Two IF frequencies are used in this system to facilitate tuning across the receiver range. PIN diode switches are utilized to select either the 74 MHz or 137.75 MHz filter paths. Circuit action is basically the same in either case, but for the following discussion assume that the 137.75 MHz signal path has been selected.

The 20-520 MHz RF input from the filter network at J1 is sent thru an RF amplifier (AR1) to the input of the notch filter. The IF switching control signal from the data processor is input at E6 to the PIN diode switch driver (AR3, AR4) which sets the level and provides isolation. The A,A' and B inputs determine the status of the PIN diodes in the

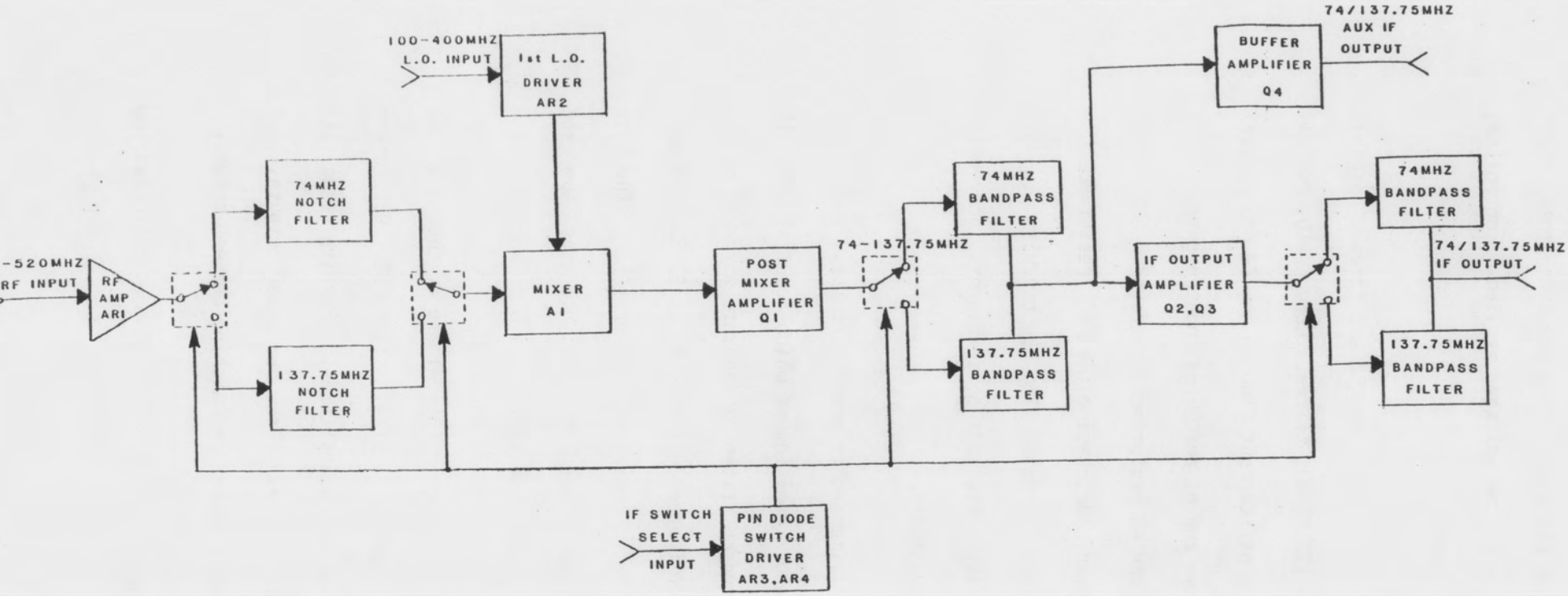


Figure 3. Block Diagram, First Converter

notch filter. The PIN diode characteristics are such that their resistance varies in proportion to the voltage applied, controlling the current flow in the signal path.

With the B switching input positive, CR1 and CR3 are forward biased, allowing current flow thru the 137.75 MHz filter. Conversely, CR4 and CR6 are reverse biased, cutting off current flow in the 74 MHz filter. With A switching input positive and A' switching input negative, CR2 is reverse biased, increasing the AC resistance to ground. CR5 in the 74 MHz filter is forward biased, decreasing the AC resistance to ground, and shunting the input signal. The LC circuits in the switching inputs act as isolation decoupling components preventing feedback to the switching circuitry.

In conjunction with bandpass filtering in prior circuits, the notch filter aids in suppressing any signal inputs which occur at the IF frequency. The output of the notch filter is fed into mixer A1 at pin 1. The first local oscillator frequency is fed in at E2/E3, and goes to pin 4 of the mixer via the local oscillator driver (AR2). The high level SchottKy double balanced mixer (A1) outputs the sum and difference frequencies to the post mixer amplifier.

All IF amplifiers in the first converter (Q1-Q4) are of the grounded gate JFET type. They are used in parallel (i.e. Q2, Q3) where required for better signal handling capabilities. Ferrite beads (Z1-Z4) suppress UHF parasitic oscillations in the amplifier outputs, and autotransformers (T1, T2) provide impedance matching between stages.

In the post mixer amplifier output, the sum frequency is blocked by

the 74 MHz/137.75 MHz filter. With the C switching input positive and the C' input negative, CR7 is forward biased allowing signal flow thru the 137.75 MHz filter, and CR8 is reverse biased preventing current flow thru the 74 MHz filter.

The characteristics of the filter are such that at the IF frequency the combination of L15 and C29 appear inductive and form a parallel resonant circuit with C30 (and C31 trimmer). This provides maximum impedance to ground, coupling the IF through to the final stages. The combination of L15 and C29 also form a series tank at the second mixer image frequency, forming a minimum impedance to ground. (The combination of L18, C34 and L17 perform a similar function in the 74MHz filter). At the filter output, L19 and C32 form a diplexer. At 74MHz C32 capacitive reactance is very high and it appears as an open, and at 137.75MHz L19 inductive reactance causes it to appear as an RF choke, blocking reverse current flow. Thus, L19 and C32 act as output switches and PIN diode switching is not necessary.

At the output of this filter there are two signal paths. The main signal path is thru the final IF amplifier (Q2, Q3) and to another selectable IF filter. With the D switching input positive and the D' switching input negative, CR10 is forward biased and CR9 is reverse biased. Signal will flow thru the 137.75MHz filter to J2. The first IF output at J2 is sent to the second converter.

There is a second (AUX IF) output thru a buffer amplifier (Q4) and out E4/E5. This signal, which is picked off before the final filter has a wide bandpass characteristic.

1.2.3 Second Converter

Refer to the block diagram (figure 4) and schematic drawing 7100527 during the following description.

All IF amplifiers (Q1-Q8) are grounded gate JFETS used in parallel, as necessary, for better signal handling capability. Ferrite beads (Z1-Z8) suppress UHF parasitic oscillations in the amplifier outputs, and autotransformers (T1-T6) provide impedance matching between stages.

The IF input at E1/E2 (74 MHz or 137.75 MHz as selected at the first converter) is fed to a buffer amplifier (Q1) which provides gain and isolation. The output of Q1 is sent thru an IF amplifier (Q2, Q3) and to the pin 1 input of the second mixer (A1).

These first two stages of amplification (Q1 and Q2/Q3) have wide band filtering in their external circuitry. This allows either 74 MHz or 137.75 MHz to be passed through to the mixer. High frequency peaking is provided by L1 and L2. Automatic gain control is provided by PIN diode action in both circuits.

The automatic gain control (AGC) circuitry works in the following manner. The AGC shaper and driver (AR2) provides amplification and shaping of the DAGC voltage input. External components in the AR2C circuitry shape the AGC voltage to maintain more constant gain across the range of the system. A positive AGC voltage is present at all the PIN diodes when the input signal is above threshold. PIN diode resistance will vary in proportion to the voltage across it, and this will control the current flow through the diodes.

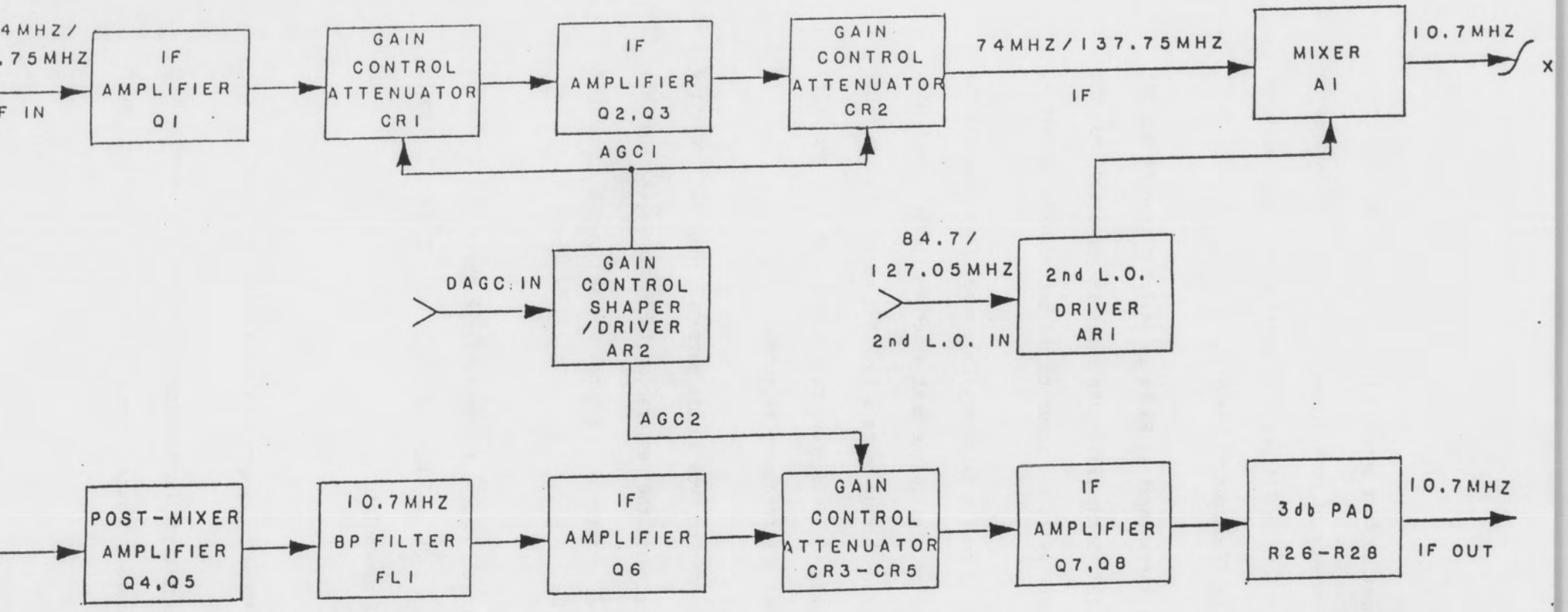


Figure 4. Block Diagram, Second Converter

The (GC1) positive input is felt across PIN diodes CR1 and CR2. This will decrease the resistance of both diodes, decreasing resistance in the AC ground path of both amplifiers. A portion of the IF will be shunted, decreasing the IF output to the mixer.

The second local oscillator input at E3/E4 is 84.7 MHz (for 74 MHz IF) or 127.05 MHz (for 137.75 MHz IF). The input is amplified by the local oscillator driver (AR1), and input to the second mixer at pin 4.

The high level Schottky double balanced diode mixer (A1), outputs the sum and difference frequencies to the post mixer amplifier (Q4, Q5). The post mixer amplifier output is to a 10.7 MHz ceramic filter (FL1) with a 280 kHz bandpass. The difference frequency of 10.7 MHz (IF) will be passed, and the sum frequency rejected.

IF amplifier Q6 uses gain control in its output. The AGC positive voltage (AGC2) will decrease the resistance of PIN diodes CR3 and CR5, thus decreasing the AC resistance to ground, and shunting a portion of the IF signal.

The 10.7 MHz IF output of Q6 goes to the final IF amplifier (Q7, Q8), and is output across a 3 db pad (R26, R27, R28) to E5/E6. The E5/E6 output goes to the IF/demodulator.

1.2.4 Synthesizer Filter

Refer to schematic 7100543 during the following discussion.

The first local oscillator (synthesizer) frequency (100-400 MHz) is input at J1, where it passes through a series of filters which

remove spurious outputs. The J1 input goes through (L7-L9, C13-C16) a lowpass filter, a 3 db pad (R1-R3), a high pass filter (L1, L2,C1-C3), through a 7 db pad (R4-R6), a high pass filter (L3-L5, C6-C9), and through another 3 db pad to an amplifier (AR1).

Amplifier AR1 has approximately 12 db gain, and the filtered output frequency is sent to the first converter via J2.

1.2.5 Data Receiver

Refer to schematic drawing 7100529 during the following discussion.

Serial data from the data processor is input on the power and signal bus at P1 (pins 49, 51, 55), and sent to the data receiver (U1,U2) (pins 1,2,3). Data receiver U1 outputs switching signals to the eight bandpass filters of the filter network on P4 (pins 2-4 and 9-13). An active high on one of the eight lines will select a filter with a range corresponding to the frequency the receiver is tuned to.

Data receiver U2 outputs one switching signal (pin 4) to the BITE generator. An active low turns the BITE generator on by switching +12V power into the oscillator circuit. Data receiver U2 outputs the BITE $\overline{\text{ON}}$/OFF signal to the filter network on P4 (pin 6).

A vertical tone signal from the bus line (P1, pin 22) is fed through to the RF filter network (P4, pin 7) where it supplies tone modulation for the BITE generator output. A delayed AGC input from the IF demodulator is fed through from J3 (pin 10) to the J2 (pin 3) output where it is used by the second converter. An IF switching signal from J3 (pin 5) is fed through to the J2 (pin 4) output where it is used to

control the first converter.

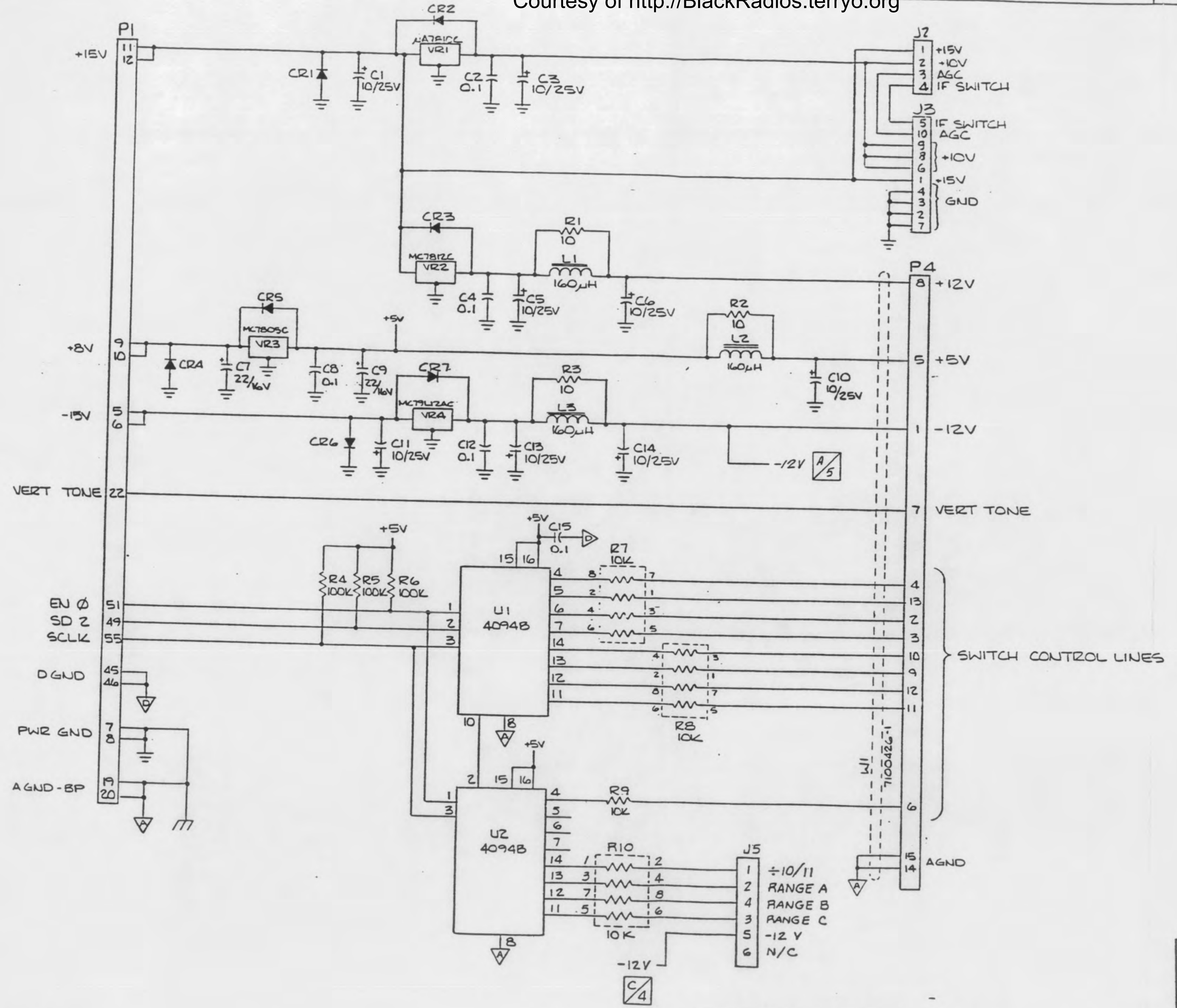
Regulators (VR1-VR4) on the data receiver board use power supply inputs from the bus line (P1, pins 5, 6 and 9-12) to provide regulated power to the other RF module boards. Diodes CR1, CR4 and CR6 provide inverse voltage protection, and diodes CR2, CR3, CR5, and CR7 provide a discharge path for the capacitors when power is turned off, protecting the regulators.

The VR2, VR3 and VR4 regulator outputs are filtered, and provide +12V (pin 8), +5V (pin 5), and -12Vdc (pin 1) outputs respectively, via P4 to supply power to the RF filter network board. +5Vdc is tapped off prior to the filter at the VR3 output to supply board power for the data receiver circuits.

+10Vdc from VR1 is supplied to the second converter and synthesizer filter via J2 (pin 2). +10Vdc is supplied to the first converter via a cross connect at the second converter. VR1 also supplies three +10Vdc outputs to the IF/Demodulator at J3 (pins 6, 8, 9). The +15Vdc power input at P1 (pins 11 and 12) is tapped off prior to VR1 and input to the IF/demodulator at J3 (pin 1), and to the first converter at J2 (pin 1).

DWG NO. 7100529 SH 1 B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	ADDED +15V TO J3 & J2	1-9-84	B.BODIKER
B	ADDED R10 & J5 REF ECR 5469	3-15-4	B.BODIKER



4. ALL INDUCTORS ARE 025-719-1.
3 ALL UNMARKED DIODES ARE IN4001.
2 CAPACITANCE IS IN MICROFARADS.
1 RESISTORS ARE 1/8W, ±5%, RESISTANCE IS IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED							
C	CR	J	L	P	R	U	VR
15	7	5	3	4	10	2	4

REFERENCE DESIGNATIONS NOT USED: J1, J4, P2, 3

7100329

OCEAN APPLIED RESEARCH CORP

G. Landi 11/4/83

SCHEMATIC
DATA RCVR, RF MODULE

D 7100529 B

7100529 B

DWG NO. 7100530 SH 1 F

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
D	REDRAWN INCORP ECN 5958; EFF 042 & ON AD 4-25-85	5/1/85	B. BODIKER
E	INCORP ECN 5997; EFF 042-044, 074 & ON KD 4-25-85	5/1/85	B. BODIKER
F	INCORP ECN 6017; EFF 074 & ON KD 4-25-85	5/1/85	B. BODIKER

RF IN — J1 — C1 1000pF — CR1 — C12 1000pF — C3 1000pF — R3 470 — L46 .39uH

R1 820 — C2 1000pF — R74 820 — C6 1000pF — R76 820 — C14 1000pF

C4 100pF — C10 100pF — C16 100pF

R2 180 — R75 180 — R77 1.2K

A — B/25 — B — A/26 — C — B/21

FL1 400-520MHz: CR3, CR26, Z6 470, L47 .39uH, L2 3.3uH, R8 6.8, R9 470, CR7, CR10, L48 .39uH, C5 1000pF, C8 0.1, C9 1000pF

FL2 280-400MHz: CR4, CR5, R5 10K, R10 470, L49 .39uH, CR2, R13 470, L50 .39uH, CR8, CR9, R33 10K, CR11, R11 6.8, L3 3.3uH, C11 100pF, C13 0.1, C15 100pF

FL3 175-280MHz: CR12, CR13, CR14, CR15, R14 10K, R15 470, L51 .68uH, W2, W3, CR16, CR17, CR19, R17 470, R18 10K, L52 .68uH, L5 3.3uH, R16 6.8, C18 270pF, C21 270pF, C25, C20 270pF, CR18

51-83MHz: W4, W5, CR21, CR20, R19 470, L53 43uH, C23 62pF, L6, L7, C24 150pF, C26 47pF, C27 100pF, L8, C28 62pF, L9, C30 100pF, L4, C31 100pF, C32 62pF, R20 470, L54 43uH, CR22, CR39, C82 1000pF, J2, RF OUT, R35 470, L63 .39uH, L10 3.3uH, C22 .01, C33 .01

83-115MHz: CR23, CR24, W6, R21 470, L55 1.0uH, L11, L12, L13, C37 33pF, C38 18pF, C39 18pF, C40 33pF, C41 27pF, C42 56pF, C43 56pF, L14, L15, L16, C44 33pF, R23 470, L56 .68uH, CR25, CR26, R22 6.8, L17 3.3uH, C34 .01, C35 100pF, C36 .01

115-175MHz: CR27, CR28, R24 470, L57 .68uH, L18, L64, C46 20pF, C47 12pF, C48 20pF, L20, L21, L22, L23, C49 15pF, C50 43pF, C51 43pF, C52 43pF, C53 27pF, W7, CR29, CR30, R26 470, L58 .68uH, R25 6.8, L24 3.3uH, C45 1000pF, C54 100pF, C55 100pF, C56 1000pF

32-51MHz: CR31, CR32, W8, R28 470, L59 43uH, L65, L26, C58 100pF, C60 68pF, C62 160pF, L27, L28, C59 270pF, C61 75pF, C63 100pF, C65 160pF, C67 100pF, W9, CR33, CR34, R29 470, L60 43uH, L29 3.3uH, C57 .01, C68 .01

20-32MHz: CR35, CR36, R27 10K, R30 470, L61 43uH, L30, L31, C70 150pF, C73 110pF, C75 270pF, L66, L67, C74 150pF, C76 250pF, C80 150pF, W10, CR37, CR38, R31 470, L62 43uH, R32 10K, C71 33pF, C72 390pF, C74 120pF, L34 3.3uH, C69 .01, C81 .01

IND VAR.	PART NO.	IND VAR.	PART NO.
L4	7100744-2	L26	7100732-26
L6	7100732-6	L27	7100732-27
L7	7100732-7	L28	7100732-28
L8	7100744-1	L30	7100733-4
L9	7100744-1	L31	7100733-5
L11	7100732-11	L40	7100744-4
L12	-12	L44	7100744-5
L13	-13	L64	7100732-64
L14	-14	L65	-65
L15	-15	L66	-66
L16	-16	L67	7100732-67
L18	-18		
L20	-20		
L21	-21		
L22	-22		
L23	7100732-23		

4. FOR UNMARKED INDUCTORS SEE TABLE.
3. DIODES ARE MA47054.
2. RESISTORS ARE 1/8W, RESISTANCE IS IN OHMS ±5%.
1. CAPACITANCE IS IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF MATERIAL

QTY PER ASSY	-1 ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √

HOLE SIZES PER AND10387

7100330 NEXT OR ASSOC ASSEMBLY

	BY	DATE
DWN BY:	Tim Dixon	4/25/85
CHECK:	B. BODIKER	5/1/85
APVD:		5/7/85
APVD:		5/8/85
		5/13/85
RLSE:		

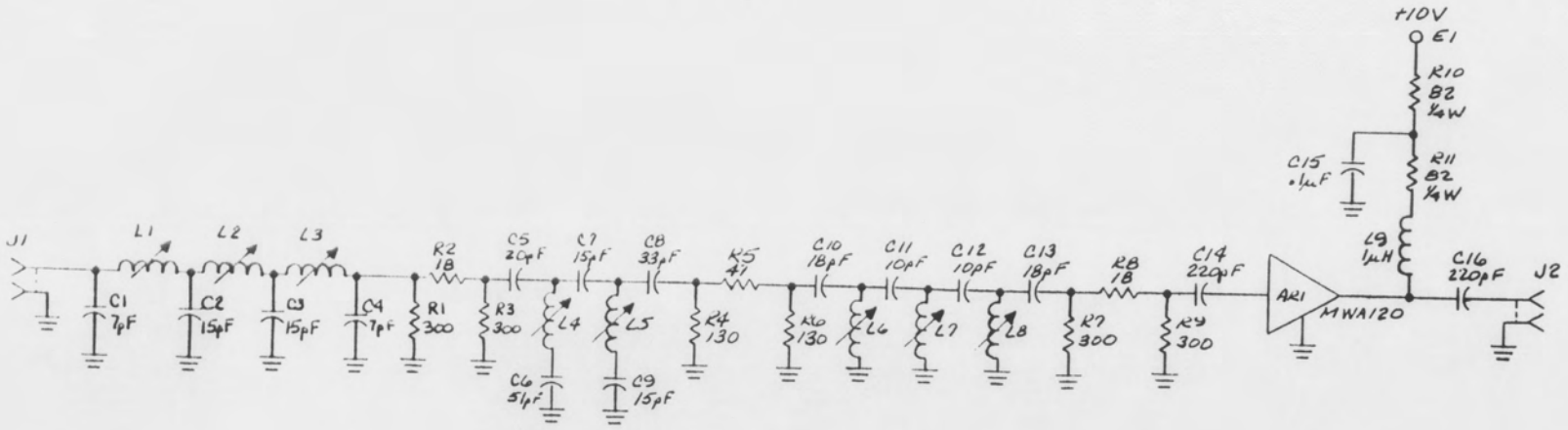
OCEAN APPLIED RESEARCH CORP — A DIVISION OF GENERAL INDICATOR CORP — OAR

SCHEMATIC DIAGRAM RF FILTER NETWORK VHF/UHF RECEIVER

SIZE D | FSCM NO. 06994 | DWG NO. 7100530 | REV F | SCALE | SHEET 1 OF

7100530 F

B INCORP ECN 5738 WA B. BODIKER 10/4/84



. CAPACITANCE IS IN PICO FARADS.
RESISTORS ARE ½W, 5%. RESISTANCE IS IN OHMS.
OTES:

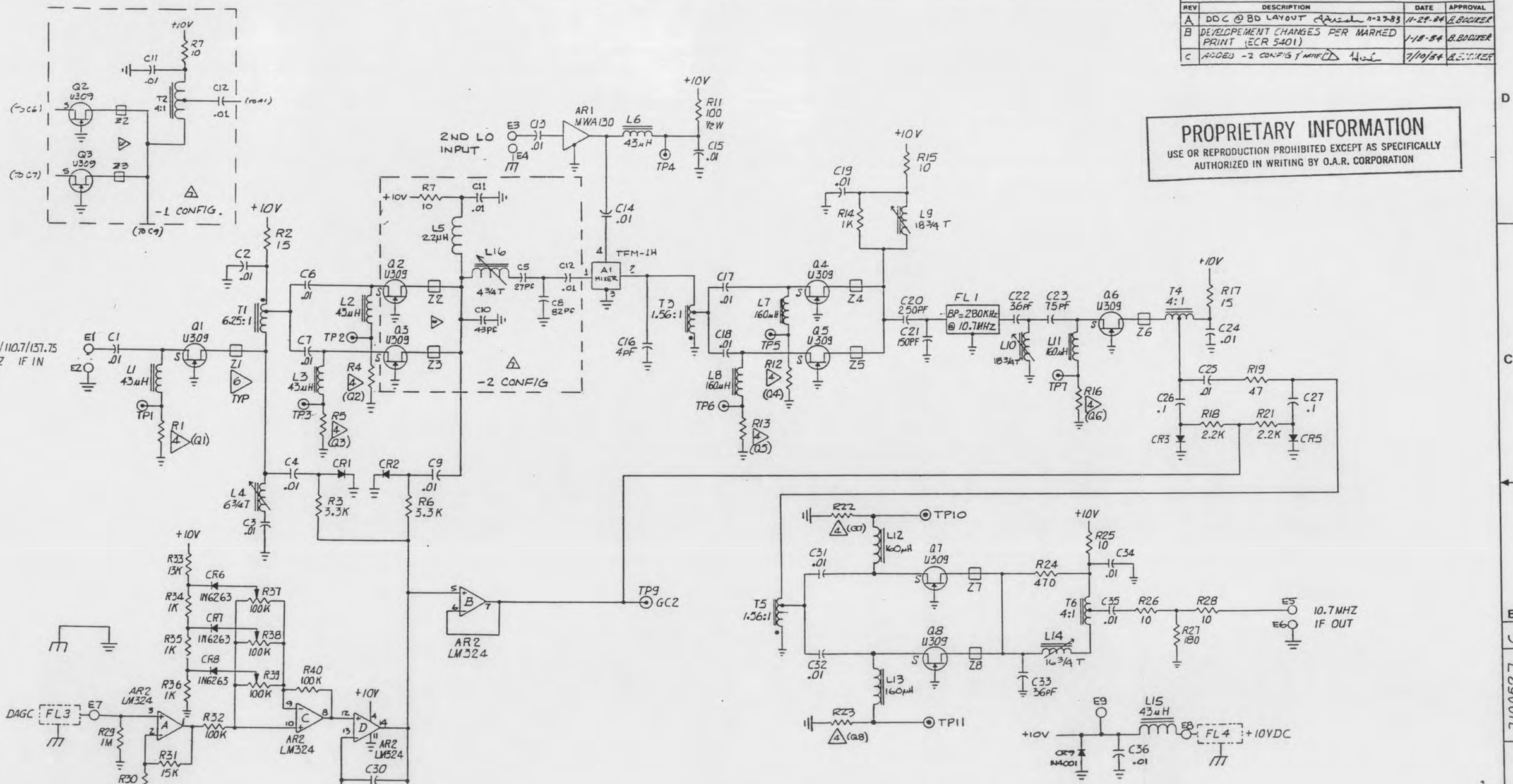
APP'D : U Mai 10/9/84
APP'D : [illegible] 10/10/84
APP'D : [illegible] 10/12/84
[illegible] 10/15/84

SYNTH FILTER 345/3045
7100543 REV B

DWG NO. 7100527	SH 1	C

REVISIONS

REV	DESCRIPTION	DATE	APPROVAL
A	DDC @ BD LAYOUT	11-29-83	B.BOOKER
B	DEVELOPMENT CHANGES PER MARKED PRINT (ECR 5401)	1-18-84	B.BOOKER
C	ADDED -2 CONFIG & NOTE 7	7/10/84	B.BOOKER



7. FOR HF 2ND CONV USE -2 CONFIGURATION, FOR VHF/UHF USE -1 CONFIGURATION.
6. NONSTANDARD SYMBOL, FERRITE BEAD.
5.
4. SOURCE RESISTOR IS MATCHED TO INDICATED TRANSISTOR. SEE 025-908.
3. DIODES ARE HP 5082-3081.
2. CAPACITORS ARE 50 WVDC MIN; CAPACITANCE IS IN MICROFARADS.
1. RESISTORS ARE ⅛ W; RESISTANCE IS IN OHM ±5%.

NOTE: UNLESS OTHERWISE SPECIFIED

LAST REF DES USED

A1	AR2	C36	CR9	E9	FL1	L16	Q8	R41	T6	TP11	Z8

REF DES NOT USED

			CR4					R8 R9 R10 R20	T7		
		C28 C29									

LIST OF MATERIAL

QTY PER ASSY	-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

7100327
NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER AND10387

DWN BY: Tom Duong	11/7/83	
CHECK: B. BOOKER	11/15/83	
APVD:	11/17/83	
APVD:	11/17/83	
	11/7/83	
PLSE:		

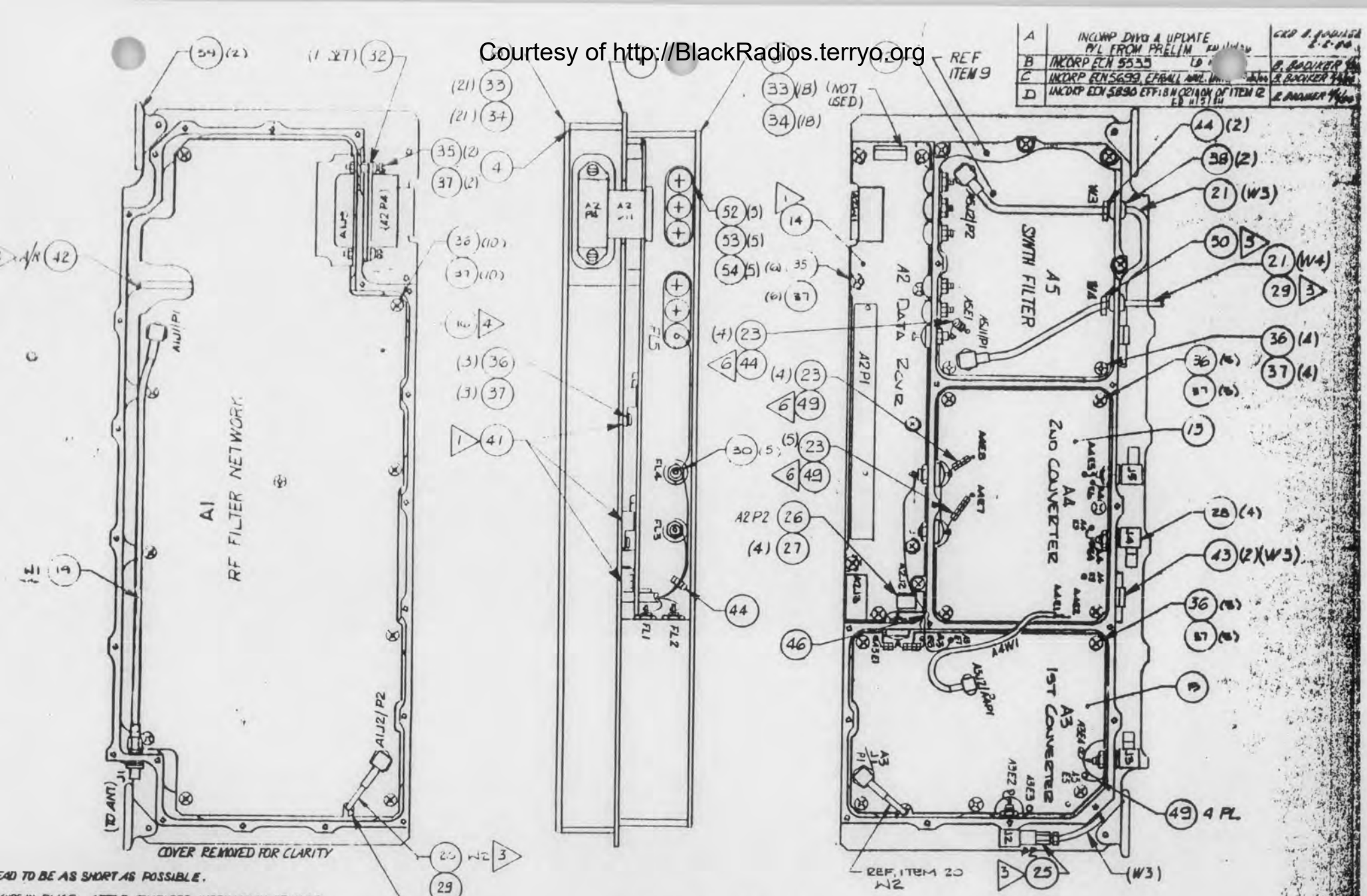
OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC DIAGRAM SECOND CONVERTER

SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100527	C

SCALE: | SHEET 1 OF 1

7100527 C



A	INCORP DWG & UPDATE P/L FROM PRELIM	
B	INCORP ECN 5535	
C	INCORP ECN 5699, EFF ALL	
D	INCORP ECN 5890 EFF: B/N 021 NOW OF ITEM 12	

HEAD TO BE AS SHORT AS POSSIBLE.

CURE IN PLACE AFTER COMPLETE INSTALLATION OF WIRE AND MATING CONNECTORS USING ITEM 50.

PPLY 3 LAYERS OF TAPE (ITEM 42) ACROSS ENTIRE NGTH OF RIB PRIOR TO INSTALLATION OF ITEM 16.

SS CABLE THRU HOLE IN BULKHEAD PRIOR TO TACHING CONN

NTIFY BY BAGGING & TAGGING WITH PT NO. PLICABLE DASH NO & REV LTR.

E INSULATOR ITEM 41 BENEATH V REGLTR'S ON TA RCVR (ITEM 14) AT TIME OF INSTALLATION.

S: UNLESS OTHERWISE SPECIFIED

(1) -1 RF MODULE

SEE SEPARATE PARTS LIST
OAR CORPORATION

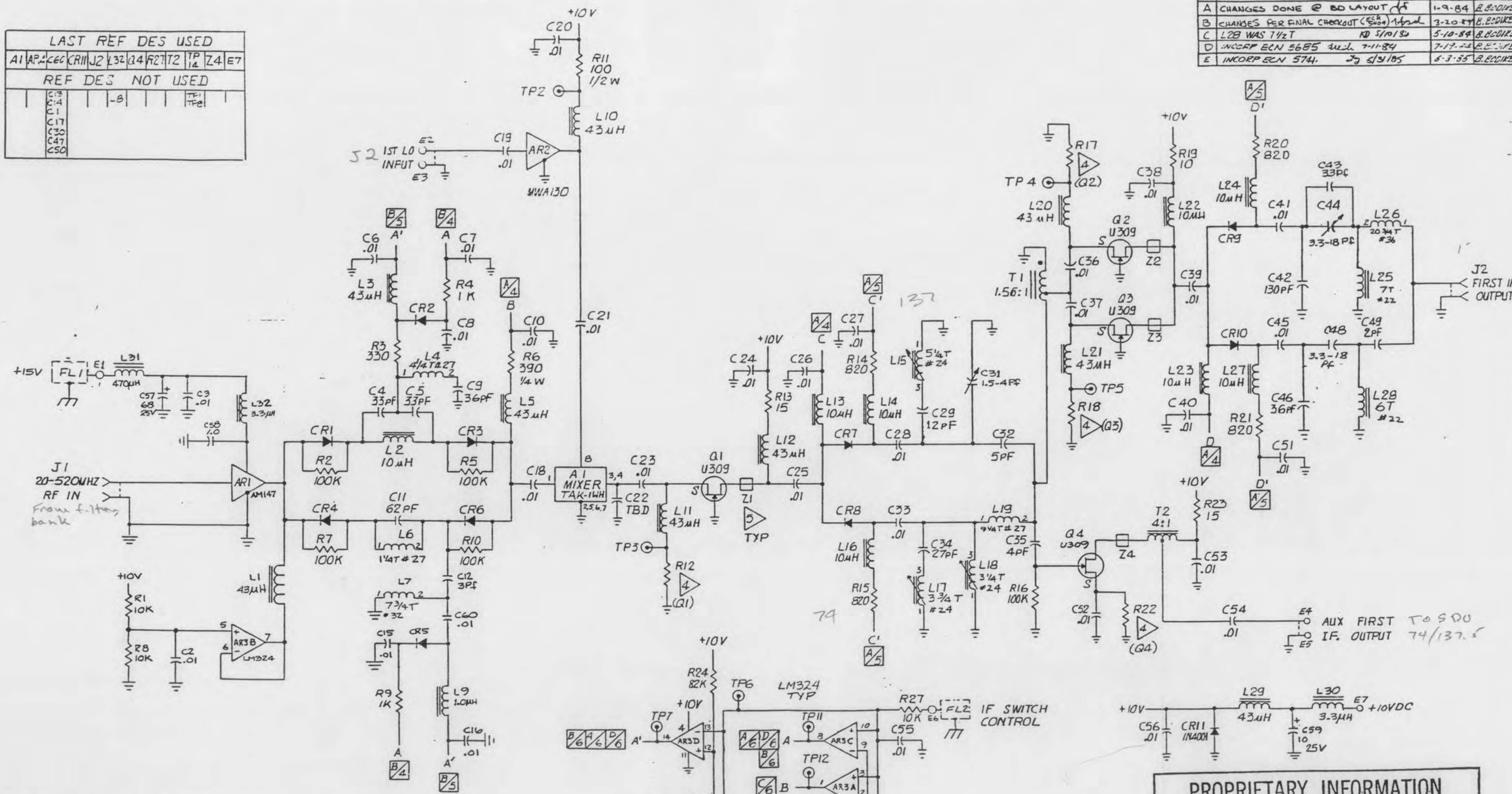
RF MODULE
(3045 RCVR) REV
7100422 D

SCALE: NONE DRAWN BY

DWG NO. 7100528 | E | SH 1

LAST REF DES USED											
A1	AR4	C60	CR11	J2	L32	Q4	R27	T2	TP14	Z4	E7
REF DES NOT USED											
		C13, C14, C1, C17, C30, C47, C50			-8				TP1, TP2		

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	CHANGES DONE @ BD LAYOUT	1-9-84	B.BODIKER
B	CHANGES PER FINAL CHECKOUT (ECR 5404)	3-20-84	B.BODIKER
C	L28 WAS 7½T KD 5/10/84	5-10-84	B.BODIKER
D	INCORP ECN 5685 7-11-84	7-17-84	B.BODIKER
E	INCORP ECN 5744. 5/31/85	6-3-85	B.BODIKER



7. 43µH INDUCTORS ARE 025-705-1.
6. TEST POINTS ARE NOT SEPARATE PARTS.
5. NONSTANDARD SYMBOL, FERRITE BEAD.
4. SOURCE RESISTOR IS MATCHED TO INDICATED TRANSISTOR. SEE 025-908.
3. DIODES ARE MA 4P 3401, BY MACOM.
2. CAPACITORS ARE 50 WVDC MIN; CAPACITANCE IS IN MICROFARADS.
1. RESISTORS ARE 1/8W; RESISTANCE IS IN OHM; ±5%.

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°-30′ DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER AND10387
NEXT OR ASSOC ASSEMBLY: 7100328

DWN BY:		10/5/83
CHECK:	B. BODIKER	10/6/83
APVD:		10/10/83
APVD:	R. Dean	13 JAN 84
		11/5/83

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

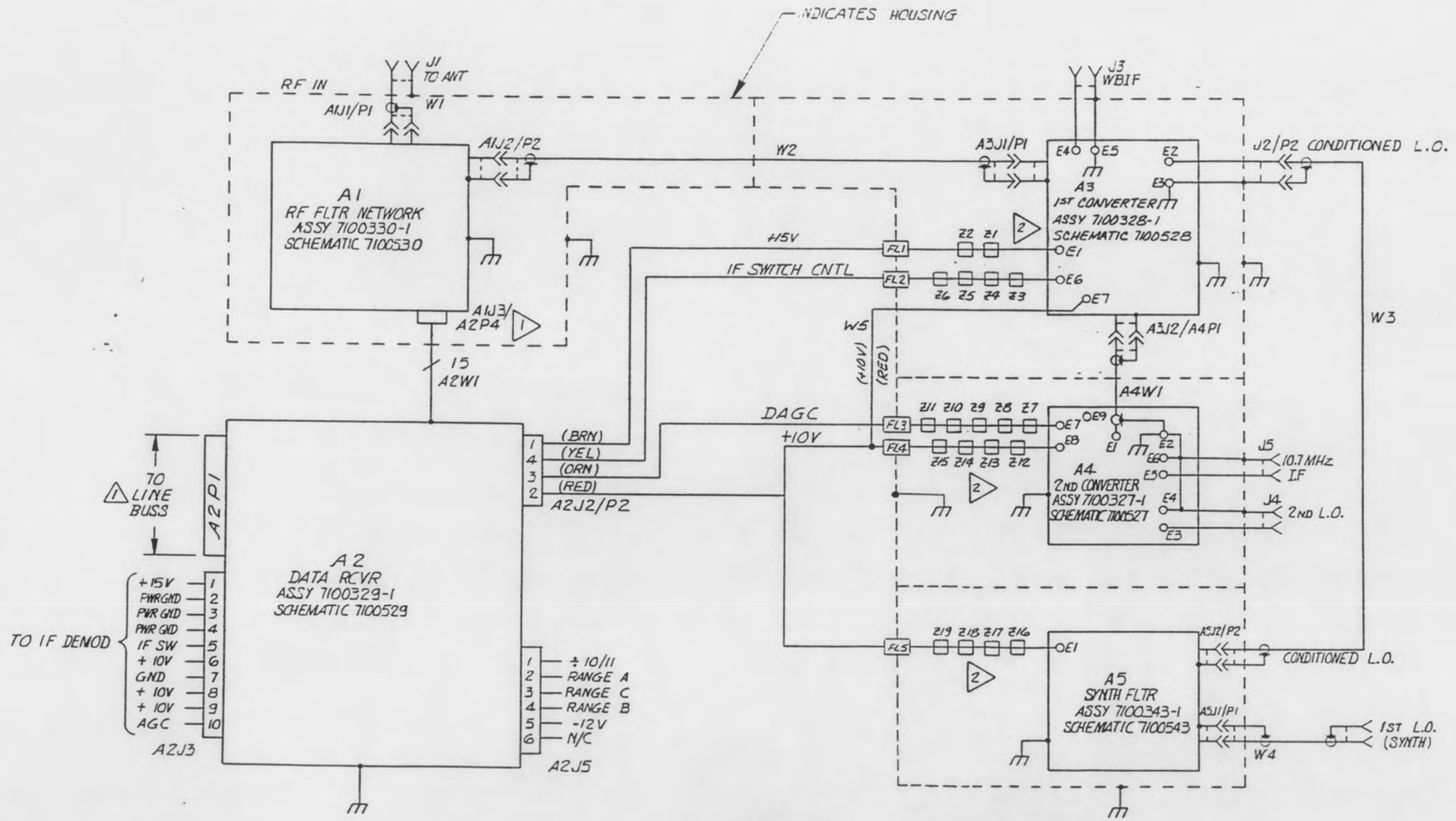
SCHEMATIC DIAGRAM FIRST CONVERTER VHF/UHF RECEIVER

SIZE D | FSCM NO. 06994 | DWG NO. 7100528 | REV E
SHEET 1 OF 1

7100528 E

DWG NO.	7100822	SH	1

REVISIONS				
REV	DESCRIPTION		DATE	APPROVAL
A	REVISED & REDRAWN	KDL 11/1/84	4/24/84	B. BODIKER
B	INCORP ECN 5742	[illegible] 5/31/85	6/3/85	B. BODIKER
C	INCORP ECN 5763			



A2W1	
LINE	FUNCTION
1	-12V
2	SWITCH CONTROL LINE
3	SWITCH CONTROL LINE
4	SWITCH CONTROL LINE
5	+5V
6	SWITCH CONTROL LINE
7	VERTICAL TONE
8	+12V
9	SWITCH CONTROL LINE
10	
11	
12	
13	SWITCH CONTROL LINE
14	AGND
15	AGND

A2P1	
PIN NO.	FUNCTION
5	-15V
6	-15V
7	PWR GND
8	PWR GND
9	+8V
10	+8V
11	+15V
12	+15V
19	AGND-BP
20	AGND-BP
22	VERT TONE
45	DGND
46	DGND
49	SD2
51	ENØ
55	SCLK

FOR UNUSED BUS FUNCTIONS SEE 7100524

2 NON STANDARD SYMBOL ⊖: FERRITE BEAD, P/N 2643000101.

1 SEE APPLICABLE TABULATION BLOCK FOR FUNCTIONS.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √J HOLE SIZES PER AND10387

7100422 NEXT OR ASSOC ASSEMBLY

DWN BY:	Lin Duong	4/11/84
CHECK:	B. BODIKER	4/30/84
APVD:	[illegible]	5-1-84
APVD:	T. Mahaffey	5-1-84
	[illegible]	5/3/84
RLSE:		

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

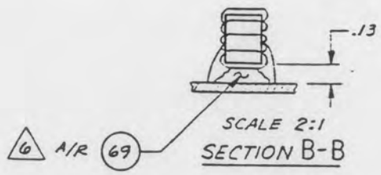
INTERCONNECT DIAGRAM RF MODULE 3045 RCVR

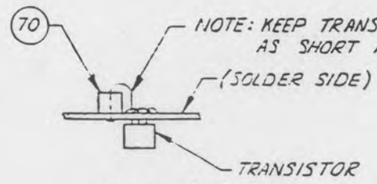
SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100822	C
SCALE		SHEET 1 OF	

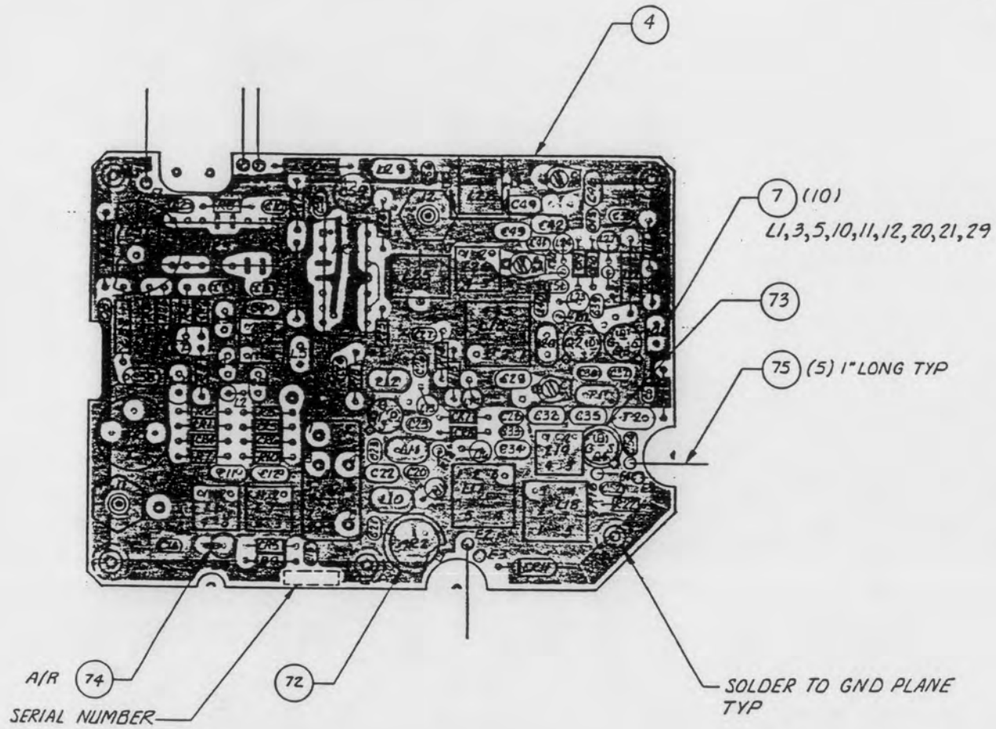
7100822

DWG NO. 7100328 SH 1 E

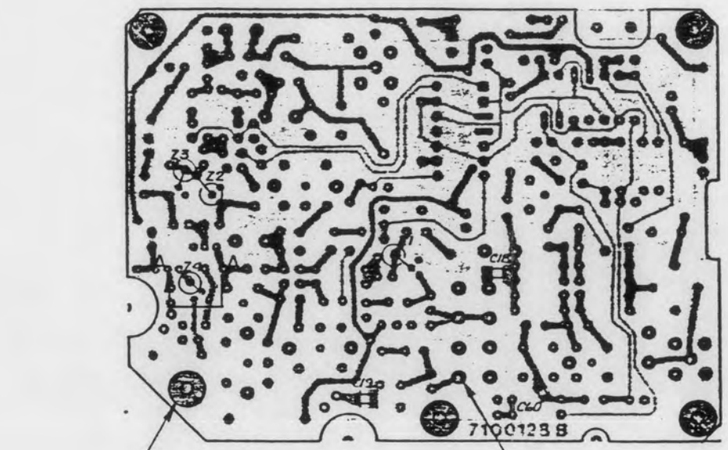
REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
E	PEGRAM, UPDATE TO ART WORK REV E, ECR 2 ECN 5705, EFF: S/N 040 & UP CCR 217184	8/8/84	R. ROOKER
E24	FIXED VIEW, SCALE (EEN INCORP AS ...	1/15/85	R. ROOKER







(1) -1 COMPONENT SIDE SHOWN



SOLDER SIDE SHOWN

SEE SEPARATE PARTS LIST

6 USE MINIMUM AMOUNT OF EPOXY ITEM 69 TO SECURE INDUCTOR IN LOCATION INDICATED.

5. IDENTIFY WITH PIN 7100328. DASH NO. & REV LTR. BY BAGGING & TAGGING.
4. FOR SCHEMATIC REFERENCE 7100528.
3. FOR COMPONENT TYPES & VALUES SEE SEPARATE PARTS LIST.
2. STAKE VERTICAL COMPONENTS AS REQUIRED.
1. MOUNT ALL COMPONENTS FLUSH TO BOARD.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

QTY PER ASSY — LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X ± .1 .XX ± .03 .XXX ± .010 SURFACE J

HOLE SIZES PER AN010387

DWN BY: C. KENNEDY	7/31/84	OCEAN APPLIED RESEARCH CORP (OAR) A DIVISION OF GENERAL INDICATOR CORP
CHECK: R. ROOKER	8/5/84	
APVD: [illegible]	9-14-84	1 ST CONVERTER VHF / UHF
APVD: T. Nanaghey	8-15-84	
[illegible]	5/17/89	
RLSE:		SIZE D FSCM NO. 06994 DWG NO. 7100328 REV E
		SCALE: 2/1 SHEET 1 OF 1

7100422
NEXT OR ASSOC ASSEMBLY

7100328 E

DWG NO. 7100530 SH 2 F

J3
+5V 5
+12V 8
-12V 1
GND 14
GND 15
ON/OFF 4
32-51 MHz 13
51-83 MHz 2
83-115 MHz 3
115-175 MHz 10
175-280 MHz 9
280-400 MHz 12
400-520 MHz 11
BITE OFF/ON 6
VERTICAL TONE 7

L35 160uH 025-719-1
L36 4.7uH
L37 160uH 025-719-1
L38 160uH 025-719-1
R36 10
R37 10
R38 10
C83 .1
C84 10/25V
C85 .1
C86 22/16V
C87 .1
C88 10/25V
C89 .1
C90 .1
C91 10/25V
C92 .1
20-32MHz

Q1 MPS6523
Q2 MPS6523
Q3 MPS6523
Q4 MPS6523
Q5 MPS6523
Q6 MPS6523
Q7 MPS6523
Q8 MPS6523
Q9 MPS6523
Q10 MPS6523
Q11 MPS6523
Q12 MPS6523
Q13 MPS6523
Q14 MPS6523
Q15 MPS6523
Q16 MPS6523
CR41 IN4148
CR42 IN4148
CR43 IN4148
CR44 IN4148
CR45 IN4148
CR46 IN4148
CR47 IN4148
CR48 IN4148
R39 6.8K
R40 6.8K
R41 6.8K
R42 6.8K
R43 6.8K
R44 6.8K
R45 6.8K
R46 6.8K
A/6 B/6 C/6 D/6 E/6 F/6 G/6 H/6 J/6 K/6 L/6

BITE OSCILLATOR
L39 160uH
C96 .1
R60 22
C97 .1
R61 100
C101 .01
C98 .1
C99 .01
L41 10uH
C7 .01
L42 10uH
C103 100pF
R63 18
C106 33-18pF
R66 18
C107 .01
CR52 5082-3081(x2)
CR53
C109 .01
R71 24
CR54 CR55 CR56
BITE RF C C/7
R72 24
C110 100pF
C111 0.1
R58 10K
T1 1:4
C102 50pF
Q19 2N5179
Q20 BFW92A
Y1 10MHz
L40 13 3/4 T #32
C100 390pF
R57 560
R59 10K
C104 1000pF
C105 680pF
R73 1.8K
CR51 IN4148
L43 47uH
R62 300
R64 300
R65 300
R67 300
R68 820
R69 6.8K
R70 820
L44 3/4T#27
L45 10uH
L33 10uH
C108 .001
C112 .01

+12V
R47 110K,1%
C94 .1
R50 100K,1%
C93 10/25V
R48 10K 1%
C95 .1
R51 604K,1%
R49 10K
U1-A U1-B LM358
CR50 IN4148
R54 10K
R55 1K
Q18 MPS6521
-12V
R56 100K
A B/7
R52 1K
R53 10K
CR49 IN4148
Q17 MPS6523
B B/7

LAST REF DES USED										
AR	C	CR	FL	J	L	Q	R	T	W	Y
1	112	56	3	3	67	20	77	1	10	1

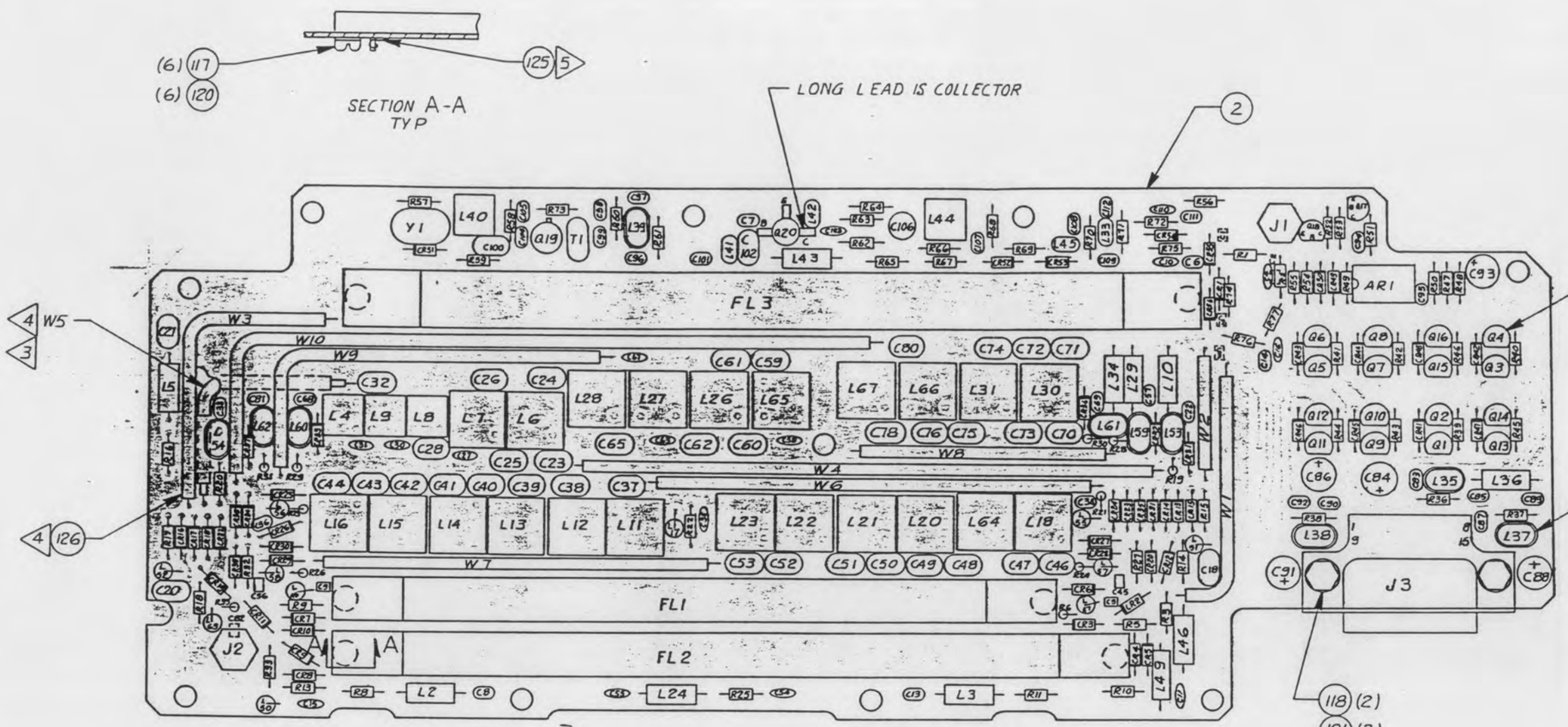
REF DES NOT USED
C17, 19, 29, 64, 66, 77, 79
CR40
L1, 19, 25, 32
R4, 7, 12, 34

SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100530	F
SCALE:		SHEET 1	

7100530 F

DWG NO. 7100330	SH 1	L

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
L	INCORP ECN 6178; EFF: 085 & ON KD 8-1985	9-4-85	R. BOOKER



(1) -1 COMPONENT SIDE SHOWN

7. IDENTIFY WITH P/N 7100330, DASH NO. & REV LTR.
6. FOR SCHEMATIC DIAGRAM SEE 7100530.
5. CONNECT INPUT & OUTPUT PIN OF FL1-3 TO BOARD BY WRAPPING WIRE AROUND FILTER PIN, SOLDER WIRE TO PIN, THEN SOLDER WIRE TO TRACE AS SHOWN. DO NOT SOLDER DIRECTLY TO BRD. NOTE: KEEP WIRE AS SHORT AS POSSIBLE.
4. ON COAX JUMPERS W1-W10 EACH SHIELD MUST BE SOLDERED TO GROUND PLANE AT EACH END OF JUMPER.
3. INSTALL SHRINK TUBING ON W5 PRIOR TO INSTALLATION TO ISOLATE FROM TRACK ON F.S OF BOARD, EXCEPT FOR GND PLANE AT ENDS.
2. CHIP CAPACITORS C1,3,12 & 82 TO BE INSTALLED ON F.S OF BOARD.
1. MOUNT ALL COMPONENTS FLUSH TO BOARD SURFACES.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY					

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010 SURFACE √ HOLE SIZES PER AN010387	DWN BY: Kim Quong	8/17/85
	CHECK: R. BOOKER	9/4/85
	APVD: J. May	9/11/85
	APVD: T. Mahaffey	9/11/85
		9/10/85

7100422
NEXT OR ASSOC ASSEMBLY

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

RF FILTER NETWORK
VHF/UHF RECEIVER

SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100330	L

SCALE: 2/1 SHEET 1 OF 1

7100330 L

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL		DATE 2/2/84
APPVD R Dean		DATE 2/2/84
CHECK B. BODIKER		DATE 2/2/84
DRAWN Cin Duong		DATE 1/11/84

TITLE
RT MODULE
(3045 RCVR)

PARTS LIST
710422
SHEET 1 OF 4 REV D
MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	345-410			
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410			
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	REV & REDRAW P/L FROM PRELIM & INCORP DWN	KD 1/11/84	B. BODIKER	2/2/84
B	INCORP ECN 5535	KD 4/16/84	B. BODIKER	4/30/84
CR2	INCORP ECN 5699; EFF: ALL AVAILABLE UNITS	KD 11/5/84	B. BODIKER	11/6/84
D	INCORP ECN 5890; EFF: S/N 021 & ON OF ITEM 12	KD 11-5-84	B. BODIKER	11/6/84

7100422
SH 2 OF D

ITEM	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-10	-11			REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	-1	RF MODULE		X										
	-11	GASKET, COVER	40-21-1015-1212 CHOMERICS	1		X								
	7100822	INTERCONNECT DIAGRAM		REF										
	7100096-1	HOUSING (MACH)		1										
	7100097-1	COVER (MACH)		1										
	7101059-1	COVER, RF MODULE		1										
	7100343-1	SYNTH FILTER		1										A5
	7100327-1	2ND CONVERTER		1										A4
	7100329-1	DATA RCVR		1										A2
	7100328-1	1ST CONVERTER		1										A3
	7100330-1	RF FL NTWRK		1										A1
	7100424-2	CABLE ASSY (RF FL TO BLKHD)		1										W1
	7100425-1	CABLE ASSY (1ST CONV TO RF AMPL)		1										W2
	7100425-2	CABLE ASSY		2										W3,4

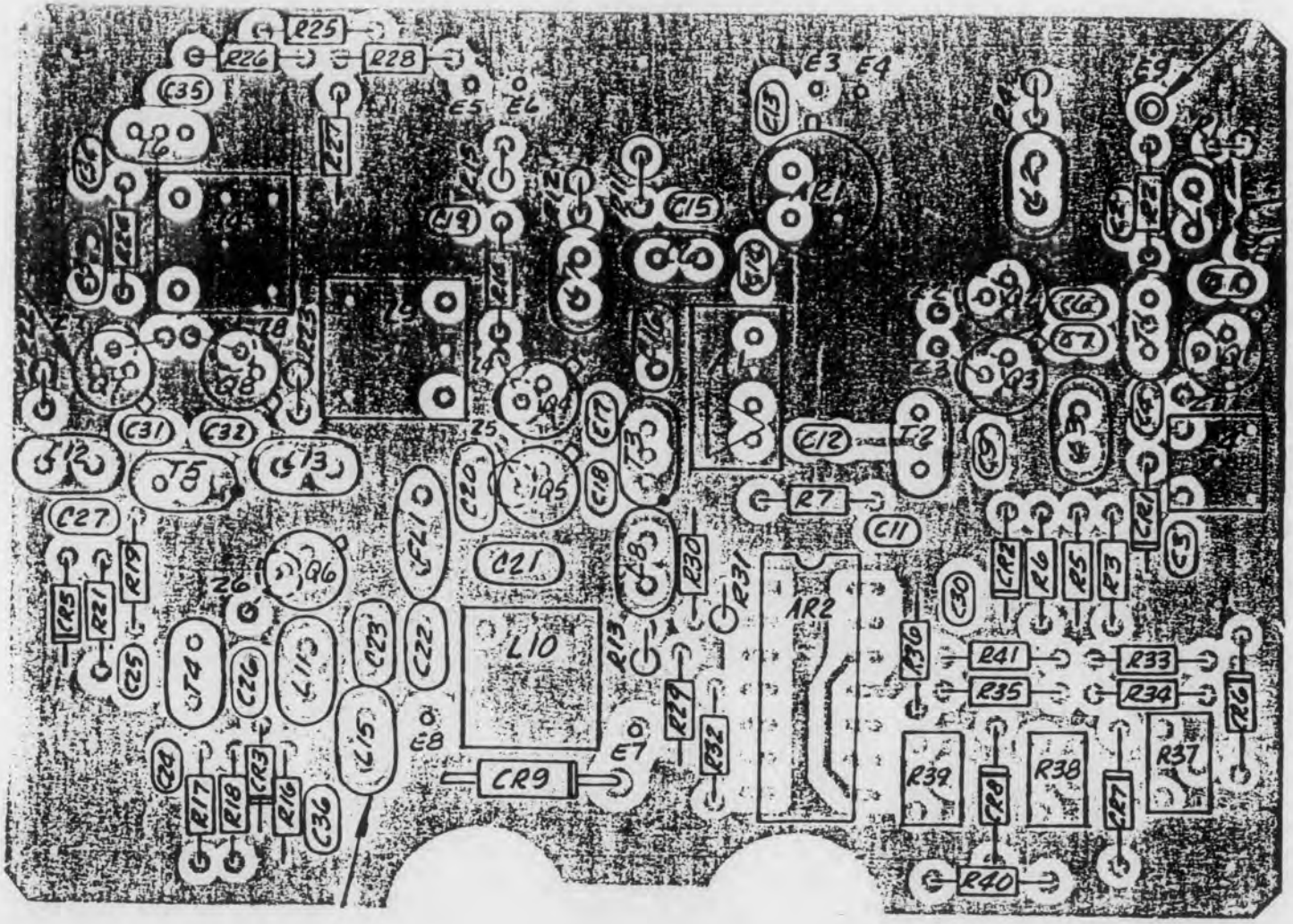
1100422

SHT 3 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER -1	QTY PER -10	QTY PER -11	QTY PER	QTY PER	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
3	2643000101	FERRITE BEAD	FAIR-RITE	19										Z1-19
4														
5	51-007-0000	CONN ST PLUG	SEALECTRO	1										P2
6	22-01-3047	CONN, 4 SOC	MOLEX	1										A2 P2
7	08-55-0102	CONTACT	MOLEX	4										
8	51-047-0000	CONN, BLKHD	SEALECTRO	4										J2-5
9	51-328-3188	CONN PLUG	SEALECTRO	2										A1P2, A5P1
0	4219-3633-0002	FILTER	VICLAN	5										FL1-5
1														
2	D20418-2	SCREW LOCK	CANNON	2										
3	2-56 x 3/16	SCREW	PAN HD PHILLIPS	39										
4	NO. 2	LOCK WASHER	SPLIT	39										
5	4-40 x 5/16	SCREW	PAN HD PHILLIPS	8										
6	4-40 x 3/16	SCREW	PAN HD PHILLIPS	27										
7	NO. 4	WASHER	SPLIT	35										
8	91114	GROMMET	H.H SMITH	2										
9	S203	EJECTOR	SCANBE	2										
0														
1	60-11-8302-1674	INSULATOR	CHOMERICS	3										
2	.002 THK x 1/2	TAPE, MYLAR	PERMACEL	A/R										
3	HPC-12	CABLE, CLIP	WECKESSER	2										
4	T18S	CABLE, TIE	TYTON CORP	4										

7100422
SH 4 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-10	-11			REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
45	E-26 AWG, BRN	WIRE, INSUL	MIL-W-16878	AR										
46	" , RED	"	"	AR										
47	" , ORN	"	"	AR										
48	E-26 AWG, YEL	WIRE, INSUL	MIL-W-16878	AR										
49	22 AWG	WIRE, TINNED BUS	QQ-W-343	AR										
50	RTV 108	ADHESIVE	G.E	AR										
51														
52	.10-32 1/4	SCREW	PAN HD PHIL	5										
53	NO. 10	WASHER	SPLIT	5										
54	10-32	NUT HEX	SMALL PATTERN	5										
55														
56														
57														
58														
59														
60														
61														
62														
63														
64														
65														
66														



7100327-1. SECOND CONVERTER

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL	DATE	TITLE	7100427
	APPVD R.D. Lee	DATE 8/	SECOND CONVERTER	
	CHECK B. BODIKER	DATE 1/18/84		SHEET 1 OF 5 REV D
	DRAWN M Hebb	DATE 1-12-84		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100422	7100423		
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
B	REWRITTEN WITH CHANGE (ECR 5401)	B. BODIKER	1/18/84
C	INCORP ECN 5596 7-4-84 Hfresh EFF: S/N 001 & ON	B. BODIKER	7/10/84
DR1	INCORP ECN 5713 EFF 4-6223 & ON KD 5-7-85	B. BODIKER	5/8/85

7100327
SH 2 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY REQ ASSEMBLY -1	QTY REQ ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	CONV VHF/UHF		X	-						
2	-2	CONV HF		-	X						
3	7100527	SCHEMATIC		REF	REF						
4	7100227-1	BOARD		1	1						
5	7100425-1	CABLE		1	1						(W1)
6	025-705-1	INDUCTOR 43μH CHOKE		5	5						L1,2,3,6,15
7	025-719-1	INDUCTOR 160μH CHOKE		5	5						L7,8,11,12,13
8	7100743-1	INDUCTOR, VARIABLE		1	1						L4
9	7100742-1	INDUCTOR, VARIABLE		2	2						L9,10
10	7100742-2	INDUCTOR, VARIABLE		1	1						L14
11	7100754-1	INDUCTOR VARIABLE		-	1						L16
12	025-739-1	TRANSFORMER 6.25:1		1	1						T1
13	025-704-1	TRANSFORMER 4:1		3	-						T2,4,6
14	025-711-1	TRANSFORMER 1.56:1		2	2						T3,5
15	025-704-1	TRANSFORMER 4:1		-	2						T4,6
16	025-079-1	INSULATOR		10	10						
17	025-908-1	XSTR/RES SET, U309		8	8						SEE SH 5
18	WEE-2.2	INDUCTOR 2.2μH	NYTRONICS	-	1						L5
19											
20	TFM-1H	MIXER	MINICIRUITS	1	1						A1
21	MWA-130	HYBRID IF AMPL	MOTOROLA	1	1						AR1
22	LM324N	IC OPER AMPL	NAT	1	1						AR2

M	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	ASSEMBLY -1	ASSEMBLY -2				QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100327 SH 3 OF D REMARKS
	DM5-EC270J	CAP, MICA 27pf	ELMENCO	-	1									C5
	0805C820G2T	CAP, CHIP 82 Pf	VICLAN OR ≈	-	1									C8
	C315C103K5R5CA	CAP, CER .01μF	KEMET	23	23									SEE SH 5
	DM5-CC040D	CAP, MICA, 4pF	ELMENCO	1	1									C16
	DM5-FY251J	CAP, MICA, 250pF	ELMENCO	1	1									C20
	DM5-FY151J	CAP, MICA, 150pF	ELMENCO	1	1									C21
	DM5-EC360J	CAP, MICA, 36pF	ELMENCO	2	2									C22, 33
	DM5-EY750J	CAP, MICA, 75 pF	ELMENCO	1	1									C23
	C320C104K5R5CA	CAP, CER, .1μF	KEMET	2	2									C26, 27
	DM5-EC430J	CAP, MICA, 43Pf	ELMENCO	-	1									C10
	HP5082-3081	DIODE,	HEWLETT-PACKARD	4	4									CR1, 2, 3, 5
	IN6263	DIODE		3	3									CR6, 7, 8
	IN4001	DIODE		1	1									CR9
	SFE10.7MA5-ZA	FILTER, 280KHz BW @ 10.7MHz	MURATA	1	1									FL1
	15Ω	Res, 1/8W, 5%	CARBON FILM	2	2									R2, 17
	3.3K	1/8W, 5%	↕	2	2									R3, 6
	10Ω	1/8W, 5%	↕	5	5									R7, 15, 25, 26, 28
	100Ω	RES, 1/2W, 5%	CARBON FILM	1	1									R11

7100327
SH 4 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2				REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
45	1K	RES, 1/8W, ±5%	CARBON FILM	4	4									R14,34,35,36
46	2.2K			2	2									R18,21
47	47Ω			1	1									R19
48	470Ω			1	1									R24
49	180Ω			1	1									R27
50	1M			1	1									R29
51	27K			1	1									R30
52	15K			1	1									R31
53	100K			2	2									R32,40
54	13K	RES, 1/8W, 5%	CARBON FILM	1	1									R33
55	3262W-1-104	RES, VAR, 100K	BOURNS	3	3									R37,38,39
56	10K	RES, 1/8W, 5%	CARBON FILM	1	1									R41
57														
58	2643000101	FERRITE BEAD	FAIR-RITE	8	8									Z1-8
59	4521B	TERMINAL	USECO	1	1									E9
60	AWG 24	WIRE, (1" LG)	TINNED, SOLID ANL QQ-W-343	A/R	A/R									E3,E5,E7,EE
61														
62														
63														
64	10234N	TRANSIPAD	MILTON ROSS	8	8									
65														
66														

REFERENCE DESIGNATORS

PL 7100327
SH 5 REV D

(ITEM 17)

Q1	≤	R1
Q2	≤	R4
Q3	≤	R5
Q4	≤	R12
Q5	≤	R13
Q6	≤	R16
Q7	≤	R22
Q8	≤	R23

.01 μF
(ITEM 25)

C1	C17
C2	C18
C3	C19
C4	C24
C6	C25
C7	C30
C9	C31
C11	C32
C12	C34
C13	C35
C14	C36
C15	

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	DATE	TITLE	PARTS LIST 7100428
APPVD	DATE	FIRST CONVERTER VHF/UHF RECEIVER	SHEET 1 OF 5 REV E
CHECK B. BODIKER	DATE 3/26/84		MWO
DRAWN [illegible]	DATE 9/15/83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100422			
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410			
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	ITEM 39 WAS 4P3401, MA/COM; ITEM 40 WAS IN4005	B. BODIKER	3/26/84
B	CHANGES PER BD LAYOUT / PER R. DEAN 1-8-84	B. BODIKER	3/26/84
BRI	ADDED ITEM 71 & 73 KD 3/1/84	B. BODIKER	3/26/84
BR2	SEE ECN 5404 [illegible] 3-20-84	B. BODIKER	3/26/84
C	ITEM 71 WAS 350-1498-09-05; ITEM 73 WAS 7717-3 EFF: S/N 001 & ON DISP: NONE KD 5/18/84	B. BODIKER	5/21/84
DR3	INCORP ECN 5482 EFF: S/N 002 & ON: DISP: REWORK CDK 7/12/84	B. BODIKER	7/20/84
E	INCORP ECN 5705; EFF: S/N 040 & ON CDK 8/7/84	B. BODIKER	8/8/84
R4	PICTORIAL CHG ONLY AB 11/5/84	B. BODIKER	11/5/84

FORM 101 A

M	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	7100328-1	CONVERTER		X										
	7100528	SCHEM		R										
	7100228-1	BOARD		1										
	025-705-1	INDUCTOR 43μH		9										L1,3,5, 10,11,12, 20,21,29
	025-079-1	INSULATOR		9										
	025-711-1	XFMR 1.56:1		1										T1
	025-704-1	XFMR 4:1		1										T2
0														
1	TAK-1WH	MIXER	MINI-CIRCUIT LAB	1										A1
2														
3	AM-147	RF AMPL HYB	ANZAC	1										AR1
4	MWA130	IF AMPL HYB	MOTOROLA	1										AR2
5	LM324N	IC QUAD OPER AMPL	NAT	2										AR3,4
6														
7	106RLR025M	CAP, 10μF 25V	ILL CAP	1										C59
8														
9	C315C103K5R5CA	CAP, CER, .01μF	KEMET	30						C2,3,6-8,10,15,16,20,21,23-28,33,36-41 45,51-56				
0	DM5-EC330J	CAP, MICA, 33pF	ELMENCO	2										C4,5
1	DM5-EC270J	27pF		1										C34
2	DM5-[illegible]620J	62pF												[illegible]11

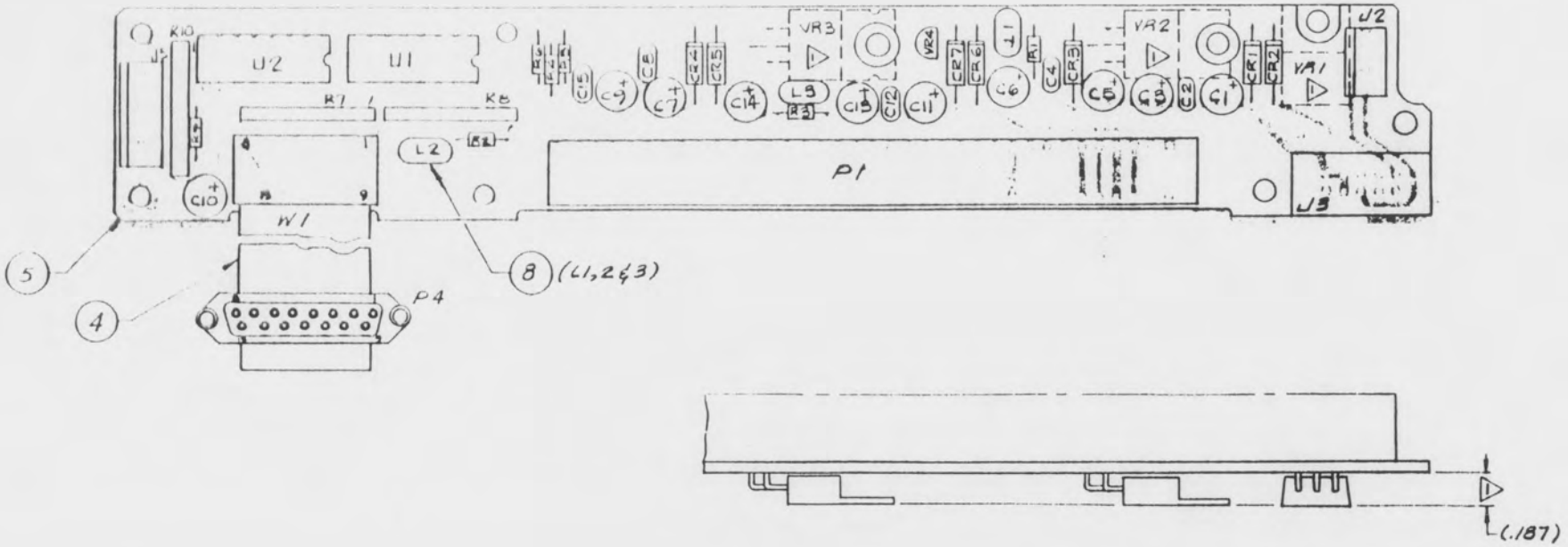
ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100329 3 OF 5 E REMARKS
3	DM5-CC030 D	CAP, MICA, 3pF	ELMENCO	1										C12
4														
5	GKU14R000	CAP. VAR 1.5-4 PF	SPRAGUE	1										C31
6	DM5-TBD	CAP, MICA TBD	ELMENCO	1										C22
7														
8	GKU18000	CAP, VAR 3.3-18 pF	SPRAGUE	2										C44,48
9	DM5-CC050 D	CAP, MICA, 5pF	ELMENCO	1										C32
10	DM5-CC040 D	4pF		1										C35
11	DM5-FY131 J	130pF		1										C42
12	DM5-CC120 J	12pF		1										C29
13	DM5-EC360 J	36pF		2										C46, 9
14	DM5-EC330 J	33pF		1										C43
15	DM5-CC020 D	CAP, MICA, 2pF	ELMENCO	1										C49
16	T350L686M025AS	CAP, TANT, 68 uF	KEMET	1										C57
17	C330C105K5R5CA	CAP, CER, 1 uF	KEMET	1										C58
18	0805B103K 2T	CHIP CAP 1 .01	VICLAN	3										C19, 18, 60
19	MA4P3401	DIODE, PIN	MA COM	10										CR1-10
20	1N4001	DIODE, RECT		1										CR11
21														
22														
23	51-051-0000	CONN COAX.	SEALECTRO	2										J1, J2
24	1-331677-4	SOCKET	AMP	8										

M	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100328 SH4 OF 5 E REMARKS
5	MS21400-13 SW-W-10	INDUCTOR 10μH CHOKE	NYTRONICS	8										L2,13,14,16,22 23,24,27
6	MS21401-19 SW-W-470	INDUCTOR 470μH, CHOKE	NYTRONICS	1										L31
7	WEE-1.0	INDUCTOR 1.0 μH CHOKE	NYTRONICS	1										L9
8	7100747-3	INDUCTOR, VAR		1										L17
9	7100747-4	INDUCTOR, VAR		1										L15
0	7100746-1	INDUCTOR, TOROID		1										L25
1	MS21400-7 SW-W-3.3	INDUCTOR 3.3μH CHOKE	NYTRONICS	2										L30, L32
2	025-908-1	FET / RES SET		4										Q1-4 R12,17,18,22
3	7100747-2	INDUCTOR		1										L18
4	7100746-2	IND. TOROID		1										L28
5	100Ω 1/2W	RES, CARB FILM 5%		1										R11
6	100K 1/8W			5										R2,5,7,10,16
7	330Ω			1										R3
8	11K			2										R4,9
9	390Ω 1/4W			1										R6
0														
1	15Ω 1/8W			2										R13,23
2	820Ω			4										R14,15,20,21
3	10Ω			1										R19
4	82K			1										R24
5	220K			1										R25
6	22K													R26

7100326 5 OF 5 E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
7	10K 1/8W	RES, CARB FILM 5%		3										R1,8,27
8														
9	IC WHITE	EPOXY PATCH	HYSOL	A/R										
0	2643000101	FERRITE BEAD	FAIR-RITE	4										Z1-4
1	350-1498-09-04	SPACER SWAGED	CAMBION OR EQ	5										
2	7-120-BA	HEATSINK	1 ERC	1										
3	10234N	TRANSIPAD	MILTON ROSS	1										
4	#26 AWG	SLEEVE, INSUL		A/R										
5	#26AWG	WIRE, BUSS		A/R										
6	7100756-1	INDUCTOR		1										L6
7	7100748-2	↑		1										L4
8	↕ -3	↕		1										L19
9	↕ -6	↕		1										L7
0	7100748 -5	INDUCTOR		1										L26

REVISED PER ECN 5468 CDK 3-15-84 B. BOOKER 3/14/84



SEE SEPARATE PARTS LIST

2. IDENTIFY BY BAGGING & TAGGING WITH PART NO. APPLICABLE DASH NO & REV LTR.
▷ INSTALL VR1, VR2, & VR3 USING JIG 7100931.
NOTES: UNLESS OTHERWISE SPECIFIED

QTY PER ASSY	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30 DECIMAL .X ± .1 .XX ± .03 .XXX ± .010 SURFACE J HOLE SIZES PER ANSI B32

7100423
7100422
NEXT OR ASSOC ASSEMBLY

DRAFT	C. KENNEDY	9/15/83
CHK'D	B. BOOKER	3/14/84
APP'D	MAY	3/20/84
APP'D		
PACKAGE		

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

DATA RCVR, RF MODULE

SIZE C | RSCM NO. 06994 | DWG NO. 7100329 | REV B

SCALE 2/1 | SHEET 1 OF 1

7100329 B

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE [illegible]	TITLE DATA-RCVR, RF MODULE	PARTS LIST 7100329
	APPVD R Decin	DATE 28 NOV 83		SHEET 1 OF 3 REV B
	CHECK G. Lauchi	DATE 11/4/83		MWO
	DRAWN [illegible]	DATE 10/28/83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100422	7100423		
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410	240-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	ITEM 20 WAS PT. NO. 22-23-2031	DR 1/6/83	B. BODIKER	1/9/84
B	INCORP ECN 5468	CDK 3-16-4	B. BODIKER	3/16/84

7100329

SH 2 OF B

ITEM NO	PART NO	DESCRIPTION	MFG CODE OR MANUFACTURER	ASSEMBLY -1	REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	7100329-1	DATA RCVR		X						
2										
3										
4	7100426-1	CABLE ASSY		1						W1 (P4)
5	7100229-1	P.W.B.		1						
6	7100529	SCHEMATIC		REF						
7										
8	025-079-1	INSULATOR		3						
9	025-719-1	INDUCTOR 160NH		3						L1,2,3
10	106RLR025M	CAP, 10μF, 25V	ILLINOIS CAP INC	8						C1,3,5,6, 10,11,13,14
11	C320C104K5R5CA	CAP, 0.1μF, 50V	KEMET	5						C2,4,8,12,15
12	226RLR016M	CAP, 22μF, 16V	ILLINOIS CAP INC	2						C7,9
13										
14										
15	IN4001	DIODE		7						CR1-7
16										
17										
18										
19	1-102584-0	CONNECTOR 10 POS RECPT	AMP	1						P1
20	22-11-2042	CONN, 4PIN	MOLEX	1						J2
21	609-1027	CONN, 10 PIN	T&B/ANSLEY	1						J3
22	22-11-2062	CONN, 6PIN	MOLEX	1						J5

7100329 3 OF 8

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
3														
4														
5														
6														
7														
8	10Ω	RES, CARB FILM 1/8W, ±5%		3										R1,2,3
9	100K	RES, CARB FILM 1/8W, ±5%		3										R4,5,6
10	MSP08A03-103J	RES, 10K, 8 PIN SIP	DALE OR EQ	3										R7,8,10
11	10K	RES, CARB FILM 1/8W, ±5%		1										R9
12														
13														
14														
15														
16	4094BP	I.C.		2										U1,2
17														
18	UA7810CKC	VOLTAGE REGULATOR	TEXAS INS.	1										VR1
19	MC7812CT	VOLTAGE REGULATOR	MOTOROLA	1										VR2
20	MC7805CT	VOLTAGE REGULATOR	MOTOROLA	1										VR3
21	MC79L12ACP	VOLTAGE REGULATOR	MOTOROLA	1										VR4
22														
23														
24														

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San Diego, Cal. 92121

REL	DATE	TITLE	PARTS LIST
APPVD D. Mag	DATE 5-11-84	RF FILTER NETWORK UHF/VHF RECEIVER	710[illegible]330
CHECK B. BODIKER	DATE 2/13/84		SHEET 1 OF 7 REV L
DRAWN [illegible]	DATE 2-3-84		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100422			
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410			
RELEASE DATE MTL REQD	⚠1 DASH NO. = REF DESIGNATION				
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
B	REVISED & REWRITTEN, SEE OBSOLETE FILE FOR "A" LEVEL, 2-3-84	[illegible]	B. BODIKER	2/13/84
C	INCORP ECN 5568	KD 4/24/84	B. BODIKER	5/3/84
D	INCORP ECN 5611, EFF: 001 & ON	KD 8/31/84	B. BODIKER	9/21/84
E	INCORP ECN 5634, EFF: 001 & ON	KD 8/31/84	B. BODIKER	9/21/84
F	REDRAWN EFF: 020 & ON	KD 8/31/84	B. BODIKER	9/21/84
G	INCORP ECN 5957 EFF 042 & ON	KD 2-28-85	B. BODIKER	3/5/85
H	INCORP ECN 5976 EFF: 042, 043, 044, 074 & ON	KD 2-28-85	B. BODIKER	3/5/85
JR2	INCORP ECN 6018 EFF: 074 & ON	KD 3-13-85	B. BODIKER	5/1/85
K	INCORP ECN 6105 EFF: 074 & ON	KD 5-23-85	B. BODIKER	6/5/85
L	INCORP ECN 6178, EFF: 085 & ON	KD 8-15-85	B. BODIKER	9/4/85

7100330
SH 2 OF 7 | L

ITEM NO	PART NO	DESCRIPTION	MANUFACTURER OR MANUFACTURER	DATA FEED ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	-1	FL NTWK		/										
	7100230-1	PWB		1										
	7100530	SCHEM		REF										
	025-705-1	INDUCTOR, RF CHOKE, 43uH		6										L53,54,59-62
	025-719-1	CHOKE		4										L35, 37, 38, 39
	025-079-1	INSULATOR		11										
	7100732-1	IND, VARIABLE	DASH NO = REF DESIGNATOR	20										L6, 7, 11-16, 18, 20-23 26-28, 64-67
	7100733-4	IND,		1										L30
	7100733-5	IND,		1										L31
	7100744-4	IND,		1										L40
	7100744-1	IND,		2										L8,9
	7100744-2	IND, VARIABLE		1										L4
	7100744-5	INDUCTOR, VARIABLE		1										L44
	025-746-1	INDUCTOR RF CHOKE, 10uH		4										L33,41,42,45
	025-736-1	XFMR		1										T1
	7100738-1	XTL 10MHz		1										Y1

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100330 SH 3 OF 7 L REMARKS
3	7100710-1	FLTR (400/520)	K&L P/N (8-B380-460/136-P/P)	1										FL1
4	7100710-2	FLTR (280/400)	K&L P/N (8-B380-340/136-P/P)	1										FL2
5	7100710-3	FLTR (175/280)	K&L P/N (7-B120-227.5/119-P/P)	1										FL3
6	7100438-1	COAX, STRAIGHT	(RG 405)	1										W2
7	7100438-2			1										W8
8														
9	7100438-4			1										W7
10	7100438-5			1										W6
11	7100438-6	COAX, STRAIGHT		1										W4
12	7100439-1	COAX, BENT		1										W5
13	7100439-2			1										W3
14	7100439-3			1										W9
15	7100439-4			1										W10
16	7100439-6	COAX BENT	(RG 405)	1										W1
17	51-051-0000	CONN, COAX	SEALECTRO	2										J1, J2
18	56-712-003	CONN, FLTR ISP	SPECTRUM CONTROL	1										J3
19	MS21399-8 SW-W 0.39	INDUCTOR .39 μH	NYTRONICS	6										L46-50, 63
20	MS21400-7 SWW-3.3	INDUCTOR 3.3 MH	NYTRONICS	8										L2, 3, 5, 10, 17 24, 29, 34
21	MS21400-9 SW-W-4.7	INDUCTOR 4.7 MH	NYTRONICS	1										L36
22														
23	MS21401-7 SW-W-47	INDUCTOR 47 MH	NYTRONICS	1										L43
24	MS21399-11 SW-W 0.68	INDUCTOR .68 μH	NYTRONICS	4										L51, 52, 57, 58

7100330
SH 4 OF 7 L

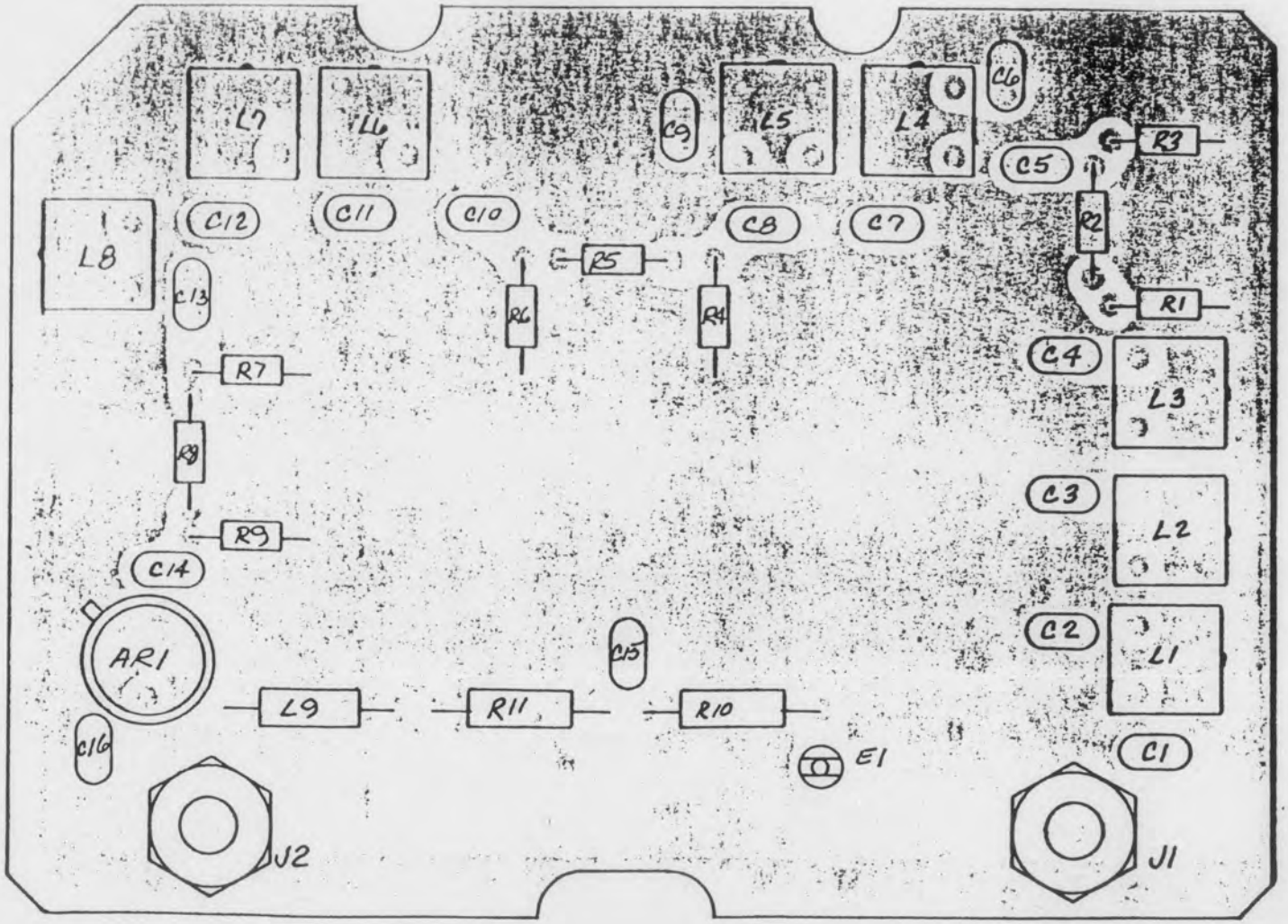
ITEM NO	PART NO	DESCRIPTION	MANUFACTURER OR MANUFACTURER	ASSEMBLY -1					TOTAL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
5	MS21400-1 SW-W 1.0	INDUCTOR 1.0uH	NYTRONICS	2										L55,56
6	LM358N	IC	NAT	1										AR1
7														
8	0805C102K2T	CAP, CHIP, 1000 pf	VICLAN	9										C1,2,3,5,9,12,45 56,82
9														
10	DM5-FY101J	CAP, MICA 100 pf	ELMENCO	16								C4,10,11,15,16,27,30,31,35,54,55, 58,63,67,103,110		
11														
12														
13														
14	DM5-FY271J	CAP, MICA 270pf	ELMENCO	5										C18,20,21, 59 75
15	C315C103K5R5CA	CAP CER, .01 MF	KEMET	14									C7,22,33,34,36,57,68, 69,81,101,107,109,99,112	
16														
17														
18	DM5-EC620J	CAP, MICA, 62 Pf	ELMENCO	3										C23,28,32
19	DM5-FY161J	160Pf		3										C24,62,65
20	DM5-EC430J	43Pf		4										C25,50-52
21	DM5-EC470J	47Pf		1										C26
22	DM5-EC330J	33Pf		4										C37,40,44 71
23	DM5-CC180J	18Pf		2										C38,39
24	DM5-EC270J	27Pf		2										C41,53
25	DM5-EC560J	CAP, MICA 56 Pf	ELMENCO	2										C42,43
26														

ITEM NO	PART NO	DESCRIPTION	MANUFACTURER OR MANUFACTURER	QTY PER ASSEMBLY -1					TOTAL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	100330 SH 5 OF 7 L REMARKS
7														
8	DM5-CC200J	CAP, MICA 20pf	ELMENCO	2										C46,48
9	DM5-CC120J	12pf		1										C47
0	DM5-CC150J	15pf		1										C49
1	DM5-EY680J	68pf		1										C60
2	DM5-EY750J	75pf		1										C61
3	DM5-FY151J	150 pf		3										C70,76,80
4	DM5-FY391J	390 pf		2										C72,100
5	DM5-FY111J	110 pf		1										C73
6	DM5-FY121J	120 pf		1										C74
7	DM5-FY251J	CAP, MICA 250pf	ELMENCO	1										C78
8														
9	106RLR025M	CAP, 10MF 25V	ILL CAP	4										C84,88,91,93
0	226RLR016M	CAP, 22 µF 16V	ILL CAP	1										C86
1	C320C104K5R5CA	CAP, CER, .1 MF	KEMET	14										C8,13,83,85,87,89,90, 92,94-98,111
2														
3	C315C681K2R5CA	CAP, CER, 680pF	KEMET	1										C105
4	DM5-EC500J	CAP, MICA 50pf	ELMENCO	1										C102
5	GKU18000	CAP, VARIABLE 3.3-18pf	SPRAGUE	1										C106
6	C315C102K1R5CA	CAP, CER .00lmF	KEMET	4										C6,14,104,108
7	MA-47054	DIODE	MACOM	42										CR1-39,54-56
8	IN4148	DIODE		11										CR41-51

7100330
SH 6 OF 7 L

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
9	HP5082-3081	DIODE	H.P.	2						CR52, 53
0	MPS6523	XSTR	MOT	17						Q1-17
	MPS6521	XSTR	MOT	1						Q18
2	2N5179	XSTR		1						Q19
3	BFW 92A	XSTR	MOT	1						Q20
4	820Ω 5%	RES. CF 1/8W		5						R1,68,70,74,76
5	180Ω			2						R2, 75
6	470Ω			18						R3,6,9,10,13,15,17,19-21,23, 24,26,28-31,35
7										
8	6.8Ω			5						R8,11,16,22,25
9	10K			11						R5,14,18,27,32,33 49,53,54,58,59
00	10Ω			3						R36-38
01	6.8K 5%	1/8W		9						R39-46, 69
02	RNC50H1103FS	METAL FILM RES 1/20W, 1% 110K		1						R47
03	RN50C1002F	10K		1						R48
04	RN50C1003F	100K		1						R50
05	RNC50H6043FS	METAL FILM RES 1/20W, 1% 604K		1						R51
06	1K 5%	1/8W		2						R52, 55
07	100K			1						R56
08	560Ω			1						R57
09										
10	22Ω 5%	1/8W								60

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					TOTAL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	100330 SH 7 OF 7 L REMARKS
1	100Ω 5%	RES, CF, 1/8W		1										R61
2	300Ω	"		4										R62, 64, 65, 67
3	18Ω	"		2										R63, 66
4	1.8K	"		1										R73
5	24Ω 5%	RES, CF, 1/8W		2										R71, 72
6	1.2K, 5%	RES, CF, 1/8 W		1										R77
7	2-56 X 3/16	SCREW,	PH PN HD	6										
8	4-40 X 5/16	SCREW	PH PN HD	2										
9														
10	#2	WASHER, SPLIT		6										
11	#4	WASHER, SPLIT		2										
12														
13	4-40	NUT, RADIO		2										
14														
15	AWG 22	WIRE, BUS	MIL-W-343	AR										
16	FP-301-1/8	TUBING HEAT SHRINK	ECC	AR										
17														
18														
19														
20														
21														
22														



7100343-1. Synthesizer Filter

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	DATE 4/3/84	TITLE	HARIS LIST 7100343
APPVD	DATE	SYNTEK FLTR 3045	
CHECK B. BODIKER	DATE 3/29/84		SHEET 1 OF 3 REV C
DRAWN	DATE 3-26-84		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100422			
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410			
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD DATE
A	INCORP ECN 5620 (BY ADDING ITEM 2) 6/11/84	B. BODIKER 6/11/84
B	INCORP ECN 5739 lot 9/26/84 EFF: 3-6372 & ON	B. BODIKER 10/4/84
C	INCORP ECN 5811 lot 9/26/84 EFF: SERNO 021 & ON	

7100343
SH 2OF C

ITEM NO	PART NO	DESCRIPTION	SOURCE OR MANUFACTURER	QTY PER ASSEMBLY -1					REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	BD ASSY		/										
2														
3														
4	7100243-1	PWB		1										
5	7100543	SCHEMATIC		REF										
6														
7														
8	7100750-3	INDUCTOR		1										L5
9	7100750-2	INDUCTOR		1										L4
10	7100750-4	INDUCTOR		3										L1, L2, L3
11	7100750-1	INDUCTOR		3										L6, L7, L8
12														
13	MWA120	AMPLIFIER	MOTOROLA	1										AR1
14														
15	DM5-CC070D	CAP, MICA, 7pF	ELMENCO	2										C1, C4
16	DM5-CC150J	CAP, MICA, 15pF	ELMENCO	4										C2, C3, C7, C9
17	DM5-CC200J	CAP, MICA, 20pF	ELMENCO	1										C5
18	DM5-EC510J	CAP, MICA, 51pF	ELMENCO	1										C6
19	DM5-EC330J	CAP, MICA, 33pF	ELMENCO	1										C8
20	DM5-CC180J	CAP, MICA, 18pF	ELMENCO	2										C10, C13
21	DM5-CC100J	CAP, MICA, 10pF	ELMENCO	2										C11, C12
22	DM5-FY221J	CAP, MICA, 220pF	ELMENCO	2										C14, C16

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3 OF C

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
3														
4	C320C104K5R5CA	CAP, CER .1μF	KEMET	1										C15
5														
6	2000B	TERMINAL	USECO	1										E1
7	51-051-0000	CONNECTOR	SEALECTRO	2										J1, J2
8	MS21400-1 SW-W-1.0	INDUCTOR, 1μH	NYTRONICS	1										L9
9														
10														
11	300Ω	RES, CF 1/8W 5%		4										R1, R3, R7, R9
12	18Ω	RES, CF 1/8W 5%		2										R2, R8
13	130Ω	RES, CF, 1/8W 5%		2										R4, R6
14	47Ω	RES, CF, 1/8W 5%		1										R5
15	82Ω	RES, CF, 1/4W 5%		2										R10, R11
16														
17														
18														
19														
20														
21														
22														
23														
24														

FREQUENCY SYNTHESIZER

ASSEMBLY: 7100418

SCHEMATIC: 7100818
7100504
7100505
7100540
7100805
7100819

SECTION I

DESCRIPTION

1.1 General

The first local oscillator frequency is generated by a phase-locked synthesizer. A phase-locked synthesizer multiplies the reference frequency by a variable number, N. It does this by dividing its output frequency (LO output) by that variable number and adjusting the output frequency so that, after division, it is equal to the reference frequency. A simple loop is shown in figure 1.

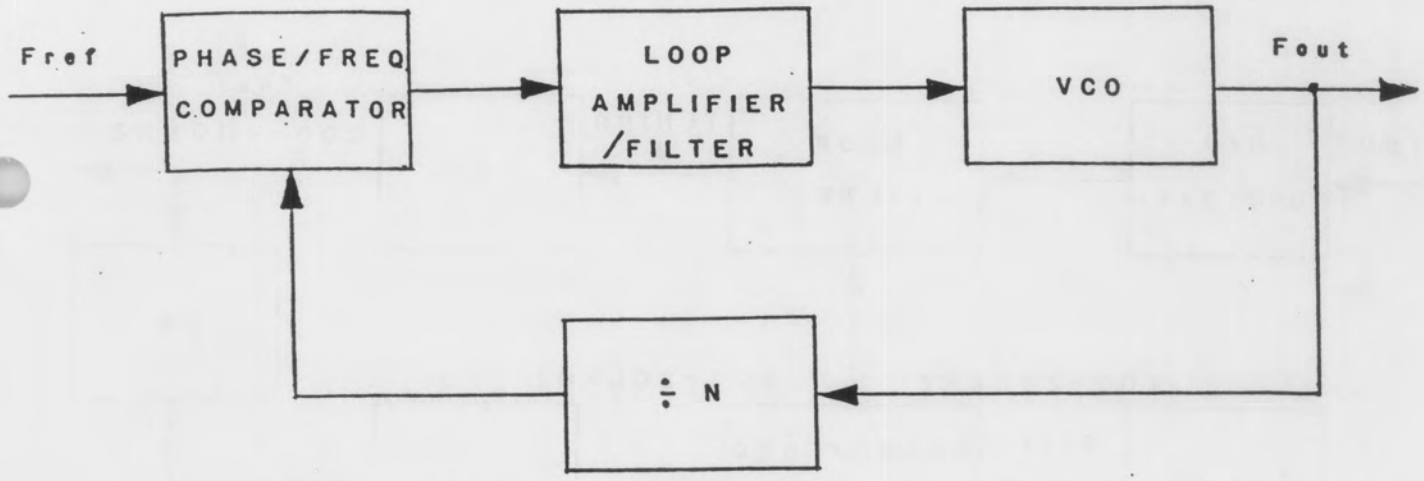


Figure 1. Simplified Block Diagram, Phase-Lock Synthesizer.

When the synthesizer is locked, the two inputs to the phase comparator have a constant phase relationship and must, therefore, have the same frequency. The output freuency, fo is:

$$fo = Nfr$$

When the voltage controlled oscillator (VCO) frequency drifts, the phase detector begins to produce short duration pulses (positive or negative as required). The filter integrates these pulses to provide a tuning voltage to the VCO, causing the VCO frequency to increase or decrease to counteract the drift. The loop filter suppresses frequencies that could cause undesirable modulation of the VCO. The loop filter also affects acquisition of lock, response speed and loop stability.

Current systems require a rapid lock rate, high (step) resolution and high spectral purity. The single loop configuration is not compatable with all these requirements. A multi-loop synthesizer is required to attain the desired performance characteristics. A simplified block diagram of the multi-loop synthesizer is shown in figure 2.

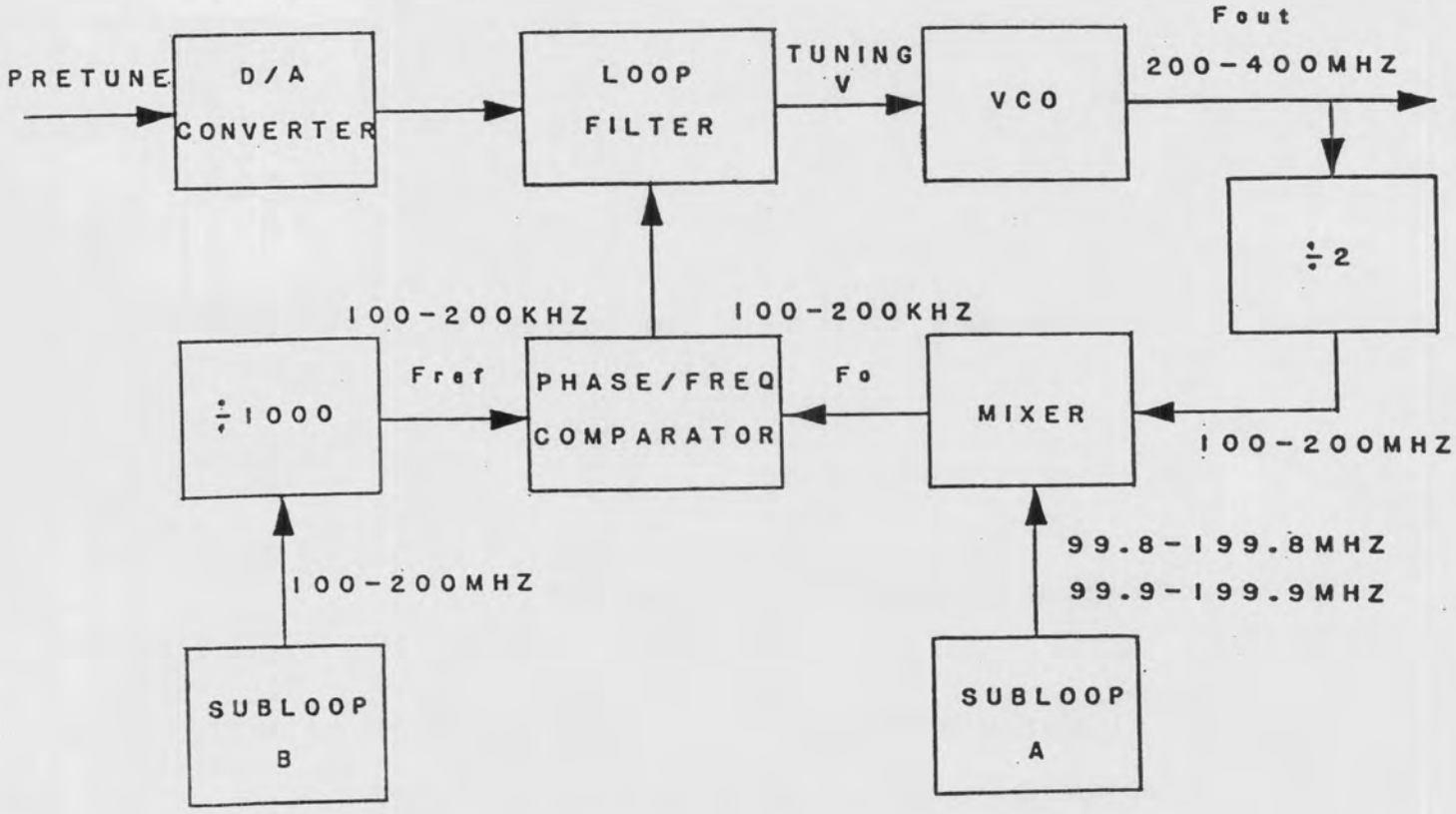


Figure 2. Simplified Block Diagram, Multi-Loop Synthesizer.

Coarse tuning of the VCO is accomplished by the digital to analog converter during the period the subloops are tuning. Control of the main loop is accomplished thru the use of the two subloops.

The two subloops are identical. They contain a modulo controlled, ÷ by 20/22 prescaler and ÷ by N logic circuitry and a four range VCO with an output range of approximately 100-200 MHz. Subloop "A" provides the 100 kHz through 100 MHz increments, while subloop "B" provides the 100 Hz through 10 kHz increments for tuning the main loop.

The main loop works as follows. The VCO output of 200-400 MHz is divided by two (÷ 2) and mixed with subloop "A" output frequency (100-200 kHz below) to provide a difference frequency (fo-fa) of 100-200 kHz. The actual difference frequency is dependent on the frequency setting of subloop "B".

The frequency set by subloop "B" is divided by 1000 (÷1000) and compared to the difference (fo-fa) frequency in the phase/frequency comparator. The division by 1000 produces 100 Hz increments in the reference frequency of the main loop. Therefore, the reference frequency of the main loop is 100 to 200 kHz varied in 100 Hz increments.

The phase/frequency comparator output will vary when the VCO output frequency drifts in comparison to the reference. The output of the phase/frequency comparator will be pulses whose duty cycle varies due to phase shift of the VCO frequency in comparison to the reference frequency. These pulses are integrated in the loop filter which removes undesirable noise modulation and provides a dc tuning voltage to the VCO.

The level of this tuning voltage will vary in accordance with the phase or

frequency difference between the reference frequency and the VCO frequency. If the VCO frequency increases, the tuning voltage will decrease. This causes a decrease of VCO output frequency. In like manner, a decrease in VCO frequency will cause an increase in tuning voltage, thus increasing VCO frequency and once again stabilizing the loop.

The two subloops input data from the microprocessor to the main loop for tuning the VCO. The 100 Hz to 10 KHz inputs are processed by subloop "B" and the 100 KHz to 100 MHz inputs are processed by subloop "A". The subloops operate between 100-200 MHz.

The key to understanding operation of the subloops is in the frequency division circuits. A simplified block diagram of the subloop appears in figure 3.

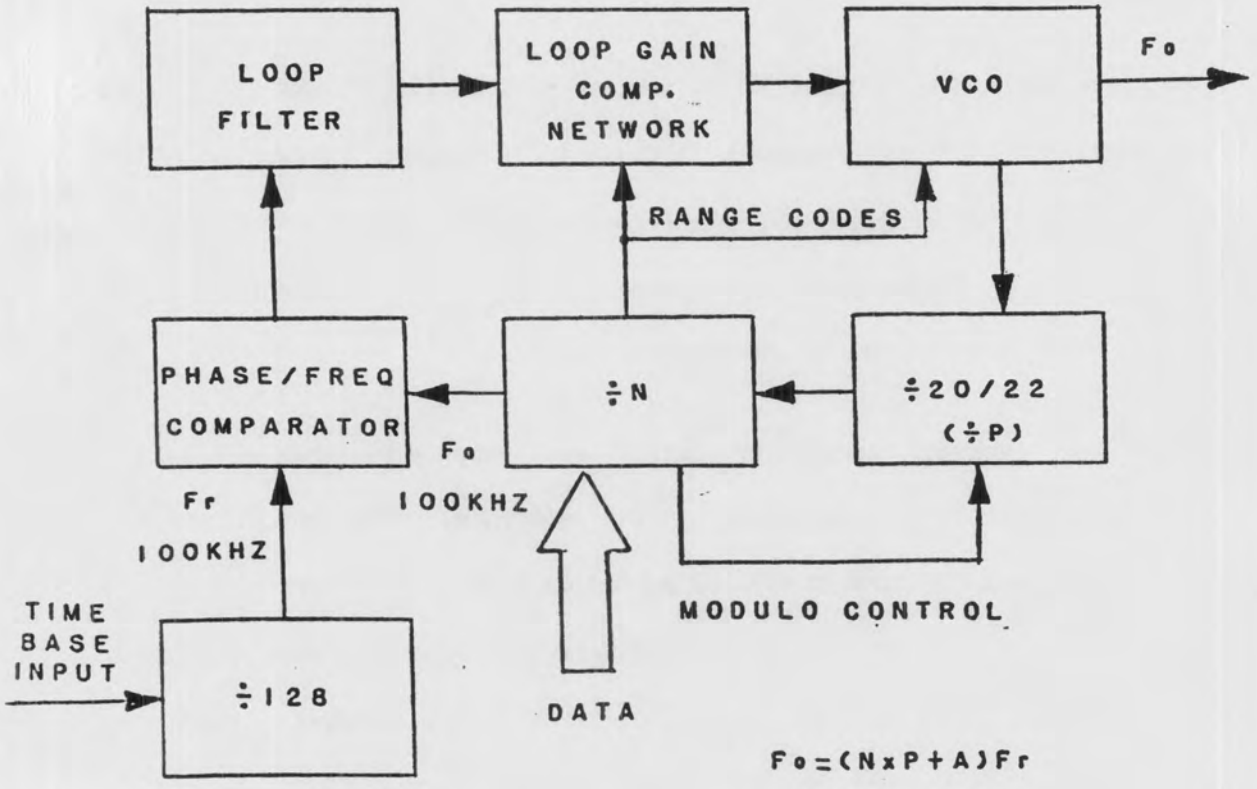


Figure 3. Simplified Block Diagram, Subloop.

As previously stated the formula for the frequency out of a basic loop is:

$$fo = Nfr$$

Adding the prescaler to this the formula is:

$$fo = (NxP)\ fr$$

If the subloop reference frequency is 100 kHz and assuming the basic division of the prescaler is 20, the formula is:

$$fo = (20xN)\ 100\ kHz$$

With these conditions the frequency out (100-200 MHz) can only vary in 2 MHz steps. This is limited by the reference frequency (which if lowered would change the performance characteristics), and the division by N which requires an integer input to attain the 100 kHz reference frequency at the output. N will vary between 50 and 100. Consider the examples below:

N = 52	N = 53
fo = (20x52) 100 kHz	fo = (20x53) 100 kHz
fo = 104 MHz	fo = 106 MHz

The output frequency must be variable in 100 kHz steps. To accomplish this the modulo control, which consists of an additional counter and control logic circuitry is added to the circuitry and to the equation. The modulo (A) control is a variable between 0 and 20. The formula has now become:

$$fo = (NxP+A)\ fr$$

The modulo control will determine whether the output frequency will be divided by 20 or 22 in the prescaler. For ease of understanding consider the problem in this manner. In the previous examples the output

frequencies were 104 MHz and 106 MHz. Suppose the output frequency desired is 105 MHz, halfway between 104 and 106 MHz. The loop filter acts as an averaging filter for the loop. Therefore, if the output over twenty loop cycles would appear to the loop filter as 104 MHz ten times and 106 MHz ten times it would average out to 105 MHz. This is the effect attained thru the use of the modulo control. The formula for 105 MHz now becomes:

$$fo = (NxP+A)\ fr$$

$$fo = (52x20+10)\ 100\ kHz$$

$$fo = 105\ MHz$$

(where A is the modulo count number)

In order to attain a difference of 100KHz in the output, assume that the output frequency is 104.1 MHz. This now allows the output to appear to the loop filter as 104 MHz nineteen times and 106 one time. The formula for 104.1 MHz now becomes:

$$fo = (NxP+A)\ fr$$

$$fo = (52x20+1)\ 100\ kHz$$

$$fo = 104.1\ MHz$$

The control center for the subloop is contained in one chip (U2), an MC145156 PLL frequency synthesizer. This chip contains the $\div N$ circuitry, the modulo control ($\div A$), the phase detector and the $\div$ 128 function which establishes the 100 kHz reference frequency. U2 also provides the coded inputs to the range switches. The connection diagram for this chip is figure 4.

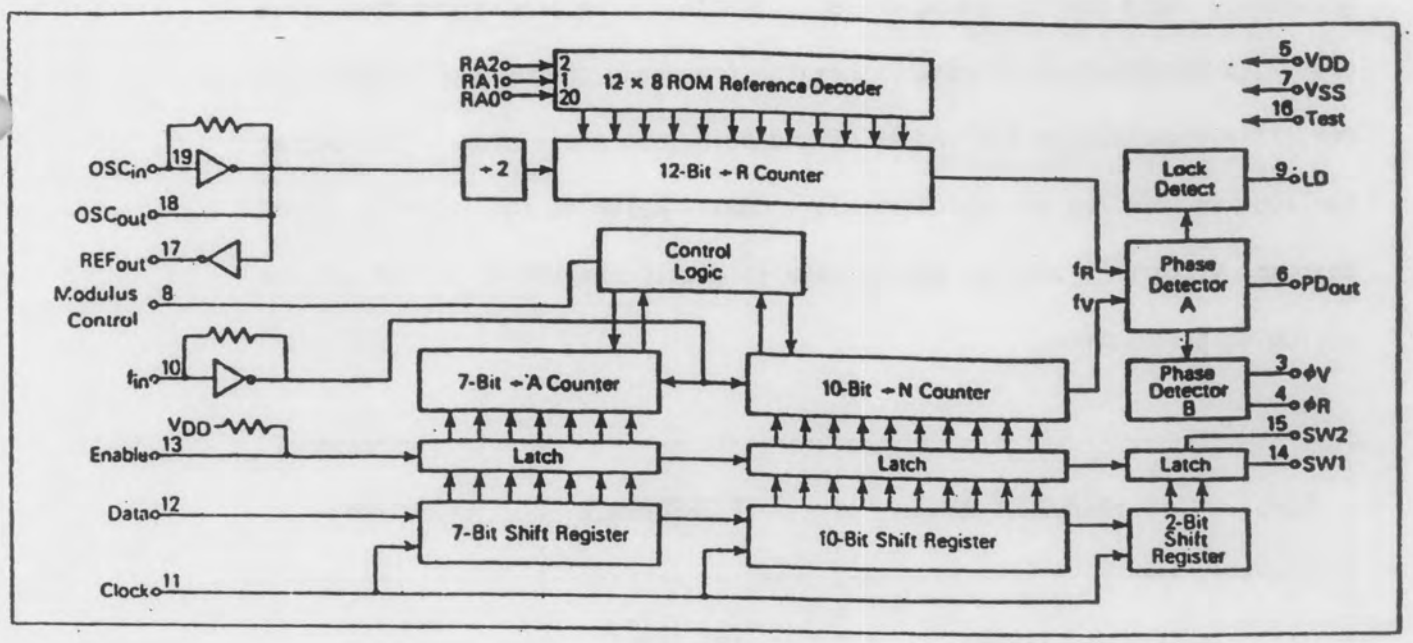


Figure 4. Connection Diagram, MC145156 Frequency Synthesizer

The loop filter integrates the phase detect outputs, and provides a dc control voltage output to the VCO. The loop gain compensation network adjusts VCO control voltage to give a more constant gain across the various ranges of the VCO.

The entire assembly is mounted on a carrier board, with the main loop and subloop assemblies enclosed in cast metal housings and with machined covers, providing RFI protection to the synthesizer (A2) module.

1.2 Circuit Description

The multiloop synthesizer is the first local oscillator for the ADFS system. It develops the first IF across eight ranges and is adjusted 110.7 MHz above the RF input for all ranges of the model 240/2040 receiver. For the model 345/3045, the adjustment is either above or below the RF input in

accordance with the following table (Table 1). The inputs are data from the data processor which establishes the frequency output and compensates for differences across the ranges of the main loop oscillator. The output is 100 to 400 MHz at approximately +5dbm. Refer to the overall block diagram (figure 5) and the appropriate schematic drawing as listed in the following discussions.

BAND	RF FREQUENCY RANGE	IF FREQUENCY	INJECTION
1	20-115MHZ	137.75MHZ	+
2	115-175MHZ	74MHZ	+
3	175-260MHZ	137.75MHZ	+
4	260-280MHZ	74MHZ	+
5	280-290MHZ	74MHZ	-
6	290-400MHZ	137.75MHZ	-
7	400-425MHZ	74MHZ	-
8	425-520MHZ	137.75MHZ	-

Table 1. First Local Oscillator Frequency Ranges (3045)

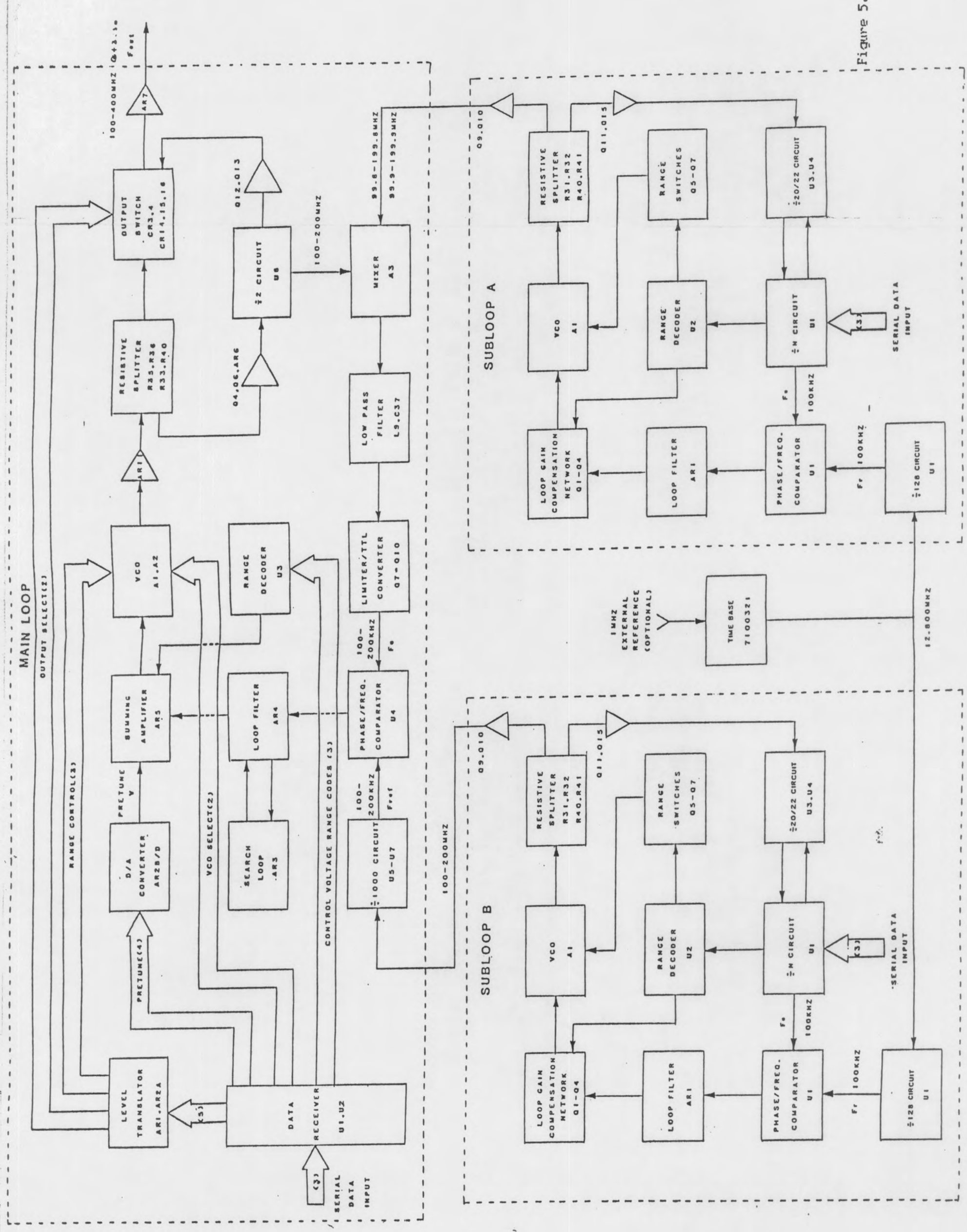


Figure 5. Multiloop Synthesizer Block Diagram

1.2.1 Synthesizer Subloop Board

Refer to the synthesizer subloop schematic (drawing 7100504) during the following discussion. The microprocessor inputs at P1 (pins 5, 6 and 7) consist of a serial data input to pin 12 of U1, a clock input to pin 11, and an enable input to pin 13. Fault detection is provided by AR2. A reference of about 4.5 volts is set at pin 5 input of AR2 by division of the +9V supply voltage. The active input is a high from pin 9 of U1 when lock is detected. If lock cannot be achieved, AR2 will output +12Vdc and output a $\overline{\text{FAULT}}$ signal at P1 pin 8, and light LED CR11.

Q16 is a capacitance multiplier developing +9Vdc from the +12Vdc input as supply voltage to U2 and to other circuits on the board. Voltage regulators VR1, VR2 and VR3 also develop input power of +12V, -12V and +5Vdc to the board, CR13, CR15 and CR17 provide reverse polarity protection to the circuitry. Diodes CR14, CR16, and CR18 protect the regulators during capacative discharge when power is turned off.

The serial data at pin 12 of U1 consists of 19 bits clocked into a shift register. The data input from the data processor consists of a two bit code input to the range decoder (output at U1 pins 14 and 15), and local oscillator frequency information binary coded to program the $\div$ N and $\div$ A counters. When all nineteen bits are clocked in, a high enable transfers them to the counter inputs.

The $\div$ N counter counts down from its programmed value, counting the prescaled VCO frequency (input at U1, pin 10). When count down is completed a phase pulse is output to the phase comparator circuit

of U1. 12.800 MHz from the time base is fed to U1 pin 19 via P1, pin 10 divided by 128 to provide a stable 100 KHz reference signal to the phase comparator.

The phase/frequency comparator output from U1 is at pins 3 and 4. When the reference frequency input and the ÷ N input (from the VCO) are both 100 KHz and in phase, the loop is locked and the VCO is on frequency. Thus, pin 9 output is high to the fault detector, and pins 3 and 4 are both high, matching the inputs to the loop filter AR1. A quiescent dc control voltage level is established to the input of the VCO.

If VCO frequency increases or leads in phase, low pulses will be output from U1 (pin 3) to the non-inverting input of AR1. Then -12V pulses at the output of AR1 (pin 6) are integrated and decrease the control voltage driving the VCO frequency down until lock is attained.

If VCO frequency decreases or lags in phase, low pulses will be output from U1 pin 4 to the inverting input of AR1. +12V pulses at the output are integrated and increase the control voltage driving the VCO frequency up until lock is attained.

When the microprocessor tunes the VCO to a different frequency the ÷ N integer will increase or decrease to match the setting. The output frequency of the local oscillator will divide to above or below 100 KHz and drive the local oscillator up or down until lock is attained.

The loop filter AR1 establishes a 3 KHz loop bandwidth, and R1 balances the sidebands by adjusting the impedance across the two inputs. The loop filter suppresses noise and spurious frequencies

that could cause undesirable modulation of the VCO.

The loop gain compensation network (Q1-Q4) adjusts the quiescent VCO control voltage at C6 by switching resistance into the circuit to maintain more constant gain across the four VCO ranges. Range switches (Q5-Q7) switch inductors into the VCO. Two bit binary inputs from U1 (pins 14 + 15) to U2 (pins 2 + 3) will output a low to the selected range switches with results as shown in Table 2.

	U2 INPUTS		U2 OUTPUTS				SWITCHING OUTPUTS						
RANGE SETTINGS	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	Q1	Q2	Q3	Q4	Q5	Q6	Q7
BAND 1 100-120MHZ	0	0	0	1	1	1	ON	OFF	OFF	OFF	OFF	OFF	OFF
BAND 2 120-140MHZ	0	1	1	0	1	1	OFF	ON	OFF	OFF	ON	OFF	OFF
BAND 3 140-168MHZ	1	0	1	1	0	1	OFF	OFF	ON	OFF	OFF	ON	OFF
BAND 4 168-200MHZ	1	1	1	1	1	0	OFF	OFF	OFF	ON	OFF	OFF	ON

TABLE 2. Loop Gain Compensation Network Operation

The switched range VCO is a plug-in subassembly (A1), and Q8 is a capacitance multiplier providing -8Vdc to the oscillator from the -12 V source on the subloop board. VCO output frequency (fo) at A1 pin 12 is amplified by Q9 and output to the main loop via J2. The oscillator frequency at the output (J2) is 100-200 MHz at approximately +3dbm.

The oscillator frequency is also fed back to U4 to complete the loop. A resistive splitter consisting of resistors R31, R32 and R40, R41

provides outputs to amplifiers Q12 and Q9. Two stages of amplification provide a +3dbm output to U4 from a -20dbm input to Q12.

U3 and U4 form the ÷ 20/22 circuit with output to the ÷ N counters via pin 10 of U1. When modulo control is used, the ÷ A counter will output a high prior to the end of the ÷ N count. When the high from U1 (pin 8) is present on pin 11 of U4, the prescaler will divide by 22. This will alter the (clock) frequency input to U1 (pin 10) thus varying the time 1/N to attain 100 KHz output. The phase/frequency comparator output at U1, pins 3 and 4, is then fed to the loop filter completing the loop.

1.2.2 Switched Range VCO

The switched range VCO (schematic drawing 7100805) is a circuit board mounted in a metal box for RF shielding. The metal box plugs into, and is a subassembly of the synthesizer subloop board. The VCO output (at E7) is 100-200 MHz in four separate ranges as selected by the switches on the subloop board. The switches control the inductance of the oscillator tuned circuit by forward biasing the PIN diodes (CR5-CR7) as applicable. The capacitance of the tuned circuit is controlled by the dc input from the PLL at E3. Varying control voltage across the varactors (CR1-CR4) varies the oscillator frequency, allowing the PLL to adjust the VCO output.

Supply voltage of -8Vdc is input at E3 from Q8 on the subloop board. External ground is provided at E2.

1.2.3 Synthesizer Main Loop Board

Refer to schematic drawing 7100505 during the following discussion.

The main loop synthesizer provides the first local oscillator frequency (100-400MHz) to the receiver. Frequency output is 200-400 MHz from the oscillator, provided by two VCO's splitting the band between A1 (200-282 MHz) and A2 (282-400 MHz). Each oscillator board also provides four range selection, providing the benefit of lower tuning sensitivity, and higher Q, by splitting the output across eight ranges. The data receiver (U1, U2) provides switching and pre-tune inputs to the circuitry as shown in Table 3. Subloops 1 and 2 inject frequencies (at P2, P3) to tune the main loop oscillator, and VR1, VR2 and VR3 provide additional regulation and isolation for power supply inputs to the board. Q2, Q5 and Q14 are capacitance multipliers providing Vcc to their respective circuits.

Data from the microprocessor is input at P1 (pins 3, 4 and 6) to the data receiver (U1, U2). The outputs of U1 control the switching circuits of the VCOs. The level translator (AR1, AR2A) provides isolation and adjusts the level of the switching inputs. When turned on by a high output from U1 pins 6 or 7, either Q1 or Q3 will forward bias the oscillator to provide an output of either 200-282 MHz (A1) or 282-400 MHz (A2).

Simultaneously, a high input from U1 (pin 12,13 or 14)will turn on one of three PIN diodes in the oscillator to select BAND 2, 3 or 4 within the range chosen. With all three PIN diodes off, the oscillator operates in BAND 1. Oscillator output through RF amplifier Q11 is either fed directly to the coaxial output (W1) thru AR7 (when a high switching input from AR1A turns PIN diodes CR3 and CR4 on) to provide 200-400 MHz out; or fed thru the ÷ 2 circuit to AR7 (when a high

switching input from AR1B turns PIN diodes CR14, CR15 and CR16 on) to provide a 100-200 MHz output. This arrangement provides a 100-400 MHz output at W1. A resistive splitter consisting of R35, R36 in the direct output, and R33, R40 in the ÷ 2 output divides the VCO signal between the two output paths.

TITLE	DATA RECEIVER OUTPUT	LEVEL TRANSLATOR OUTPUT	SELECT OUTPUT	SWITCH RESULTANT
OUTPUT SELECT	U1 PIN 4	AR1A PIN 1	HI	CR3, CR4 ON 200-400MHz OUT
	U1 PIN 5	AR1B PIN 7	HI	CR14,CR15,CR16 ON 100-200MHz OUT
OSCILLATOR SELECT	U1 PIN 6		HI	Q1 ON, A2 VCO OUT 282-400 MHz RANGE
	U1 PIN 7		HI	Q3 ON, A1 VCO OUT 200-282 MHz RANGE
RANGE SELECT, BAND 2	U1 PIN 14	AR1D PIN 14	HI	CR1 ON, BOTH VCO L1 IN CIRCUIT
RANGE SELECT, BAND 3	U1 PIN 13	AR1C PIN 8	HI	CR2 ON, BOTH VCO L2 IN CIRCUIT
RANGE SELECT, BAND 4	U1 PIN 12	AR2A PIN 1	HI	CR3 ON, BOTH VCO L3 IN CIRCUIT
RANGE SELECT (CODE)	U2 PIN 4		HI/LO	CODED SELECTION TAPS ONE OF EIGHT RESISTORS INTO CKT DEPENDANT ON RANGE. PROVIDES EQUALIZATION.
	U2 PIN 5		HI/LO	
	U2 PIN 6		HI/LO	
PRETUNE (CODE)	U2 PIN 7		HI/LO	CODED SELECTION D/A CONVERTOR AVERAGES INPUTS PROVIDES A STEP PRESELECT TUNING VOLTAGE TO VCO.
	U2 PIN 14		HI/LO	
	U2 PIN 13		HI/LO	
	U2 PIN 12		HI/LO	

TABLE 3. DATA RECEIVER OUTPUTS AND SWITCHING CONTROLS.

Amplification of the VCO ÷ 2 output occurs in Q4, Q6 and AR6 at the input of U8, and Q12, Q13 at the output of U8. These amplifiers, the circuitry connected with them, and impedance matching circuits keep the two VCO outputs approximately equal in amplitude at the input of AR7.

The ÷ 2 circuit (U8) cuts the output frequency in half, the 200-400 MHz from the local oscillator (input at pin 7) is divided by two to provide 100-200 MHz output to AR7 (from pin 3) and to the mixer (from pin 2).

In the mixer the 100-200 MHz local oscillator signal is combined with the subloop "A" input from P3. The output is a 100-200 KHz difference frequency, dependant on the frequency setting of subloop "B". (Subloop A is tuned 100-200 KHz below the 100-200 MHz local oscillator frequency).

The 100-200 KHz difference frequency is put through a low-pass filter and limited by Q9, Q10 and Q8. The output square wave at Q8 is clamped at a TTL level (+5V to 0) by Q7, then input to pin 3 of the phase comparator U4. The other input to the phase comparator is from subloop "B". 100-200 MHz from subloop "B" is input at P2, divided by 1000 in U5, U6 and U7 and the resultant 100-200 KHz signal input to pin 1 of U4.

In the phase/frequency comparator, the two 100-200 KHz inputs are compared, and any difference in phase or frequency results in pulsed negative outputs from pin 13 ($\overline{UP}$) or pin 2 ($\overline{DN}$) which will drive the local oscillator in the indicated direction to attain lock. When the

loop is locked, the outputs of U4 will be high and balanced at the AR4 inputs.

AR2C is a fault detector and will light CR20 and give a $\overline{\text{FAULT}}$ output when lock cannot be attained.

AR4 and associated components form the loop filter. The loop filter integrates and filters the output of U4. The output of AR4 is a negative ($\overline{\text{UP}}$), or positive (DN) dc voltage. The loop bandwidth is about 3 KHz and R61 is the balance adjustment. The dc voltage from AR4 is input to the summing amplifier AR5 where it is amplified and inverted. The output of AR5 is the control voltage to the VCO. Positive control voltage drives the VCO up, and negative control voltage drives the VCO down until lock is attained.

On initial turn on, and during retuning, the local oscillator frequency may be above the input frequency. In this case positive feedback occurs and the local oscillator would be driven to the stops. The search loop (AR3) prevents this occurence. Assume that the control voltage normally varies between +6 Vdc; when the local oscillator is driven down beyond these limits, at about -9V, AR3 will turn on and reverse the drive. Local oscillator frequency will increase until AR3 resets at approximately +6Vdc. The phase/frequency detector then tunes the VCO towards lock. If lock is not attained on the first pass, the local oscillator will exceed the point where AR4 turns on, and the local oscillator will tune UP repeating the cycle.

The local oscillator is pretuned by a coded input from the microprocessor. Data receiver binary outputs at pins 12, 13, 14 and 7 of U2 are averaged by the digital to analog converter (AR2B/D) to

present a dc output voltage to the summing amplifier which will rough tune the VCO to the approximate frequency desired. The loop filter output then fine tunes the VCO.

The data receiver (U2) also outputs a three digit coded range signal at pins 4, 5 and 6, which select one of eight ranges at the output of range decoder U3. The resistor selected by U3 in combination with C12 will provide equalization and maintain a more constant control voltage across the eight ranges of the local oscillator by adjusting loop gain.

1.2.4 Main Loop VCO

The main loop VCO (schematic drawing 7100819) consists of two separate boards (A1 and A2) which are identical except for the frequency determining components. A1 covers the range of 200-282 MHz, and A2 covers the range of 282-400 MHz. Both boards are housed in metal boxes for RF shielding, and are plug-in subassemblies of the main loop board.

The frequency determining components are L1 thru L4 in the tuned circuit of the VCO. Frequency output of the VCO is split into four ranges. Band 1 frequency is determined by L4 which is always in the circuit. Band 2, 3 and 4 frequency is determined by L1, L2 and L3 respectively. These inductors are switched into the circuit by positive inputs at E1-E3 from the main loop, switching on one of the PIN diodes CR1-CR3.

Control voltage from the phase locked loop at E4 adjusts the capacitance of the tuned circuit by adjusting the voltage to the

varactors (CR4, CR5). Oscillator output frequency is present at E6, provided the oscillator is forward biased. To forward bias the oscillator Q2 must be turned on, driving the top of R11 positive. Q2 is cut on or off by the E5 input voltage which is determined by the output switches on the main loop board.

-8Vdc is input from a capacitance multiplier (Q2) on the main loop board at E7, and E8 provides an RF ground to the oscillator.

1.2.5 Carrier Board

The carrier board provides external connections for the subloop and main loop assemblies of the frequency synthesizer module (A2). Refer to schematic 7100818 during the following discussion.

Each loop of the frequency assembly has its own plug-in oscillator. The main loop (A1) and the two subloop (A2, A3) boards are mounted on standoffs to both sides of the carrier board. Each board is enclosed in a separate metallic housing, and both sides are covered, providing RFI shielding from other units.

The main loop (A1) board plugs into two 10 pin connectors (XA1J1, XA1J4) on the carrier board. On the other side of the board subloop #1 (subloop A) plugs into a 10 pin connector (XA2J1), and subloop #2 (subloop B) plugs into another 10 pin connector (XA3J1). The subloop outputs are connected to the main loop by two feed through connectors (J2/P2 and J2/P3).

With all subassemblies mounted, the carrier board becomes the synthesizer module and plugs into the power signal and bus board

via a 70 pin connector (P1). External data and power connections to the synthesizer board are made on the carrier board via this connector.

Data to the main loop board enters on P1 (pins 47, 54, 55) and is fed directly to the main loop through to XA1J1 (pins 3, 4 and 6). Signals entering the board consist of serial data (SDO), an enable (EN3) and a data clock (SCLK).

Data to the two subloops enters on P1 (pins 48, 49, 54, 55) and are input to the data buffer (U1) which provides isolation between the boards. Data outputs to subloop #1 are from U1 (pins 9, 13, 3) to XA2J1 (pins 5-7). Data outputs to subloop #2 are from U1 (pins 11, 1, 5) to XA3J1 (pins 5-7).

Note that serial data inputs consist of three separate signals (SD0, SD1, SD2), while all three boards receive the same clock (SCLK) and enable (EN3) signals. Thus allowing separate data signals to be input to the three boards simultaneously. Plug P1 (pins 45, 46) also provides data ground.

A FAULT (data high) indication will be present on the carrier board when the main loop (XA1J1-1), subloop #1 (XA2J1-8), or subloop #2 (XA3J1) fail to lock (XA1J1-1 is not connected on the main loop board). When any of the three synthesizer loops output a FAULT, Q1 will be forward biased, supplying a ground to L.E.D. CR1, turning it on to provide a visual fault indication. Transistor Q2 will also be forward biased, transmitting a low $\overline{\text{FAULT}}$ data signal to the data processor (P1-67).

All power inputs occur on P1; -15V (pins 5-6), +8V (pins 9-10), +15V (pins 11-12), and power ground (pins 7-8). Power inputs to the main loop occur on XA1J4 (pins 7, 8, 10), and to the subloops on XA2J1 and XA3J1 respectively (pins 1, 3, 4). A +5V regulator for each subloop is located on the carrier board and plugs into J3 (pins 1-3). The main loop and subloop boards are also externally grounded on the carrier board. Power to the carrier board circuitry (+5V) is supplied via pin 9 of the subloop connectors (XA2J1, XA3J1).

The first local oscillator output is on a coaxial line (W1) to J2. The reference clock input to the subloops (pin 10) is via J3.

DWG NO.	SH
7100818	1

REVISIONS

REV	DESCRIPTION	DATE	APPROVAL
W/A	FUNCTION CALLOUT "FAULT" ADD "FAULT" PULL UP	5-22-84	R. BOOKER

P1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
-15V
-15V
PWR GND
PWR GND
+8V
+8V
+15V
+15V

XA1J4|P4
1 2 3 4 5 6 10 8 7 9 10 9 8 7 5 2 6 4 3 1
-15V
+8V
+15V
SDO
EN3
SCLK
FAULT

A1
MAINLOOP
ASSY 7100305-1
SCHEMATIC 7100505

XA1J1|P1
P3
P2

W1
J2
L.O OUT

+5VB
R1 100K
R2 100K

+5VA
CR1 5082-4494
R5 1K
Q1 MPS6521
R6 10K
R7 10K

+5VB +5VB
R4 100K
R3 100K

P3|J3 +5V
VR1
1 +5V
2 GND
3 +8V
J2
A2
SUBLOOP NO.1
ASSY 7100304-1
SCHEMATIC 7100504
P1 XA2J1
1 3 4 8 9 5 6 7 2 10

J2
A3
SUBLOOP NO.2
ASSY 7100304-1
SCHEMATIC 7100504
P1 XA3J1
1 3 4 8 9 5 6 7 2 10
J3|P3 +5V
VR2
MC7805 CT
TYP VR1, VR2

J3
REF CLOCK IN

DGND
D GND
SDO
SDI
SD2
EN3
SCLK
FAULT

42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70

+5VB
C1 .01uF
U1 74C906
SCLK 4 6
EN3 2 12
SDI 8
SD2 10
14 7
9 13 3 11 1 5

Q2 MPS6521
R8 10K
R9 10K

-15V
+8V
+15V
FAULT
SDI
EN3
SCLK
SD2
EN3
SCLK

FOR UNUSED BUS FUNCTIONS
SEE 7100524

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES,
TOLERANCES:
ANGLES ± 0°-30'
DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010
SURFACE √
HOLE SIZES PER AND10387

DWN BY:	4/26/84
CHECK: R. BOOKER	5/11/84
APVD:	5/16/84
APVD:	5-16-84
	5/18/84
RLSE:	

7100418
NEXT OR ASSOC ASSEMBLY

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

INTERCONNECT DIAGRAM
SYNTHESIZER

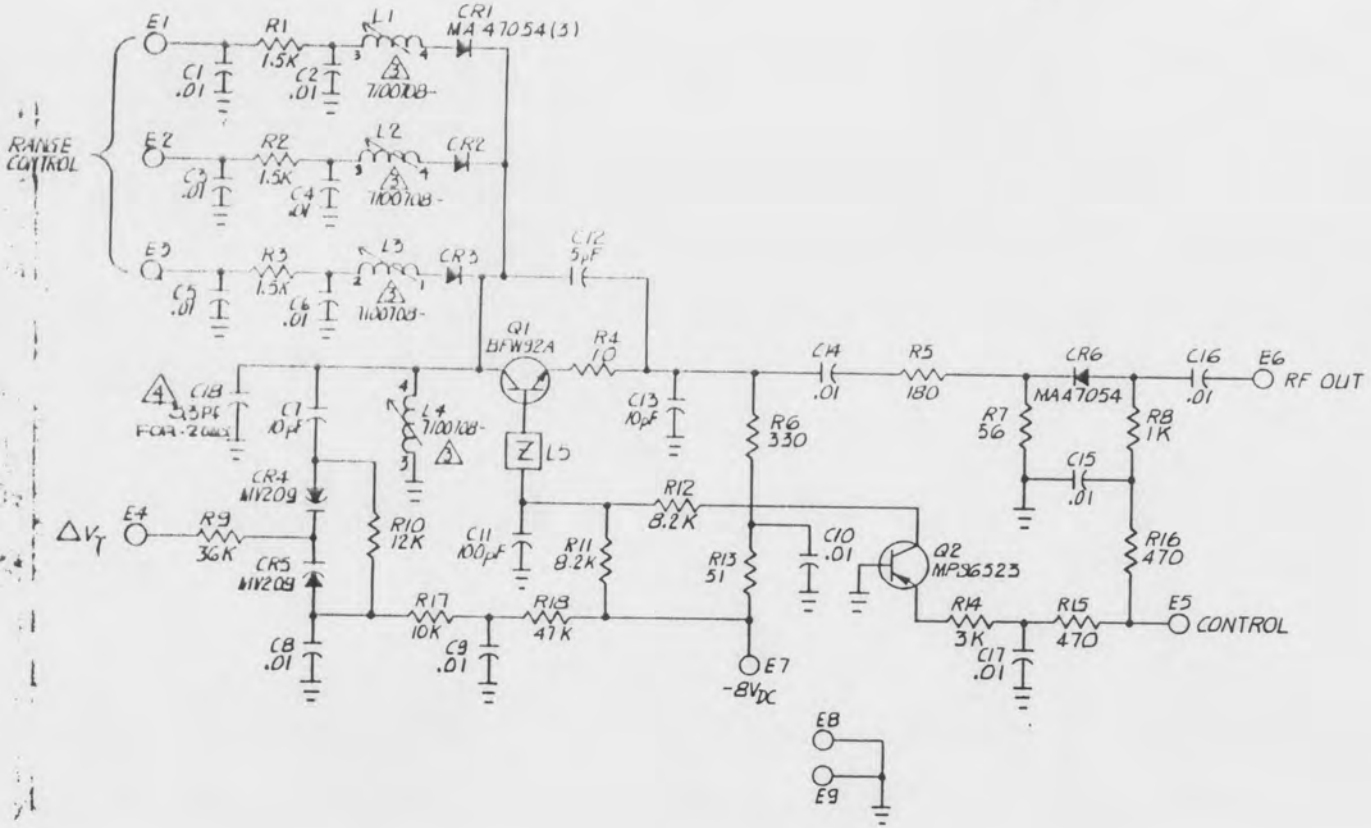
SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100818	

SCALE · SHEET 1 OF

NOTE: UNLESS OTHERWISE SPECIFIED

7100818

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REDRAWN WITH CHG (REF ECR 5421) FD 2/14/84	2/16/84	R. BOOKER
B	ECN 5511 EFF: 001 & ON MAR 11-1-84	3/28/85	R. BOOKER
C	ECN 5661 EFF 001 & ON MAR 11-1-84	3/28/85	R. BOOKER



	3 INDUCTOR WINDING	
–	-1 (200-282 MHz)	-2 (282-400 MHz)
L1	5¼T	2 3/4
L2	4¼T	2¼T
L3	3¼T	1¾T
L4	2¼T	3/4T

LAST REFERENCE DESIGNATION USED										
C	CR	E	L	Q	R					
18	6	9	5	2	18					
REFERENCE DESIGNATION NOT USED										

-1, 200-282 MHZ
REF 7100308-1 & 7100419-1

-2, 282-400 MHZ
REF 7100308-2 & 7100419-2

4 APPLICABLE FOR 282-400 MHZ ONLY

3 USE INDUCTOR WINDING CHART FOR FREQ AND TURN INFORMATION.

2. RESISTORS ARE IN OHMS, 1/8W 5%.

1. CAPACITORS ARE IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

7100419
7100308
NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30' DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010 SURFACE √ HOLE SIZES PER ANSI 0387

DRAFT	Tim Duong	1/14/84
CHECK	R. BOOKER	2/16/84
APP'D		4/4/84
APP'D		28 MAR 84
APP'D	T. Nahabedian	2/23/84
RELEASE		2/23/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

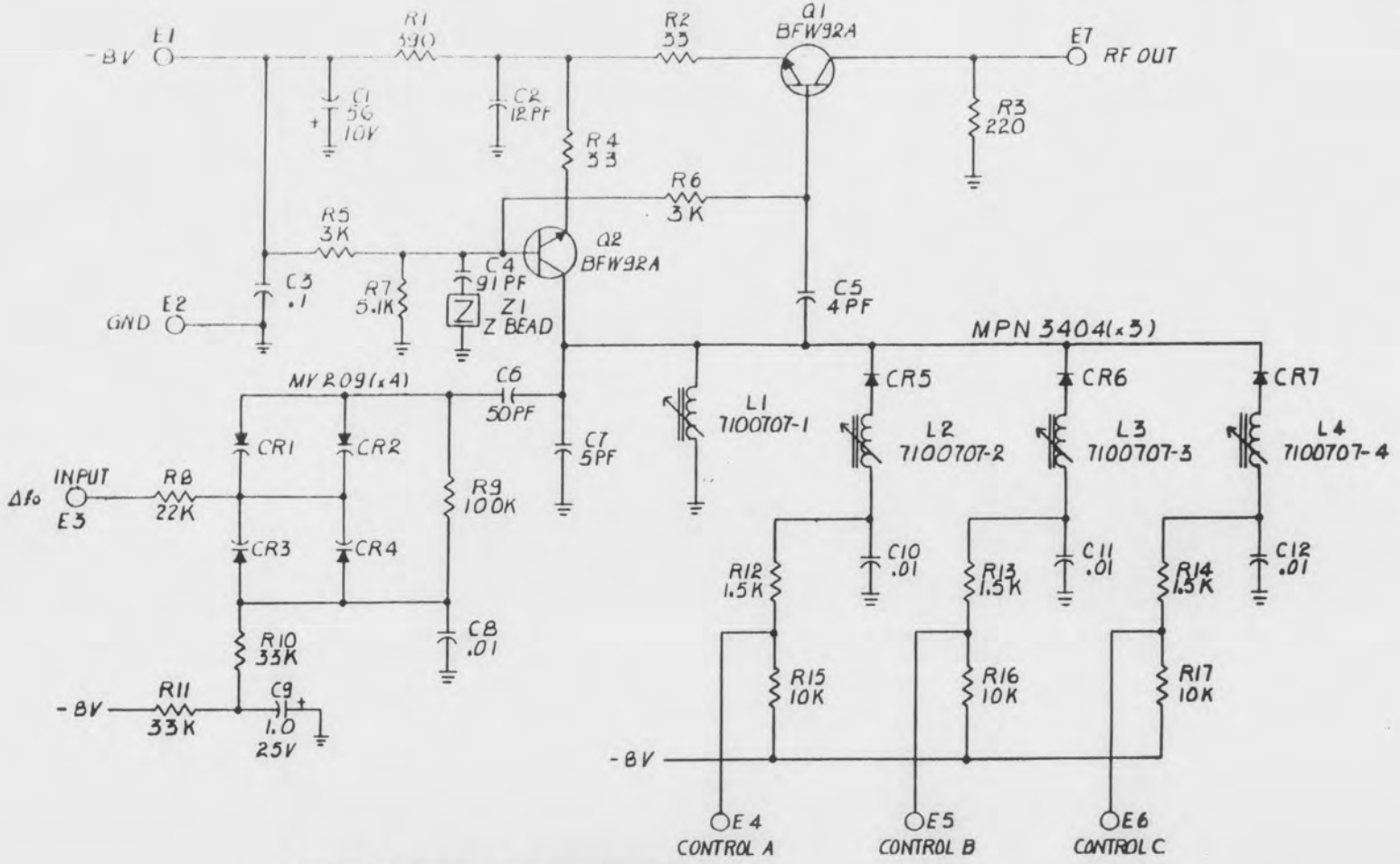
SCHEMATIC
VCO, MAINLOOP

SIZE	FSCM NO.	DWG NO.	REV
C	06994	7100819	C

SCALE —— SHEET 1 OF

7100805 B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	RB WAS 51K ZI WAS L5 (REF PER ECR 5411) EB 11/11/14	1-19-84	R. BADIKER
B	WCORP ECN 5532 EFF: 001R ON KD 6-10-85	6/26/85	R. BADIKER



PROPRIETARY INFORMATION
USE OR REPRODUCTION PROHIBITED EXCEPT AS SPECIFICALLY AUTHORIZED IN WRITING BY C.A.R. CORPORATION

LAST REFERENCE DESIGNATION USED											
C	CR	E	L	Q	R	Z					
12	7	7	4	2	17	1					
REFERENCE DESIGNATION NOT USED											

2. RESISTORS ARE IN OHMS, 1/8 W 5%.
1. CAPACITORS ARE IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30' DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010 SURFACE √ HOLE SIZES PER ANSI B32.7

DRAFT pmdong 7/21/83
CHECK R. BADIKER 7/24/83
APP'D [illegible] [illegible]
APP'D T. Hughes 8/10/83
RELEASE [illegible] 8/20/83

7100309
NEXT OR ASSOC ASSEMBLY

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
CAR

SCHEMATIC
VCO, SWITCHED RANGE

SIZE C | PSCM NO. 06994 | DWG NO. 7100805 | REV B
SCALE 2/1 | SHEET 1 OF 1

DWG NO. 7100505 SH 1 E

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REVISED PER BD LAYOUT	9-14-83	B.BOOKER
B	REVISED ENG UPDATE PER ECN 5359 4-19-84	2-17-84	B.BOOKER
C	REVISED PER ECN 5359 4-19-84	4-25-84	B.BOOKER
C1	P-1 FUNCTION CALLOUT WAS:	5-22-84	B.BOOKER
D RZ	ECN 5729 EFF: 024,025,027 & ON MAR 11-16-84	11/8/84	B.BOOKER
E	DDC ZONE B/4 ADD C90, EFF 001 & ON #3-19-85	7/22/85	B.BOOKER

OUT PUT SELECT

RANGE CONTROL

ΔV_T

SELECT 282-400

SELECT 200-282

(PRE-TUNE D/A)

(MYLAR)

(BALANCE)

SUBLOOP #2

FAULT

P3 SUB LOOP #1 INPUT

RFOUT W1

RTN

6. ALL 347'S AND 351'S ARE POWERED FROM ± 12V
5. ALL UNMARKED DIODES ARE IN4148.
4. INDUCTORS ARE IN MICRO HENRIES.
3. CAPACITORS IN MICRO FARADS.
2. RESISTORS ARE 1/8W, 5%, EXCEPT ONES WITH * ARE 1%.
1. RESISTANCE INDICATED IN OHMS.

NOTE: UNLESS OTHERWISE SPECIFIED

LAST REFERENCE DESIGNATION USED

A	AR	C	CR	L	P	Q	R	U	VR
3	17	90	26	13	4	14	132	8	3

REFERENCE DESIGNATIONS NOT USED

		86			10			83	
		39						85	

LIST OF MATERIAL

QTY PER ASSY	-1 ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES ± 0°-30'
DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010
SURFACE √
HOLE SIZES PER AN010387

7100305
NEXT OR ASSOC ASSEMBLY

DWN BY:		8-5-83
CHECK:	B.BOOKER	8/15/83
APVD:		13 MAR 84
APVD:		8/24/84
		3/15/84
RLSE:		

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC DIAGRAM
MAIN LOOP

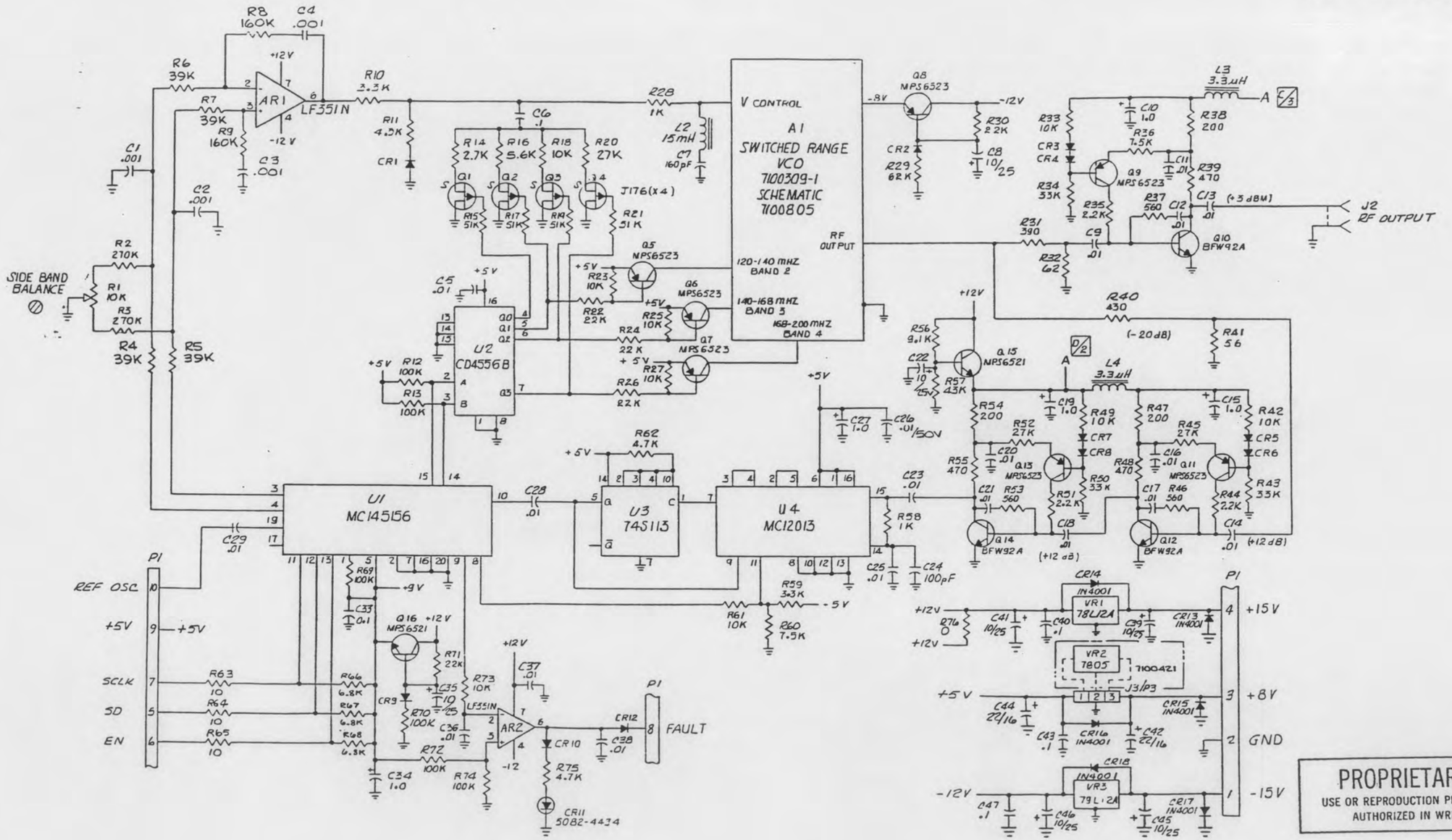
SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100505	E

SCALE — SHEET 1 OF 1

7100505 E

DWG NO. 7100504 SH 1 C

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	UPDATE PER ENGR Dwng 7164B3	11/2/83	B.BOOIKER
B	INCORP ECN 5505 AO 0/10/83	6/21/85	B.BOOIKER
C	INCORP ECN 5636 AO 6/10/85	6/21/85	B.BOOIKER



LAST REFERENCE DESIGNATIONS USED										
A	AR	C	CR	J	L	Q	R	U	VR	P1
1	2	47	18	3	4	16	76	4	3	.

REFERENCE DESIGNATIONS NOT USED							
	C30 C31 C32	J1	L1				VR2

3. DIODES ARE IN4148.

2. CAPACITORS ARE 50WVDC MIN, CAPACITANCE IS IN MICROFARADS.

1. RESISTORS ARE 1/2 W, RESISTANCE IS IN OHMS ± 5%.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √

HOLE SIZES PER AND10387

7100304

NEXT OR ASSOC ASSEMBLY

DWN BY: DanDreang	7/6/83	
CHECK: B. BOOIKER	8/18/83	
APVD: L. Olsen	11/1/83	
APVD: T. Maiorana	11/7/83	
	11/3/83	
RLSE:		

OCEAN APPLIED RESEARCH CORP (OAR)
A DIVISION OF GENERAL INDICATOR CORP

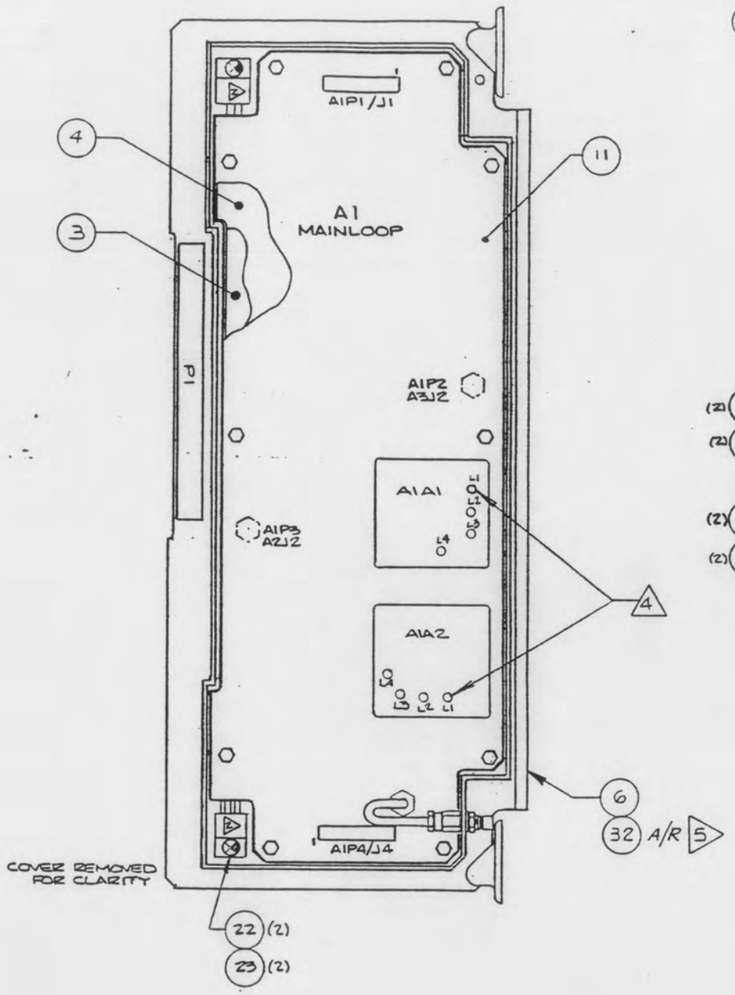
SCHEMATIC, SYNTHESIZER SUBLOOP

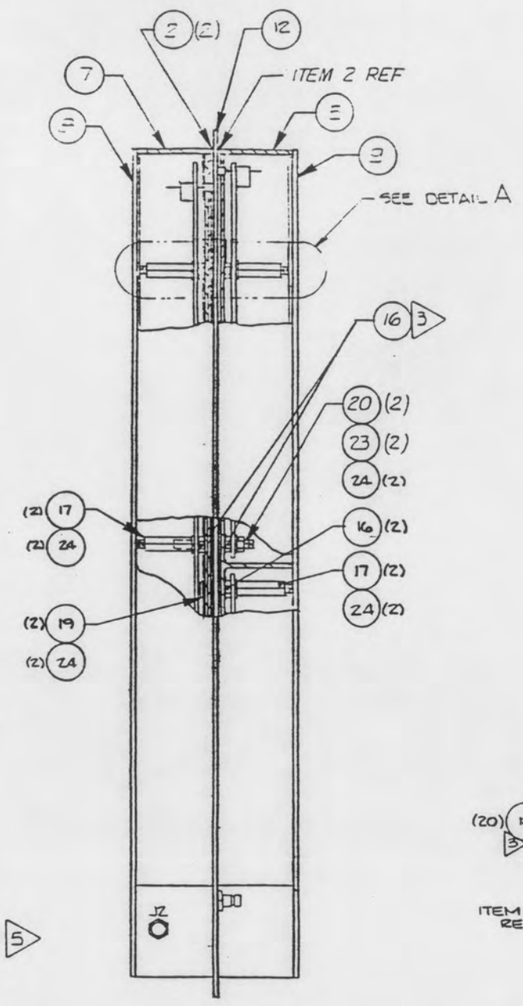
SIZE D | FSCM NO. 06994 | DWG NO. 7100504 | REV C | SCALE: | SHEET 1 OF 1

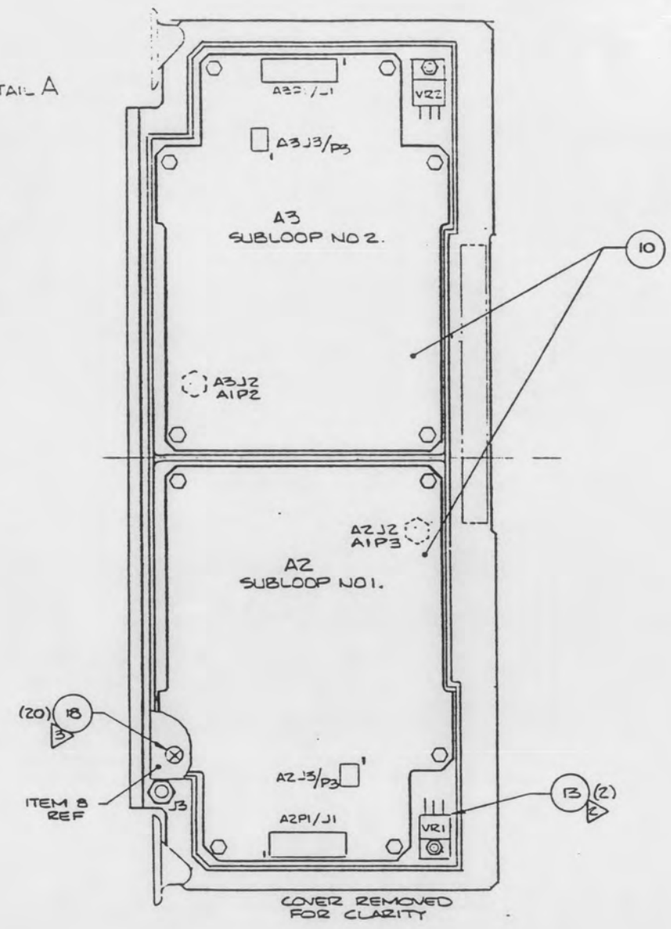
7100504 C

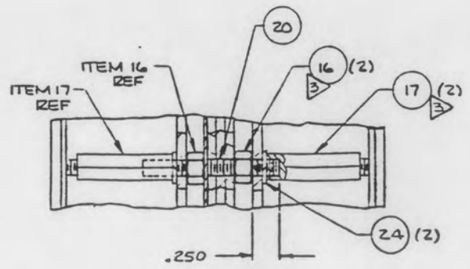
DWG NO. 7100418 | SH 1 | F

REV	DESCRIPTION	APPROVAL
A	PAL WAS REWRITTEN & DWG WAS INCORP 11/15/83	G Leuchi 11-18-83
B	INCORP ECN 5497	B. BODIKER 9/5/84
C	INCORP ECN 5605	B. BODIKER 5/22/85
D	INCORP ECN 5587 EFF: 4-6172 & ON MAR. 11-2-84	B. BODIKER 11/1/84
E	INCORP ECN 6111: EFF: 5-2067 & ON KD 6-17-85	B. BODIKER 8/26/85
F	INCORP ECN 6176 EFF: 630 & ON	10 3/19/86 B. BODIKER 9/4/86









DETAIL A
TYP 8 PLCS
SCALE: 2/1

SEE SEPARATE PARTS LIST.

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

QTY PER ASSY

345-410

240-410

NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER ANSI B4.2-1978

DWN BY: 11/15/83
CHECK: G Leuchi 11-18-83
APVD:
APVD: T. Mahoney 11/23/83
APVD:
RELSE:

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

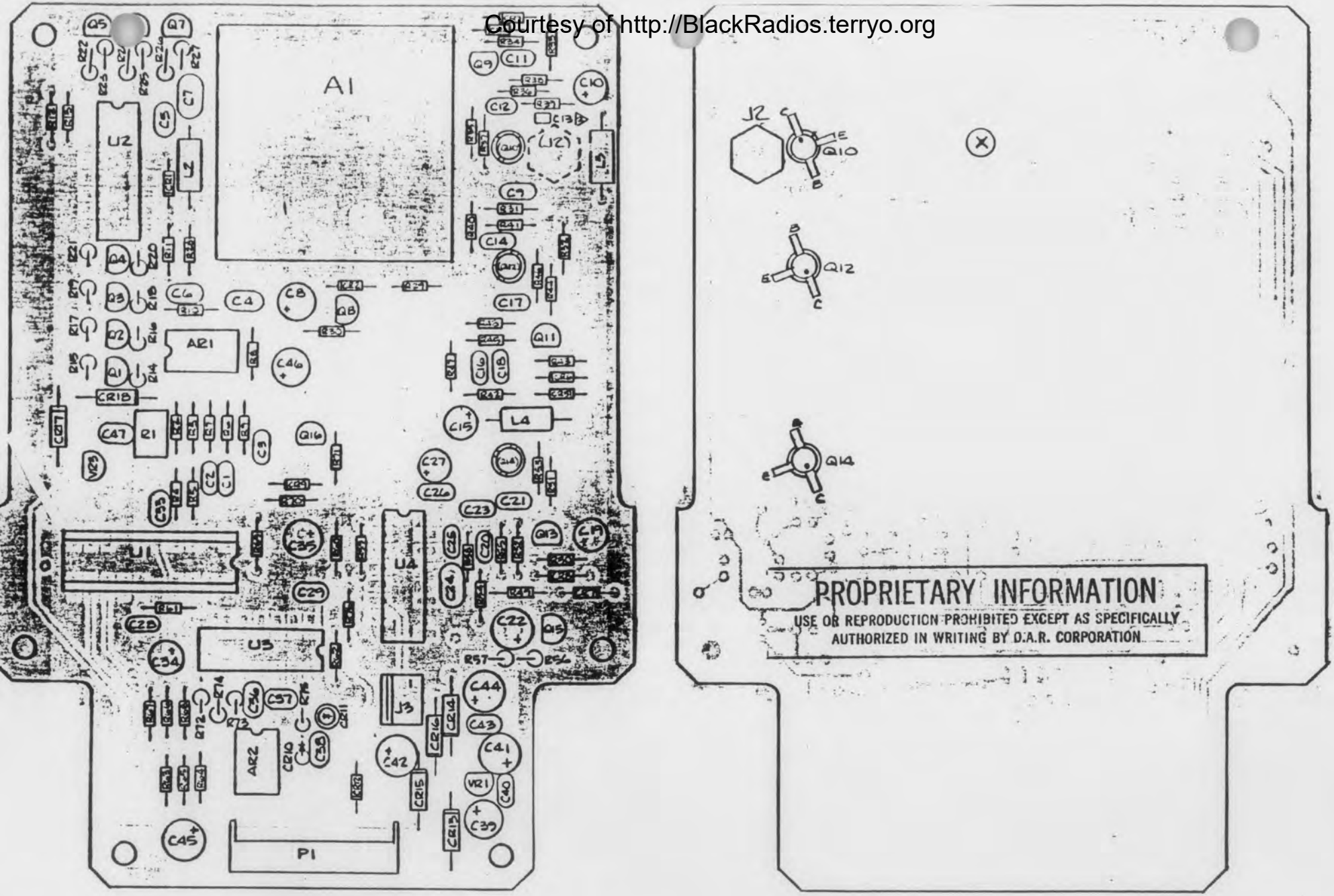
SYNTHESIZER

SIZE D | FSCM NO. 06994 | DWG NO. 7100419 | REV F
SCALE 1/1 | SHEET 1 OF 1

1. THERMAL EPOXY ITEM 32 TO BE MIXED & CURED AFTER ASSY PER MFGR'S INSTRUCTIONS.
2. COVER TUNING HOLES CFL1 THRU L4 ON A1A1 & A1A2 WITH ADHESIVE BACKED METAL TAPE, ITEM 30, AFTER FINAL ADJUSTMENT.
3. APPLY RTNG COMPOUND, ITEM 28, TO HARDWARE INDICATED AT TIME OF ASSY.
4. PLACE INSULATOR, ITEM 13 UNDER VOLTAGE REGULATOR.
5. IDENTIFY BY BAGGING OR TAGGING WITH PART NO., APPLICABLE DASH NO. & REV LTR.

NOTES: UNLESS OTHERWISE SPECIFIED

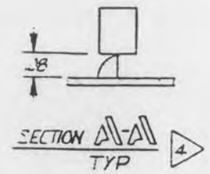
7100418 F

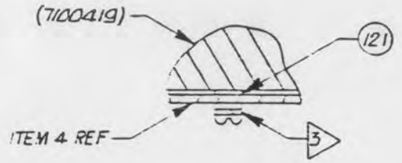


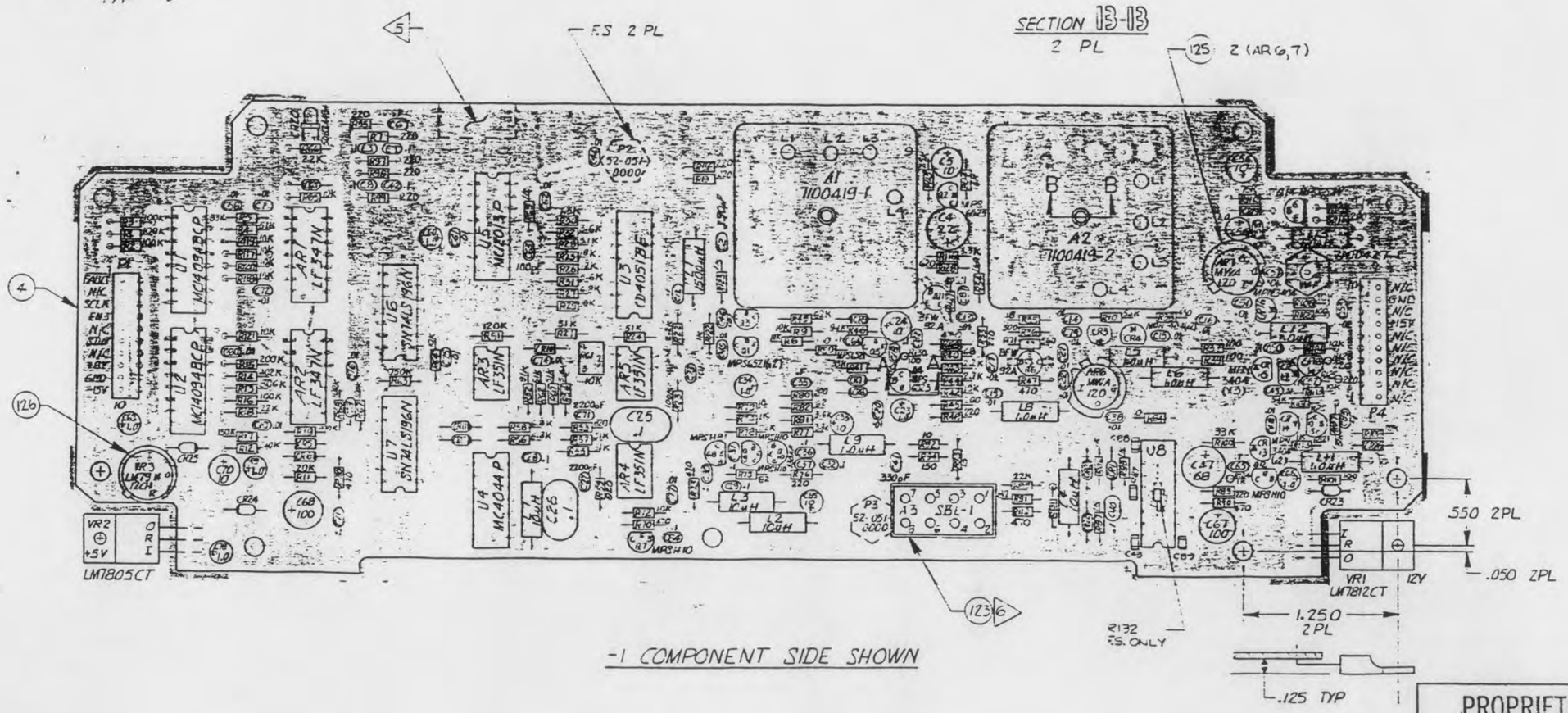
7100304-1. SYNTHESIZER SUB LOOP

DWG NO. 7100305 SH 1 G

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
B	REDRAWN, INCORP ECN 5420 @ 3/6/84	3/12/84	B. BACKER
C	ECN 5550 4-19-84	5/2/84	B. BACKER
C-1	REVISED VIEW TO CLARIFY ORIENTATION OF A1 & A2	11/8/84	B. BACKER
D	ECN 5613 EFF: S/N 012 & ON MAR 1-6-84	11/8/84	B. BACKER
E	ECN 5613 EFF: 024, 025, 027 & ON.	11/8/84	B. BACKER
F	DDC: ADDED NOTE 7 REF: ECN 5774 MAR 1-6-84	11/8/84	B. BACKER
G	INCORP ECN 5905 SERIAL NO. 313/33	4/3/85	B. BACKER







-1 COMPONENT SIDE SHOWN

6 PLACE TAPE (ITEM 23) WHERE INDICATED ON COMPONENT SIDE OF BOARD PRIOR TO INSTALLATION OF A3.

5 IDENTIFY WITH PART NO. 7100305, DASH NO & REV LTR.

4 BEND MIDDLE LEAD ON TRANSISTORS TO FIT BOARD PATTERN, NOTE ORIENTATION OF FLAT ON CASE.

3 HARDWARE SUPPLIED WITH A1 & A2 MODULES. REMOVE TO INSTALL MODULE TO BOARD THEN REUSE AS SHOWN.

2. ALL COMPONENT TYPES & VALUES ARE FOR REFERENCE ONLY, SEE SEPARATE PARTS LIST FOR ACTUAL TYPES & VALUES.

1. MOUNT ALL COMPONENTS FLUSH TO BOARD SURFACE.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER ANSI B87

DWN BY: [illegible] 3/6/84
CHECK: B. BACKER 3/4/84
APVD: [illegible] 3/4/84
APVD: [illegible] 3/4/84
RLSE:

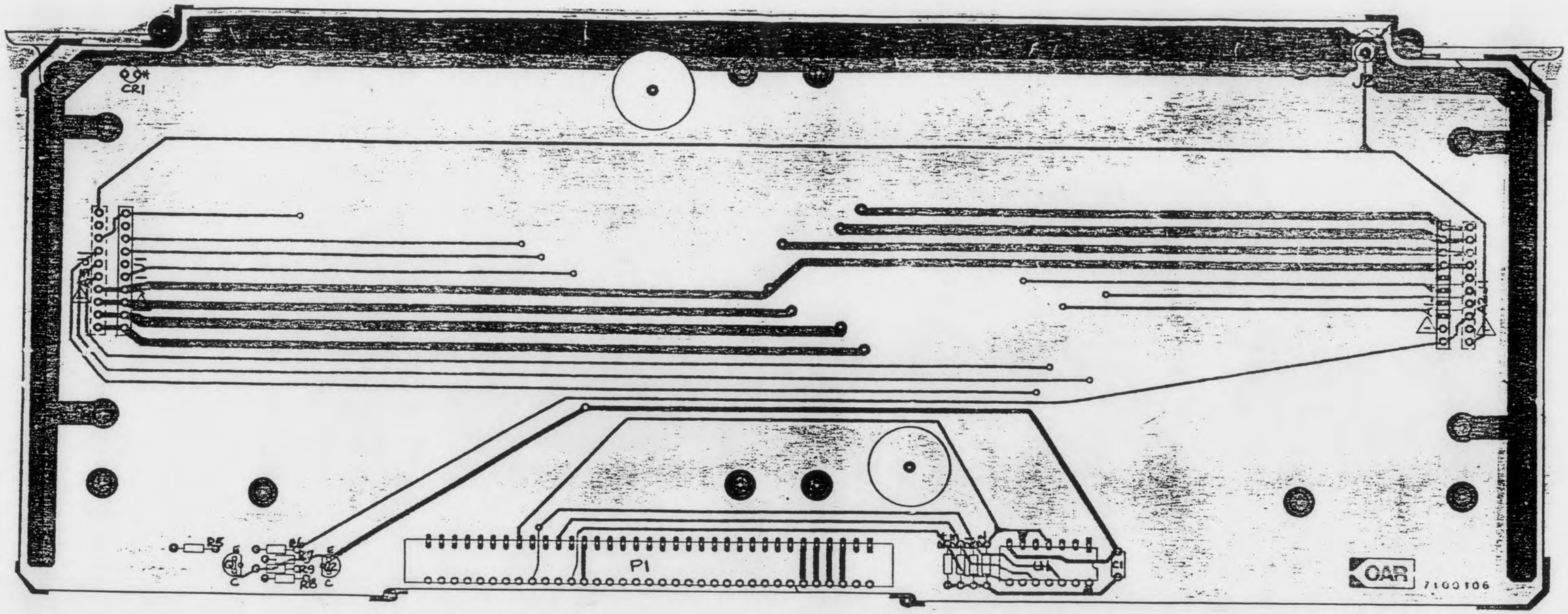
OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

MAIN LOOP, SYNTHESIZER

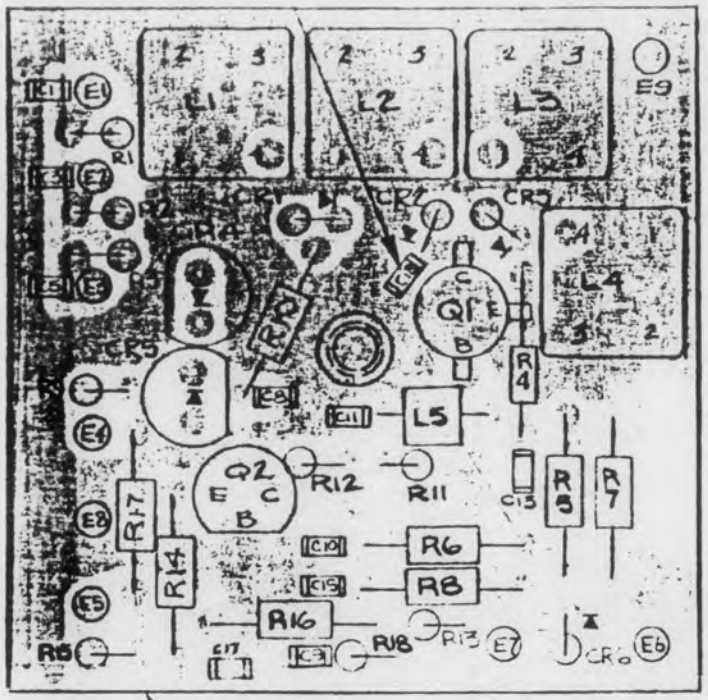
7100418
NEXT OR ASSOC ASSEMBLY

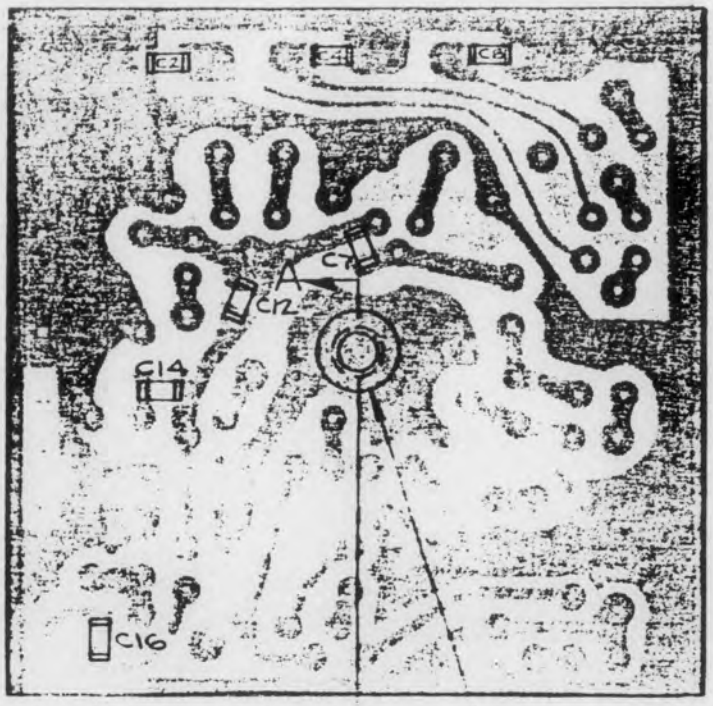
SIZE D | FSCM NO. 06994 | DWG NO. 7100305 | REV G
SCALE [illegible] | SHEET 1 OF 1

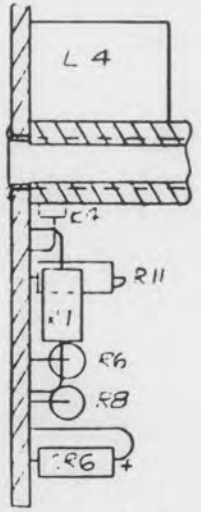
7100305 G



7100306-1. CARRIER BOARD, SYNTHESIZER







SECTION A-A

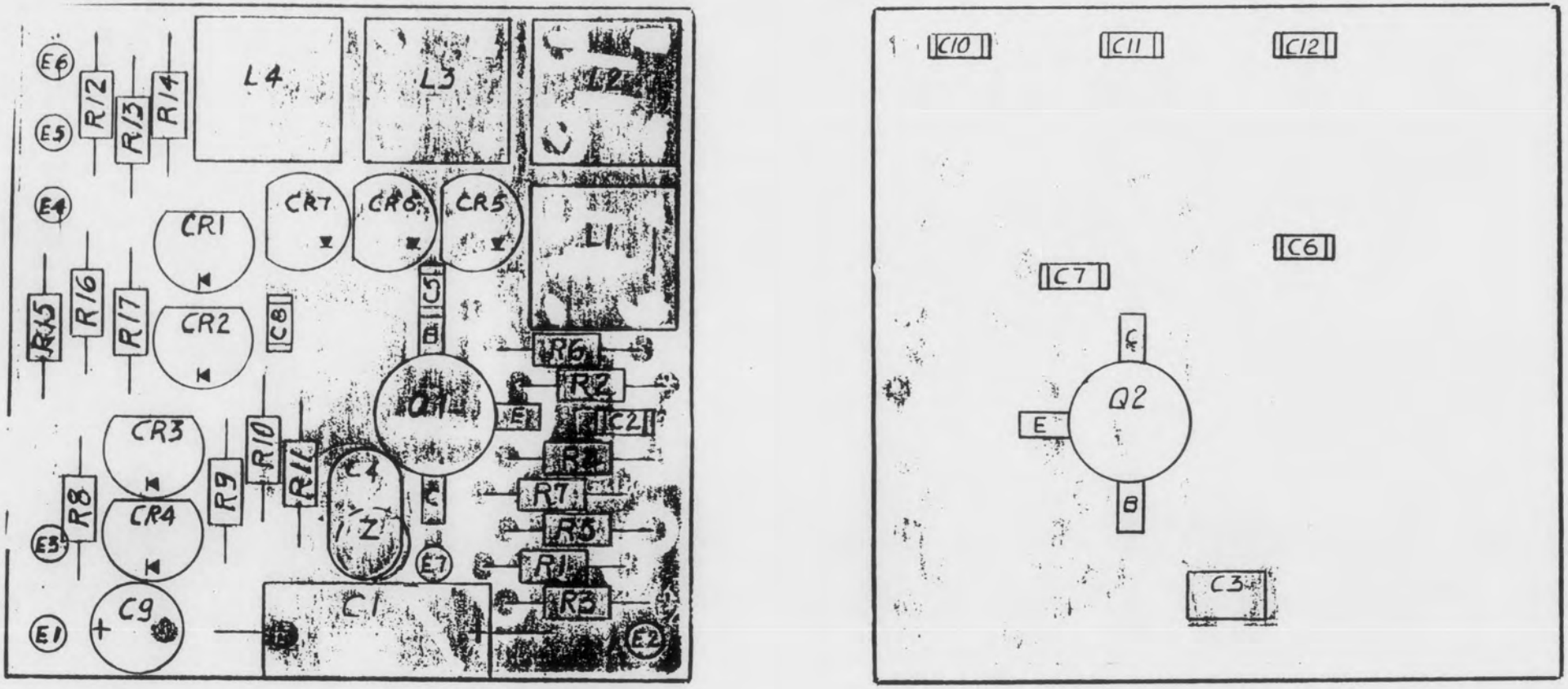
4

A

37 SWAGE N.S & SOLDER TO F.S

-1 VCO, LOW BAND
-2 VCO, HIGH BAND
See Parts List for Differences

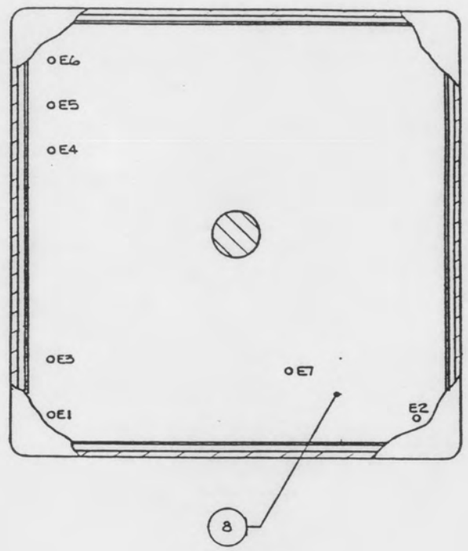
7100308. Circuit Board, Main Loop VCO

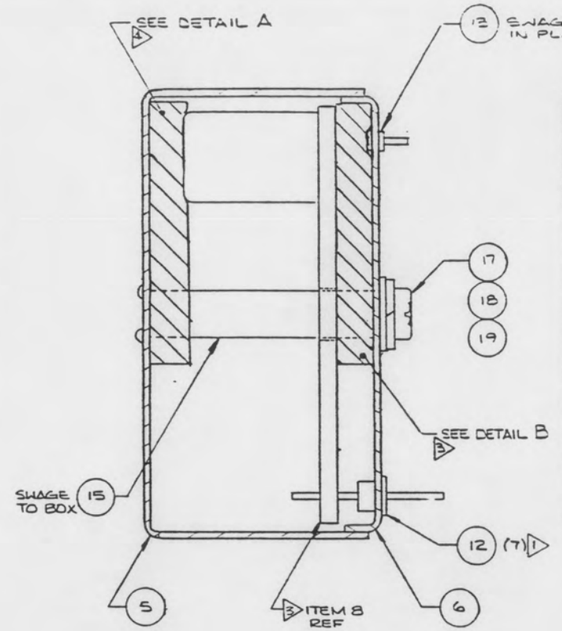


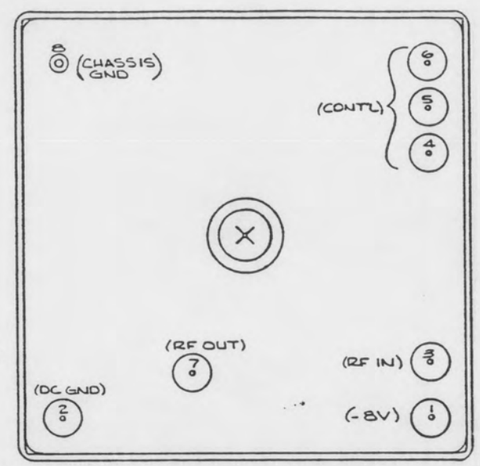
7100309-1. CIRCUIT BOARD ASSEMBLY VCO, SWITCHED RANGE

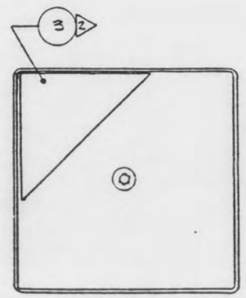
DWG NO. 7100405 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL

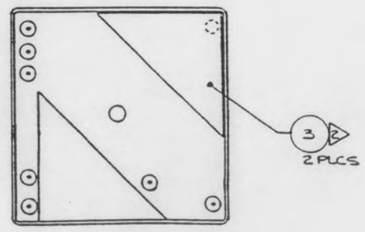




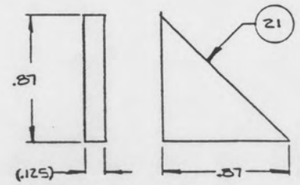




DETAIL A
BOX PAD LOCATION
SCALE: 2/1



DETAIL B
COVER PAD LOCATION
SCALE: 2/1



3 -10 PAD DETAIL
SCALE: 2/1

5 IDENTIFY BY BAGGING AND TAGGING WITH PT. NO., APPLICABLE DASH NO. & REV. LTR.

2 NEOPRENE PAD IN BOX MUST BE PLACED OVER INDUCTOR PORTION OF BD WHEN INSTALLING BOX TO COVER

3 NEOPRENE PADS IN COVER MUST NOT BE COMPRESSED WHILE INSTALLING AND SOLDERING BOARD.

4 SECURE NEOPRENE PAD WITH ADHESIVE, ITEM 22.

1 SOLDER TERMINALS FLUSH TO SURFACE.

NOTE: UNLESS OTHERWISE SPECIFIED

1 -1 SWITCHED RANGE VCO MODULE ASSY

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER AND10387

7100304
NEXT OR ASSOC ASSEMBLY

DWN BY: R Kam L	3/16/83	OCEAN APPLIED RESEARCH CORP (OAR)
CHECK: B. BODIKER	3/18/83	A DIVISION OF GENERAL INDICATOR CORP
APVD: T. Hanaffee	3/18/83	MODULE ASSY, SWITCHED RANGE VCO
APVD:		
RLSE		

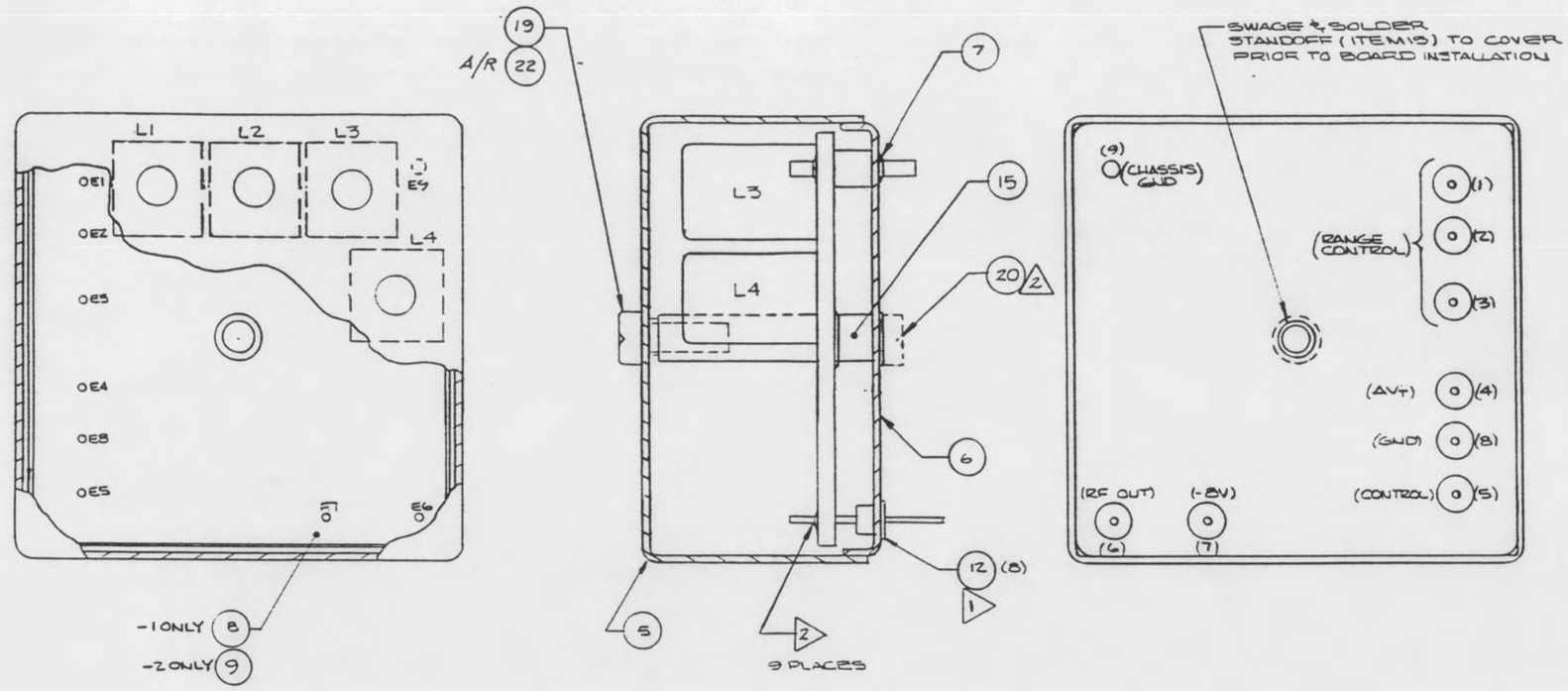
SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100405	

SCALE: 2/1 SHEET 1 OF 1

7100405

DWG NO. 7100419 REV 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REVISED PER ECN #5440 2-28-84 LK	2-28-84	R.BAUKER
B	REVISED PER ECN # 6879 EFF: S/N 101 & ON	11-6-84	R.BAUKER
C	INCORP ECN 6161 EFF: 181 & ON A.O. 7/24/85	9-4-85	R.BAUKER



3. IDENTIFY BY BAGGING OR TAGGING WITH PT. NO., APPLICABLE DASH NO & REV LTR.

⚠2 SECURE BOARD TO COVER USING TEMPORARY FASTENER, ITEM 20, BEFORE SOLDERING BOARD TO FEEDTHRU TERMINALS. RETURN FASTENER TO STOCK.

⚠1 SOLDER TERMINALS FLUSH TO SURFACE.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

QTY PER ASSY

7100505 NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √

HOLE SIZES PER AND10387

DWN BY: 10/30/85
CHECK: 10/31/85
APVD: 10/31/85
APVD: 11/1/85
RELSD: 11/1/85

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

VCO MODULE, MAIN LOOP

SIZE D | FSCM NO. 06994 | DWG NO. 7100419 | REV C

SCALE: 4/1 | SHEET 1 OF 1

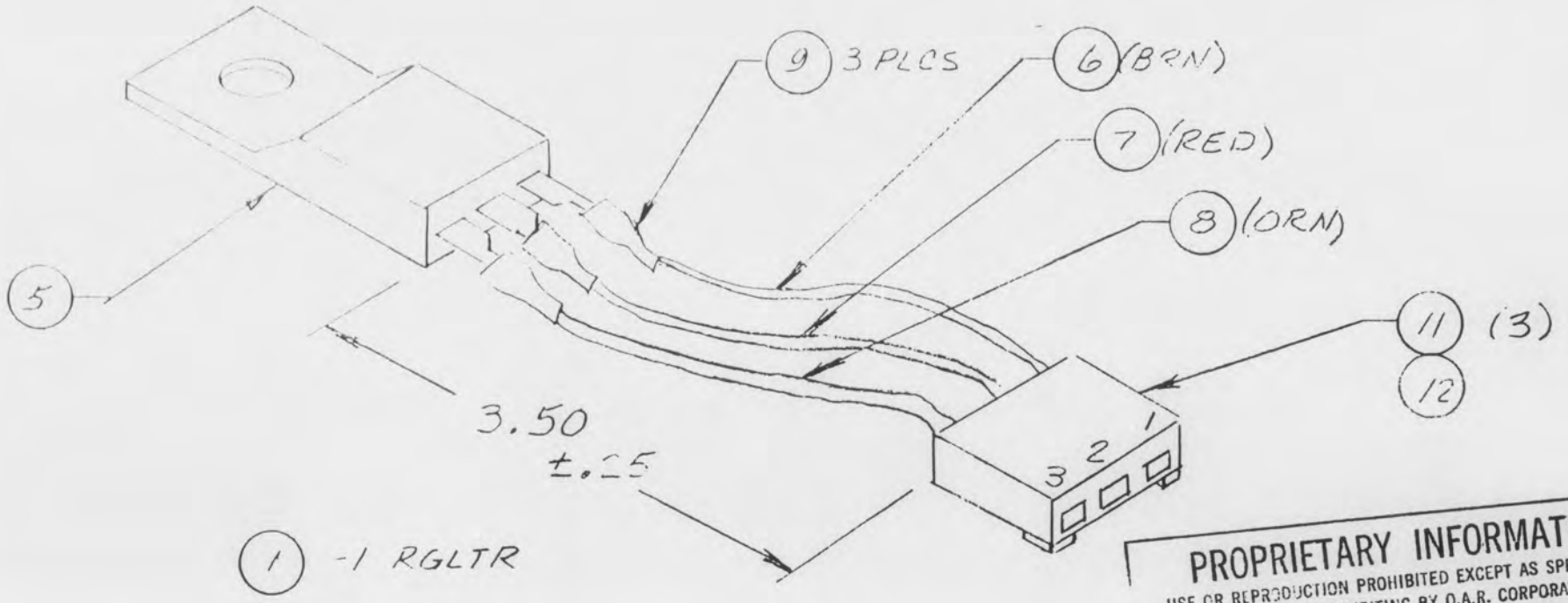
7100419C

DWG NO. 7100421 SH. 1

NOTE: UNLESS OTHERWISE SPECIFIED

1. BAG & TAG WITH PART NO., DASH NO. AND REV LTR.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A R1	INCORP ECN 6132 IR 6/6/85 EFF: 001 & ON	6/6/85	B. BODIKER



SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY					

LIST OF MATERIAL

7100418

NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES:

ANGLES ±0°30′ DECIMAL .X =±.1 .XX =±.03 .XXX=±.010 SURFACE √

HOLE SIZES PER AND 10387

DWN BY: L Gomez	6/5/85	
CHECK: B. BODIKER	6/6/85	
APVD: D. Mau	6/6/85	
APVD: T. Hanchey	6/6/85	
	6/6/85	
RLSE: Marsha Rodgers	6/06/85	

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

OAR

VOLTAGE REGULATOR

SIZE	FSCM NO.	DWG NO.	REV
A	06994	7100421	A

SCALE: — SHEET 1 OF 1

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL		DATE 11/21/83	TITLE: SYNTHESIZER
APPVD		DATE	
CHECK G. Landis		DATE 11-18-83	
DRAWN		DATE 10-4-83	

PARTS LIST 710418
SHEET 1 OF 3 | REV F
MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	240-410	345-410		
QTY REQUIRED THIS RELEASE	FINAL ASSY	240-410	345-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	P/L WAS REV 4 REDWN WITH ALT MACHINED PARTS	DR 11/15/83	G. LANDIS	11/19/83
B	INCORP ECN 5497	KD 3/28/84	B. BODIKER	4/5/84
C	INCORP ECN 5605	KD 8/28/84	B. BODIKER	8/30/84
D	INCORP ECN 5887 EFF: 4-6172 & ON	MAR 11-5-84	B. BODIKER	11/6/84
E	INCORP ECN 6111; EFF: S/O 5-2067 & ON	KD 6-17-85	B. BODIKER	6/26/85
F	INCORP ECN 6176; EFF: 030 & ON	AO 8-19-85	B. BODIKER	9/4/85

7100418

SH 2 OF F

ITEM NO	PART NO	DESCRIPTION	MATERIAL MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	SYNTHSIZEIR		X						
2	7101056-1	INSULATOR		2						
3	7101011-1	SHIELD		1						
4	7101011-2	INSUL, SHIELD		1						
5	7100037-1	HOUSING, SUB LOOP		1						
6	7101069-1	HEAT SINK BLOCK		1						
7	7100037-2	HOUSING, MAIN LOOP		1						
8	7101055-1	COVER		1						
9	7101055-2	COVER		1						
10	7100304-1	SUBLOOP		2						A2, A3
11	7100305-1	MAIN LOOP		1						A1
12	7100306-1	CARRIER BD		1						
13	7100421-1	V RGLTR		2						VR1 & VR2
14	7100818	DIAGRAM		REF						
15	60118302-1674	INSULATOR TYPE II	CHOMERICS	4						
16	2051-440-SS-20	SPACER, 4-40 x 1/8	R.A.F.	20						DIST. FASTENERS UNLTD
17	2061-440-SS-20	SPACER, 4-40 x 3/4	R.A.F.	20						"
18	4-40 x 3/8" L	SCREW, S.S.	FL HD 100° PHILLIPS	20						
19	4-40 x 5/8" L	SCREW, S.S.	PH PN HD	2						
20	4-40 x 1" L	THD ROD, S.S.		10						
21										
22	4-40 x 1/2 L	SCREW, S.S.	PH PN HD							

FORM 183

7100418
3 OF F

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23	4-40	NUT, HEX, S.S.	(RADIO)	4										
24	#4	WASHER	S.S. INT STAR.	24										
25														
26														
27														
28	GRADE C	RTNG CMPD	LOCTITE	A/R										
29														
30	1181	TAPE, COPPER, 1/4 WIDE	3M	A/R										
31														
32	4951	THERMAL EPOXY	THERMALLOY, INC.	A/R										
33														
34														
35														
36														
37														
38														
39														
40														
41														
42														
43														
44														

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	DATE	
APPVD L. Clark	DATE	
CHECK B. BODIKER	DATE 11/2/83	
DRAWN MH	DATE 7/13/83	

TITLE: SYNTH SUBLOOP

7100304

SHEET 1 OF 6 | REV E

MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100418			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	UPDATE PER ENGR	K Duong 10/26/83	B. BODIKER	11/2/83
B	INCORP ECN 5331	DR 11/11/83	B. BODIKER	11/15/83
C	INCORP ECN 5353	Dung Vong 11/10/84	B. BODIKER	1/10/84
D	INCORP ECN 5504, EFF: 001 & ON	KD 6-11-85	B. BODIKER	6/21/85
E	INCORP ECN 5548 EFF: 001 & ON	KD 6-11-85	B. BODIKER	6/21/85

7100304
SH 2 OF E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	7100304-1	SUBLOOP		X						
3	7100504	SCHEMATIC		REF						
4	7100204-1	BOARD		1						
5										
6	7100405-1	VCO		1						A1
7	7100805	SCHEMATIC, VCO		REF						
8	349-900	CHIP CAP PROCEDURE		REF						
9										
10	LF351N	I.C, OP AMP	NATIONAL	2						AR1,2
11	0805B103K3T	CAP, CHIP, .01μF	VICLAN	1						C13
12	226RLR016M	CAP, AL EL, 22μF	ILLINOIS CAPACITOR	2						C42, C44
13	C320C104K5R5CA	CAP CER .1μF	KEMET OR EQ	5						C6,33,40,43,47
14	23BJ210	CAP, MYLAR, .001μF	MOUSER	4						C1, 2, 3, 4
15										
16	C315C103K5R5CA	CAP, CER, .01	KEMET	18						SEE SH 6
17										
18	DM15-FY161J	CAP, MIC, 160PF	ELMENCO	1						C7
19	106RLR025M	CAP, AL EL, 10μF	ILLINOIS CAPACITOR	7						C8, 22, 35, 39, 41, 45, 46
20	105RLR050M	CAP, AL EL, 1μF	ILLINOIS CAPACITOR	5						C10, 15, 19, 27, 34,
21	DM15-FY101J	CAP, MIC, 100PF	ELMENCO	1						C24
22										

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100304 SH 3 OF 3 REV E REMARKS
23	1N4148	DIODE, RECT		11										CR1-10, 12,
24	5082-4494	DIODE, LED	HP	1										CR11
25	1N4001	DIODE		6										CR13-18
26	22-23-2031	CONN, 3 PIN	MOLEX	1										J3
27	22-17-2102	CONN, 10 PIN	MOLEX	1										P1
28	52-052-0000	CONN, PLUG	SEALECTRO	1										J2
29														
30	SWD 15000 MS90537-63	INDUCTOR, RF CHOKE, 15000 UH	NITRONICS	.1										L2
31	SWW 3.3 MS21400-7	INDUCTOR, RF CHOKE, 3.3 UH	NITRONICS	2										.L3, 4
32														
33	J176	XSTR, FET	NATIONAL	4										Q1-4
34	MPS6523	XSTR, PNP	MOTOROLA	7										Q5-9, 11, 13
35	BFW92A	XSTR, NPN	MOTOROLA	3										Q10, 12, 14
36	MPS6521	XSTR, NPN	MOTOROLA	2										Q15, 16
37														
38	3262W-1-103	RES, VAR, 10K	BOURNS	1										R1
39	27K	CARB FILM RES, 1/8W, 5%		2										R2, 3
40	39K			4										R4-7
41	160K			2										R8, 9
42	3.3K			1										R10
43	4.3K			1										R11
44	100K	CARB FILM RES, 1/8W, 5%		6										R12, 13, 69, 70, 72, 74

7100304

SH 4 OF E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
45	2.7K	CARB FILM RES, 1/8W, 5%		1										R14
46	51K			4										R15,17,19,21
47	5.6K			1										R16
48	10K			9										R18,23,25,27,33, 42,49,61,73
49	27K			3										R20,45,52
50	22K			5										R22,24,26,30,71
51	10Ω			3										R63-65
52	1K			2										R28,58
53	62K			1										R29
54	390Ω			1										R31
55	62Ω			1										R32
56	33K			3										R34,43,50
57	2.2K			3										R35,44,51
58	7.5K			2										R36,60
59	560Ω			3										R37,46,53
60	200Ω			3										R38,47,54
61	470Ω			3										R39,48,55
62	430Ω			1										R40
63	56Ω			1										R41
64	6.8K			3										R66-68
65	9.1K			1										R56
66	3K	CARB FILM RES, 1/8W, 5%												R57

7100304 SHEET 3 OF E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
57	3.3K	CARB FILM RES, 1/8W, 5%		1										R59
58	4.7K	CARB FILM RES, 1/8W, 5%		2										R62,75
59	0Ω	CARB FILM RES, 1/8W, 5%		1										R76
60														
61														
62	MC145156P	I.C.	MOTOROLA	1										U1
63	CD4555BE	I.C.	RCA	1										U2
64	74S113N	I.C.	NATIONAL	1										U3
65	MC12013P	I.C.	MOTOROLA	1										U4
66														
67	MC78L12ACP	+12V REG	MOTOROLA	1										VR1
68														
69	MC79L12ACP	-12 V RGLTR	MOTOROLA	1										VR3
70		WASHER, INT STAR, NO.2		1										
71														
72	520-AG19D	SOCKET	AUGAT	1										XU1
73														
74														
75														
76														
77														
78														

CAPACITOR REFERENCE DESIGNATORS:

-ITEM 16, .01UF: C5, 9, 11, 12, . . 14, 16, 17, 18, 20, 21, 23, 25, 26, 28, 29, . . 36, 37, 38,

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	DATE	
APPVD M. Dela	DATE 11/9/83	
CHECK B. BODIKER	DATE 9/15/83	
DRAWN J Fresh	DATE 8-10-83	

TITLE: MAIN LOOP, SYNTHESIZER

PARTS LIST 7100305
SHEET 1 OF 7 | REV G
MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100418			
QTY REQUIRED THIS RELEASE	FINAL ASSY	240-410	345-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	CHANGED PER PROTO TYPE 8/25/83		B. BODIKER	2/29/84
B	INCORP ECN 5420 J Fresh 2-20-84		B. BODIKER	2/29/84
C	INCORP ECN 5560 J Fresh 4-19-84		B. BODIKER	5/2/84
C R1	PICTORIAL CHG ONLY	MAR 11-6-84	B. BODIKER	11/8/84
D	ECN 5613 EFF: S/N 012 & ON	MAR 11-6-84	B. BODIKER	11/8/84
E R3	ECN 5608 EFF: 024, 025, 027 & ON	MAR 11-6-84	B. BODIKER	11/8/84
F	DDC: ADDED NOTE 7 REF: ECR 5774	MAR 11-6-84	B. BODIKER	11/8/84
G	INCORP ECN 5905 EFF: 001 & ON	JJ 6/3/85	B. BODIKER	6/3/85

7100305 SH 2 OF 7 G

ITEM NO	PART NO	DESCRIPTION	MFR OR MANUFACTURER	ASSEMBLY -1	REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	7100305-1	MAIN LOOP		/						
2										
3	7100427-1	CABLE ASSY		1						W1
4	7100205-1	PWB		1						
5	7100505	SCHEM		REF						
6	7100419-1	VCO, MODULE		1						A1
7	7100419-2	VCO, MODULE		1						A2
8	SBL-1	MIXER	MINI CIRCUITS	1						A3
9	LF347N	OPAMP	NAT	2						AR1, AR2
10	LF351N	OPAMP	NAT	3						AR3-5
11	MWA120	AMP	MOT	2						AR6, 7
12	Ø8Ø5B103K2T	CAP, CHIP .01MF	VICLAN	4						C43 C87-89
13	C315C103K5R5CA	CAP, CER, .01µF, 50V	KEMET	32						C1, 10, 13-22, 38 44-46, 48-51, 53, 55
13				↑						C57, 58, 61, 62, 72-77 79, 80, 81
14	C315C391K2R5CA	CAP, CER, 390 PF	KEMET	1						C2
15	T350H226K025AS	CAP, TANT 22µF 25V	↑	1						C4
16	T350E106K025AS	CAP, TANT 10µF 25V	↕	4						C5, 24, 54, 70
17	T350A105K025AS	CAP, TANT, 1µF 25V	↓	6						C9, 23, 34, 56 60, 78
18	C320C104K5R5CA	CAP, CER .1µF,	KEMET	22						C3, 6-8, 11, 12, 28-32, 35, 36 40, 42, 52, 59, 64, 65 82-84
19	23BJ410	CAP, MYLAR .1µF	MOUSER	2						C25, 26
20	C315C[illegible]K1R5CA	CAP, CER, 2200PF	KEMET	2						C27, 71
21	T350C106K010AS	CAP, TANT, 10µF, 10V	KEMET	2						C33, 85

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100305 SH 3 OF 7 G REMARKS
22														
23	C315C331K2R5CA	CAP, CER, 330pf	KEMET	2										C37, 41
24														
25	T350H 686K010AS	CAP, TANT, 68µF, 10V		1										C47
26	C312C101K2G5CA	CAP, CER, 100pf		1										C63
27	T350A 105K035AS	CAP, TANT, 1µF, 35V	KEMET	2										C66, 69
28	107RMR025M	CAP 100µF, 25V	ILL CAP	2										C67, 68
29														
30	MPN 3404	DIODE	MOT	8										CR3, 4, 13-18
31	1N4148	DIODE		17										CR1, 2, 5-12, 19, 21-26
32	5082-4494	LED	H. P.	1										CR20
33														
34														
35														
36	22-17-2102	CONNECTOR, 10SOC	MOLEX	2										P1, P4
37	52-051-0000	COAX CONN	SEALECTRO	2										P2, 3
38	MS21401-25 SW-W-1500	INDUCTOR 1500µH	NYTRONICS	1										L1
39	MS21400-1 SW-W-1.0	INDUCTOR 1.0µH	NYTRONICS	7										L5, 6, 8, 9 11-13
40	MS21400-13 SW-W-10	INDUCTOR 10µH	NYTRONICS	4										L2-L4, L7
41	MPS6521	XSTR, NPN	MOT	5										Q1, 3, 5, , 13, 14
42	MPS6523	XSTR, PNP	MOT	2										Q2, 4
43	BFW92A	XSTR. NPN	MOT	2										Q6, 11

7100305 SH 4 OF 7 G

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	BLOCK NO. ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
4														
5	MPSH10	XSTR	MOT	4										Q7,9,10,12
6	MPSH81	XSTR	MOT	1										Q8
47	100K 1/8W 5%	RES CARB FILM		6										R1-3,23,67,68
48	51K			8										R4,21,24,55,57 60,62,107
49	33K			3										R5,41,100
50	10K			17										R6,9,42,64,68,72, 79,103,104,106
/	10K CONT'D			↑										R108, R117-121 R127
52														
53	5.1K			3										R10,28,102
54	20K 1/8W 5%			1										R11
55	806K 1/8W 1%			1										R13
56	402K 1/8W 1%			1										R14
57	200K 1/8W 1%			1										R15
58	100K 1/8W 1%			1										R16
59	150K 1/8W 5%			1										R17
60	22K			3										R18,78,85
61	470K			1										R19
62	470Ω			6										R20,47,70,73 90,112
63	2.2K			3										R22,43,66
64	18K			2										R25,29
65	12K 1/8W 5%	RES CARB FILM		1										R26

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY REQ ASSEMBLY -1					KEY QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	100305 SH 5 OF 7 G REMARKS
66	6.8K 1/8W 5%	RESCARB FILM		3										R27,56,58
67														
68														
69	7.5K			2										R30,115
70	5.6K			1										R31
71														
72	220Ω 1/8W 5%			13										R7,8,33,48,76,89, 95-99,125,726
73	160Ω			1										R34
74	18Ω			1										R35
75	68Ω			1										R40
76	100Ω			5										R37,39, 101,105,130
77	330Ω			1										R38
78														
79	2.7K			1										R44
80	200Ω			2										R45,111
81	9.1K			2										R46,109
82	62K			1										R49
83	820Ω			2										R53,59
84	120K			1										R51
85	91K			1										R52
86	620Ω			1										R128
87	5.6K 1/8W 5%	RES CARB FILM		1										R54

7100305
SH 6 OF 7 | G

ITEM NO	PART NO	DESCRIPTION	VENDOR OR MANUFACTURER	QTY REQD ASSEMBLY -1	REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
88	560Ω 1/8W 5%	RES CARB FILM		1						R71
89										
90										
91	3262W-1-103	TRIM POT 10K	BOURNS	1						R61
92	750K 1/8W 5%	RES CARB FILM		1						R63
93	1K			9						R69,74,86-88,113, 122-124
94	82Ω			2						R75,91
95	3.9K			1						R77
96										
97	300Ω			2						R80,R36
98	3.6K			2						R81,R32
99	62Ω			1						R82
100										
101										
102	3.3K			1						R116
103	10Ω			6						R92,93,79,50 R131,84
104	150Ω			1						R94
105	75K			1						R110
106	16K			1						R114
107	51Ω			1						R132
108	430Ω			1						R129
109	240K 1/8W 5%	RES CARB FILM								R12

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REV. QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
10	MC14094BCP	IC	MOT	2										U1, 2
11	CD4051BE	IC	RCA	1										U3
12	MC4044P	IC	MOT	1										U4
13	MC12013P	IC	MOT	1										U5
14	SN74LS196N	IC	TI	2										U6, 7
15	MC12090P	IC	MOT	1										U8
16	LM7812CT	REG	NAT	1										VR1
17	LM7805CT	REG	NAT	1										VR2
18	LM79M12CH	REG	NAT	1										VR3
19														
20														
21	#2	WASHER	INT STAR	2										
22														
23	.003THK × ½WIDE	TAPE, MYLAR	PERMACEL	A/R										
24														
25	7-120-BA	HEATSINK	IERC	2										
26	60-11-4374-1674	THERMAL TRANSIPAD	CHROMERICS	1										
27														
28														
29														
30														
31														

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE [illegible]	TITLE CARRIER BOARD, SYNTHESIZER	7100306
	APPVD [illegible]	DATE [illegible]		SHEET 1 OF 2 REV A
	CHECK G Landi	DATE 11-15-83		MWO
	DRAWN J Fresh	DATE 9-29-83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100418			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD DATE
A	DDC ITEM 7 P/N WAS 5082-4494 JT 2-23-86	L CHAVEZ 3/10/86

7100306 SH 2 OF A

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	7100306-1	CARRIER BD		/						
2										
3	7100818	SCHEM		REF						
4	7100206-1	P.W.B.		1						
5										
6	CK05BX103K	CAP, CER. 01		1						C1
7	HLMP-1002	LED	H.P.	1						CR1
8	MPS6521	XSTR, NPN	MOTOROLA	2						Q1, 2
9	100K 1/8W 5%	RES CARB FILM		4						R1-4
10	1K 1/8W 5%	RES CARB FILM		1						R5
11	10K 1/8W 5%	RES CARB FILM		4						R6-9
12	MM74C906N	IC, N CH BUFFERS	NAT	1						U1
13										
14	TS-120-G-D-Z-1	TERMINAL STRIP, 20 PIN HEADER	SAMTEC	2						A1J1 A1J4 A2J1, A3J1
15	51-051-0000	CONN, RECEPT.	SEALECTRO	1						J3
16	1-102584-0	CONN. 70 SOC	AMP	1						P1
17	S203	EJECTOR, CARD	SCANBE	2						
18										
19										
20										
21										
22										

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	DATE	
APPVD	DATE	
CHECK B. BODIKER	DATE 7/28/83	
DRAWN	DATE 7-27-83	

TITLE: CIRCUIT BOARD, MAIN LOOP VCO

PARTS LIST 7100308

SHEET 1 OF 3 | REV D

MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100419			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	ECN # 5441 Issued 2-22-84		B. BODIKER	2/28/84
B	ECN # 5512 M. ROBERTSON 10-31-84	EFF: 007 & ON	B. BODIKER	2/18/85
C	ECN # 5594 M. ROBERTSON 10-31-84	EFF: 001 & ON	B. BODIKER	2/18/85
D	ECN # 5877 M. ROBERTSON 10-31-84	EFF: 107 & ON	B. BODIKER	2/18/85
ORI	ADDED SECTION A-A TO F/D	EFF: 107 & ON KD 5-2-85	B. BODIKER	5/2/85

7100308 SH 2 OF 3 D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	BD ASSY		/	-						(LOW BAND)
2	-2	BD ASSY		-	/						(HIGH BAND)
3											
4	7100208-1	P.W.B.		1	1						
5	7100819	SCHEMATIC		REF	REF						
6	7100708-1	INDUCTOR		1	—						-1: L1 / -2: —
7	7100708-2	INDUCTOR		—	1						-1: — / -2: L4
8	7100708-3	INDUCTOR		1	—						-1: L2 / -2: —
9	7100708-4	INDUCTOR		—	1						-1: — / -2: L3
10	7100708-5	INDUCTOR		1	—						-1: L3 / -2: —
11	Ø8Ø5B1Ø3K3T	CAP, CHIP, .01µF	VICLAN	13	13						C1-6, 8-10 14-17
12	Ø8Ø5C1ØØD2T	CAP, CHIP, 10pf	VICLAN	2	2						C7, 13
13	0805C101J2T	CAP, CHIP, 100pf	VICLAN	1	1						C11
14	Ø8Ø5C5RØD2T	CAP, CHIP, 5 Pf	VICLAN	1	1						C12
15	7100708-6	INDUCTOR		1	1						-1: L4 / -2: L2
16	MA-47054	DIODE	MA/COM	4	4						CR1-3, 6
17	MV2Ø9	DIODE	MOT	2	2						CR4, 5
18	2743ØØ1111	SHIELD BEAD	FAIR-RITE	1	1						L5
19	7100708-7	INDUCTOR		—	1						-1: — / -2: L1
20	BFW92A	TRANSISTOR	MOT	1	1						Q1
21	MPS6523	TRANSISTOR	MOT	1	1						Q2
22	0805[illegible]R3D2T	CAP, CHIP, 3.3Pf	VICLAN	[illegible]	1						C18

FORM 189

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2				QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100308 SH 3 OF 3 D REMARKS
23	1.5K 1/8W 5%	RES, CARB FILM		3	3									R1-3
24	12K			1	1									R10
25	47K			1	1									R18
26	8.2K			2	2									R11, 12
27	470Ω			2	2									R15, 16
28	51Ω			1	1									R13
29	3K			1	1									R14
30	36K.			1	1									R9
31	330Ω			1	1									R6.
32	10K.			1	1									R17
33	10Ω			1	1									R4
34	180Ω			1	1									R5
35	56Ω			1	1									R7
36	1K 1/8W 5%	RES, CF		1	1									R8
37	350-2188-13-05	SPACER SWAGE 2-56x1/2	CAMBION OR ≈	1	1									
38														

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL Mustafa Yakus	DATE 7/28/83	TITLE CIRCUIT BOARD ASSY VCO, SWITCHED RANGE	PARTS LIST 7100309
APPVD L. Ok	DATE 7/28/83		SHEET 1 OF 3 REV B
CHECK B. BODIKER	DATE 7/28/83		MWO
DRAWN A. Tesla	DATE 7-27-83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100405			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	INCORP ECN 5411 KD 1/17/84	B. BODIKER	1-19-84
B	INCORP ECN 5472 EFF: 001 & ON KD 6-11-85	B. BODIKER	6/26/85

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100309 SH 2 OF 3 B REMARKS
1	7100309-1			/										
2														
3	7100209-1	P.W.B		1										
4	7100805	SCHEMATIC		REF										
5	7100707-1	INDUCTOR		1										L1
6	7100707-2			1										L2
7	7100707-3			1										L3
8	7100707-4	INDUCTOR		1										L4
9	T14ØB566KØ1ØAS	CAP, TANT 56µF 10V	KEMET	1										C1
10	Ø8Ø5C12ØJ2T	CAP, CHIP, 12pf	VICLAN	1										C2
11	12Ø9BIØ4K2T	CAP, CHIP .1µF	VICLAN	1										C3
12	DM5-FY91ØJ	CAP, MICA, 91Pf	ELMENCO	1										C4
13	ØBØ5C4RØD2T	CAP, CHIP, 4Pf	VICLAN	1										C5
14	Ø8Ø5C5ØØJ2T	CAP, CHIP, 50pf	VICLAN	1										C6
15	Ø8Ø5C5RØD2T	CAP, CHIP, 5Pf	VICLAN	1										C7
16	Ø8Ø5BIØ3K3T	CAP, CHIP, .01µF	VICLAN	4										C8, 10, 11, 12
17	T39ØAIØ5KØ25AS	CAP, TANT, 1MF	KEMET	1										C9
18														
19	MV2Ø9	DIODE	MOT	4										CR1-4
20	MPN34Ø4	DIODE	MOT	3										CR5-7
21	2643000101	BEAD	FAIR-RITE PROD	1										Z1
22														

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REF QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100309 SH 3 OF 3 B REMARKS
23	BFW92A	XSTR	MOT	2										Q1,2
24														
25	390Ω 1/8W 5%	RES,CARB FILM		1										R1
26	33Ω			2										R2,4
27	220Ω			1										R3
28	3K			2										R5,6
29	5.1K			1										R7
30	22K			1										R8
31	100K			1										R9
32	33K			2										R10,11
33	1.5K			3										R12,13,14
34	10K 1/8W 5%	RES,CARB FILM		3										R15,16,17
35														
36	RTV118	RTV ADHV	GE	A/R										
37														
38														
39														
40														

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL	DATE	TITLE	PARTS LIST 7100205
	APPVD	DATE	MODULE ASSY, SWITCHED RANGE VCO	SHEET 1 OF 2 REV
	CHECK B. BODIKER	DATE 8/18/83		MWO
	DRAWN [signature]	DATE 8/9/83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100304			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE

7100405
SH 2 OF 2

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -10	QTY PER ASSEMBLY	QTY PER ASSEMBLY	QTY PER ASSEMBLY	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	7100405-1	MODULE ASSY		X										
2														
3	7100405-10	NEOPRENE PAD		3	X									
4														
5	7100048-1	BOX		1										
6	7100048-2	COVER		1										
7														
8	7100309-1	VCO, SWITCHED RANGE BD		1										
9														
10														
11														
12	TF125/20SCSC	TERMINAL FEEDTHRU	GLASS SEAL	7										
13	7719A	TERMINAL PN	USECO	1										
14														
15	350-2188-07-07-00	STANDOFF 2-56 x .75	CAMBION	1										
16														
17	NO. 2	WASHER, SPLIT		1										
18	NO. 2	WASHER, FLAT		1										
19	2-56 x 5/16	SCREW	PAN HD PHILLIPS	1										
20														
21	R-411-N x .125	NEOPRENE FOAM	RUBATEX	—	A/R									
22	NO 7	SPRAY ADHESIVE	3M	A/R										

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REL	10/10	DATE	
APPVD		DATE	
CHECK	Gilandri	DATE	10/13/83
DRAWN	Fresh	DATE	10-5-83

TITLE: VCO MODULE, MAIN LOOP

PARTS LIST 7100[illegible]-19

SHEET 1 OF 2 | REV C

MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100305			
QTY REQUIRED THIS RELEASE	FINAL ASSY	7100418			
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	ECN # 5440 Fresh 2-22-84	B. BODIKER	2/28/84
B	INCORP ECN 5819 EFF: S/N 107 & ON MAR 11-6-84	B. BODIKER	11/6/86
C	INCORP ECN 6161; EFF: 181 & ON A.O. 7/26/85	B. BODIKER	9/4/85

7100417 SH 2 OF 2 C

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	7100419-1	VCO		X	-						
2	7100419-2	VCO		-	X						
3											
4											
5	7100049-1	BOX		1	1						
6	7100049-2	COVER		1	1						
7	7101017-1	SPACER		1	1						
8	7100308-1	CKT BOARD		1	-						(LOW BAND)
9	7100308-2	CKT BOARD		-	1						(HIGH BAND)
10											
11											
12	TF125/205CSC	FEED THRU	GLASS SEAL	8	8						
13											
14											
15	350-1249-01-05	STAND OFF	CAMBION	1	1						
16											
17											
18											
19	2-56X 1/4	SCREW, SS	PH PN HD	1	1						
20	2-56X 3/8	SCREW	PH PN HD	1	1						
21											
22	22	RETAING CMPD	LOCTITE	A/R	A/R						

OCEAN APPLIED RESEARCH CORPORATION
San Diego, Cal. 92121

REL	[illegible]	DATE 6/6/85	
APPVD	[illegible]	DATE [illegible]	
CHECK	B. BODIKER	DATE 6/6/85	
DRAWN	J. Fresh	DATE 9-30-83	

TITLE: VOLTAGE REGULATOR, SUBLOOP

PARTS LIST 7100[illegible]21

SHEET 1 OF 2 | REV A

MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100418			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	INCORP ECN 6132 EFF: 001 & ON JJ 6/6/85	B. BODIKER	6/6/85

7100421

SH 2 OF 2 | A

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	-1	V RGLTR		/						
2										
3										
4										
5	MC7805CT	VREGULATOR	MOTOROLA OR EQ	1						
6	E-24	WIRE, BRN	MIL-W-16878	A/R						
7	E-24	WIRE, RED	"	A/R						
8	E-24	WIRE, ORN	MIL-W-16878	A/R						
9	FIT-300-1/8	INS TUBING HEAT SHRINK	ALPHA OR EQ	A/R						(MIL-I-23053/4)
10										
11	08-55-0102	CONTACTS	MOLEX	3						
12	22-01-3037	CONNECTOR, 3	MOLEX	1						

TIME BASE/LOCAL OSCILLATOR ASSEMBLY

ASSEMBLY: 7100429.2

SCHEMATIC: 7100829
7100507
7100511
7100520

SECTION I

DESCRIPTION

1.1 General

The time base/local oscillator assembly is made up of the time base board, and the second and third local oscillator boards, which are mounted on the time base board. The second and third local oscillator boards are contained in a common housing, and the time base board includes its own modular assembly, the VC-TCXO (7100721). The whole assembly is mounted on, and externally connected to the power and signal bus board.

The time base provides an extremely stable reference frequency output of 12.8 MHz to the first local oscillator. The heart of the circuitry is a voltage controlled, temperature compensated reference oscillator (VC-TCXO) accurate within two parts per million. The oscillator normally is allowed to free run. It also may be locked to a 1 MHz external frequency standard. When an external standard is used the oscillator frequency is phase locked to the external signal thru the action of a phase-locked loop. In the absence of an external signal the phase-locked loop is disconnected.

The second local oscillator provides two output frequencies, 84.7 MHz or 127.05MHz, as determined by PIN diode switching in the oscillator circuits. The data processor selects the output to match the IF inputs to the second converter, 74 MHz or 137.75 MHz respectively. Therefore, oscillator output is either 10.7 MHz above or below the selected IF.

The second local oscillator is a crystal oscillator operating at a frequency of 42.35 MHz. Oscillator output is multiplied by x2 or x3 (as

selected), to obtain the desired output. Fine tuning in the oscillator circuit varies the frequency in nineteen 10 Hz steps (42.35 MHz + 0 Hz, to 42.35 MHz + 190 Hz). Fine tuning and temperature compensation inputs are combined to provide a single control input to the oscillator tuned circuit.

Fine tuning of the second local oscillator provides the 10 Hz frequency resolution of the overall system. Temperature compensation is also provided to the oscillator by the temperature compensation generator. Oscillator output is through a power amplifier whose output is fed to a splitter; providing one output to the second converter and an auxiliary output, which is currently unused. A fault detector monitors the output and provides an indication when output is low or missing.

The third local oscillator operates at 11.155 MHz for all modes, and provides the means of conversion from 10.7 MHz to 455 kHz IF. The oscillator is a standard Colpitts design, with a buffer amplifier in the output which limits the effects of output load variations on the operating frequency.

1.2 Circuit Description

The time base/local oscillator assembly (see diagram 7100829) is connected to the power and signal bus board via the 70 pin connector (P1). Data and power inputs to the time base board occur on this 70 pin connector. An external 1 MHz frequency reference may be connected to the time base board via the rear panel, and enters at J1. The time base board provides two 12.8 MHz reference frequency outputs; the J2 output to the frequency synthesizer, and the J3 auxiliary output (currently unused).

External signals to the second and third local oscillators are input from

the signal bus via two multiple pin connectors on the time base board. A ten line connection is made from XA1 on the time base board to P1 on the second local oscillator board. A six line connection is made from XA2 on the time base board to P1 on the third local oscillator board. Power and data inputs to the oscillators are connected via these lines. Serial data is fed from the data processor to the third local oscillator data receiver via the second local oscillator data receiver and is interconnected via the QS' line. The second local oscillator has two outputs; J6 to the second converter module of the preselector, and J5 (AUX). The third local oscillator output at J4 is to the 455 kHz mixer on the IF/demodulator board.

1.2.1 Time Base Board

Refer to the block diagram (figure 1) and schematic drawing 7100507 during the following discussion.

The VC-TCXO (A3) has a square wave output with a frequency of 12.8 MHz. The inverters (U1, B, C, D) isolate the output from the load, buffering the oscillator, and preventing frequency pulling when the load changes. The 12.8 MHz output goes to the synthesizer (J2), with an auxiliary output at J3. The square wave output at U1C (pin 8) is also fed back to pin 3 of U3. In U3, the 12.8 MHz is divided by 128, and provides a 100 kHz input to a phase comparator.

When an external reference is present, the two 100 kHz signals are compared in the phase comparator circuit of U3. When no external signal is present, the output of U3 is disabled.

The 12.8 MHz output at U1C (pin 8) is also input to the fault detector (AR1C), where it charges C26, providing a positive input to AR1C pin

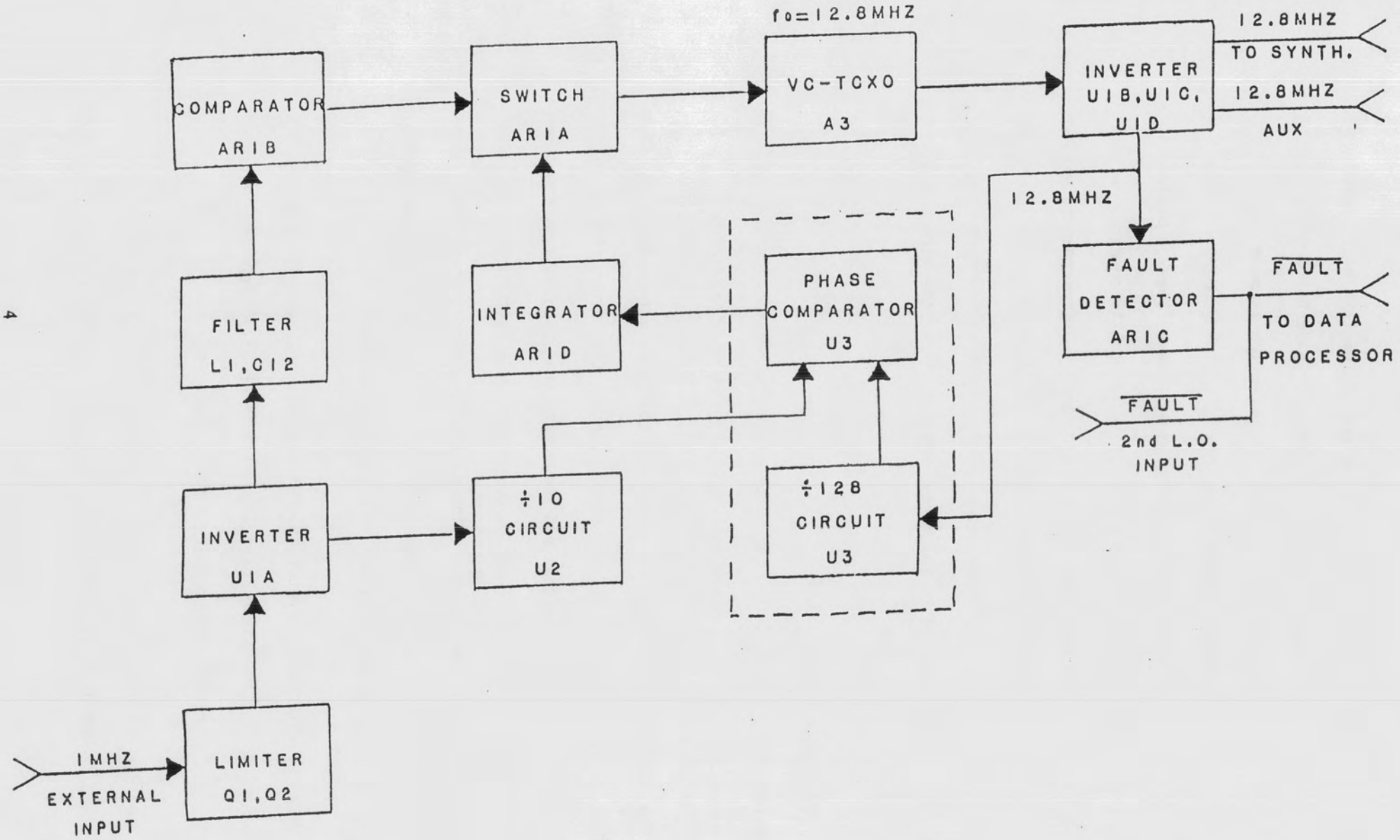


Figure 1. Block Diagram, Time Base

9. If oscillator output should fail (or decrease radically) capacitor C26 will discharge, driving the AR1C output to +12V. This forward biases CR15, which lights the LED (CR16) and presents a $\overline{\text{FAULT}}$ output to P1 pin 67. Another $\overline{\text{FAULT}}$ output will occur at pin 67 when the second local oscillator has a fault (XA1-8).

When an external frequency standard is connected to J1, the 1 MHz input is limited to produce a square wave at the output of Q1, which is clamped by CR9 to alternate between +5 V and 0 V at the output of Q2. Inverter U1A provides isolation and its output is branched to the ÷ 10 circuit (U2) and to the 1 MHz band pass filter (L1, C12).

When a 1 MHz input is detected by the bandpass filter, C12 is charged positive, the comparator AR1B is enabled, and the output is driven to +12V. This reverse biases CR11 and allows the phase-locked loop to control the output of AR1A. When no 1 MHz external signal is present, AR1B output drops to -12V. This forward biases CR11 and turns the switch (AR1A) off, disabling the loop input.

The phase-locked loop operates in this manner. The 1 MHz external input is divided by ten by U2. The 100 kHz output of U2 (pin 7) is one of the phase comparator inputs of U3. It is compared to the 100 kHz input from the local oscillator (fo ÷ 128). If the local oscillator frequency should vary, the output of U3 will go to a high or a low state, dependant on the direction of fluctuation.

If the oscillator frequency should decrease, the phase comparator output of U3 (pin 5) would go high at the pin 13 input of the integrator, AR1D. The output of AR1D will go negative, driving the output of AR1A positive. Because of the +12V at the output of AR1B,

the pullup action of R18 at the junction of CR12 and R22 will maintain forward bias on CR12. This allows the positive output of AR1C to charge C21 positive. The positive control voltage will increase the oscillator frequency, driving it up until the phase-lock loop is locked.

If oscillator frequency increases, the output of the phase comparator will go low, driving the output of the integrator (AR1D) positive. The positive input to AR1A drives the output (pin 1) negative, forward biasing CR12 and charging C21 negative. A negative control voltage to the oscillator will decrease the output frequency until the phase-locked loop is once again locked.

Connectors XA1 and XA2 provide interface between the time base board and the second and third local oscillator boards. Power inputs of +15 V, -15 V and +8 V dc, are used by regulators VR1-VR3 to provide regulated +12 V, +5 V, and -12 Vdc to the time base board. Diodes CR1, CR3 and CR5 provide reverse polarity protection, and diodes CR2, CR4, and CR6 provide a path for capacitive discharge, protecting the regulators when power is off.

1.2.2 Second Local Oscillator Board

Refer to the block diagram (figure 2) and schematic drawing 7100520 during the following discussion.

The crystal oscillator (Q1) is a grounded base Colpitts configuration, with the crystal (Y1) located in the feedback path. Inductor L3 coarse tunes the oscillator (with no input to the varactor) for a 42.35 Mhz output. Fine tuning and temperature compensation adjust the

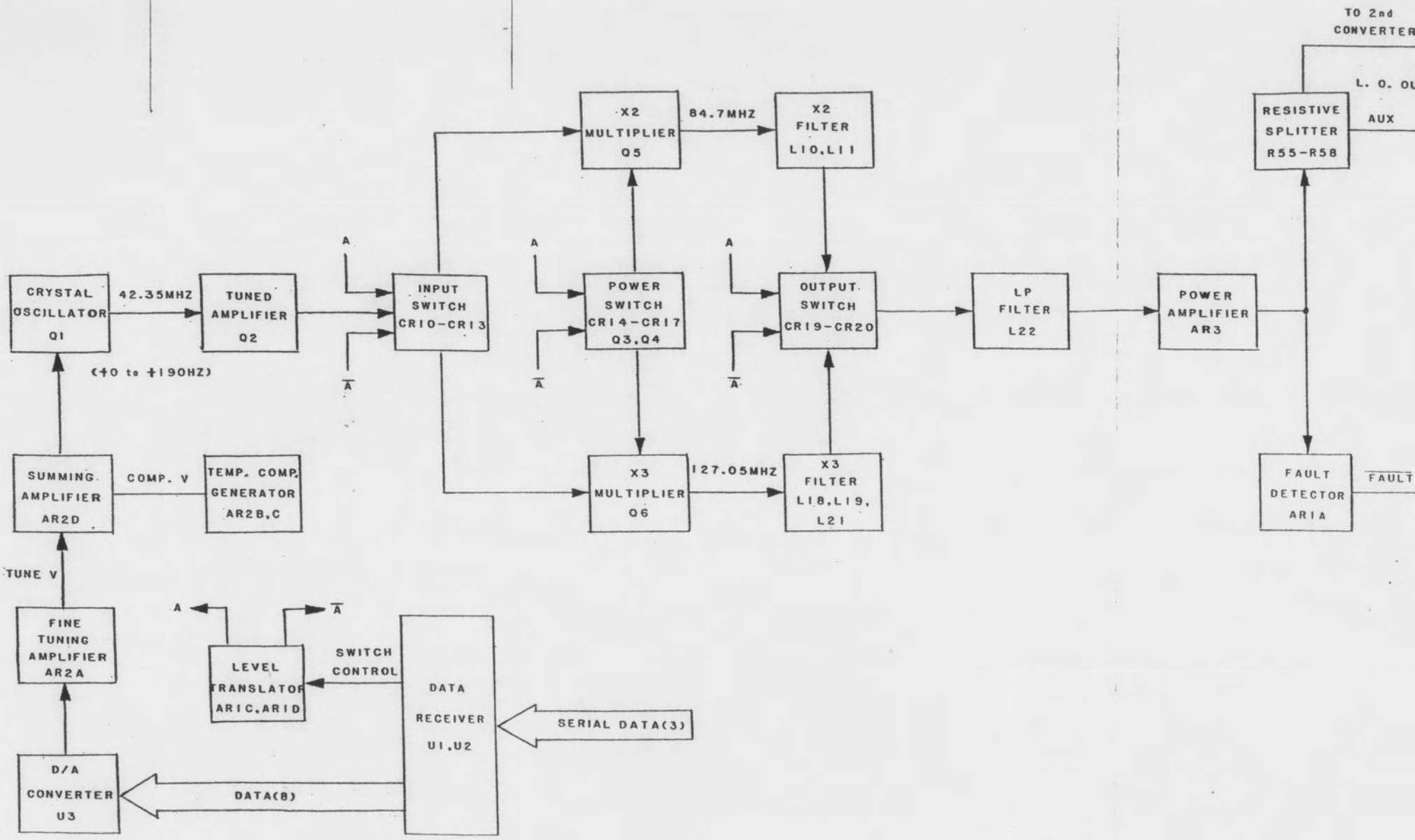


Figure 2. Block Diagram, Second Local Oscillator

local oscillator, by varying the voltage across varactor VR1.

Serial data input from P1 (pins 2-4) to data receiver U1 (pins 1-3), is output from U1 as parallel data (pins 4-7, 11-14) to U3 (pins 1-8). The data is converted in the digital-to-analog converter U3, to provide nineteen discrete (step) voltage levels at the input of tuning amplifier AR2A. With no input (0 Hz), AR2A is zero set by R65. With maximum input (+190 Hz), AR2A output level is set by R24. The fine tuning voltage at pin 13, is one of two inputs to the summing amplifier, AR2D.

Temperature compensation is generated by AR2B and AR2C. Diodes CR1 and CR2 at the input of AR2B, act as temperature sensors, changing the Pin 5 input as a function of temperature. Reference voltage level at pin 6 of AR2B is set for +6 Vdc at an approximate temperature of 25 degrees Centigrade. The second amplifier (AR2C), in conjunction with diodes CR3-CR6 forms a break point generator. The characteristic curves of the output of AR2C and the oscillator (Q1) are similar, but opposite, providing a fairly linear temperature characteristic.

The output of the temperature compensation generator is summed with the fine tuning input at pin 13 of the summing amplifier, AR2D. The summing amplifier output (pin 14) is to the varactor (VR1) providing fine tuning and temperature compensation to the oscillator (Q1).

The oscillator output is amplified by Q2, a tuned amplifier. The Q2 output is tuned by L4, and routed to either the X2 or X3 multiplier as determined by the PIN diode switches (CR10-CR13). PIN diode resistance varies proportionally with voltage to control current flow. Switching

data is provided from the data receiver (U2). Data is fed through from U1 (pin 10) to U2 (pin 2) and clock and enable signals are input at U2 (pins 1,3). Data is output as either a high or low level at pin 4. The level translater (AR1C, AR1B) provides both a positive and negative output. If U2 (pin 4) is high, the output at AR1D is positive, and the output of AR1C is negative. These two outputs are designated A and A. With A positive, and A negative PIN diode CR10 is forward biased, providing a signal path to the X2 multiplier; and PIN diode CR13 is forward biased, providing AC grounding at the X3 output. Pin diode CR11 is reverse biased, blocking the X3 signal path and PIN diode CR12 is reverse biased removing AC ground from the X2 output. (If U3 output at pin 4 is low, the opposite conditions exist and output is to the X3 multiplier).

With A input negative CR14 and CR15 are forward biased, and transistor Q3 is switched on, providing power (+12V) to the X2 multiplier Q5. Transistor Q4 is switched off by the positive A input reverse biasing CR16 and CR17, and removing power from Q6 (X3 multiplier), thus preventing noise contamination. The output of Q5 is the second harmonic of the oscillator, 84.7 MHz, as selected by the tuned circuits, the output of Q6 is the third harmonic, 127.05 MHz. Thus, the output is tuned 10.7 MHz above or below the IF of 74 or 137.75 MHz, respectively.

Notch filters in the multiplier output pass the desired frequency while rejecting the unwanted frequencies generated in the multiplication process. Autotransformers (T1 and T2) provide impedance matching in the outputs.

With conditions as previously described, the A and $\overline{A}$ inputs will forward bias CR19 providing a signal path for the X2 multiplier output, and reverse bias CR20 blocking the X3 multiplier output.

The selected output frequency is fed through a low pass filter to the power amplifier (AR3). The amplified output at pin 2 of AR3 is fed to a resistive splitter, providing two outputs; one at E1 to the second converter, and another auxiliary output at E2 which is currently unused.

The fault detector (AR1A) monitors the second local oscillator output by comparing it to a reference level. If output is low, or missing, AR1A is turned off, providing +12V to light LED CR27 as an aid in trouble shooting. Transistor Q7 is turned on, providing a $\overline{\text{FAULT}}$ indication to the data processor.

Power supply inputs are via regulators VR2 and VR3 providing +5V and +12V regulated dc inputs to the board. Diodes CR5 and CR7 provide inverse polarity protection. Diodes CR24 and CR26 provide a path for capacitive discharge, protecting the regulators when power is shut off.

1.2.2 Third Local Oscillator Board

Refer to the block diagram (figure 3) and schematic drawing 7100511 during the following discussion.

Oscillator Q5 is a standard Colpitts oscillator with its feedback elements consisting of capacitors C14 and C15. Output frequency is set by crystal Y1 when the output (pin 4) of the data receiver is high.

The data receiver is actually the third in a series of receivers, and attains its serial data input (QS') from the data receivers in the second local oscillator. Data is input at P1 (pins 3, 4, 5). The data receiver uses the serial input to select one-of-eight outputs. In this case only the pin 4 output is active. This is because the 11.155 MHz output is used for all mode selections (AM, FM, CW, USB, LSB).

A high at U1 (pin 4) is present when any mode is selected. The high output of pin 4 will forward bias Q1. This places about +4.5 Vdc on the emitter of Q1, forward biasing PIN diode CR1, and establishing a current path through R5, CR1 and R12. Resistor R12 is bypassed by capacitor C13, providing an RF feedback path to ground. This enables crystal Y1, and the oscillator will operate at 11.155 MHz.

The oscillator frequency is output through buffer amplifier Q6, to terminal E1. The buffer amplifier provides isolation and prevents signal pulling due to variations in the load. Regulators VR1 and VR2 provide regulated +12V and +5V inputs respectively from the +15V and +8V power supply inputs. Diodes CR5 and CR6 provide capacitive discharge paths, protecting the regulators when power is shut off.

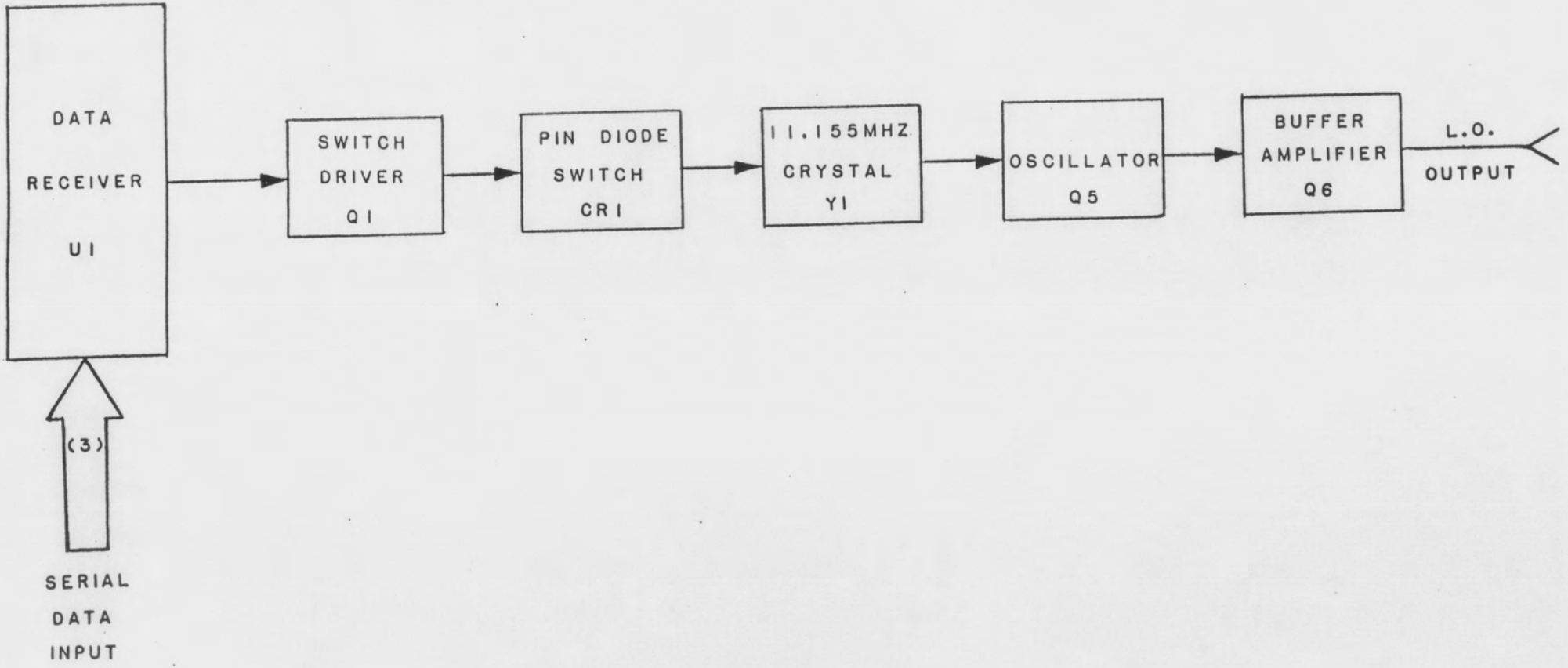
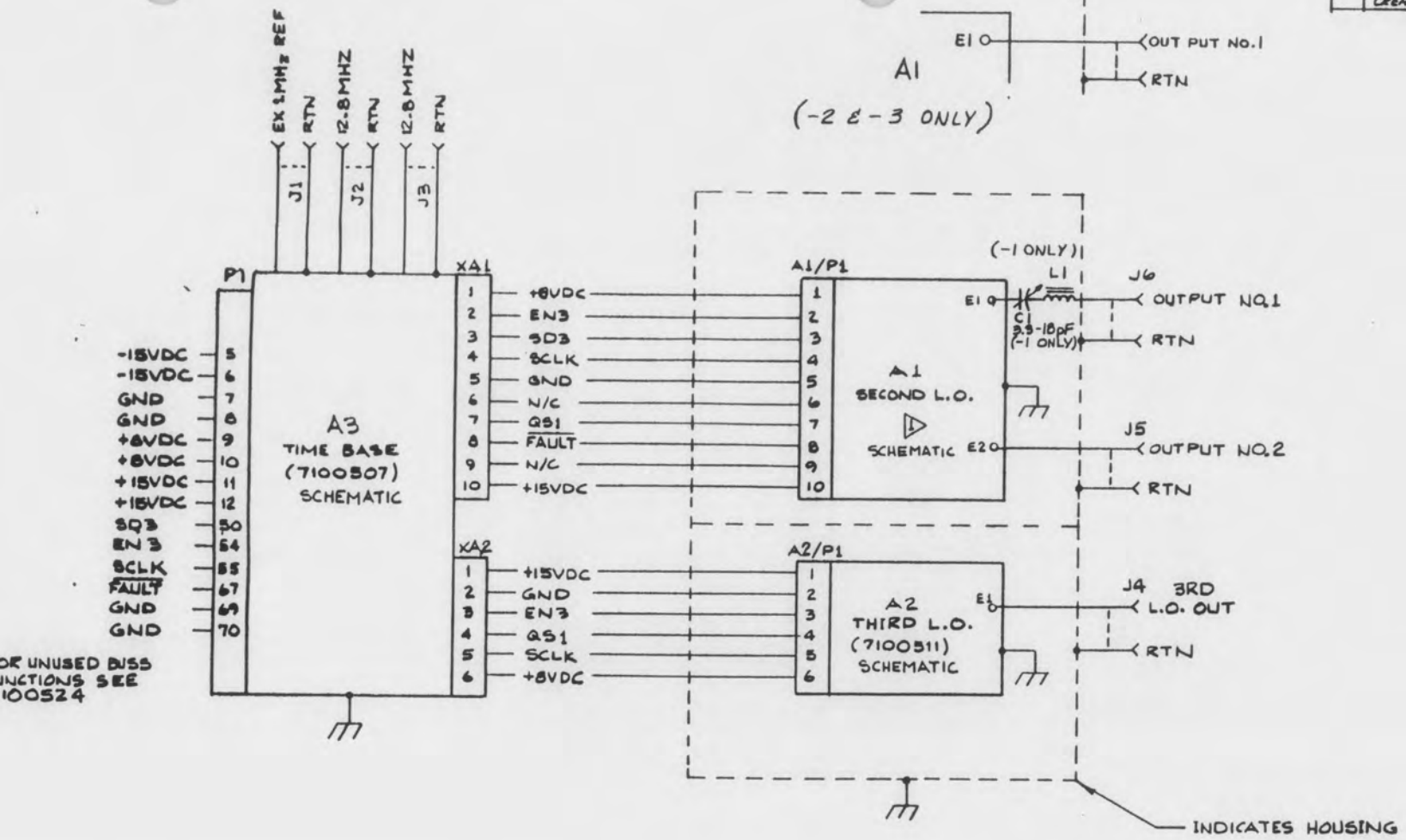


Figure 3. Block Diagram, Third Local Oscillator

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	DOC. REF FOR 5635: ADDED L... CREATED -2&-3 CK'D/4/...	7/13/84	R. BOOKER



-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30', DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010, SURFACE √, HOLE SIZES PER ANSI B32.1

DRAFT	Lovell	4-26-84
CHECK	[illegible]	4-30-84
APP'D	D. Mack	5-1-84
APP'D	T. Mahaffey	5-17-84
	[illegible]	5/21/84
RELEASE	[illegible]	5/21/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

INTERCONNECT DIAGRAM
TIME BASE MODULE, HF RECEIVER

SIZE	DSCM NO.	DWG NO.	REV
C	06994	7100829	A

SCALE N/A SHEET 1 OF 1

7100429
NEXT OR ASSOC ASSEMBLY

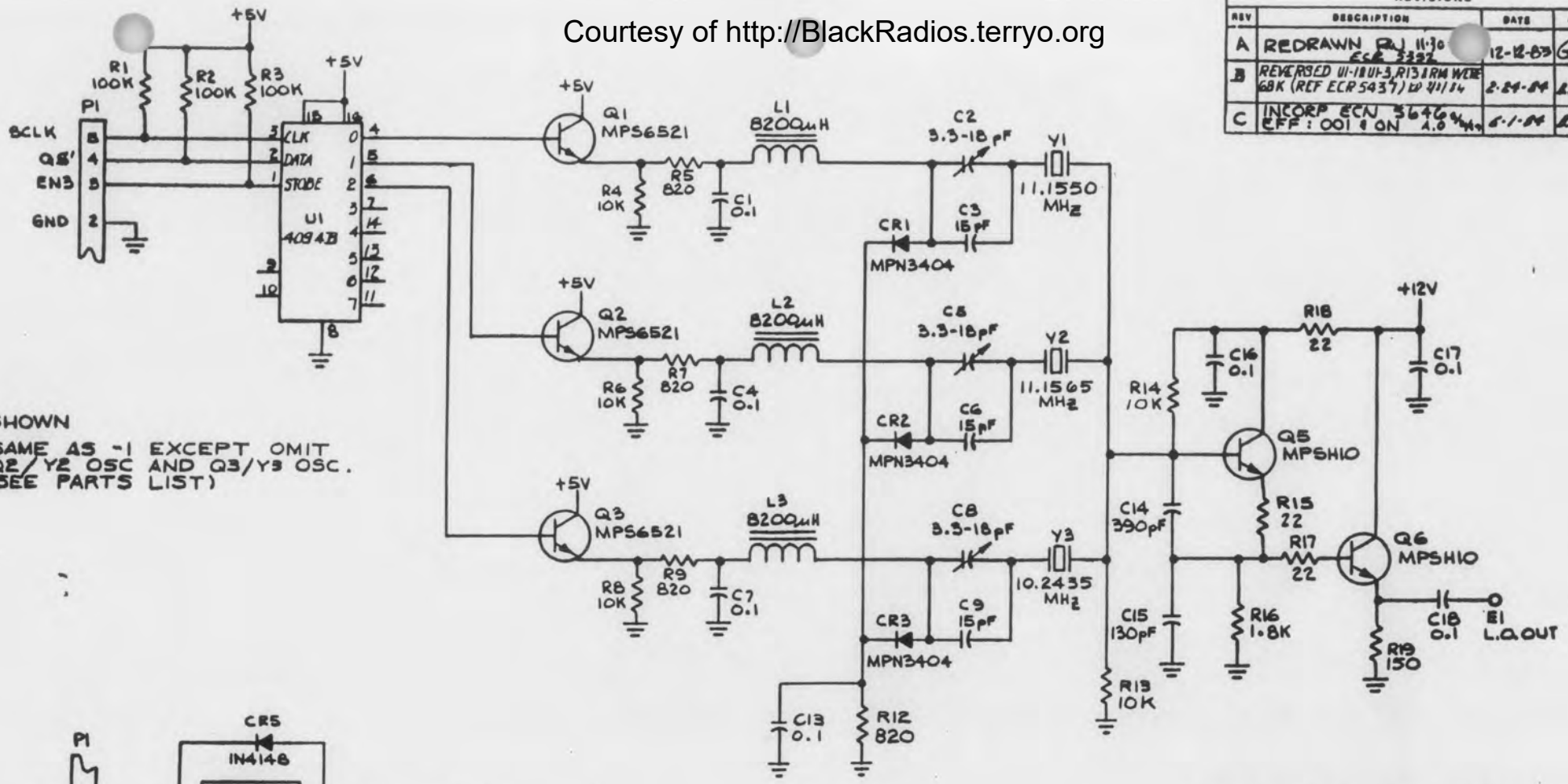
1. FOR VHF/UHF RECEIVER SEE 7100520, (SECOND L.O.).
FOR HF RECEIVER SEE 7100510, OR 7100545 (SECOND L.O.).

1 UNLESS OTHERWISE SPECIFIED

4 3 2 1

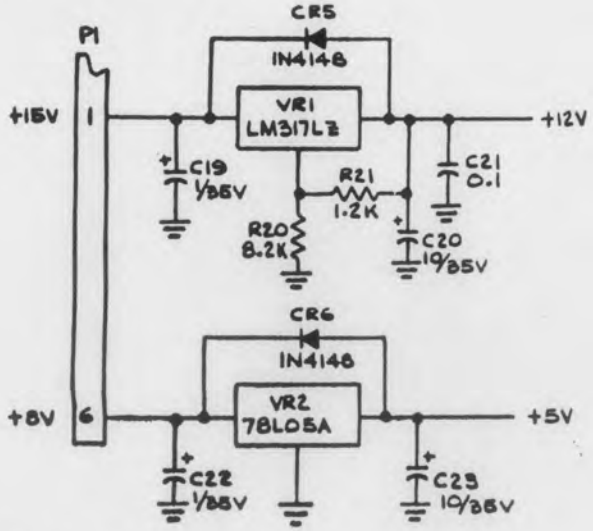
D C B A

7100829



SHOWN

SAME AS -1 EXCEPT OMIT Q2/Y2 OSC AND Q3/Y3 OSC. (SEE PARTS LIST)



CAPACITANCE IN MICROFARADS
RESISTORS ARE 1/8 W, VALUE IN OHMS, ± 5%
-1 UNLESS OTHERWISE SPECIFIED

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REDRAWN BY ECR 5332	11-30 12-12-83	G. Lauder
B	REVERSED U1-18 U1-3, R13 & R14 WERE 68K (REF ECR 5437)	2-24-84	R. BARKER
C	INCORP ECN 5646 EFF: 001 & ON	5-1-84	R. BARKER

HIGHEST REF DES USED									
C23	CR6	E1	L3	P1	Q6	R21	U1	VR2	Y3
REF DES NOT USED									
C10	CR4				Q4	R10			
C11						R11			
C12									

QTY PER ASSY	-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √ HOLE SIZES PER ANSI B32.7

DRAFT	E. WALKER	11-30-83
CHECK	G. Lauder	12-12-83
APPD	[illegible]	12/19/83
APPD	T. Raudsepp	12/19/83
PROJ ENG	R. Dean	12/19/83
RELEASE	[illegible]	12/19/83

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC
3RD L.O. 2040/8045

SIZE	TECH NO.	DWG NO.	REV
C	06994	7100511	C

SCALE — SHEET 1 OF 1

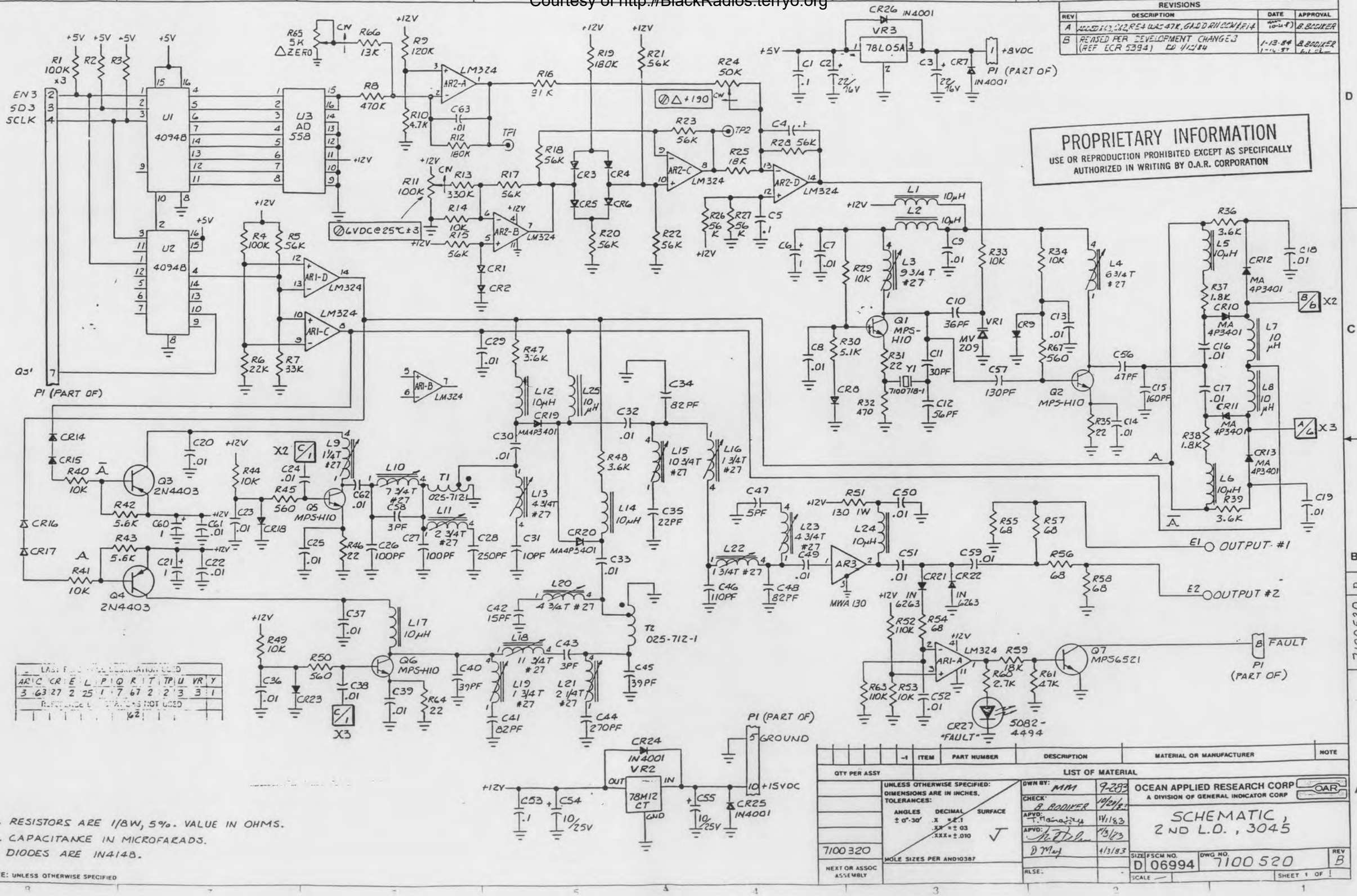
7100311
NEXT OR ASSOC ASSEMBLY

7100511

4 3 2 1

DWG NO. 7100520 SH 1 B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	MODIFIED R43, R42, R54 WAS 47K, ADDED R11 CCW PER ECR 5394	10-24-84	B. BODIKER
B	REVISED PER DEVELOPMENT CHANGE 3 (REF ECR 5394) ED 1/12/84	1-13-84 1-16-84	B. BODIKER



LAST FUNCTION DESIGNATION USED														
AR	C	CR	E	L	P	Q	R	T	TP	U	VR	Y
3	63	27	2	25	1	7	67	2	2	3	3	1

REFERENCE DESIGNATIONS NOT USED

3. RESISTORS ARE 1/8W, 5%. VALUE IN OHMS.
2. CAPACITANCE IN MICROFARADS.
1. DIODES ARE IN4148.

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF MATERIAL

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY					

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X ± .1 .XX ± .03 .XXX ± .010 SURFACE √
HOLE SIZES PER AND10387

7100320
NEXT OR ASSOC ASSEMBLY

DWN BY: MM	9-28-83	
CHECK: B. BODIKER	10/20/83	
APVD: T. Mainzing	11/1/83	
APVD: M. Tobin	11/3/83	
D May	4/3/83	
RLSE:		

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

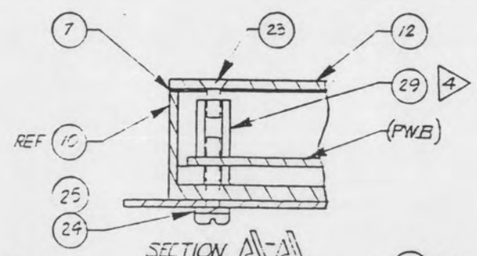
SCHEMATIC, 2 ND L.O., 3045

SIZE D | FSCM NO. 06994 | DWG NO. 7100520 | REV B
SCALE — | SHEET 1 OF 1

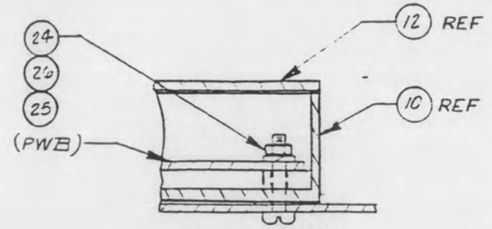
7100520 B

DWG NO. 7100429 SH 1 REV C

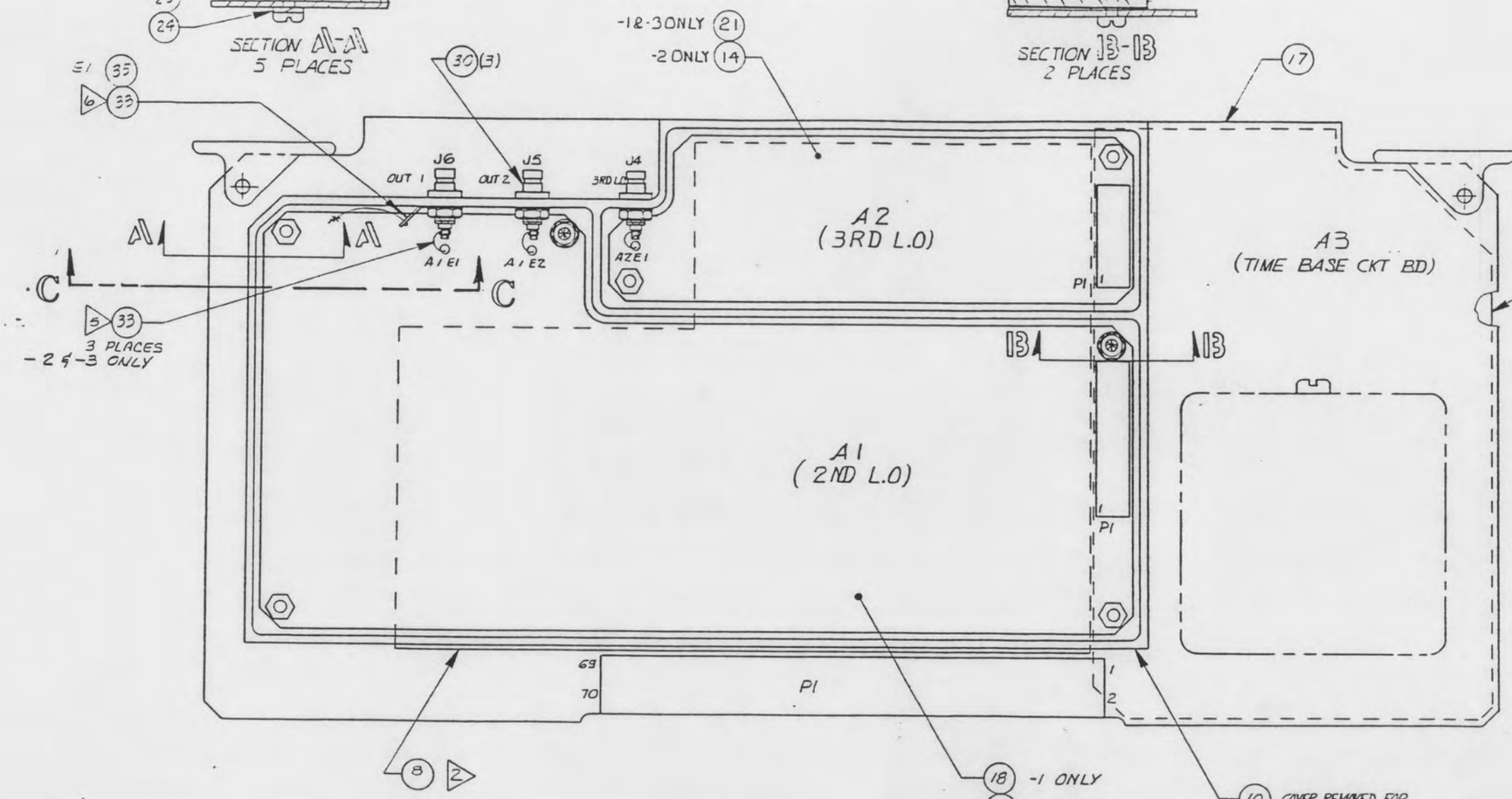
REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	PREVIOUS RELEASE WAS PL ONLY TO S/N 162 INCORP ECN 5519	5/14/84	B.BOOKER
B	INCORP ECN 5635. ADDED SECT. C-C EFF: ON COI & ON: DISP. READY CDR 6-6-85	6/11/85	B.BOOKER
C	INCORP ECN 5701, EFF: COI & ON	7/15/85	B.BOOKER
C	ZONE D5 ADDED - 2 ONLY (14) RI: ECR 6265 S DESANTI 10-24-85	11/7/85	L. CHAVEZ

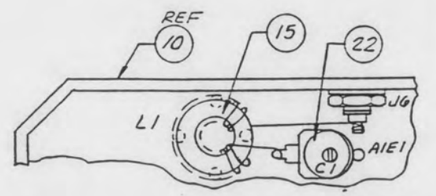


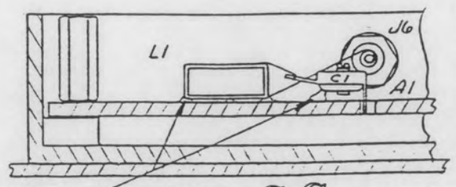
SECTION A-A
5 PLACES



SECTION B-B
2 PLACES







SECTION C-C -1 ONLY
SCALE 3/1

SEE SEPARATE PARTS LIST

(1) -1 HF TIME BASE

(2) -2 VHF/UHF TIME BASE

(3) -3 HF TIME BASE

6 SOLDER WIRE TO LUG AND TO GROUND PLANE OF BOARD.

5 WIRE TO EITHER TERMINAL OR CIRCUIT PAD, (BOARDS VARY).

4 APPLY RETAINING COMPOUND (ITEM 34) TO HARDWARE INDICATED AT TIME OF ASSY.

3. IDENTIFY WITH P N 7100429, DASH NO. & REV LTR.

2 INSTALL INSULATOR APPROX WHERE SHOWN PRIOR TO HOUSING & SECURE WITH SMALL AMOUNT OF RTV (ITEM 40)

1. PARTS NOT REQ'D FOR ASSEMBLY PURPOSES ARE NOT SHOWN IN VIEW.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES,
TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER AN010387

345-410
240-410
NEXT OR ASSOC ASSEMBLY

DWN BY: Ben Duong 4/8/84
CHECK: B. BOOKER 5/14/84
APVD: [illegible] 5/15/84
APVD: [illegible] 5/15/84
RLSE: [illegible] 5/17/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

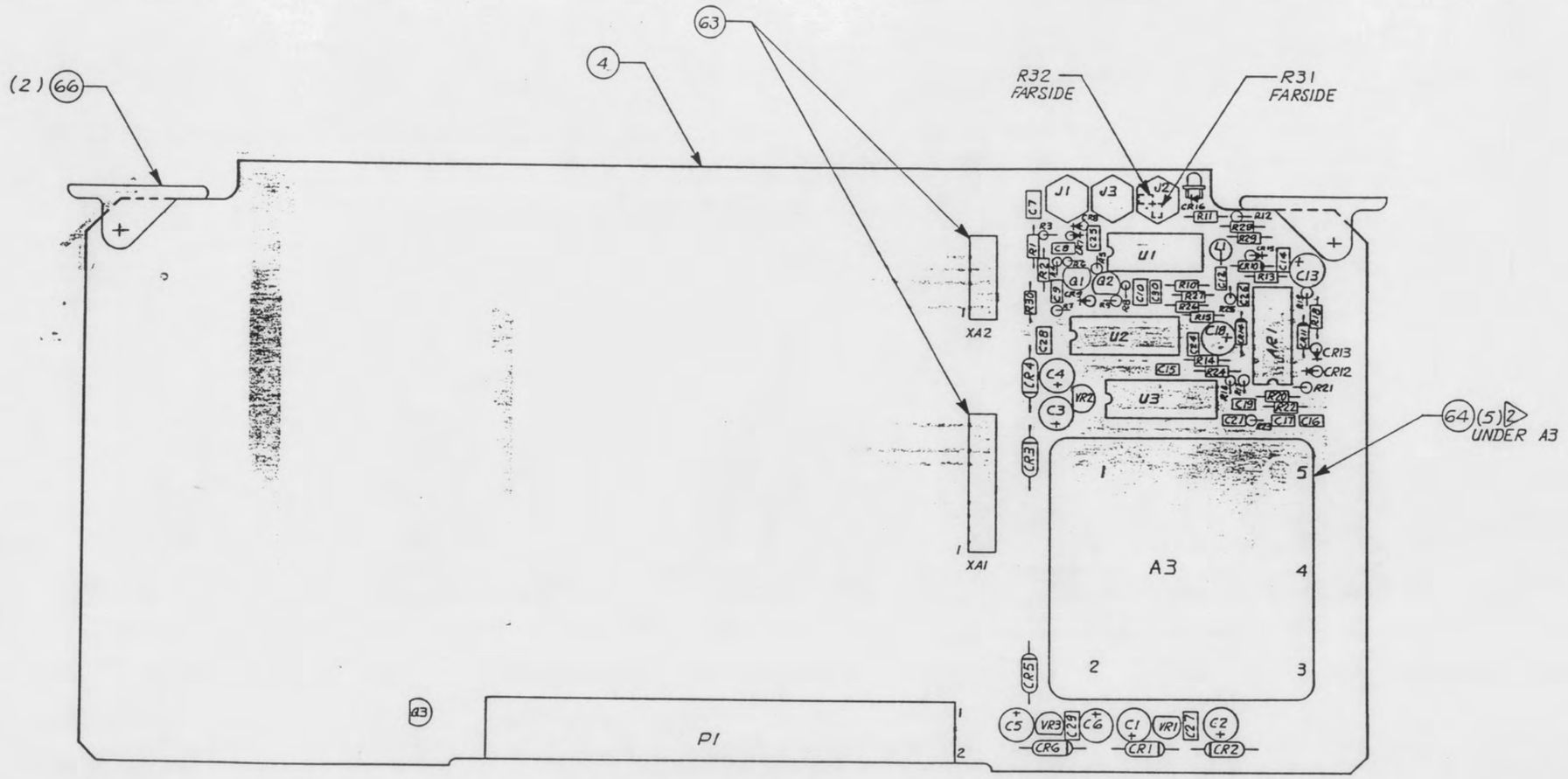
TIME BASE

SIZE D | FSCM NO. 06994 | DWG NO. 7100429 | REV C
SCALE -1 | SHEET 1 OF

7100429

DWG NO. 7100307 SH 1 E

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
C	REDRAWN INCORP ECN5854 EFF:033 &ON KD 7-25-85	9/9/85	B. BOOKER
D	INCORP ECN5900 EFF: SN 052 &ON KD 7-25-85	9/18/85	B. BOOKER
E	INCORP ECN6123 EFF: SN 053 &ON KD 7-25-85	9/18/85	B. BOOKER



(1) -1 TIME BASE

PROPRIETARY INFORMATION
USE OR REPRODUCTION PROHIBITED EXCEPT AS SPECIFICALLY AUTHORIZED IN WRITING BY O.A.R. CORPORATION

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

QTY PER ASSY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ± .1 .XX = ± .03 .XXX = ± .010 SURFACE √

HOLE SIZES PER ANSI B47.1

PROPRIETARY INFORMATION

NEXT OR ASSOC

7100429

DWN BY:		7/25/85
CHECK:	B. BOOKER	9/18/85
APVD:		10/2/85
APVD:		10/4/85
		10-23-85

PLOT

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

TIME BASE

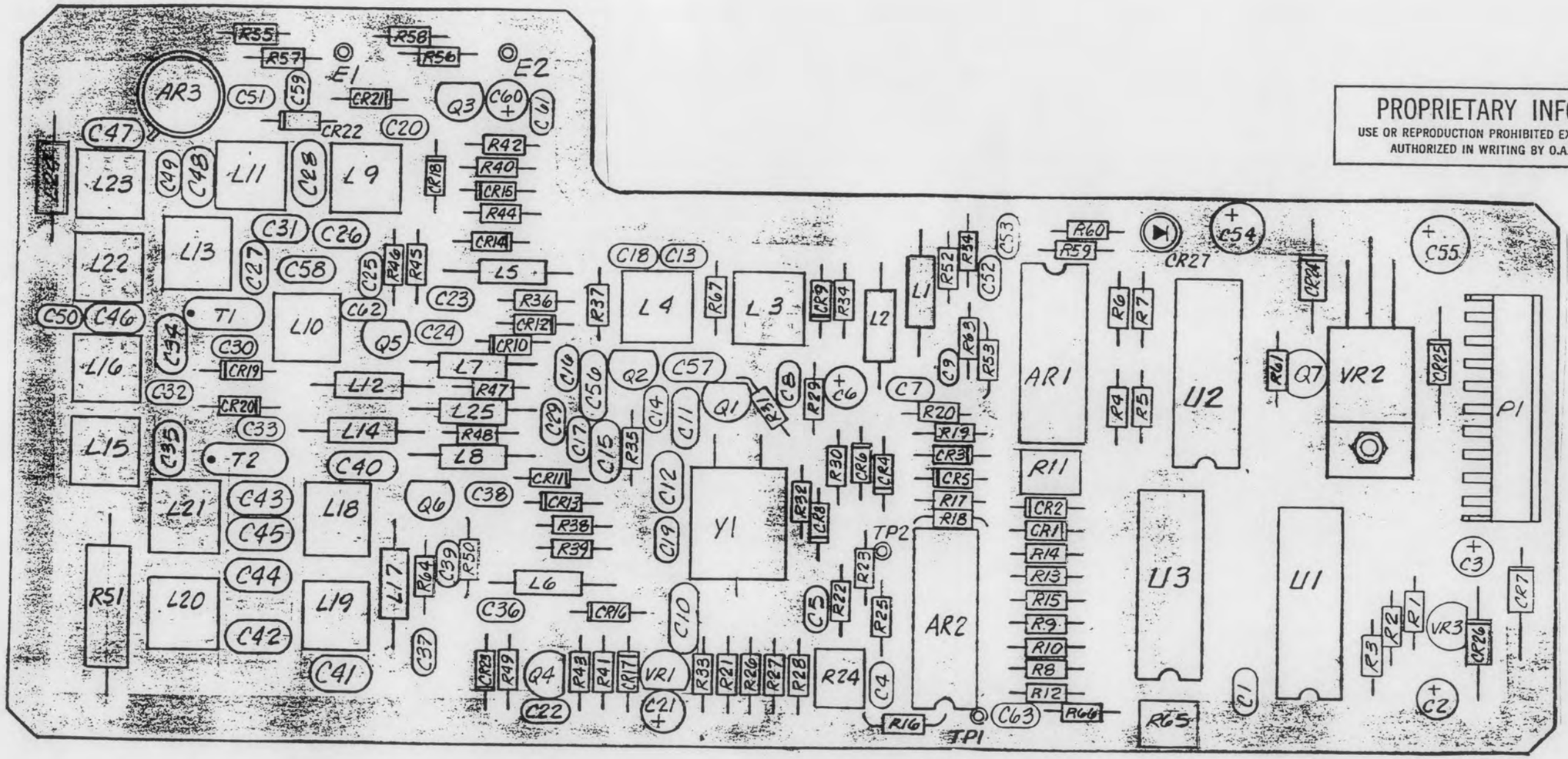
SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100307	E

SCALE 2:1 SHEET 1 OF 1

(2) REMOVE ADJUSTMENT HOLE COVER PRIOR TO INSTALLATION.
1. IDENTIFY WITH PART NO., DASH NO. & REV LTR.

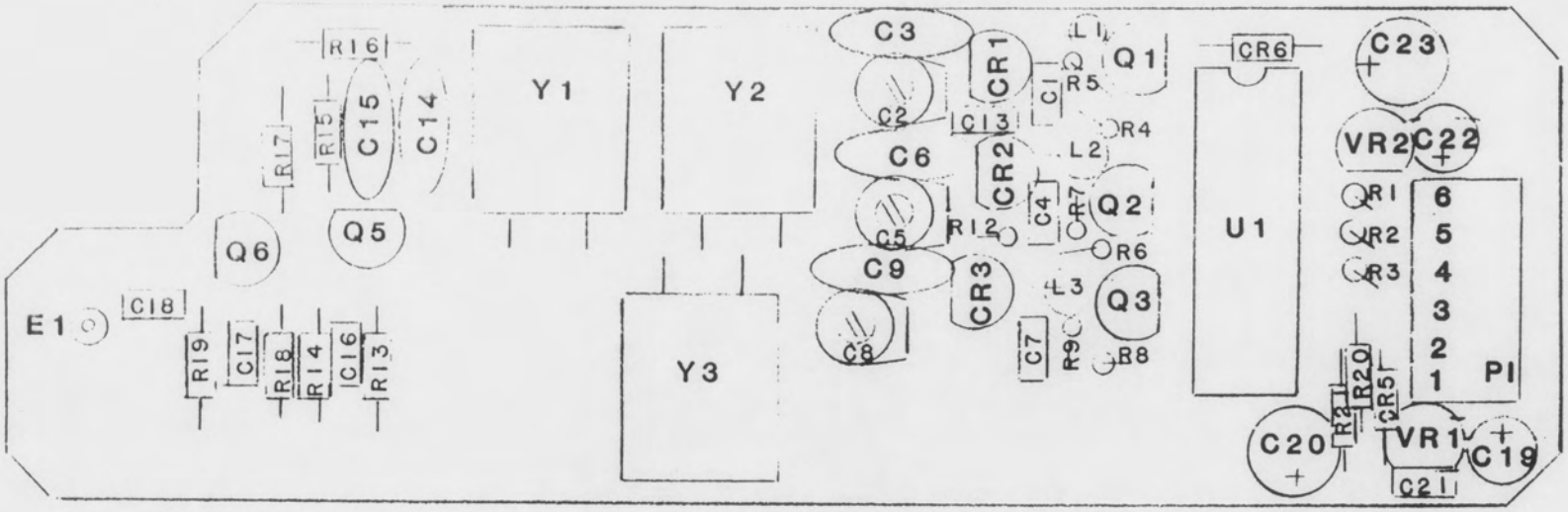
NOTE: UNLESS OTHERWISE SPECIFIED

7100307 E



7100320-1

SECOND LOCAL OSCILLATOR



-1 SHOWN.
-2 SAME AS -1 EXCEPT OMIT
Q2/Y2 OSC AND Q3/Y3 OSC.

7100311. Third Local Oscillator.

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL	DATE	TITLE	PARTS LIST 7100429
	APPVD	DATE	TIME BASE	
	CHECK B. BODIKER	DATE 6/11/84		SHEET 1 OF 3 REV B
	DRAWN C. KENNEDY	DATE 6-8-84		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	345-410	240-410		
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410	240-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
B	INCORP ECN 5635, PARTS LIST REWRITTEN AND REVISED OBSOLETE REV A, EFF: S/N 001 & ON; DISP: REWORK C.D.K. 6/6/84	B. BODIKER	6/11/84

7100429 SH 2 OF 3 B

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-10	-11	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	TIME BASE		X										HF
2	-2	TIME BASE			X									VHF/UHF
3	-3	TIME BASE				X								
4														
5														
6	-10	INSULATOR	.005 THK MYLAR SHT	1	1	1	X							
7	-11	GASKET, COVER	CHOMERICS 40-21-1015-1212	1	1	1		X						
8														
9														
10	7100073-1	HOUSING, L.O.		1	1	1								
11	7100033-1	HOUSING, L.O. MACHINED		ALT	ALT	ALT								ALT FOR ITEM 10
12	7100074-1	COVER, L.O.		1	1	1								
13	7100034-1	COVER, L.O. MACHINED		ALT	ALT	ALT								ALT FOR ITEM 12
14														
15	7100753-1	IND. TOROID		1	—	—								L1
16	7100829	DIAGRAM		REF	REF	REF								
17	7100307-1	TIME BASE CIRCUIT BD		1	1	1								A3
18	7100310-1	2ND L.O.		1	—	—								A1 HF
19	7100320-1	2ND L.O.		—	1	—								A1 VHF/UHF
20	7100345-1	2ND L.O.		—	—	1								A1 HF
21	7100311-1	3RD L.O.		1	1	1								A2
22	[illegible]KU18000	CAP, 3.3-18PF	SPRAGUE GOODM.	1	—	—								C1

7100429 SH 3 OF 3 B

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-10	-11	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23	4-40 X 5/16	SCREW	PH, FL, HD (100°)	5	5	5								
24	4-40 X 7/16	SCREW	PH, PN, HD	7	7	7								
25	NO. 4	LOCK, WASHER	SPLIT	7	7	7								
26	4-40	NUT	SMALL, PATTERN	2	2	2								RADIO
27														
28														
29	2056-440-SS-20	SPACER	R.A.F. OR EQ	5	5	5								3/16-HEX CRES 4-40 X 7/16
30	51-045-0000	CONN, JACK	SEALECTRO	3	3	3								J4, J5, J6
31														
32														
33	26 AWG	WIRE, BUSS		A/R	A/R	A/R								
34	GRADE C	RTNG CMPD	LOCTITE	A/R	A/R	A/R								
35	1410-10	TERMINAL, LUG	H.H. SMITH	1	1	1								E1
36														
37														
38														
39														
40	RTV 118	ADHESIVE	G.E.	A/R	A/R	A/R								
41														
42	HYSOL 1C WHITE	EPOXY	THE DEXTER CORP	A/R	—	—								
43														
44														

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL Init	DATE 9-19-83	TITLE	PARTS LIST 7100307
	APPVD	DATE	TIMEBASE	SHEET 1 OF 4 REV E
	CHECK B. BODIKER	DATE 11/7/83		MWO
	DRAWN MM	DATE 11-5-83		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100321			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD	(1) PART OF 20 PINS BREAK APART STRIP				
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	ADDED ITEMS 63 & 64	MM 11-5-83	B. BODIKER	11/7/83
B	INCORP ECN 5415	KD 1/11/84	B. BODIKER	1/17/84
C	INCORP ECN5854; EFF: S/N 033 & ON	KD 7-25-85	B. BODIKER	9/18/85
D	INCORP ECN5900 R1 ; EFF: S/N 052 & ON	KD 7-25-85	B. BODIKER	9/18/85
E	INCORP ECN6123 R2 ; EFF: S/N 053 & ON	KD 7-25-85	B. BODIKER	9/18/85

7100307
SH 2 OF E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	TIMEBASE		/						
2										
3	7100507	SCHEM		REF						
4	7100207-1	PWB		1						
5										
6										
7										
8	7100721-1	OSCILLATOR		1						A3
9										
10										
11										
12										
13										
14										
15	LF347N	IC OPER AMPL	NATIONAL	1						AR1
16										
17										
18	106RLR025M	CAP 10μF 25V	ILL CAP	6						C1,2,5,6 13,18
19										
20	226RLR016M	CAP. 22μF 16V	ILL CAP	2						C3,4
21	C315C102K2R5CA	CAP. .001μF	KEMET	2						C9,12
22	C320C104K5R5CA	CAP. .1μF	KEMET	9						C8,10,14,15,19, 25,27-29,

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	710030 SH 3 OF E REMARKS
23	C315C103K5R5CA	CAP .01μF	KEMET	7						C7, 16, 17, 21, 24 26, 30
24										
25										
26	IN4001	DIODE		6						CR1-6
27	IN4148	DIODE		9						CR7-15
28	5082-4494	LED	HP	1						CR16
29										
30	51-051-0000	CONN, COAX JACK	SEALECTRO	3						J1, J2, J3
31	1-102584-0	CONN. PLUG	AMP	1						P1
32										
33	SW-W-22 MS21401-3	INDUCTOR 22μH CHOKE	NYTRONICS	1						L1
34										
35	MPS6521	XSTR	MOTOROLA	3						Q1, 2, 3
36										
37	1K	RES, CARB FILM 1/8W 5%		4						R1, 4, 8, 10
38	3K			1						R2
39	6.8K			2						R3, 19
40	390Ω			2						R5, 7
41	100Ω			1						R6
42	10K			4						R22, 24, 27, 29
43	22K			3						R13, 14, 15
14	4.7K			2						R12, 28

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100307 SH 4 OF E REMARKS
45	51K			3										R9,11,16
46	3.9M			1										R17
47	2.2K			1										R18
48	39K			3										R20,21,26
49	1M			1										R23
50	100K			1										R25
51	47K	RES. CARB FILM ¼W 5%		1										R30
52	CR3AA51R0J150	51Ω CERMET CHIP RESISTOR	CAL-R	1										R32
53	CR3AA3900J150	390Ω CERMET CHIP RESISTOR	CAL-R	1										R31
54	74HC00N	IC AND GATE		1										U1
55	MC14510BCP	IC UP-DN COUNTER	MOTOROLA	1										U2
56	MC145145P	IC SYNTH	MOTOROLA	1										U3
57														
58														
59	MC78L12ACP	IC 12V RGLTR	MOTOROLA	1										VR1
60	MC78L05ACP	IC 5V RGLTR	MOTOROLA	1										VR2
61	MC79L12ACP	IC -12V RGLTR	MOTOROLA	1										VR3
62														
63	TS-120-G-D-2-2	CONN, 20-PIN	SAMTEC	1										XA1,XA2 1
64	902-093	SPACER	BIVAR	5										
65														
66	S-203	EJECTOR	SCANBE	2										

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE 9/15	TITLE	PARTS LIST 7100311
	APPVD [illegible]	DATE 11/22/83	3RD L.O.	SHEET 1 OF 3 REV E
	CHECK R. BODIKER	DATE 10/7/83		MWO
	DRAWN [illegible]	DATE 9/15		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100429			
QTY REQUIRED THIS RELEASE	FINAL ASSY	240-410	345-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD	DATE
A	INCREASED QTY ITEM 9 (7) TO (9); ITEM 10 (2) TO (4); ITEM 11 (2) TO (4); ITEM 18 (2) TO (4); ITEM 23 (2) TO (4); ITEM 27 (2) TO (4); ITEM 32 (3) TO (5); ITEM 33 (2) TO (4): REVISED REF DES: ADDED ITEMS 5, 7, 8 - REF ECR 5352 T350 CAPS WERE T390.	12-8-83	G. Lauchi	12-12-83
B	INCORP ECN 5437	RD 2/6/84	B. BODIKER	2/24/84
C	INCORP ECN 5484; EFF: 001 & ON	LJ 6/3/85	B. BODIKER	6/4/85
D	INCORP ECN 5590; EFF: 001 & ON			
E	INCORP ECN 5786; EFF: 001 & ON			

7100311
SH 2 OF 3 E

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	7100311-1	3RD L.O.		/							2040.
2	" -2	3RD L.O.			/						3045
3	7100511	SCHEMATIC		REF	REF						
4	7100211-1	PWB		1	1						
5		"									
6	7100720-2	CRYSTAL		1	—						Y3
7	7100720-3	CRYSTAL		1	—						Y2
8	7100720-4	CRYSTAL		1	1						Y1
9	C320C104K5R5CA	CAP. .1μF	KEMET	8	—						C1,4,7,13,16 17,18,21
10	GKU18000	CAP. VAR 3.3-18pF	SPRAGUE	3	1						C2,5,8 (-1) C2 (-2)
11	DM5-CC150J	CAP. 15PF	ELMENCO	3	1						C3,6,9 (-1) C3 (-2)
12	DM5-FY391J	CAP. 390PF	ELMENCO	1	1						C14
13	DM5-FY131J	CAP. 130PF	ELMENCO	1	1						C15
14	T350G106K035AS	CAP. 10μF 35V	KEMET	2	2						C20,23
15	T350A105K035AS	CAP. 1μF 35V	KEMET	2	2						C19,22
16	C320C104K5R5CA	CAP .1μF	KEMET	—	6						C1,13,16,17, 18,21
17											
18	MPN 3404	DIODE	MOTOROLA	3	1						CR1,2,3 (-1) CR1 (-2)
19	1N4148	DIODE		2	2						CR5,6
20											
21											
22	RTV 161	ADHESIVE	G.E.	AR	AR						

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100311 SH 3 OF 3 E REMARKS
23	MS21401-34	INDUCTOR, 8200μH	(NYTRONICS).	3	1						L1,2,3 (-1) L1 (-2)
24											
25	22-17-2062	CONN. INTERFACE	MOLEX	1	1						P1
26											
27	MPSG521	TRANSISTOR	MOTOROLA	3	1						Q1,2,3 (-1) Q1 (-2)
28	MPS-H10	TRANSISTOR	MOTOROLA	2	2						Q5,6
29											
30											
31	100K 1/8W 5%	RES, CARB FILM		3	3						R1-3
32	820Ω 1/8W 5%	RES, CARB FILM		4	2						R5,7,9,12 (-1) R5,12 (-2)
33	10K 1/8W 5%	RES, CARB FILM		5	3						R4,6,8,13,14 (-1) R4,13,14 (-2)
34	150Ω 1/8W 5%	RES, CARB FILM		1	1						R19
35	22Ω 1/8W 5%	RES, CARB FILM		3	3						R17,18,15
36	1.8K 1/8W 5%	RES, CARB FILM		1	1						R16
37	1.2K 1/8W 5%	RES, CARB FILM		1							R21
38	8.2K 1/8W 5%	RES, CARB FILM		1							R20
39											
40											
41	MC14094BP	IC, REGIS	MOTOROLA	1	1						U1
42	LM317LZ	VOLT REG	NATIONAL	1	1						VR1
43	MC78L05ACP	VOLT REG	MOTOROLA	1	1						VR2
44	NO. 24	INS TUBING THIN WALL	TEFLON AMS 3655	A/R	A/R						

FORM 109

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE 11/7/83	TITLE 2ND LOCAL OSC DF3045	PARTS LIST 7100320
	APPVD T. Mahaffey	DATE 11/1/83		SHEET 1 OF 7 REV D
	CHECK B. BODIKER	DATE 10/20/83		
	DRAWN [illegible]	DATE 9/15/83		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100321			
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	MISC CHGS INCLUDING CHANGING VOLT REGS [illegible] PH 7-83	B. BODIKER	10/21/83
B	ADDED R63, R54 WAS 47K, ADDED C62 [illegible] 10-21-83	B. BODIKER	10/21/83
C	INCORP ECN 5406 KDH 1/19/84	B. BODIKER	1/24/83
D	REDRAWN & REVISED INCORP ECN 5509 EFF: S/N 001 & ON COK 7/17/84	B. BODIKER	7/30/84

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100320 SH 2 OF 7 D REMARKS
1	7100320-1	2ND LO BD		/						3045
2	7100220-1	PWB		1						
3	7100520	SCHEMATIC		REF						
4										
5										
6	7100716-10	INDUCT, VAR 1 1/4T # 27		1						L9
7	7100716-9	INDUCT, VAR 6 3/4T # 27		1						L4
8	7100716-1	INDUCTOR, VAR 9 3/4T # 27		1						L3
9	7100716-2	INDUCTOR, VAR 1 3/4T # 27		3						L16, 22, 19
10	7100716-3	INDUCTOR, VAR, 7 3/4T # 27		1						L10
11	7100716-4	INDUCTOR, VAR, 2 3/4T # 27		1						L11
12	7100716-5	INDUCTOR, VAR 10 3/4T # 27		1						L15
13	7100716-6	INDUCTOR, VAR 11 3/4T # 27		1						L18
14	7100716-7	INDUCTOR, VAR 2 1/4T # 27		1						L21
15	7100716-8	INDUCTOR, VAR 4 3/4T # 27		3						L20, 23, 13
16										
17	7100718-1	CRYSTAL		1						Y1
18										
19	025-712-1	XFMR 9:1		2						T1, 2
20										
21										
22										

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100320 SH 3 OF 7 D REMARKS
23	LM324N	OP AMP	NATIONAL	2										AR1,2
24	MWA 130	AMP	MOTOROLA	1										AR3
25	DM5-EC360J	CAP, MICA, 36pF	ELMENCO	1										C10
26	C315C103K5R5CA	CAP. .01μF	KEMET	30										C7-9,13,14,16-20,22-25,29,3[illegible]
27														32,33,36-39,49-52,59,61-63
28	T390A105K1025AS	CAP. 1μF, 25V	KEMET	3										C6,21,60
29	C320C104K5R5CA	CAP. .1μF, 50V	KEMET	4										C1,4,5,53
30	DM5-EC560J	CAP. 56PF, 300V	ELMENCO	1										C12
31	DM5-EC300J	CAP. 30PF, 300V	ELMENCO	1										C11
32	DM5-FY101J	CAP. 100PF, 50V	ELMENCO	2										C26,27
33	DM5-FY251J	CAP. 250PF, 50V	ELMENCO	1										C28
34	DM5-CC100J	CAP. 10PF, 300V	ELMENCO	1										C31
35	DM5-EY820J	CAP. 82PF, 50V	ELMENCO	3										C34,41,48
36	DM5-CC220J	CAP. 22PF, 300V	ELMENCO	1										C35
37	DM5-EC390J	CAP. 39PF, 300V	ELMENCO	2										C40,45
38	DM5-CC150J	CAP. 15PF, 300V	ELMENCO	1										C42
39	DM5-CC030D	CAP. 3PF, 300V	ELMENCO	2										C43,58
40	DM5-FY271J	CAP. 270PF, 50V	ELMENCO	1										C44
41	DM5-FY111J	CAP. 110PF, 50V	ELMENCO	1										C46
42	DM5-CC050D	CAP. 5PF, 300V	ELMENCO	1										C47
43	DM5-EC470J	CAP. 47PF, 300V	ELMENCO	1										C56
44	DM5-FY131J	CAP, MICA, 130PF	ELMENCO	1										C57

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100320 SH4 OF 7 D REMARKS
45										
46	DM15-FY161J	CAP. 160μF 50V	ELMENCO	1						C15
47	106RLR025M	CAP 10μF 25V	ILL CAP	2						C54, 55
48	226RLR016M	CAP 22μF 16V	ILL CAP	2						C2, 3
49										
50										
51	IN4148	DIODE		14						CR1-6 8, 9, 14-18, 23.
52	IN4001	DIODE		4						CR7, 24-26
53	MA4P3401	DIODE	M/A COM	6						CR10-13, 19, 20
54	IN6263	DIODE		2						CR21, 22
55	5082-4494	LED	H-P	1						CR27
56										
57										
58										
59										
60										
61										
62										
63										
64	SW-W-10 MS21400-13	INDUCTOR, 10μH	NYTRONICS	11						L1, 2, 5-8, 12, 14, 17, 24, 25.
65										
66										

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
67	22-17-2102	CONN, INTERFACE	MOLEX	1						P1
68										
69										
70	MPS-H10	TRANSISTOR	MOTOROLA	4						Q1, 2, 5, 6
71	2N4403	TRANSISTOR		2						Q3, 4
72	MPS6521	TRANSISTOR	MOTOROLA	1						Q7
73										
74										
75										
76	10K 1/8W 5%	RES, CARB. FILM		9						R14, 29, 33 34 40 41, 44, 49, 53
77	100K 1/8W 5%	RES, CARB FILM		4						R1-4
78	56K 1/8W 5%	RES, CARB FILM		11						R5, , 15, 17, 18 20-23, 26-28,
79	22K 1/8W 5%	RES, CARB FILM		1						R6
80	33K 1/8W 5%	RES, CARB FILM		1						R7
81	47K 1/8W 5%	RES, CARB. FILM		1						R61
82	3262W-1-104	RES, VAR, 100K	BOURNS	1						R11
83										
84	330K 1/8W 5%	RES, CARB FILM		1						R13
85	91K 1/8W 5%	RES, CARB FILM		1						R16
86	3262W-1-503	RES, VAR 50K	BOURNS	1						R24
87	18K 1/8W 5%	RES, CARB. FILM		1						R25.
88	5.1K 1/8W 5%	RES, CARB. FILM		1						R30

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	7100320 SH 6 OF 7 D REMARKS
89	22Ω 1/8W 5%	RES, CARB FILM		4										R31,35,46,64
90	470Ω 1/8W 5%	RES, CARB FILM		1										R32
91	3.6K 1/8W 5%	RES, CARB FILM		4										R36,39,47,48
92	1.8K 1/8W 5%	RES, CARB FILM		2										R37,38
93	5.6K 1/8W 5%	RES, CARB FILM		2										R42,43
94	560Ω 1/8W 5%	RES, CARB FILM		3										R45, 50, 67
95	130Ω, 1W, 5%	RES, CARB FILM		1										R51
96	110K 1/8W 5%	RES, CARB FILM		2										R52,63
97	68Ω 1/8W 5%	RES, CARB FILM		5										R54-58
98	18K 1/8W 5%	RES, CARB FILM		1										R59
99	2.7K 1/8W 5%	RES, CARB FILM		1										R60
100	3262W-1-502	RES, VAR, 5K POT	BOURNS	1										R65
101	13K, 1/8W 5%	RES, CARB FILM		1										R66
102	470K,	"		1										R8
103	120K,			1										R9
104	4.7K,			1										R10
105	180K, 1/8W 5%	RES, CARB FILM		2										R12, 19
106	MC14094BP	IC, REGISTER	MOTOROLA	2										U1, 2
107	AD558KN	IC, DAC	ANALOG DEVICES	1										U3
108	2061 B	TERMINAL	USECO	4										E1, E2, TP1, TP2
109														
110														

7100320
SH 7 OF 7 D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
111	MV209	VARACTOR	MOTOROLA	1						VR1
112	MC78M12CT	VOLT. REG	MOTOROLA	1						VR2
113	MC78L05ACP	VOLT. REG	MOTOROLA	1						VR3
114										
115										
116										
117										
118	60-11-8302-1674	INSULATOR	CHOMERICS	1						
119										
120	B52200F003	WASHER, COMP	MOTOROLA	1						
121										
122										
123	4-40 x 1/4	SCREW	PAN HD, PHILLIPS	1						
124										
125	4-40 HEX	NUT SMALL PATTERN	(RADIO)	1						
126										
127										
128										
129	GRADE C	RTNG CMPD	LOCTITE	A/R						
130										
131										
132										

IF AMPLIFIER AND DEMODULATOR BOARD

ASSEMBLY: 7100316-2

SCHEMATIC: 7100516-2

SECTION I

DESCRIPTION

1.1 General

A simplified block diagram of the 7100316 IF and Demodulator Board is shown in figure 1. 10.7 MHz signals from the second converter in the RF Module are first filtered by one of four band-pass filters. The filter may be manually selected by the operator or automatically selected. In automatic, the bandwidth of the filter selected depends on the demodulation mode. The signal is amplified next in the IF strip. The amount of amplification (gain) of the IF strip depends on the automatic gain control (AGC) level from the output of the demodulator. The AGC maintains a constant IF strip output over a wide range of input RF levels. The AGC level is proportional to the RF signal and is used to indicate the signal field strength.

The 10.7 MHz output from the IF strip is next demodulated for several parallel outputs. One FM discriminator is used for wide-band FM (WBFM) and a second for narrow-band FM (NBFM) demodulation. The two discriminators also develop differential voltages for automatic frequency control (AFC). The NBFM or WBFM AFC output is selected automatically by a switch depending on the demodulation mode. The IF input is also mixed with the 3rd LO and BFO frequencies to obtain a CW/SSB detected output.

The AM detected audio contains the 165 Hz tones used to identify the N-S and E-W antenna inputs as well as the audio intelligence imposed on the RF. This signal is used for the video output to the display circuits. The 165 HZ tones are "notched" out of the detected signal for the AM audio output.

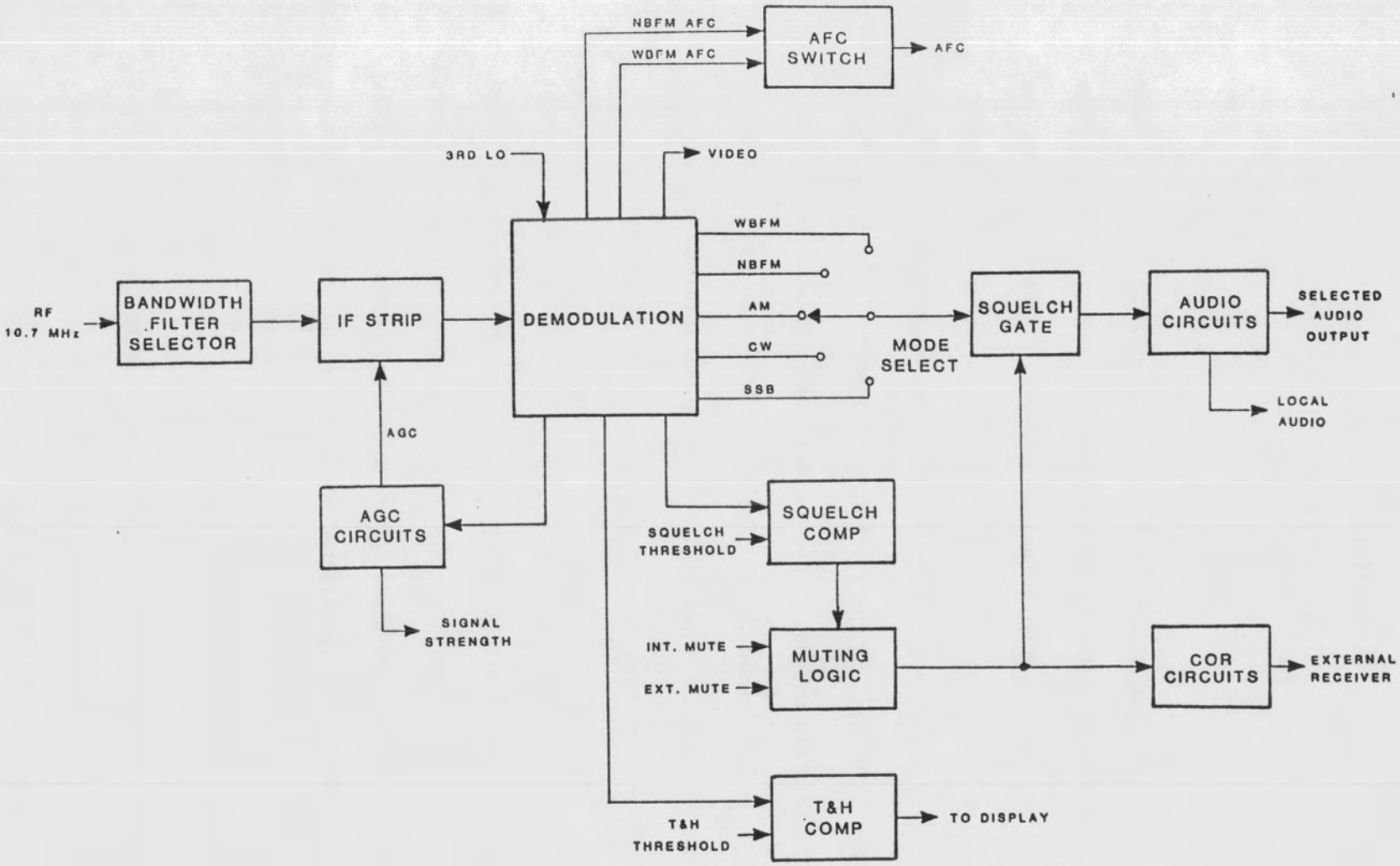


Figure 1. Simplified Block Diagram, IF and Demodulator Board (7100516)

The AM audio signal level is also used for input to the AGC, Squelch, and Track-and-Hold (T&H) circuits. In both the T&H and Squelch Comparators the audio is compared to a threshold level (operator controlled by the squelch potentiometer) to determine the presence of a signal. The T&H comparator output is used for the display and the squelch output is used in an OR circuit with mute commands to control the squelch gate.

the presence of a signal. The T&H comparator output is used for the display and the squelch output is used in an OR circuit with mute commands to control the squelch gate.

One of the five audio outputs is selected at the squelch gate input. The squelch gate inhibits the audio if it receives a mute command or the audio falls below the squelch threshold level. The squelch gate control is also used to open and close a carrier operated relay (COR) for external receivers or recorders. Output from squelch gate is amplified for local and external audio.

1.2 Functional Description.

Figure 2 is a more complete, functional diagram of the receiver. The input IF signal is switched in and out of one of four bandpass filters (FL1-FL4) by AR1 and AR2. The correct filter for each mode is automatically selected in response to a 4 bit (B0-B3) command from the Receiver Control Logic which will be described later. The filter automatically selected for each mode over a given frequency range is shown in Table 1. The selected bandwidth is not updated with frequency changes unless the mode is changed.

DETECTION MODE	FREQUENCY RANGE (MHz)				
	20-30	30-80	80-115	115-225	225-520
FM	6 kHz	30 kHz	200 kHz	13 kHz	30 kHz
AM	6 kHz	6 kHz	13 kHz	13 kHz	13 kHz
CW	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz
USB/LSB	6 kHz	6 kHz	6 kHz	6 kHz	6 kHz

NOTE: Automatic bandwidth selection may be over-ridden by the operator.

Table 1. Automatic IF Bandwidth Selection.

The 10.7 MHz signal is next amplified by AGC controlled amplifier U3. The gain of U3 is inversely proportional to the AGC level so that weaker signals are amplified more than strong ones. The AGC feedback loop will be described later.

Bandpass filter, FL5 provides some bandwidth shaping but its primary purpose is to block any 3rd LO pick-up. U4 also regulates the gain of the IF signal to compensate for temperature changes. From U4 the signal divides into several paths for each demodulation mode. Circuits in each path are selectively enabled by control lines to output the correct mode and bandwidth in response to commands from the microprocessor. The control signals are output from two, 8-bit, serial-to-parallel decoders (latches U1 and U2). Table 2 lists the control functions. In most cases a low (0Vdc) on the control line enables a particular circuit of function.

IF AND DEMODULATOR BOARD
7100316-2

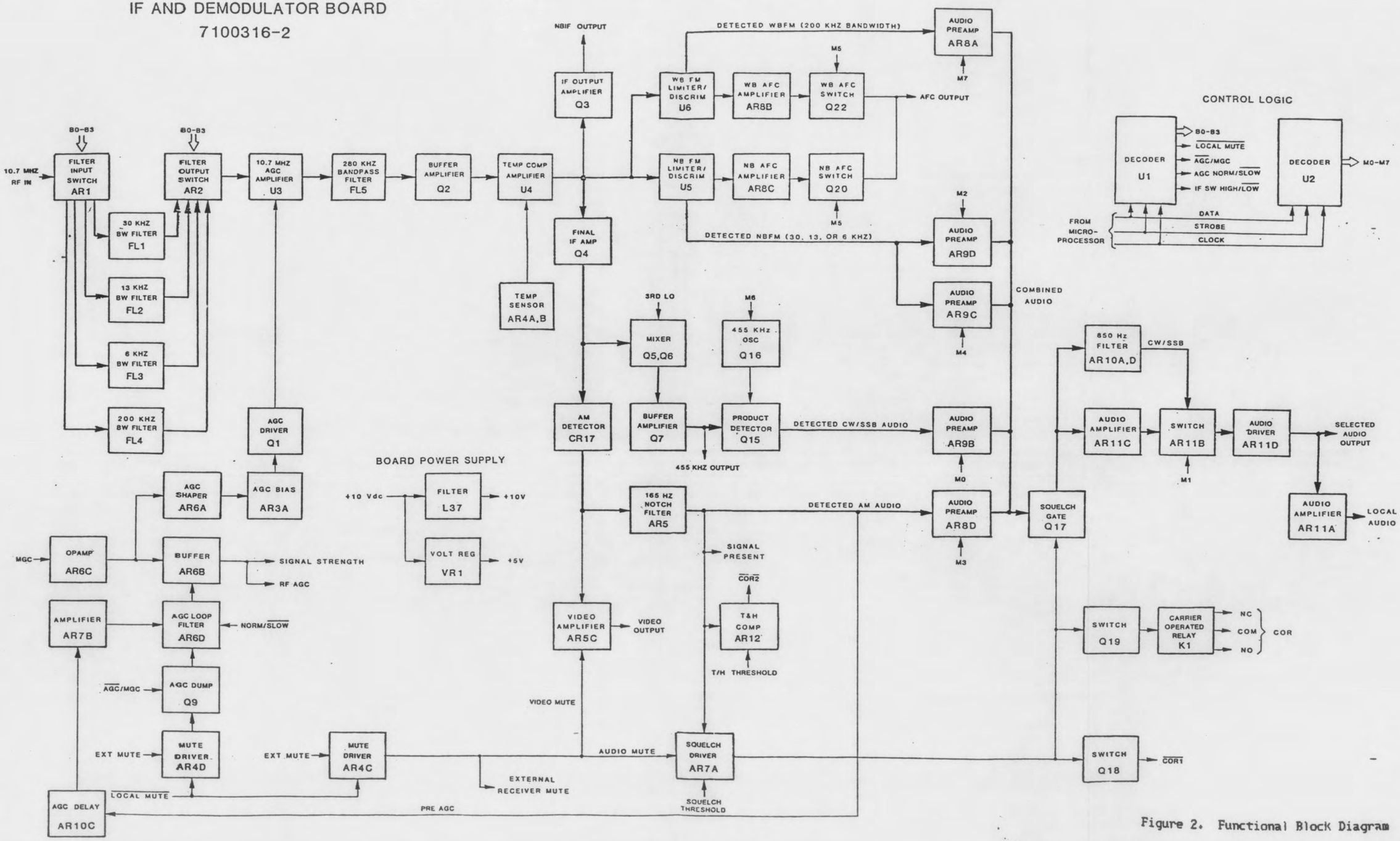


Figure 2. Functional Block Diagram

Table 2. Bit Map, Control Logic

INPUT SERIAL DATA BIT	CONTROL SIGNAL	FUNCTIONS
0	B0	30kHz BW (FL1), ON/OFF
1	B1	13kHz BW (FL2), ON/OFF
2	B2	6kHz BW (FL3), ON/OFF
3	B3	200KHZ BW (FL4), ON/OFF
4	LOCAL MUTE	RECEIVER ON/OFF
5	AGC/MGC	AUTOMATIC OR MANUAL GAIN CONTROL
6	AGCNORM/SLOW	NORMAL OR SLOW, OPERATOR SELECTED
7	IF HIGH/LOW	RF CONVERTER SWITCHING
8	M0	CW/SSB, ON/OFF
9	M1	850 Hz FILTER, ON/OFF
10	M2	WBFM (30kHz BW), ON/OFF
11	M3	AM, ON/OFF
12	M4	NBFM (13 & 6 kHz BW), ON/OFF
13	M5	AFC, NBFM/WBFM
14	M6	BFO ON/OFF
15	M7	WBFM (200kHz), ON/OFF

The IF signal from U4 divides into an FM demodulation path and an AM path. Limiter/discriminator U5 detects the FM audio signal for input to two audio preamplifiers, AR9D (30kHz BW) and AR9C (13kHz and 6kHz BW modes) that are enabled by M2 and M4 respectively.

Separate preamplifiers for each bandwidth are used to compensate for the different signal levels at each bandwidth and provide a uniform audio

output. Discriminator U5 also provides a differential output to AR8C that is proportional to frequency variations. The difference signal is smoothed at AR8C to obtain a control voltage that may be used to vary the local oscillator and automatically compensate for frequency changes (AFC). Discriminator U6 demodulates 200KHz deviation FM signals for audio output to preamplifier AR8A and an output to AR8B to develop a wide-band AFC voltage. The narrow-band AFC or wide-band AFC is enabled by M5 at switches Q20 and Q22.

The final, 10.7 MHz amplifier, Q4, has two outputs. One is mixed with the third LO frequency to obtain a 455 kHz output. The 455 kHz output is mixed with a 455 kHz signal at product detector Q15 for CW, USB, and LSB detected outputs. The correct USB and LSB frequencies relative to the suppressed carrier frequency, are obtained by off-setting the third LO in response to logic from the micro-processor.

The second 10.7 MHz output from Q4 is AM detected at CR46, amplified and used for a video output to the bearing processor. The detected AM audio to AR8D is first filtered at AR5 to remove the 165 Hz tone used to modulate the RF signals in the antenna.

All of the outputs from the audio pre-amplifiers are on a common bus to the squelch gate, Q17. Only one of the pre-amplifiers are enabled at a time depending on the detection mode selected. The squelch gate opens or closes the audio output in response to muting commands and the squelch threshold level.

Audio from the squelch gate is amplified at AR11C and AR11D for audio (selected) to rear panel connectors and at AR11A for the front panel

speaker. A low on M1 switches in a 850 Hz bandwidth audio filter automatically in CW mode: The filter may also be switched in by the operator when in SSB mode.

The squelch gate is driven by AR7A which responds to several inputs. The driver closes the squelch gate by a low on the external mute line or on the local mute line from the microprocessor to AR4C. In addition, AR7A compares the detected AM audio level with the operator-controlled squelch threshold level and also opens the gate whenever the audio is less than the threshold level. AR7A also closes carrier operated relay (COR) K1 when it opens the squelch gate. The COR output is normally open (NO) when there is an audio output and normally closed (NC) when the audio is muted or squelched. The COR may be used to turn off/on audio recorders or other remote devices. COR1 output provides a receiver status indication to the data processor.

The track-and-hold comparator (T&H), AR12 compares the threshold level with the detected audio. When the detected audio is less than the threshold, the COR2 output to the bearing processor board logic is low. This maintains the last bearing input for 25 seconds or until the signal is re-acquired and the detected audio exceeds the threshold. The detected audio level is also used to develop the pre-conditioned AGC (PRE AGC) input to the AGC delay circuit AR10C. With a SLOW input to AR6D, the AGC decay time is slowed from 60 milliseconds (NORM) to five seconds (SLOW). The AGC loop is also filtered at AR6D before distribution. The gain may also be controlled manually (MGC) by AR6C. When it is manually controlled, a high on AGC/MGC at Q9 dumps the AGC. The AGC voltage is also dumped whenever the receiver is muted. The AGC outputs are used to drive the signal strength meter, amplifiers on the RF Module (RF AGC) and the

10.7 MHz amplifier, U3. The AGC to U3 is shaped at AR6A to obtain more linear gain response over the dynamic signal range.

1.3 Circuit Description (Drawing 7100516-2)

IF bandwidth filters FL1-FL4 are switched in and out of the RF path by PIN diodes CR1-CR16. FL1 is selected by forward-biasing CR1 and CR4 and reverse-biasing CR2 and CR3. Biasing is accomplished with a low (0Vdc) on B0 control line from U1. A high (+5Vdc) on lines B1-B3 forward biases the bypass PIN diodes in the other filters (FL2-FL4), grounding their inputs and outputs. The input filter (L2, C1 and C4) and output filter (L4, C7, C10) match the high impedance of the filter to the 50 ohm input and output impedance.

Gain block amplifier U3 is preceded by a 50 ohm impedance matching section (L21, C43). The gain of U3 is controlled by the AGC at Q1. As the AGC voltage rises the output of U3 decreases. Q1 conducts more heavily, increasing the current to U3, pin 5, decreasing the gain of the amplifier. The output of U3 is tuned to 10.7 MHz by L24, C48, and C49. FL5 is a 280 kHz bandpass, 2-pole ceramic filter. In addition to restricting the IF bandwidth it blocks any 3rd LO pick-up. The filter is followed by another impedance matching network (L25, C51, C52) and buffer amplifier Q2.

U4 is a temperature compensation amplifier that operates in the following manner. As the temperature rises, sensor diodes (CR17, CR18) conduct more heavily, dropping the voltage at pin 1 of AR4A. The voltage decreases approximately 2.2 mV for each degree, Celsius. The current now increases through R55 and the gain of U4 decreases, keeping the overall gain of the IF strip constant. The output of the amplifier is tuned at L29 and C63.

The output is a narrow-band, predetected IF which is output at the rear panel via buffer amplifier Q3.

The FM is detected at one of two limiter/discriminators, U5 and U6 using quadrature detection. The discrimination bandwidth is set at 30 kHz by FL6 at U5. In U6 the bandwidth is set by T3 for 200 kHz.

Automatic frequency control (AFC) can be used in any mode using the differential output from each of the two discriminators. In the wide-band (200 kHz) FM mode AFC is taken from the outputs of U6. Pin 10 outputs a reference voltage of 5.6 volts. The output voltage from pin 7 varies above and below the reference voltage as the output frequency increases or decreases. The two outputs are smoothed by RC filters (R258, C163 and R264, C164) and input to differential amplifier AR8B. AR8B converts the difference to a single frequency control voltage. When the input differential is Zero eg., both are 5.6 Vdc, the output from AR8B is 2.5 Vdc. R260 is adjusted to obtain a 5.0 Vdc output when the discriminator output frequency is correct. The narrow-band differential output from U5 is similarly converted to a nominal 5.0 Vdc by AR8C. The correct AFC output is selected by control line M5. With a low on M5 the voltage output of Q23 increases, turning on FET Q22. Simultaneously, the voltage output from Q21 decreases, turning off FET Q20, blocking the narrow-band AGC output. With a high (+5V) on M5, the conditions are reversed and the narrow-band AGC is output through Q20.

Two audio preamplifiers, AR9C and AR9D are used for NBFM. AR9D has a gain of 1.8 for 30 kHz bandwidth and AR9C a gain of 0.75 for the stronger 13 kHz and 6 kHz bandwidth signals. Preamplifier AR8A is used for 20 kHz bandwidth signals.

The final IF amplifier, Q4 provides a high level output (approximate 12 Vp-p) to the video and audio circuits. The signal is mixed with the 3rd LO at Q5, Q6 to obtain a 455 kHz, predetected signal. The 3rd LO is one of two frequencies; 10.245 MHz in the upper side band mode (USB) and 11.155 MHz in lower side band (LSB). These frequencies vary slightly with the IF bandwidth. The output of the mixer goes to buffer amplifier Q7 and then divides. One output goes to the narrow-band, 455 kHz IF connector on the rear panel for optional recording of signals.

The audio is detected at Q15, a dual gate FET with a 455.00 kHz beat frequency oscillator (BFO) input to one gate. The crystal oscillator, Q16 is turned on with a low at M6. The detected CW or SSB audio signal is input to preamplifier AR9B.

Returning to the final IF amplifier Q4, a second output goes to the AM detector. Detection is accomplished at the Schottky diode, CR46 whose output is a pulsating dc voltage. A ripple filter consisting of C90, C91, R78 and R79 smooths the output. The detected output from buffer amplifier AR5B passes through an R-C notch filter to eliminate the 165 Hz modulating tone. The video signal (detected audio) is output from AR5C with the gain adjusted at R81. The audio is again buffered at AR5D and goes to audio preamplifier, AR8D and the video amplifier board.

The appropriate audio preamplifier for each mode selected is turned on with a low (0 Vdc) on control lines (M0, M2, M3, M4 and M7) which reverse-biases the diode at the inverting input to each amplifier. A high on all the other control lines forward-biases the diodes and the preamplifier outputs are shunted to ground. The audio preamplifiers are on a common line to the squelch gate (Q17) and the audio driver/filter. For all modes except CW, a

low on line. M1 reverse-biases CR53, turning filter switch AR11B on and AR10B off. All audio (except in CW mode) is amplified at AR11C. With a high at M1, CR53 is forward-biased, turning off filter switch AR11B, AR10A is an active 850 Hz band-pass filter. In the CW mode, a high on M1 turns off AR11B, which turns on the output amplifier in the filter AR10B.

The selected audio goes to the front panel speaker via audio driver AR11D and to the rear panel jack after limiting by AR11D.

The audio squelch gate is opened when the squelch driver AR7A cuts off, cutting off Q17 and turning on Q19 and Q18, effectively grounding their collectors. CR59 is reverse-biased and +10V is seen across K1 closing the relay and the external carrier operated relay (COR) line. Simultaneously, Q18 grounds the external COR1 line.

The squelch threshold is adjusted by varying the bias on the squelch driver, AR7A which compares the detected audio with the threshold. When the audio exceeds the threshold level, AR7A conducts, turning on Q17 and breaking the squelch. The squelch gate (Q17) is also controlled by external mute and the local MUTE output from decoder U1. A low output at Q1-14 or the external mute line (J7-1) is inverted by AR4C and AR4D. The function of AR4D will be described later. With a high output (approx. +5V) at AR4C CR22 is forward-biased and the squelch driver output is high, shutting off Q17 and opening the audio path. The video signal is simultaneously opened as CR36 is forward-biased and Q10 conducts; effectively grounding the input to the signal strength meter at P1-23.

The detected AM audio output is also used for the PRE-AGC level. The PRE-AGC is first order filtered by R123, C109 at the input to AR10C. The amount of AGC delay is adjusted with R124 at the inverting input to AR10C.

With a signal input C109 charges positive, the non-inverting input to AR7B goes positive and the amplifier conducts heavily, charging C111 in the main AGC loop filter. The charging time is the AGC attack time, which takes approximately 20 milliseconds until C111 is fully charged and AR6D is conducting at its maximum. When there is no signal, the AGC drops as C111 discharges. The AGC drop or decay time may be normal (60 milliseconds) or slow (5 seconds). In SLOW AGC, Q11 is off and C111 discharges primarily through R136, R135 and R130-132. With a high output from decoder U1-12, transistor Q11 is turned on and C111 discharges more quickly through R133, R135 and R136.

When the receiver is muted; AR4D conducts; turning on Q9, discharging C111 through R136 and dumping the AGC even more quickly (approximately 3 milliseconds). The AGC is buffered at AR6D and AR6B before going to the RF converter and signal strength meter, respectively. R154-R156 are for break-point adjustment which permits shaping AGC transfer characteristic before Opamp AR6A. The receiver board AGC is finally output to the 10.7 MHz converter, U3 via AR3A and Q1.

Comparator AR12 compares the detected AM audio output with the Track-and-Hold threshold level. When the signal level is lower than the threshold, Q8 conducts, effectively grounding the COR2 line.

The board control logic operates in the following manner. Serial data in three, 8-bit, bytes is clocked into two, 8-bit, decoder latches (U1 and U2) in the format below.

MSB FORMAT LSB

```
23 22 21 20 19 18 17 16 15 14 13 12 11  0  9  8  7  6  5  4  3  2  1  0
--------BYTE 2--------   -------BYTE 1---------    -------BYTE 0-------
```

The data is entered at U1 (which has a carry-over to U2), most significant bit (MSB) first, and least significant bit (LSB) last. After 24 clock pulses byte 0 is latched into U1 and byte 1 is latched into U2. Byte 3 (bits 16-23) is clocked in and out of U2. After the data has settled, a strobe pulse unlatches the decoders, writing each data bit onto the individual control lines. The control signal and its function for bits 0-15 are listed in Table 2. A bit map for the demodulation modes is shown in Table 3.

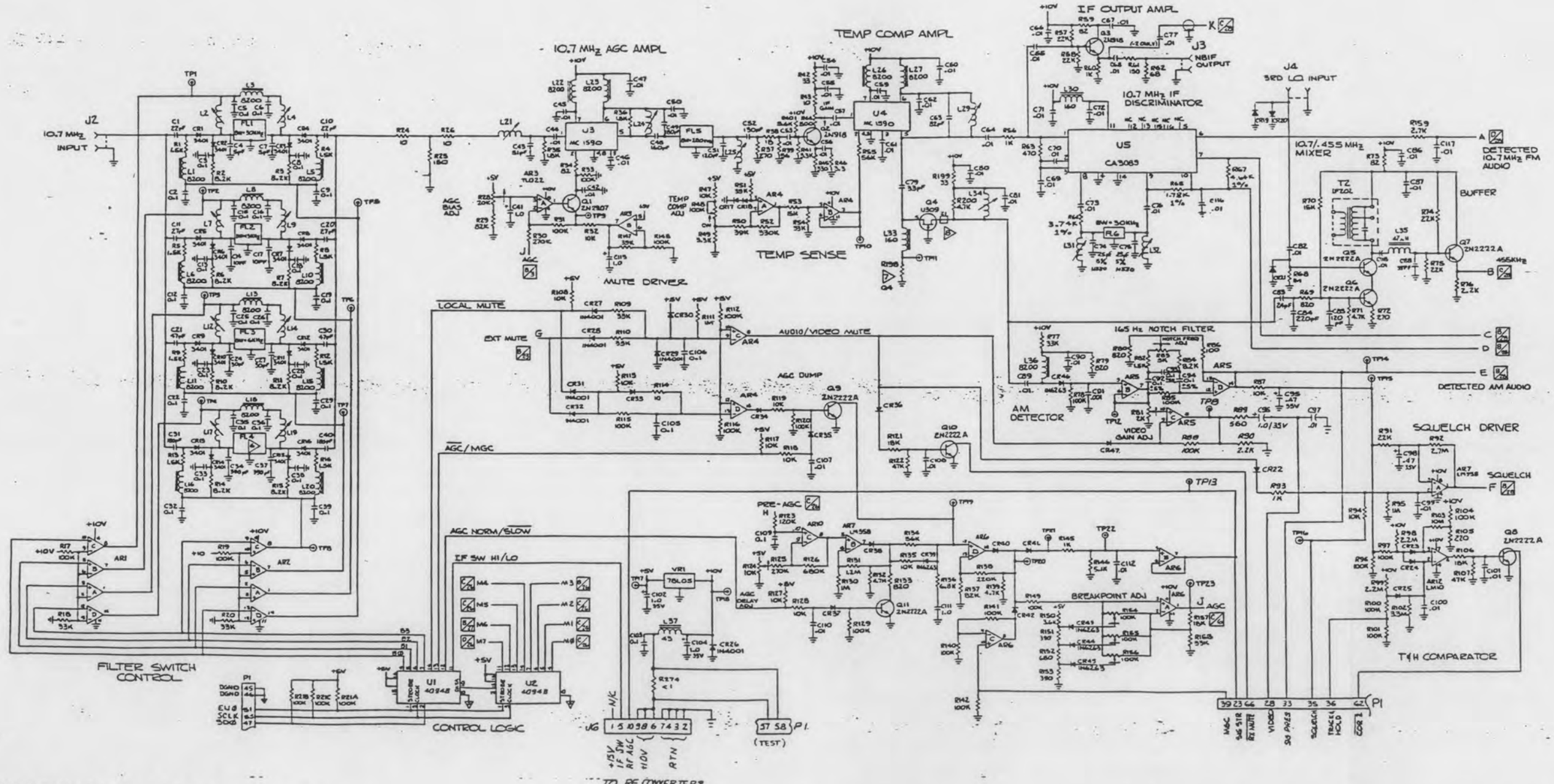
Table 3. Bit Map, Demodulation Control

MODE	BANDWIDTH kHz	BIT	8	9	10	11	12	13	14	15
		M	0	1	2	3	4	5	6	7
AM	200		1	0	1	0	1	0	x	1
	30		1	0	1	0	1	1	x	1
	13		1	0	1	0	1	1	x	1
	6		1	0	1	0	1	1	x	1
FM	200		1	0	1	1	1	0	x	0
	30		1	0	0	1	1	1	x	1
	13		1	0	1	1	0	1	x	1
	6		1	0	1	1	0	1	x	1
CW	200		0	1	1	1	1	0	x	1
	30		0	1	1	1	1	1	x	1
	13		0	1	1	1	1	1	x	1
	6		0	1	1	1	1	1	x	1
USB/ LSB	200		0	0	1	1	1	0	x	1
	30		0	0	1	1	1	1	x	1
	13		0	0	1	1	1	1	x	1
	6		0	0	1	1	1	1	x	1

Logic 0: 0Vdc
Logic 1: +5Vdc
x: OPERATOR SELECTED

DWG NO. 7100516 SH 1 E

REVISIONS				
REV	DESCRIPTION		DATE	APPROVAL
A	REVISED & REDRAWN	EJ 4-24	5-22-84	B.BOOKER
B	INCORP ECN 5425; EFF: 001, 002, 003, 005, 006, 007, 008, 015 & 020		5-31-84	B.BOOKER
C	INCORP ECN 5658 EFF: ALL		7/27/84	B.BOOKER
D	INCORP ECN 5698 EFF: ALL		7/27/84	B.BOOKER
E	INCORP ECN 6095; EFF: 050 & ON	A.D. 5/31/85	6/19/85	B.BOOKER



10. TABLE II COMPONENT VALUES THAT VARY ACCORDING TO DASH NO.
9. TEST POINTS ARE NOT COMPONENTS.
8. NON-STANDARD SYMBOL, FERRITE BEAD.
7. SOURCE RESISTOR IS MATCHED TO INDICATED TRANSISTOR. SEE PROCEDURE 025-908.
6. FOR -1 ASSY, FL4 BW IS 2.5KHz; FOR -2 ASSY, FL4 BW IS 200KHz.
5. INDUCTANCE IS IN MICROHENRIES. FOR VARIABLE INDUCTORS SEE TABLE I, ZONE D/23.
4. DIODES ARE IN4148.
3. OPERATIONAL AMPLIFIERS ARE LM324.
2. CAPACITORS ARE 50WVDC MINIMUM. CAPACITANCE IS IN MICRO FARADS.
1. RESISTORS ARE 1/8W, RESISTANCE IS IN OHMS ±5%.

NOTE: UNLESS OTHERWISE SPECIFIED

LAST REF DES USED

AR	C	CR	FL	J	L	K	P	Q	R	T	TP	U	VR	Y	Z
12	V64	63	6	7	40	1	1	23	214	3	40	6	1	1	1

REF DES NOT USED

1	53	1	28		12	22	1	24	
8	56		38		13	23			
52	57				14	27			
114	58					182			
115									

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

7100316
NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √
HOLE SIZES PER AND10387

DWN BY:	Ig Bo	4/26/84
CHECK:	B. BOOKER	5/22/84
APVD:		6/4/84
APVD:	T. Nadaffay	6/5/84
		6/19/84
RLSE:		

OCEAN APPLIED RESEARCH CORP (OAR)
A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC
IF AMPL & DEMODULATOR

SIZE D | FSCM NO. 06994 | DWG NO. 7100516 | REV E
SCALE | SHEET 1 OF 2

7100516 E

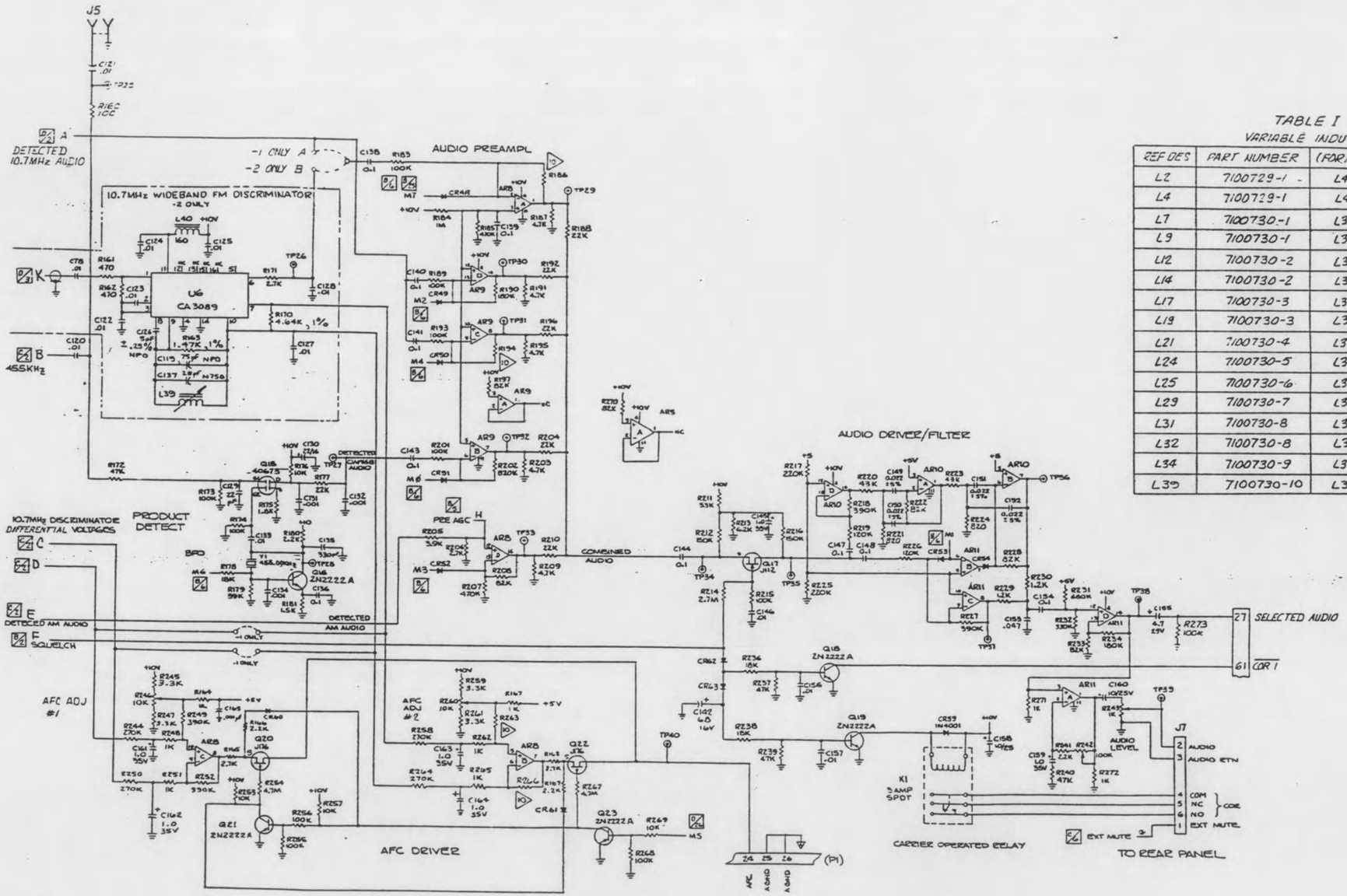


TABLE I
VARIABLE INDUCTORS

REF DES	PART NUMBER	(FORM TYPE, TURN COUNT)	
L2	7100729-1	L43-6	32 3/4
L4	7100729-1	L43-6	32 3/4
L7	7100730-1	L33-6	32 3/4
L9	7100730-1	L33-6	32 3/4
L12	7100730-2	L33-6	24 3/4
L14	7100730-2	L33-6	24 3/4
L17	7100730-3	L33-6	8 3/4
L19	7100730-3	L33-6	8 3/4
L21	7100730-4	L33-6	27 3/4
L24	7100730-5	L33-6	20 3/4
L25	7100730-6	L33-6	14 3/4
L29	7100730-7	L33-6	18 3/4
L31	7100730-8	L33-6	40 3/4
L32	7100730-8	L33-6	40 3/4
L34	7100730-9	L33-6	40 3/4
L35	7100730-10	L33-6	21 3/4

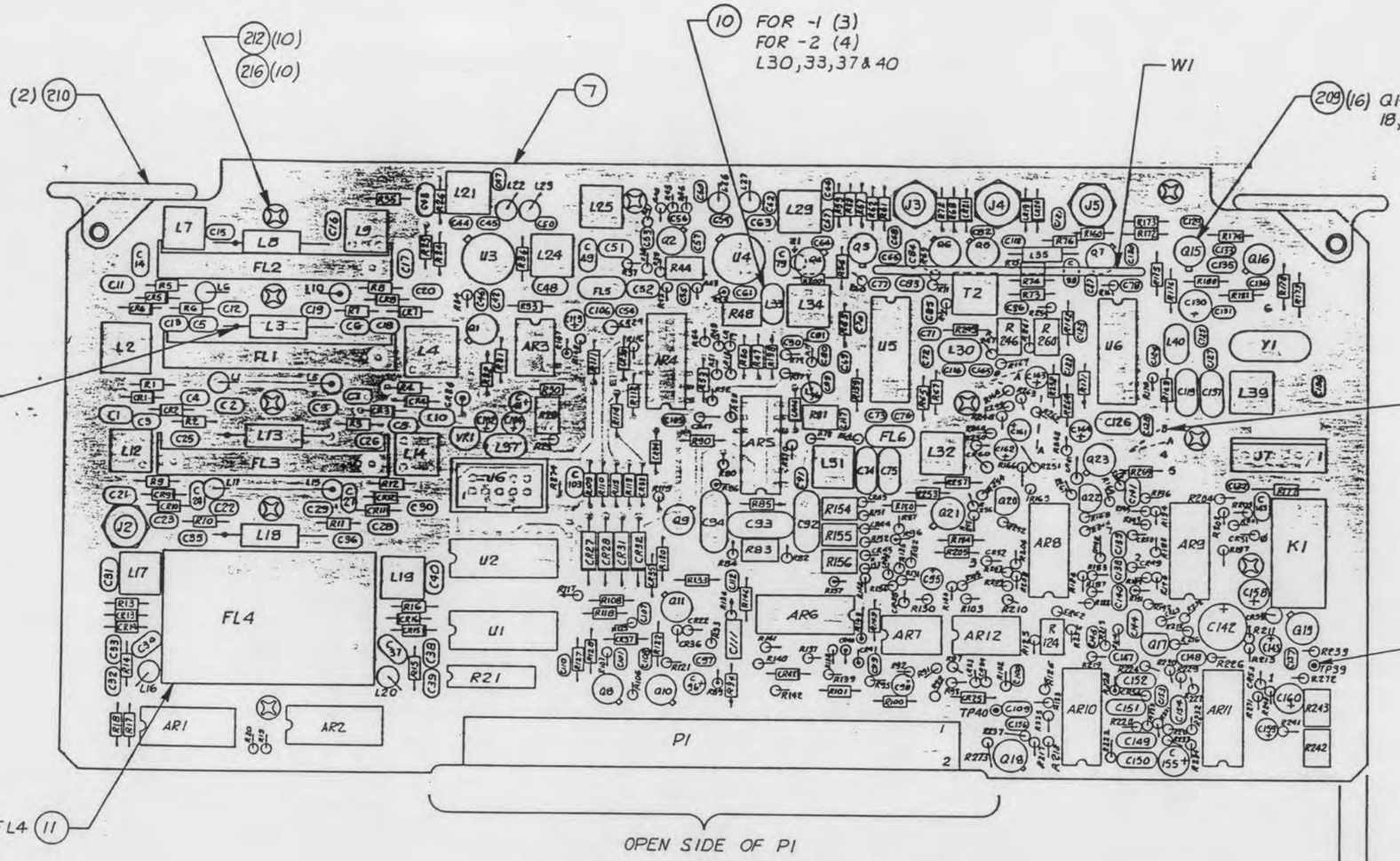
TABLE II

REF DES	VALUE	
	-1	-2
R186	75K	360K
R194	390K	75K
R263	390K	2M
R266	390K	2M

NOTE: UNLESS OTHERWISE SPECIFIED

DWG NO. 7100316 SH 1 M

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
L	INCORP ECN 6284, EFF: 050 & ON KD 8-15-85	1-16-86	L. BODIKER
M	INCORP ECN 6407 EFF: MWD 5-613 & ON SD 2-11-86	3-11-86	L. BODIKER



NOTES CONTINUED ON SHEET 2 (A/28)

5. CONFORMALLY COAT BOARD SURFACES AFTER CHECKOUT USING ITEM 228. MASK CONNECTORS, TERMINALS, RIGHT AND LEFT EDGES, AND SHIELD BAR CONTACT AREAS. (REMOVE SHIELD DURING COATING.)
4. STAKE VERTICALLY MOUNTED COMPONENTS AS REQUIRED USING ADHESIVE, ITEM 226.
3. ALL VERTICALLY INSTALLED DIODES TO HAVE CATHODE END UP.
2. BAG & TAG WITH PART NO. & REV LTR.
1. ● ON COMPONENT LEAD SPECIFIES TEST POINT LOCATION.

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

QTY PER ASSY: 345-410 / 240-410

NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ± .1, .XX = ± .03, .XXX = ± .010 SURFACE √
HOLE SIZES PER AND 10387
PROPRIETARY INFORMATION

DWN BY: Tim Duong	8/4/85	
CHECK: B. BODIKER	11/4/85	
APVD:	1/20/86	
APVD:	1/20/86	
	1-20-86	
RLSE: Jim Brooks	1/21/86	

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

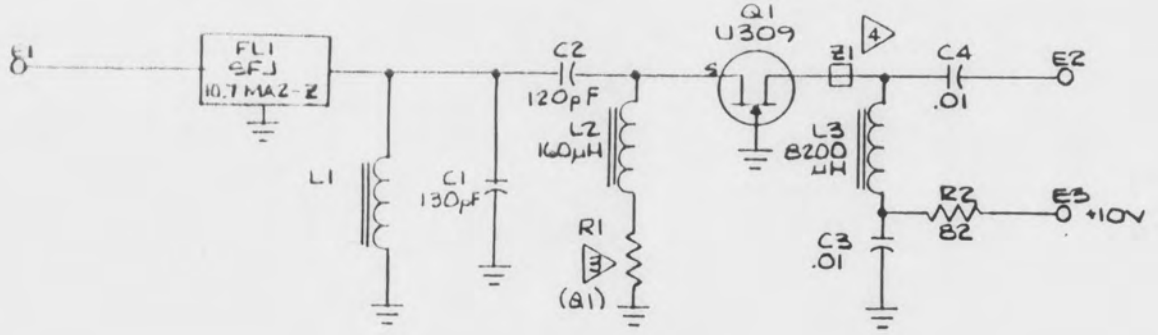
IF AMPLIFIER AND DEMODULATOR

SIZE D | FSCM NO. 06994 | DWG NO. 7100316 | REV M | SCALE: 2:1

7100316 M

DWG NO. 7100319 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	CIRCUIT WERE TBD AT 4/24/84	8-2-84	R. BARKER



4 NONSTANDARD SYMBOL, FERRITE BEAD.

3 SOURCE RESISTOR IS MATCHED TO INDICATED TRANSISTOR. SEE 025-908.

2 RESISTANCE IS IN OHMS, 1%

1 CAPACITANCE IS IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

LIST OF MATERIAL

-1 ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY				

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES ± 0° 30'
DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010
SURFACE √
HOLE SIZES PER AND10387

7100319
NEXT OR ASSOC ASSEMBLY

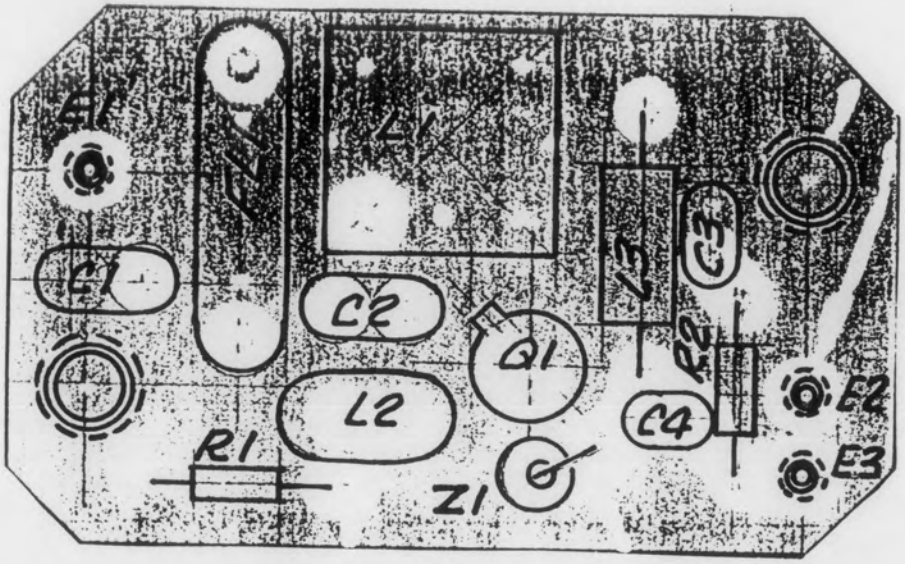
DWN BY:		1/12/83
CHECK:	B. BARKER	1/14/84
APVD:	D.S. BURMEISTER	8/3/84
APVD:	T. Mahoney	1/17/84
		8/3/84
RLSD:		1/19/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

SCHEMATIC
10.7 MHz BAND PASS FILTER
200 KHz BW

SIZE	FSCM NO.	DWG NO.	REV
B	06994	7100519	A

SCALE: — SHEET 1 OF 1



7100319-1. 10.7MHz BANDPASS FILTER, 200KHz BW

REVISIONS			
LTR	DESCRIPTION	APPROVAL	DATE
L	INCORP ECN 6284, EFF: 050 & ON KDB-15-85	B. BODIKER	1/14/86
M	INCORP ECN 6407, EFF: MWO 5-6194 + ON; S.D. 2-17-86	B. BODIKER	3/11/86

PL 7100316

FSCM NO. 06994

PL 7100316

SHEET 1 OF 12 REV M

TITLE: IF AMPLIFIER & DEMODULATOR

DRAFT: Kim Duong	8/15/85	QA:	1-20-86
CHECK: B. BODIKER	1/14/86	CM:	1/22/86
ENGR: D Mauz	1-8-86	REL: M. Brooks	1/21/86

NOTES: UNLESS OTHERWISE SPECIFIED

MWO NUMBER	QTY REQ THIS MWO	DATE MWO RELEASE	MTL REQ DATE	TOTAL COST THIS MWO

REV STATUS OF SHEET	M	L	L	L	M	L	L	L	L	L	L	L
	1	2	3	4	5	6	7	8	9	10	11	12

PL 7100316 REV L SH 2

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	-2	-10	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
1	240/2040	IF AMPL & DEMOD	-1		X	–	–					
2	345/3045	IF AMPL & DEMOD	-2		–	X	–					
3												
4	W1 (COAX JUMPER)	CABLE	-10	RG405/U MIL-C-17	–	1	X					
5												
6		SCHEMATIC	7100516		REF	REF						
7		BOARD	7100216-1		1	1						
8		SHIELD	7101032-1		1	1						
9		SHIELD BAR	7100088-1		1	1						
10		INSULATOR, CHOKE	025-079-1		3	4						
11		INSULATOR, FILTER	7100089-1		1	1						
12	FL4	FILTER, 2.5 KHz	7100745-1		1	–						
13	FL4	FILTER, 200KHz	7100319-1		–	1						
14												
15	Y1	CRYSTAL	7100728-1		1	1						
16	L2,4	INDUCTOR, VAR	7100729-1		2	2						
17	L7,9	↕	7100730-1		2	2						
18	L12,14		7100730-2		2	2						
19	L17,19		7100730-3		2	2						
20	L21		7100730-4		1	1						
21	L24		7100730-5		1	1						
22	L25		7100730-6		1	1						
23	L29	INDUCTOR, VAR	7100730-7		1	1						
24	L30,33	INDUCTOR, 160.4H	025-719-1		2	–						

PL 7100316 REV L SH 3

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	-2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
25	L30, 33, 40	INDUCTOR, 160 uH	025-719-1		-	3					
26	L31, 32	INDUCTOR, VAR	7100730-8		2	2					
27	L34	INDUCTOR, VAR	7100730-9		1	1					
28	L37	INDUCTOR, 43uH	025-705-1		1	1					
29	L39	INDUCTOR, VAR	7100730-10		-	1					
30											
31	Q4 & R198	XSTR-RES SET, U309	025-908-1		1	1					
32											
33											
34											
35	AR1, 2, 4, 5, 6, 8, 9, 10, 11	IC, OPER AMPL	LM324 N	NAT	9	9					
36	AR3	↕	TL022CP	TI	1	1					
37	AR7	↕	LM358N	NAT	1	1					
38	AR12	IC, OPER AMPL	LM10 N	NAT	1	1					
39											
40	C137	CAP, CER, 25pF, ±5% N750	561CU2HBA102AE250J	CERA-MITE	-	1					
41	C1, 10, 129,	CAP, MICA, 22pF	DM5CC220J	ELMENCO	3	3					
42	C4, 7	CAP, MICA, 5pF	DM5CC050D	ELMENCO	2	2					
43	C126	CAP, MICA, 5pF, ±25pF NPO	561CC0HBA102AESROD	CERA-MITE	-	1					
44	C11, 20	CAP, MICA, 27pF	DM5EC270J	ELMENCO	2	2					
45	C14, 17	↕ 10pF	DM5CC100J	↕	2	2					
46	C21, 30	47pF	DM5EC470J		2	2					
47	C24, 27	↕ 30pF	DM5EC300J	↕	2	2					
48	C31, 40, 49	CAP, MICA, 180pF	DM5FY181J	ELMENCO	3	3					

PL 7100316 REV L SH 4

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	-2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
49	C34, 37	CAP, MICA, 390pF	DM5FY391J	ELMENCO	2	2					
50	C43	51pF	DM5EC510J		1	1					
51	C48	160pF	DM5FY161J		1	1					
52	C51, 85	120pF	DM5FY121J		2	2					
53	C52	130pF	DM5FY131J		1	1					
54	C63	82pF	DM5EY820J		1	1					
55	C83	24pF	DM5CC240J		1	1					
56	C84	220pF	DM5FY221J		1	1					
57	C79, 88	CAP, MICA, 33pF	DM5EC330J	ELMENCO	2	2					
58	C135	CAP, MICA, 330pF	DM5FY331J	ELMENCO	1	1					
59	C74, 75	CAP, CER, 25pF ±5% N330	561CS2HBA102AF250J	CERA-MITE	2	2					
60	C41, 96, 102, 104, 113, 145, 159, 161, 162, 163, 164	CAP, Ta, 1μF, 35V	T350A105K035AS	KEMET OR EQ	11	11					
61	C95, C98	CAP, Ta, .47μF, 35V	T350A474K035AS	KEMET OR EQ	2	2					
62	C119	CAP, CER, 75pF, ±5% NPO	561C10GAA102AJ750J	CERA-MITE	-	1					
63	C155	CAP, Ta, 4.7μF, 25V	T350C475K025AS	KEMET OR EQ	1	1					
64	C158, C160	CAP, Ta, 10μF, 25V	T350E106K025AS	KEMET OR EQ	2	2					
65	C153	CAP, CER, .047μF	C320C473K5R5CA	KEMET OR EQ	1	1					
66	C111	CAP, CER, 1μF	CK06BX105K		1	1					
67	C91, 131, 132, 134, 165	.001μF	C315C102K5R5CA	KEMET OR EQ	5	5					
68	SEE LIST "B"	.01μF	C315C103K5R5CA	KEMET OR EQ	50	58					
69	SEE LIST "A"	CAP, CER, .1μF	C320C104K5R5CA	KEMET OR EQ	38	38					
70	C92, 93, 94	CAP, FILM, .1μF, 5%	23BJ410	MOUSER	3	3					
71	C149, 150, 151, 152	CAP, FILM, .022μF, 5%	23BJ322	MOUSER	4	4					
72	[illegible]30	CAP, AL, 22μF, 16V	226RLR016M	IL[illegible]DIS	1	1					

PL 7100316 REV M SH 5

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
73	C142	CAP, TA, 6.8μF, 16V	T350K686K016AS	KEMET OREQ	1	1					
74											
75	CR1-16	DIODE	MA4P3401		16	16					
76	SEE LIST "C"	DIODE	IN4148		31	31					
77	CR26,27,28,29,31,32,59	DIODE	IN4001		7	7					
78	CR39,43,44,45,46	DIODE	IN6263		5	5					
79											
80											
81	FL1	FILTER, 30KHz	PTI-1480	PIEZO	1	1					
82	FL2	13KHz	PTI-1478	PIEZO	1	1					
83	FL3	6KHz	PTI-6431	PIEZO	1	1					
84	FL5	280KHz	SFE10.7MA5-Z	MURATA	1	1					
85	FL6	FILTER, 30KHz	PTI-2283F	PIEZO	1	1					
86											
87											
88	J2,3,4,5	CONNECTOR, SMB	51-051-0000	SEALECTRO	4	4					
89	J6	CONNECTOR, IDC	609-1027	ANSLEY	1	1					
90	J7	CONNECTOR, HDR	22-11-2062	MOLEX	1	1					
91	P1	CONNECTOR, PLUG	1-102584-0	AMP	1	1					
92											
93											
94	L1,3,5,6,8,10,11,13,15,16,18,20,22,23,26,27,36	INDUCTOR 8200μH RF CHOKE	MS15089-34		17	17					
95	L35	INDUCTOR 47μH RF CHOKE	MS21401-7		1	1					
96	K1	RELAY	LM14D00	GEN INSTR	1	1					

PL 7100316 REV L SH 6

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
97											
98											
99	Q1	TRANSISTOR	2N2907		1	1					
100	Q2, 3		2N918		2	2					
101	Q5,6,7,8,9,10,11, 16,18,19,21,23		2N2222A		12	12					
102	Q17		J112	SILICONIX	1	1					
103	Q15		40673		1	1					
104	Q20,22	TRANSISTOR	J176	SILICONIX	2	2					
105											
106											
107	R1,4,5,8,9,12,13,16, 82,181	RESISTOR, 1/8W 5% CARBON FILM	1.5K		10	10					
108	R2,3,6,7,10,11,14,15,84		8.2K		9	9					
109	R18,20,54,77,109,110,158		33K		7	7					
110	R24,26,43,114		10Ω		4	4					
111	R25,61		150Ω		2	2					
112	R29,137,197,208,222, 228,233,270		82K		8	8					
113	R30,125,244,250,258,264		270K		6	6					
114	R34,59,73		82Ω		3	3					
115	R35,36,175		1.8K		3	3					
116	R37,72		270Ω		2	2					
117	R38		18Ω		1	1					
118	R39		56Ω		1	1					
119	R40		5.6K		1	1					
120	R4[illegible]5, 211,245, 247, 259,281	RESISTOR, 1/8W 5% CARBON FILM	3.3K		7	7					

PL 7100316 REV L SH 7

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
121	R42, 199	RESISTOR, 1/8W 5% CARBON FILM	33Ω		2	2					
122	R45		330Ω		1	1					
123	R46		3.3Ω		1	1					
124	R50, 51, 147, 179		39K		4	4					
125	R52, 232		330K		2	2					
126	R53, 70		15K		2	2					
127	R55, 134		56K		2	2					
128	R56, 60, 93, 145, 271, 272, T69, 167, 248, 251, 262, 265		1K		12	12					
129	R62		68Ω		1	1					
130	R63		470Ω		1	-					
131	R63, 161, 162		470Ω		-	3					
132	R205		3.9K		1	1					
133	R68, 95, 111, 130, 184		1M		5	5					
134	R69, 79, 80, 133, 221, 224		820Ω		6	6					
135	R76, 90, 180, 241 166, 169		2.2K		6	6					
136	R86, 160		100Ω		2	2					
137	R89		560Ω		1	1					
138	R92, 214		2.7M		2	2					
139	R98, 99		2.2M		2	2					
140	R102		3.3M		1	1					
141	R103		10 M		1	1					
142	R105		220Ω		1	1					
143	R106, 121, 157, 178, 236, 238		18K		6	6					
144	R107, 122, 172, 237, 239, 240	RESISTOR, 1/8W 5% CARBON FILM	47K		6	6					

PL 7100316 REV L SH 8

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
145	R123, 219, 226	RESISTOR, 1/8W 5% CARBON FILM	120K		3	3					
146	R126, 231		680K		2	2					
147	R131		1.2M		1	1					
148	R132, 254, 267		4.7M		3	3					
149	R136		6.8K		1	1					
150	R138, 217, 225		220K		3	3					
151	R146		5.1K		1	1					
152	R150		3.6K		1	1					
153	R151, 153		390Ω		2	2					
154	R152		680Ω		1	1					
155	R159, 206, 165, 168		2.7K		4	-					
156	R159, 171, 165, 168, 206		2.7K		-	5					
157											
158	R185, 207		470K		2	2					
159	R186(-1), R194(-2)		75K		1	1					
160	R190, 234		180K		2	2					
161	R194, 218, 227, 249, 252, 263, 266 (-1) R218, 227, 249, 252 (-2)		390K		7	4					
162	R202		820K		1	1					
163	R212, 216		150K		2	2					
164	R213		6.2K		1	1					
165	R220, 223		43K		2	2					
166											
167	R229, 230		1.2K		2	2					
168	R265, 266	RESISTOR, 1/8W 5% CARBON FILM	2M		-	2					

PL 7100316 REV L SH 9

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	-2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
169	R186	RESISTOR 1/8W 5% CARBON FILM	360K		-	1					
170											
171	SEE LIST "D"	RESISTOR, 1/8W 5% CARBON FILM	100K		33	33					
172	SEE LIST "E"		10K		16	16					
173	SEE LIST "F"		22K		11	11					
174	SEE LIST "G"	RESISTOR, 1/8W 5% CARBON FILM	4.7K		8	8					
175											
176	R21	RESISTOR NTWK 100K SIP	MSP06C01-104J	DALE OR EQ	1	1					
177											
178	R28	RESISTOR VAR 20K	3262W-1-203	BOURNS	1	1					
179	R44	500Ω	3262W-1-501		1	1					
180	R48,154,155,156,242	100K	3262W-1-104		5	5					
181	R81	2K	3262W-1-202		1	1					
182	R83	5K	3262W-1-502		1	1					
183	R124,246,260	10K	3262W-1-103		3	3					
184	R243	RESISTOR VAR 1K	3262W-1-102	BOURNS	1	1					
185	R64	RES, FXD FILM 3.74K ±1%	RN55C3741F		1	1					
186	R65	RES, FXD FILM 1.78K, ±1%	RN55C1781F		1	1					
187	R274	WIRE JUMPER	AWG 22 SOLID		1	1					
188	R67	RES, FXD FLM 4.64K, ±1%	RN55C4641F		1	1					
189	R163	RES, FXD FILM 1.47K, ±1%	RN55C1471F		-	1					
190	R170	RES, FXD FILM 4.64K, ±1%	RN55C4641F		-	1					
191											
192											

PL 7100316 REV L SH 10

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
193	T2	IF TRANSFORMER	421F202	MOUSER	1	1					
194											
195											
196											
197	U1,2	IC REGISTER	MC14094BCP	MOTO	2	2					
198	U3,4	IC	MC1590G	MOTO	2	2					
199	U5	IC DISCR	CA3089E	RCA	1	1					
200	U6	IC DISCR	CA3089E	RCA	-	1					
201											
202											
203	VR1	IC V RGLTR	MC78L05ACP	MOTO	1	1					
204											
205	Z1	FERRITE BEAD	2643000101	FAIR-RITE	1	1					
206											
207	TP39 & TP40 MØ – M7, E1	TERMINAL, TURRET	2061B OR 2002B	USECO	11	11					
208											
209		TRANSIPAD	10234N	MILTON ROSS	16	16					
210		EJECTOR	S203	SCANBE	2	2					
211											
212		LOCK WASHER, INT STAR	NO. 2		13	13					
213		LOCK WASHER, INT STAR	NO. 4		2	2					
214											
215		SCREW, PAN HD PHIL	2-56 x 1/8		3	3					
216		SCREW PAN HD PHIL	2-56 x 3/16		10	10					

PL 7100316 REV L SH 11

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	QUANTITY REQ'D PER ASSY -2	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
217		SCREW PAN HD PHIL	4-40 X 1/4		-	2					
218											
219	(RADIO)	NUT, SMALL PATTERN HEX	4-40		2	-					
220											
221											
222		RIBBON CABLE	455-044-10	SPECTRA-STRIP	A/R	A/R					
223		WIRE, ELEC, SLEEVED SOLID	AWG 24	QQ-W-343	A/R	A/R					
224											
225		ADHESIVE, RTV	161	GE	A/R	A/R					
226		ADHESIVE EPOXY	KIT 1C	HYSOL	A/R	A/R					
227											
228		COATING	ECCOSEAL HI-Q	EMERSON CUMMING	A/R	A/R					

LIST "A" .1 µF CAP

C2, C3, C5, C6, C8, C9, C12, C13, C15, C16, C18, C19, C22, C23, C25, C26, C28, C29, C32, C33, C35, C38, C39, C103, C105, C106, C109, C136, C138, C139, C140, C141, C143, C144, C147, C148, C154

LIST "B" .01 µF CAP

C42, C44, C45, C46, C47, C50, C53, C54, C55, C56, C57, C59, C60, C61, C62, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C76, C80, C81, C82, C86, C87, C89, C90, C97, C99, C100, C101, C107, C108, C110, C112, C116, C117, C118, C120, C121, C133, C146, C156, C157

FOR -2 ONLY: C77, C78, C122, C123, C124, C125, C127, C128

LIST "C" IN4148

CR17, CR18, CR19, CR20, CR21, CR22, CR23, CR24, CR25, CR30, CR33, CR34, CR35, CR36, CR37, CR38, CR40, CR41, CR42, CR47, CR48, CR49, CR50, CR51, CR52, CR53, CR54, CR60, CR61, CR62, CR63

LIST "D" 100KΩ RES

R17, R19, R31, R33, R78, R85, R88, R96, R97, R100, R101, R104, R112, R115, R116, R120, R129, R140, R141, R142, R148, R149, R173, R174, R183, R189, R193, R201, R215, R255, R256, R268, R273

LIST "E" 10KΩ RES

R32, R47, R87, R94, R108, R113, R117, R118, R119, R127, R128, R135, R176, R253, R257, R269

LIST "F" 22KΩ RES

R57, R58, R74, R75, R91, R177, R188, R192, R196, R204, R210

LIST "G" 4.7KΩ RES

R71, R139, R187, R191, R195, R200, R203, R209

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL	DATE	TITLE 10.7MHz BANDPASS FILTER, 200KHz BW	PARTS LIST 7100319
	APPVD	DATE		
	CHECK B. BODIKER	DATE 1/16/84		SHEET 1 OF 2 REV B
	DRAWN MWO	DATE 12/10/84		MWO

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100316			
QTY REQUIRED THIS RELEASE	FINAL ASSY	345-410			
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
A	ITEMS 5,8,9,14,20,21 & 22 AFFECTED MWO 1-16-84	B. BODIKER	1/16/84
B	INCORP ECN 5670; EFF: SERNO 001 & ON LJ 6-3-85	B. BODIKER	6/3/85

7100319
SH 2 OF 3

M	PART NO	DESCRIPTION	MANUFACTURER OR MANUFACTURER	QTY REQD ASSEMBLY -1					REQ QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
	-1	FILTER		X										
	7100519	SCHEMATIC		REF										
	7100219-1	BOARD		1										
	7100737-1	INDUCTOR, VAR		1										L1
7	025-719-1	INDUCT, RF CHOKE, 160μH		1										L2
1	025-079-1	INSULATOR CHOKE		1										
4	025-908-1	XSTR/RES SET U309		1										Q1/R1
0	DM5FY131J	CAP, MICA 130PF	ELMENCO	1										C1
1	DM5FY121J	CAP, MICA 120PF	ELMENCO	1										C2
2	C315C103K5R5CA	CAP, CER .01μF	KEMET OR EQ	2										C3,4
3	SFJ10.7MA2-ZA	FILTER (RED)	MURATA	1										FL1
4	SW-W-8200 MS21401-34	INDUCTOR, RF CHOKE, 8200μH	NYTRONICS OR EQ	1										L3
5														
6	82Ω	RES, 1/8W, 5%	CARBON FILM	1										R2
7														
8	Z643000101	FERRITE BEAD	FAIR-RITE PROD	1										Z1
9														
20	7723B	TERMINAL, PIN	USECO OR EQ	3										E1, E2, E3
21	350-1300-09-05-00	SPACER, 4-40 X .125	CAMBION OR EQ	2										
22	AWG 26	WIRE, SOLID, TINNED	QQ-W-343											

PHASE-LOCKED LOOP II BOARD

ASSEMBLY: 7100346

SCHEMATIC: 7100546

SECTION I

DESCRIPTION

1.1 General

The purpose of the phase-locked loop board is to extend the AM threshold into the noise level and to pick out weak signals with high noise background. It accomplishes this by providing a clean, low noise carrier to the demodulator to be multiplied with the input carrier. Three selectable narrowing noise bandwidths are provided. The low noise carrier provided by the phase lock loop allows it to demodulate a weak signal that would otherwise provide an unusable input to the receiver. Figure 1 is the simplified block diagram of the phase-locked loop.

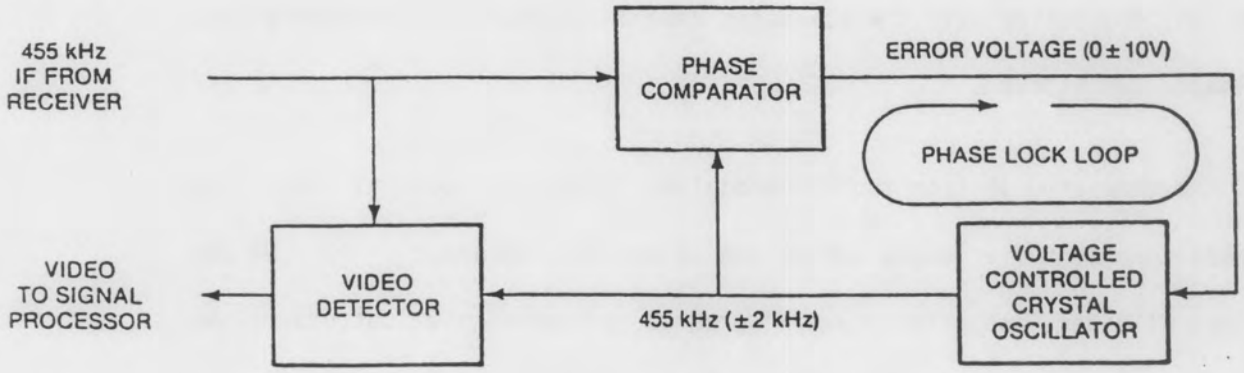


Figure 1. Simplified Block Diagram, Phase-Locked Loop

The 455 KHz IF input signal from the IF/Demodulator contains modulation components of audio intelligence on the transmitted signal as well as the sub-audio tones imposed by the ADF system to identify the magnitude of the E-W and N-S signals. The latter modulation is detected in the signal processor and used for bearing information to the CRT display and/or

digital bearing indicators.

The received signal from the IF/demodulator is multiplied with another 455 kHz signal generated by the voltage controlled crystal oscillator (VCXO) to detect the AM video signal. To synchronize the 455 kHz L.O. to the received signal, the VCXO phase is compared with that of the signal in the receiver IF. An error voltage is developed that is proportional to the phase difference of the two signals. This error voltage increases or decreases the frequency of the VCXO so that the two remain in a phase-locked state. With the phase-locked loop locked, the VCXO frequency is continually changing to match any drift in the received frequency.

1.2 Circuit Description

A complete block diagram is shown in figure 2. The block diagram should be used in conjunction with the schematic diagram (7100546) to reference the following description.

455 kHz modulated IF from the IF/demodulator board is input at J2. The cascade coupled buffer amplifier Q1 and Q2 buffers the input. Q3, Q4 and Q5 are limiter amplifiers which produce a square wave output. This square wave is converted to a +7V to -7V logic level at the output of the two inverting exclusive OR gates U1A and B. This logic level represents the 455 kHz IF/demodulator input stripped of amplitude modulation and is one of the inputs to the phase comparator (U1C) at pin 8. This input may be observed at TP1.

The other input is generated by the two crystal controlled oscillators Q9 and Q10. These two oscillators produce outputs at 10.100 MHz and 10.555 MHz respectively. The oscillator outputs are combined at mixer Q8 and the

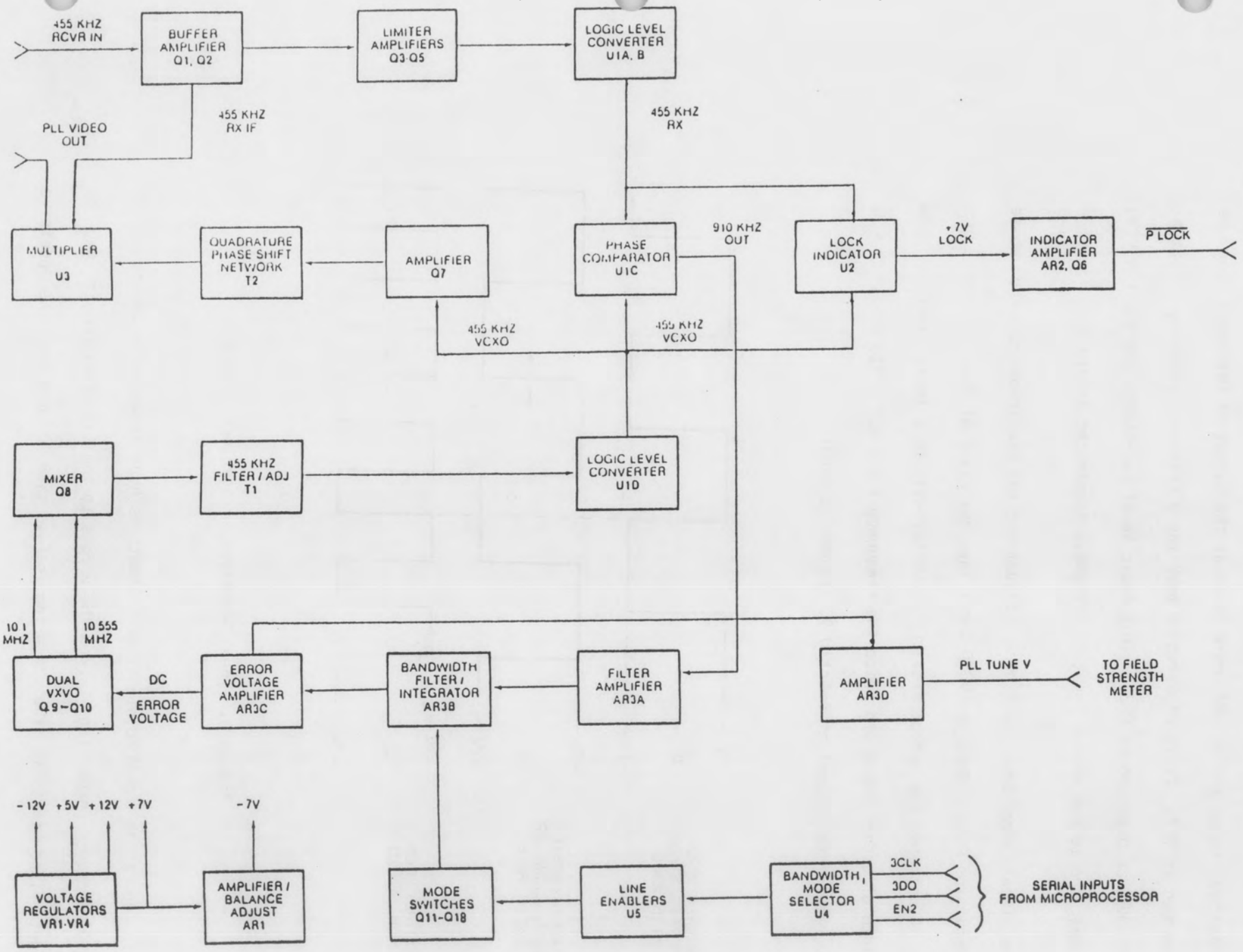


Figure 2. Block Diagram, Phase-Locked Loop

difference frequency of 455 kHz is selected by T1. The output of T1 is converted to a +7V to -7V logic level at the output of U1D which may be observed at TP2. T1 is adjusted to peak the difference frequency output at 455 kHz as observed at TP2. This logic level represents the 455 kHz VCXO output and is the second input to the phase comparator at pin 9.

The ideal waveforms in figure 3 illustrate the operation of the phase comparator U1C. When the VCXO input lags the phase of the received input by 90 degrees, the output from the converter will be a logic level half the width of either input and twice the frequency (2 x 455 = 910 kHz). The dc average of the signal at exactly 90 degrees is zero.

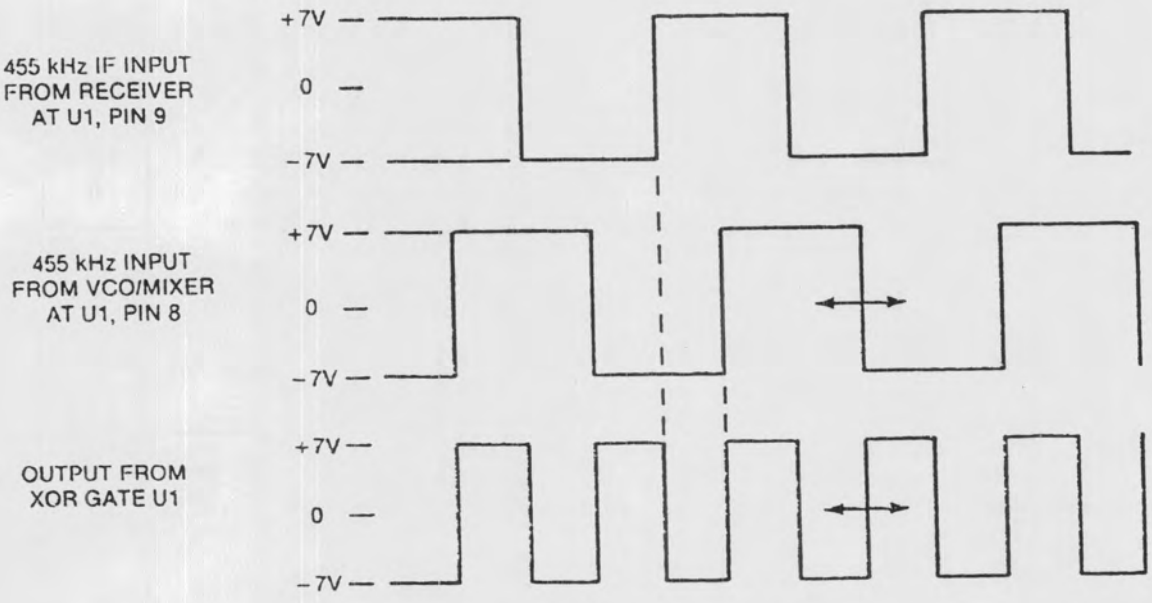


Figure 3. Ideal Waveforms, Phase-Locked Loop

In operation the VCXO signal will sometimes hunt above or below the exact 90 degrees phase lag. From the arrows in the illustration it may be determined that if the phase lag is less than 90 degrees the positive

portion of the output will widen. If the phase lag is more than 90 degrees the negative portion of the output will widen. The DC average of this signal will be positive or negative in accordance with which portion of the signal is wider.

The phase comparator output is filtered and amplified by AR3A. After amplification and integration in the bandwidth filter/integrator (AR3B), the varying pulse width becomes a varying DC level. This DC level is further amplified by the error voltage amplifier (AR3C). The output of AR3C is an error voltage varying between +10VDC and -10VDC. Whether error voltage is positive or negative will be determined by whether the VCXO input leads or lags the ideal 90 degree phase angle. The amount of lead or lag determines the size of the error voltage.

The error voltage pulls the frequencies of the two VCXO's. As positive error voltage increases, the 10.1 MHz VCXO (Q9) decreases in frequency, and the 10.555 MHz VCXO (Q10) increases in frequency. The increased difference frequency results in a higher frequency output to the phase comparator until its phase again lags the received input by 90 degrees. As negative error voltage increases the VCXO difference frequency to the phase comparator will decrease until 90 degrees phase lag is re-established. C40 and C48 in the VCXO tuned circuits are adjusted for 455 kHz output at TP2 with zero error voltage input.

The output of the bandwidth filter integrator is also amplified by AR3D and sent to P1 (pin 29), where it is used by the field strength meter in the PLL mode of operation to indicate the deviation from center frequency.

The two inputs to the phase comparator are also input to the lock indicator

U2 (pins 9 and 11). When the inputs are 90 degrees out of phase (zero error condition), every time U2 is clocked the Q output (at pin 13) will be positive (+7V). Therefore, with a zero error condition, the output will be a constant high. The threshold level at R28 is set with zero error, so that AR2A will begin conduction at the zero error level. Now, when lock is attained AR2A will conduct and +12V at the output will cause Q6 to saturate and provide a low $\overline{\text{PLOCK}}$ output at P1 pin 64. If lock should be lost, the Q output at pin 13 of U2 would no longer be a constant high, the voltage at C19 would decrease and Q6 would no longer conduct.

The inputs to AR2A are connected in parallel with AR2B, so when lock is present AR2B will conduct also. Conduction of AR2B will supply -12V at the output and Q19 will conduct, lighting LED CR10 and giving an indication of proper circuit operation. To avoid CR10 being mistaken for a FAULT indication when testing, during testing a low is present on pin 14 of U4. This low is fed thru U5 to the base of Q19, cutting Q19 off, and removing ground from the indicator. Therefore, the indicator will not light during testing.

PLL Video is detected by U3. One input is 455 kHz from the IF/demodulator. This modulated signal is picked off the Q1 emitter, adjusted by R7, and fed in at U3 pin 2. The second input is 455 kHz VCXO frequency. This input is picked off the output of U1D (pin 11) and amplified by Q7. The phase is then shifted to lag the receiver IF input another 90 degrees. This is accomplished in the quadrature phase shift network T2. The output of T2 is used to detect the video signal at U3. T2 is tuned to obtain maximum video output at pin 11 of U3. 455 kHz VCXO is input at U3 pin 5.

U3 is a multiplier/detector. 455 kHz modulated IF from the receiver is combined with 455 kHz VCXO. Since the two IF inputs are 180 degrees out of phase, they are effectively cancelled in the detector. The detector output is PLL VIDEO at pin 11 of U3, and is fed out at P1 pin 30. Selection of PLL or normal Video is controlled in the bearing processor.

PLL noise bandwidth selection is controlled by the serial inputs from the data processor at P1. The serial data inputs to the bandwidth mode selector (U4) will enable one of the four available output lines (pins 4, 5, 6 or 7). U5 acts as a level translator and provides line isolation. A low to any one of these outputs will control a series of FET switches which determine the components in the circuits associated with the bandwidth filter integrator (AR3B).

A low output at pin 5 (BW0) will cause Q18 to conduct and bandwidth will be narrow. A low output at pin 6 will cause Q13, Q14 and Q17 to conduct and bandwidth will be medium. A low output at pin 7 will cause Q11 and Q12 to conduct and bandwidth will be wide. A low output from pin 4 will cause Q15 and Q16 to conduct and will RESET the error voltage to zero. In this system BW0 is not used, and BW1 is considered narrow.

Q17 and Q18 will switch capacitance into the feed back circuity of AR3B. Q11 and Q13 will switch resistance into the input circuitry (pin 6) of AR3B. Q12 and Q14 will switch resistance into the ground path (pin 5) for the offset voltage of AR3B. Impedances are matched to avoid frequency drift when error input is zero volts.

Q15 and Q16 will conduct in a RESET condition. Q15 conduction will ground the offset at pin 5 of AR3B. Q16 conduction will short pin 7 to pin 6 and

error voltage will be held at zero volts for the duration of the reset input. This returns the VCXO to 455 kHz until the system is restored to an operate condition.

The power supply circuitry depicted in the lower right corner (P1) of the schematic provides additional power supply regulation and filtering to insure oscillator stability. The DRIFT BALANCE ADJUST potentiometer R101, insures that the differential between +7V and -7V is set at zero, as the oscillator would tend to follow any drift of the power supply. Diodes CR16, CR18 and CR21 provide reverse polarity protection. Diodes CR15, CR17, CR19 and CR20 protect the regulators during capacitive discharge when power is turned off.

DWG NO. 7100546 SH. 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL

455KHz IN — J2, C1 .1µF, R1 82K, R2 22K, R3 1K, C3 .1µF, R4 2.7K, R5 82, C2 1µF, Q1 2N2222, Q2 2N2222, -12V

VIDEO GAIN ADJ — R7 5K, C81 .1µF

Q3 2N2222 — R8 1K, C4 .01µF, C5 .01µF, R6 470, CR1, CR2, R9 82K, R10 12K, R11 82, R12 2.7K, R13 270

Q4 2N2222 — C6 1µF, C7 .01µF, C8 .01µF, R14 82K, R15 12K, R16 82, R17 2.7K, R18 270, CR3, CR4

Q5 2N2222 — C9 1µF, C10 .01µF, C11 .01µF, R19 82K, R20 12K, R21 82, R22 2.7K, R23 270, C12 1µF, C15 .01µF, CR5, CR6, CR7, CR8

+12V, C13 1µF, L1 8200µH, C14 22µF 16V, U1-B 4030B, U1-A 4030B, C16 .01µF, C17 10µF 25V, C18 10µF 25V, R24 220K, R25 TBD±1%, +7V OR -7V

TP1, TP2, TP4

LOCK THESHOLD ADJUST — R27 10K, R28 25K, R29 27K, C20 .01µF, R30 18K, CR9, Q6 2N2222, R31 47K, P1 PLOCK, CGND

U2-B 4013B, U2-A 4013B, NC

MC1458 — R22 220K NC, C19 .1µF, R32 1K 1/4W, C21 .01µF, CP10 5082-4494, Q19 2N2222, R95 10K, R96 33K, R94 33K

C34 .01µF, R54 780 ±1%, R53 220K, U1-D 4030B

TP5, R103 47K, R104 4.7K, DUTY CYCLE ADJUST, T1 JWM8901, C43 1µF

C54 5PF, R67 100K, C55 .01µF, +12V, U4C 4030B, R66 100K, C53 390PF, C56 .01µF, AR3 LF347, R68 3.3K, L2 15000µH, R70 62K, Q11 J176, C57 .1µF, R69 3M, R80 62K, Q12 J176, C58 .1µF, R81 100K, R71 56K, R72 100K, R73 100, P1 PLL TUNE V, A GND, TP3

74C906 U5 — R76 100K, R79 100K, R82 680K, C60 .1µF, Q13 J176, C59 .01µF, R84 100K, R83 680K, Q14 J176, Q15 J176, C61 .1µF, R85 100K, C62 .1µF, R86 100K, C63 47µF 25V, R87 3M

U4 140948 — OUTPUT ENABLE Q3, Q7, Q8, Q6, Q5, Q4, CLOCK, DATA, Q0, RESET 2, STROBE, Q2, Q1

R102 100K, +5V

Q16 J176 — R88 100K, C64 .1µF, R89 15K, C65 .1µF, R90 1M, C66 1µF, Q17 J176, C67 .1µF, R92 220K, C68 .1µF, Q18 J176, C70 .1µF, R91 100K, R93 100K, C69 .1µF

R74 33K, R75 100K, AR3 C, R76 27K, R77 10K

U3 XR2228CP — R42 27, C26 1µF, R43 4.7K, R44 100K, C28 22µF 16V, C27 30PF, R45 100K, R46 100K

T2 JWM8901 — C29 .1µF, C30 .1µF, R48 82, C32 1µF, Q7 2N2222, R47 10K, C31 .01µF, R49 27K, R50 33K, R52 10K, C33 .01µF, R51 33K

R33 3.9K, R34 2.7K, C22 .01µF, R35 3.1K, R36 3.1K, R37 10K, R38 10K, R39 100K, C23 22µF 16V, C24 .01µF, R40 10K, R41 2.7K, C25 1µF

P1 — 32 AGND, 30 PLL VIDEO, SCLK 55, SDO 47, EN2 53

Q8 40673, R55 1K, C37 27PF, C38 100PF, R57 2.2K, R59 10K, CR11, CR12, MV209, C40 3.3-18 PF, C41, C42 TBD, C35 22PF, R56 47K, Q9 MPSH81, C39 220PF, R58 10K, Y1 7100704-1 10.100 MHz, C47 220PF, Y2 7100704-2 10.555 MHz, R60 100K, R61 100K, C44 22PF, C45 5.1-50PF, C46 100PF, R63 2.2K, Q10 MPSH81, R65 10K, R64 10K, CR13, CR14, C48 3.3-18 PF, C49 TBD, C50 TBD, C51 .01µF, R62 47K

P1 — PLOCK, CGND; PWR GND

CR15 IN4001, VR1 79L12A, CR16 IN4001, C71 10µF 25V, C72 .1µF, C73 10µF 25V, -15V

CR17 IN4001, VR2 78L05A, CR18 IN4001, C74 22µF 16V, C75 .1µF, C76 22µF 16V, +8V

CR19 IN4001, VR3 LM317, CR20 IN4001, VR4 78L12A, CR21 IN4001, C77 .01µF, R99 11K, R98 1.21K±1%, R100 10K, R97 5.62K ±1%, R101 2K, AR1 MK1741, C78 10µF 25V, C79 .1µF, C80 10µF 25V, +15V

HIGHEST REFERENCE DESIGNATOR USED												
AR3	C81	CR21	P1	L2	Q19	R104	TP5	U5	VR4	Y2	T2	J2
REFERENCE DESIGNATOR NOT USED												

3. RESISTORS ARE 1/8 W. RESISTANCE IS IN OHMS ±5%.
2. DIODES ARE IN4148.
1. CAPACITORS ARE 50 WVDC MINIMUM.
NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

QTY PER ASSY — LIST OF MATERIAL

7100346 — NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √ HOLE SIZES PER AND10387

DWN BY: C. KENNEDY	6/18/84	
CHECK: B. BOOKER	7/3/84	
APVD:	7/23/84	
APVD: T. Rainaldi	7/25/84	
RLSE:		

OCEAN APPLIED RESEARCH CORP — A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC PHASE LOCKED LOOP II

SIZE D | FSCM NO. 06994 | DWG NO. 7100546 | REV

SCALE: | SHEET 1 OF 1

7100546 REV

DWG NO. 7100346 SH 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	REDRAWN PER ECN 5730. EFF: 020 & ON 2% 8-1-84	8/8/84	B.BOOKER
B	INCORP ECN 5780. EFF: 020 & ON 2% 8-1-84	9/4/84	B.BOOKER

(109)(5) INSTALL NEAR SIDE SNAP & SOLDER FAR SIDE TP1-TP5

(2) (127)

ALTERNATE LOCATION (-7V)

(123)

(128) (3) B1-8,5,9

(14) (124)

(14) (125)

(10)

(132) (1) 4 PLACES

(9)

(3)

(3)

(5)

(PWB SERIAL NO.)

(ITEM 3)

(1) -1 COMPONENT SIDE, PLL

2. IDENTIFY BY BAGGING AND TAGGING WITH PART NO., DASH NO., & REV LTR.

(1) APPLY .25 SQ PIECE OF TAPE, (ITEM 132) OVER CONDUCTOR PATTERN, 4 PLACES ON CIRCUIT SIDE PRIOR TO INSTALLATION OF GASKET, (ITEM 3).

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1 ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY		LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ± .1, .XX = ± .03, .XXX = ± .010 SURFACE √

HOLE SIZES PER ANSI0387

345-410

240-410

NEXT OR ASSOC ASSEMBLY

DWN BY:		8/1/84
CHECK:	B. BOOKER	8/8/84
APVD:		8/7/84
APVD:		8/8/84
		9/10/84
RLSE:		

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

PHASE LOCKED LOOP II

SIZE D | FSCM NO. 06994 | DWG NO. 7100346 | REV E

SCALE: | SHEET 1 OF

7100346 B

REVISIONS

LTR	DESCRIPITION	APPROVAL	DATE
A	INCORP ECN 5730. EFF SERNO 020 & ON LJ 8/1/84	B. BODIKER	8/8/84
B	INCORP ECN 5750; EFF: 020 & ON . KD 8/24/84	B. BODIKER	9/4/84

PL 7100346

KOAR

FSCM NO. 06994

PL 7100346

SHEET 1 OF 7 REV B

TITLE: PHASE LOCKED LOOP II

DRAFT: C. KENNEDY	6/19/84	Q A: T. Mahaffey	7/27/84
CHECK: B. BODIKER	7/3/84	[illegible]	7/31/84
ENGR: E. Barraller Jr.	7/23/84	REL: [illegible]	7/31/84

NOTES: UNLESS OTHERWISE SPECIFIED

MWO NUMBER	QTY REQ THIS MWO	DATE MWO RELEASE	MTL REQ DATE	TOTAL COST THIS MWO

REV STATUS OF SHEET	B			A		A	B			
	1	2	3	4	5	6	7	8	9	10

PL 7100346 REV A SH 4 OF

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
49	J2	CONNECTOR	51-051-0000	SEALECTRO	1					
50	P1	CONNECTOR	1-102584-0	AMP	1					
51										
52										
53	L1	INDUCTOR	SWW 8200 MS21401-34	NYTRONICS	1					
54	L2	INDUCTOR	SWD15000 MS90537-63	NYTRONICS	1					
55										
56										
57	Q1-7, 19	TRANSISTOR	2N2222		8					
58	Q9, 10	TRANSISTOR	MPSH81	MOTOROLA	2					
59	Q11-18	TRANSISTOR	J176	SILICONIX	8					
60	Q8	TRANSISTOR	40673	RCA	1					
61										
62										
63	R25,54	RESISTOR METAL FILM SELECTED VALUE	RN55CXXXX F		2					
64	R98	RES. METAL FILM 1.21K	RN50C1211F		1					
65	R97	RES. METAL FILM 5.62K	RN50C5621F		1					
66	R42	RESISTOR, 1/8W, 5% CARBON FILM	27Ω		1					
67	R5,11,16,21,48		82Ω		5					
68	R73		100Ω		1					
69	R13,18,23		270Ω		3					
70	R6		470Ω		1					
71	R3,R8,55		1K		3					
72	R57,63	RESISTOR. 1/8W, 5% CARBON FILM	2.2K		2					

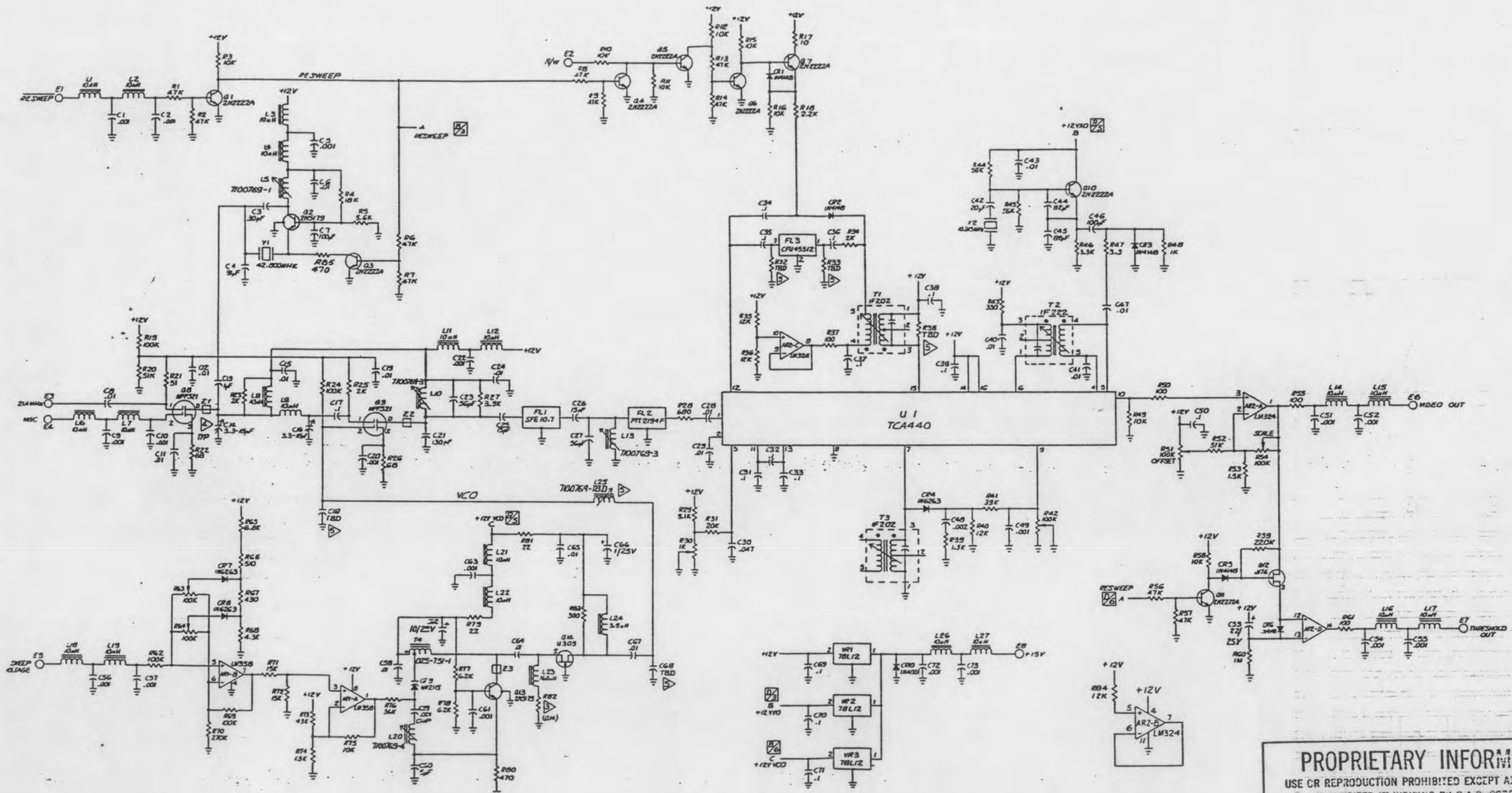
PL 7100346 REV ____ SH 5 OF 7

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
73	R4,12,17,22,34,41	RESISTOR, 1/8W, 5% CARBON FILM	2.7K		6					
74	R68		3.3K		1					
75	R33		3.9K		1					
76	R43, 104		4.7K		2					
77	R35,36		5.1K		2					
78	R27,37,38,40,47,52, 58,59,64,65,77,95,100		10K		13					
79	R99		11K		1					
80	R10,15,20		12K		3					
81	R89		15K		1					
82	R30		18K		1					
83	R2		22K		1					
84	R29,49,76		27K		3					
85	R50, 51, 74, 94, 96		33K		5					
86	R31,56,62,103		47K		4					
87	R71		56K		1					
88	R70,80		62K		2					
89	R1,9,14,19		82K		4					
90	R39,44,45,46,60,61,66,67,72, 75,78,81,84,85,86,88,91,93		100K		18					
91	R24,26,53,92		220K		4					
92	R82,83		680K		2					
93	R90		1M		1					
94	R69,87	RESISTOR, 1/8W, 5% CARBON FILM	3M		2					
95	R32	RESISTOR, 1/4W, 5% CARBON FILM	1K		1					
96										

PL 7100346 REV A SH 6 OF

ITEM NO.	REFERENCE DESIGNATION OR NOTE	DESCRIPTION	PART NUMBER	SOURCE OR MATERIAL	QUANTITY REQ'D PER ASSY -1	MWO QTY REQ	QTY ISS'D	BAL REQ	UNIT COST	TOTAL COST
97										
98	R101	RES, POT 2K	3262X-1-202	BOURNS	1					
99	R7	5K	3262X-1-502		1					
100	R28	RES, POT 25K	3262X-1-253	BOURNS	1					
101										
102	R78	RESISTOR NTWK 100K	MSP08A01-104J	DALE	1					
103	R102	RESISTOR NTWK 100K	MSP06A01-104J	DALE	1					
104										
105										
106	T1, T2	TRANSFORMER	JWM8901	MILLER	2					
107										
108										
109	TP1-TP5	TERMINAL	4521B	USECO	5					
110										
111										
112	U1	IC	CD4030BE	RCA	1					
113	U2	IC	CD4013BE	RCA	1					
114	U4	IC	MC14094BCP	MOTOROLA	1					
115	U3	IC	XR2228CP	EXAR	1					
116	U5	IC	MM74C906N	NATIONAL	1					
117										
118	VR1	VOLTAGE RGLTR	MC79L12ACP	MOTOROLA	1					
119	VR2	VOLTAGE RGLTR	MC78L05ACP	MOTOROLA	1					
120	R3	ADJUSTABLE VOLTAGE RGLTR	LM317H	MOTOROLA	1					

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	INCORP ECN 5961; EFF: UNIT # 6/3/85	6/4/85	R.BODIKER



5. TBD PARTS INSTALLED ONLY AS REQUIRED. WHEN NOT INSTALLED, LIS IS REPLACED WITH A JUMPER.
4. NOW STANDARD SYMBOL, FERRITE BEAD.
3. SOURCE RESISTOR IS MATCH TO INDICATED TRANSISTOR, SEE 025-908.
2. RESISTORS ARE 1/8W, RESISTANCE VALUES ARE IN OHMS ± 5%.
1. CAPACITORS ARE 50WVDC MIN CAPACITANCE VALUES ARE IN MICROFARADS.

NOTE: UNLESS OTHERWISE SPECIFIED

LAST REF DES USED												
AR	C	CR	FL	L	Q	R	T	U	VR	Y	Z	E
2	73	10	3	27	14	85	4	1	3	2	3	8
REF DES NOT USED												

QTY PER ASSY	-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
	LIST OF MATERIAL					

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010 SURFACE √

HOLE SIZES PER AND10387

7100350

NEXT OR ASSOC ASSEMBLY

DWN BY: Tim Duong	9/20/84	
CHECK: B. BODIKER	10/29/84	
APVD: [illegible]	11/27/84	
APVD: T. Mahaffey	12/3/84	
[illegible]	12/5/84	
RLSE: [illegible]	12/31/84	

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

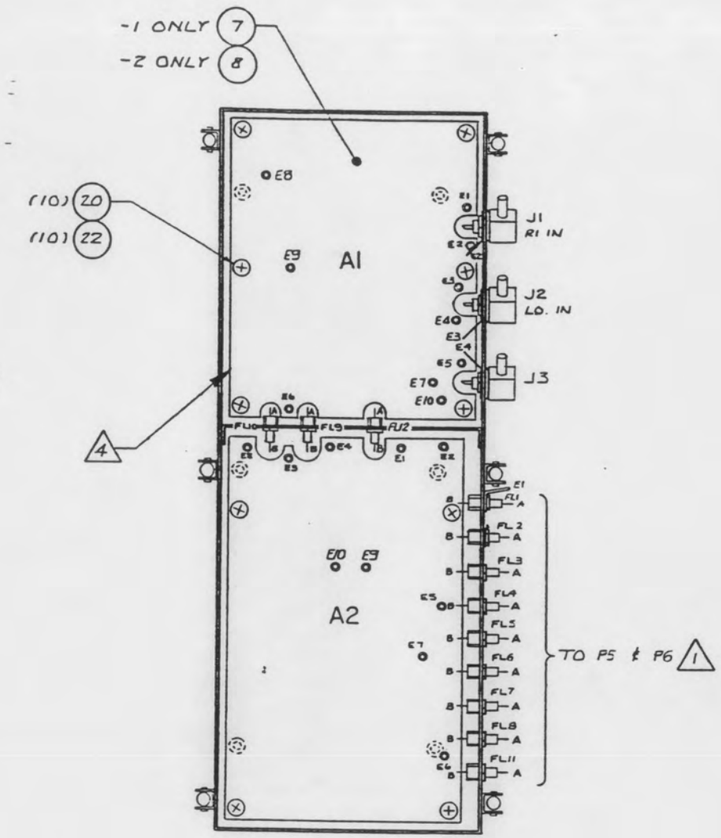
SCHEMATIC, RF BOARD, PAN RECEIVER

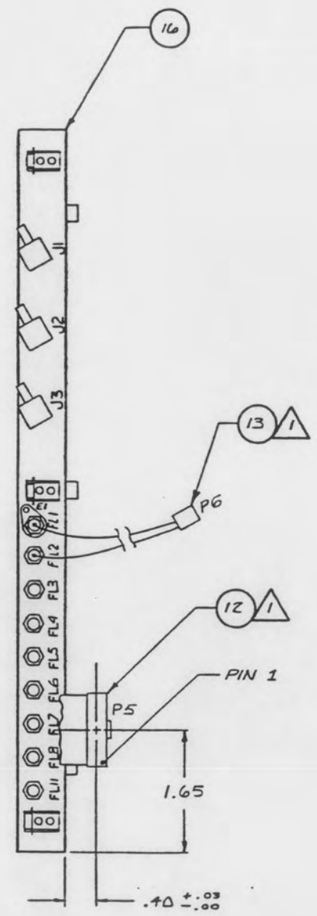
SIZE D | FSCM NO. 06994 | DWG NO. 7100550 | REV A | SCALE: | SHEET 1 OF

7100550 A

DWG NO. 7100449 SH 1 REV B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	INCORP ECN 6033 KD 3-28-85	3/29/85	R.BOOKER
B	INCORP ECN 6068 EFF: 001 & ON JT 12-30-85		
B-1	P/L ITEM 2, 2040 WAS 2045 JT 12-30-85	12/31/85	LCHAVEZ





WIRING DATA

WIRE	FROM	TO	COLOR/TYPE		FUNCTION
1	E1	P5-9	WI	WHT	GND
2	E1	P5-3		ORN	GND
3	E1	P5-10		BLK	GND
4	FL1-A	P5-7	WI	VIO	IF SWITCH
5	FL1-A	P6-3	W2	WHT	IF SWITCH
6	FL2-A	P5-11	WI	BRN	+15 V
7	FL2-A	P5-12	WI	RED	+15 V
8	FL2-A	P6-1	W2	RED	+15 V
9	FL3-A	P5-13	WI	ORN	MGC
10	FL4-A	P5-15		GRN	RESWEEP
11	FL5-A	P5-5		GRN	W/N
12	FL6-A	P5-14		YEL	SWEEP V
13	FL7-A	P5-16		BLU	THRESHOLD
14	FL8-A	P5-2		RED	VIDEO
15	FL11-A	P5-8	WI	GRY	RF FAULT
16	FL1-B	FL10-B	AWG 26	RED	IF SWITCH 4
17	FL2-B	FL9-B		ORN	+15 V
18	FL3-B	A2E4		YEL	MGC
19	FL4-B	A2E1		BRN	RESWEEP
20	FL5-B	A2E2		VIO	W/N
21	FL6-B	A2E5		WHT	SWEEP V
22	FL7-B	A2E7		BLU	THRESHOLD
23	FL8-B	A2E6		INSUL BUS	VIDEO
24	FL9-B	A2E8		ORN	+15V
25	FL9-A	A1E8		ORN	+15V
26	FL10-A	A1E9		RED	IF. SWITCH 4
27	FL12-A	A1E5		GRN	LO BITE
28	E2	A1E2		BUS	RF GND 4
29	E3	A1E4		BUS	RF GND 3
30	E4	A1E4		BUS	RF GND 3
31	J1	A1E1		BUS	74/137.75 MHz 3
32	J2	A1E3		BUS	LOCAL OSC 3 5
33	J3	A1E7		BUS	AUX 21.4MHz 3 5
34	FL11-B	A2E10		GRAY	RF FAULT
35	FL12-B	A2E9	AWG 26	GRN	LO BITE
36	A1E6	A2E3	RG196	COAX	21.4MHz 3
37	A1 GND PLANE	A2 GND PLANE	COAX	SHIELD	GND

(1) -1 ASSY SHOWN

(2) -2 SAME AS -1 EXCEPT AS NOTED

4 WIRE NO'S 16 & 28 USED ONLY IN -1 ASSY

3. SLEEVE AS REQD. CUT FOR SHORTEST POSSIBLE LENGTH COMPATIBLE WITH MINIMUM STRAIN RELIEF REQUIREMENTS.

2. IDENTIFY BY BAGGING & TAGGING WITH PART NO., DASH NO. & REV LTR.

1. SEE WIRING DATA

NOTE: UNLESS OTHERWISE SPECIFIED

SEE SEPARATE PARTS LIST

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY	LIST OF MATERIAL				

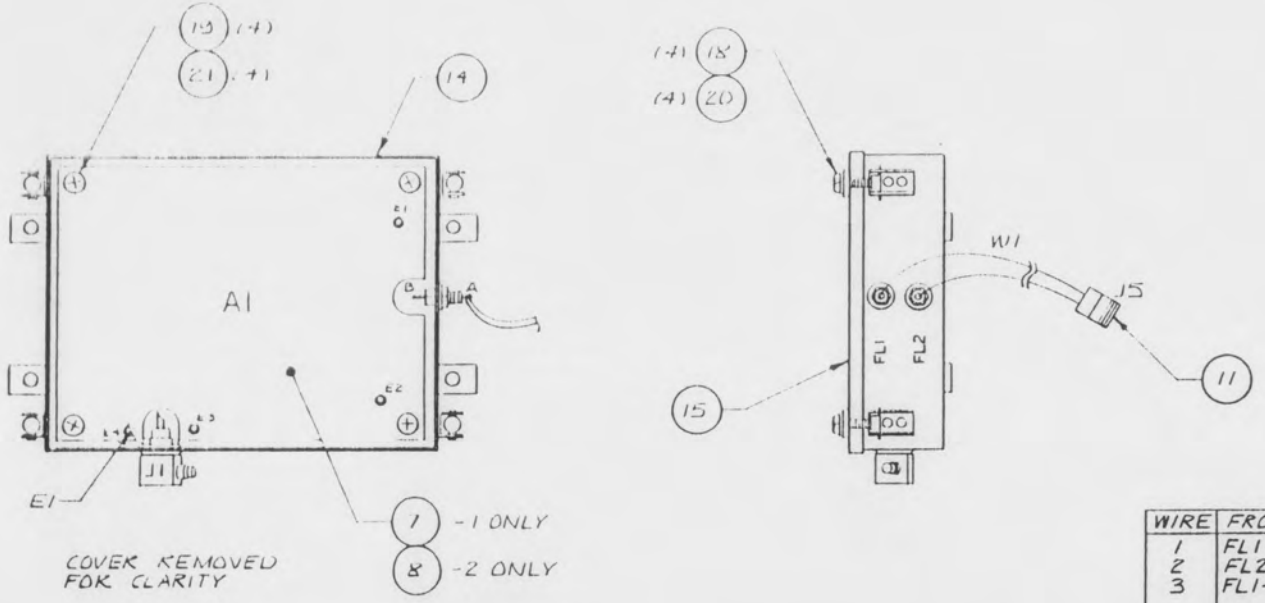
7100440
NEXT OR ASSOC ASSEMBLY

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES:
ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ± 03 .XXX = ±.010 SURFACE
HOLE SIZES PER AND10387

DWN BY: A. ORNELAS	10/1/84	OCEAN APPLIED RESEARCH CORP (OAR)
CHECK: R. BOOKER	10/30/84	A DIVISION OF GENERAL INDICATOR CORP
APVD: D May	10/31/84	PAN RF MODULE
APVD: T. Hanaike	11/1/84	
RLSE:	11/1/84	SIZE D FSCM NO. 06994 DWG NO. 7100449 REV E
		SCALE: 1 SHEET 1 OF 1

7100449 B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL



WIRING DATA

WIRE	FROM	TO	COLOR/TYPE	FUNTION
1	FL1-A	J5-3	W1-WHT	IF SWITCH
2	FL2-A	J5-1	W1-RED	+15V
3	FL1-B	A1E1	AWG 26 RED	IF SWITCH (-1 ONLY)
4	FL2-B	A1E2	AWG 26 ORN	+15V
5	J1	A1E3	AWG 26 BUS	L.O. OUT (2)
6	E1	A1E4	AWG 26 BUS	RF GND (2)

(1) -1 L.O. SHOWN

(2) -2 SAME AS -1 EXCEPT AS NOTED

SEE SEPARATE PARTS LIST

-1 QTY PER ASSY	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
			LIST OF MATERIAL		

(2) SLEEVE AS REQD. CUT FOR SHORTEST POSSIBLE LENGTH COMPATIBLE WITH MINIMUM STRAIN RELIEF REQUIREMENTS

1. IDENTIFY BY BAGGING & TAGGING WITH PART NO., DASH NO & REV LTR.

NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES: ANGLES ± 0°30' DECIMAL .X ± .1, .XX ± .03, .XXX ± .010 SURFACE √ J. HOLE SIZES PER ANDI0387

240-410
345-410
NEXT OR ASSOC ASSEMBLY

DRAFT	A ORNELAS	12/1/84
CHECK	J BROWER	12/19/84
APP'D	J May	1/14/85
APP'D	T Wilson	1/15/85
		1/17/85
RELEASE		1/17/85

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP
OAR

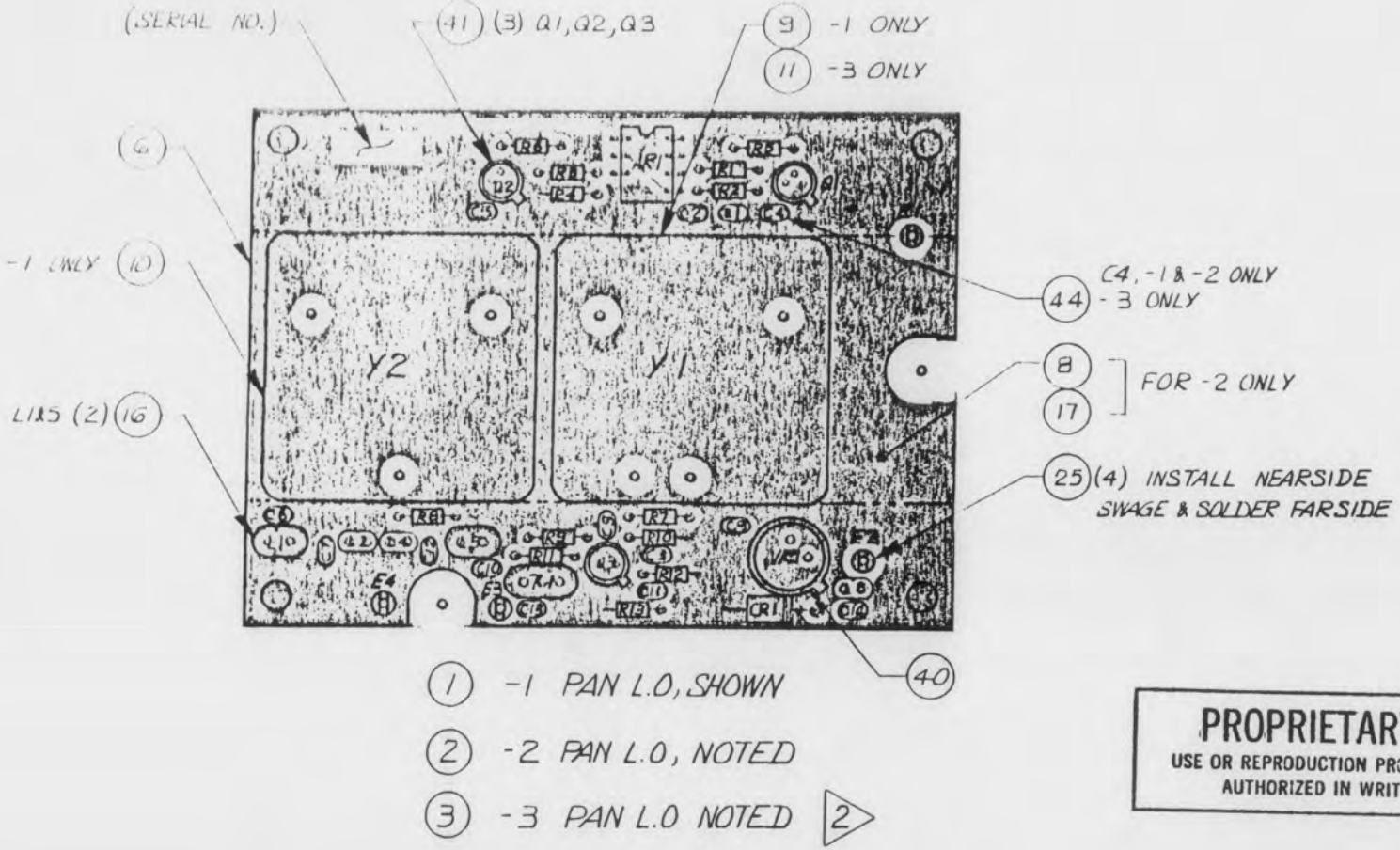
PAN LOCAL OSC MODULE

SIZE	FSCM NO.	DWG NO.	REV
C	06994	7100448	

SCALE 1:1 SHEET 1 OF 1

7100448

REV	DESCRIPTION	DATE	APPROVAL
B	REDRAWN WITH CHANGE EFF. CODE XON KD 11-6-84	12/19/84	B. BOOKER
C	PL ONLY AFFECTED PER ECN 6081	5/23/85	R. BOOKER



(1) -1 PAN L.O, SHOWN

(2) -2 PAN L.O, NOTED

(3) -3 PAN L.O NOTED <2>

SEE SEPARATE PARTS LIST

<2> FOR -3 OMIT: AR1, C1-5, R1-6, R8, Q1, Q2, & Y2, ADD JUMPER IN PLACE OF C4.

1. IDENTIFY WITH PN 7100349 DASH NO. & REV LTR.

NOTE UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY			LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30', DECIMAL .X ± .1, .XX ± .03, .XXX ± .010, SURFACE √, HOLE SIZES PER ANSI B32.1	DRAFT Lily Duong 11/6/84	OCEAN APPLIED RESEARCH CORP A DIVISION OF GENERAL INDICATOR CORP OAR	
	CHECK R. Booker 12/19/84	PAN L.O. OAR 3045	
	APP'D J. May 1/4/85		
7100448	APP'D T. Hashimoto 1/16/85	SIZE C FSCM NO. 06994 DWG NO. 7100349 REV C	
NEXT OR ASSOC ASSEMBLY	RELEASE 1/16/85	SCALE 2:1	SHEET 1 OF 1

7100349

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE 1/11/85	TITLE PAN LOCAL OSC MODULE	PARTS LIST 7100448
	APPVD D. May	DATE 1/4/85		SHEET 1 OF 3 REV
	CHECK B. BODIKER	DATE 12/19/84		MWO
	DRAWN A. ORNELAS	DATE 10/12/84		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	Z40-410	345-410		
QTY REQUIRED THIS RELEASE	FINAL ASSY	240-410	345-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE

7100448
SH 2 OF

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	ASSY		X							
2	-2	ASSY			X						
3											
4											
5											
6											
7	7100349-1	PAN L.O.		1	-						A1
8	7100349-2	PAN L.O.		-	1						A1
9											
10											
11	7100453-1	CABLE		1	1						W1
12											
13											
14	7100452-1	HOUSING		1	1						
15	7101051-1	COVER		1	1						
16											
17											
18	4-40 × 5/8	PAN HD PHIL		4	4						
19	4-40 × 3/16	PAN HD PHIL		4	4						
20	NO. 4	FLAT WASH		4	4						
21	NO. 4	LOCK WASH INT TOOTH		4	4						
22											

7100448
SH 3 OF 3

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	QTY PER ASSEMBLY -2	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23											
24											
25	B-26 RED	WIRE 600V	MIL-W-16878	A/R	A/R						
26	B-26 ORN	WIRE 600V	MIL-W-16878	A/R	A/R						
27											
28											
29											
30	AWG 26	WIRE, BUS SOLID	QQ-W-343	A/R	A/R						
31	AWG 26	SLEEVING		A/R	A/R						
32											
33											
34											
35											
36											
37											
38											
39											
40											
41											
42											
43											
44											

PANORAMIC LOCAL OSCILLATOR

ASSEMBLY: 7100448

SCHEMATIC: 7100549-1

SECTION I

DESCRIPTION

1.1 General

The panoramic local oscillator consists of two oscillator modules with outputs of 52.6 MHz and 159.15 MHz. An IF switching input selects one of the two oscillators to conform to the wideband IF inputs to the panoramic converter, 74 MHz and 137.75 MHz, respectively. The selected local oscillator frequency is output through a buffer amplifier, and sent to the panoramic converter where it is mixed with the selected IF frequency to provide a difference frequency of 21.4 MHz.

1.2 Circuit Description

Refer to the block diagram (figure 1) and schematic 7100549-1 during the following discussion.

The panoramic local oscillator is controlled by the HIFRQLO input from the PAN controller at E1, which determines which of the two local oscillator modules (Y1, Y2) will be activated. Oscillator Y1 operates at 159.15 MHz and oscillator Y2 operates at 52.6 MHz.

When the HIFRQLO input is high, transistor switch Q1 is turned on by the positive output of AR1B. With Q1 on, oscillator Y1 is biased into conduction, and the oscillator output is 159.15 MHz. The inverted low output of AR1A turns transistor switch Q2 off, removing bias from oscillator Y2.

When the IF switch input is low, the inverted AR1A output goes positive, and turns on transistor switch Q2. With Q2 on, oscillator Y2 is based into

conduction, and the oscillator output is 52.6 MHz. The negative output of AR1 turns Q1 off, removing bias from oscillator Y1.

The selected oscillator frequency is coupled out via a through buffer amplifier Q3 to an impedance matching autotransformer and out at E3. The oscillator output is mixed with the 74 MHz or 137.75 MHz IF (as selected) in the panoramic converter to provide a difference frequency of 21.4 MHz.

The +15Vdc power input at E2, provides a regulated +12Vdc output from regulator VR1. Diode CR1 provides reverse polarity protection to the regulator.

The -2 version of this board is the same with the exception of Y1 and Y2 which are part no. 7100351-1.

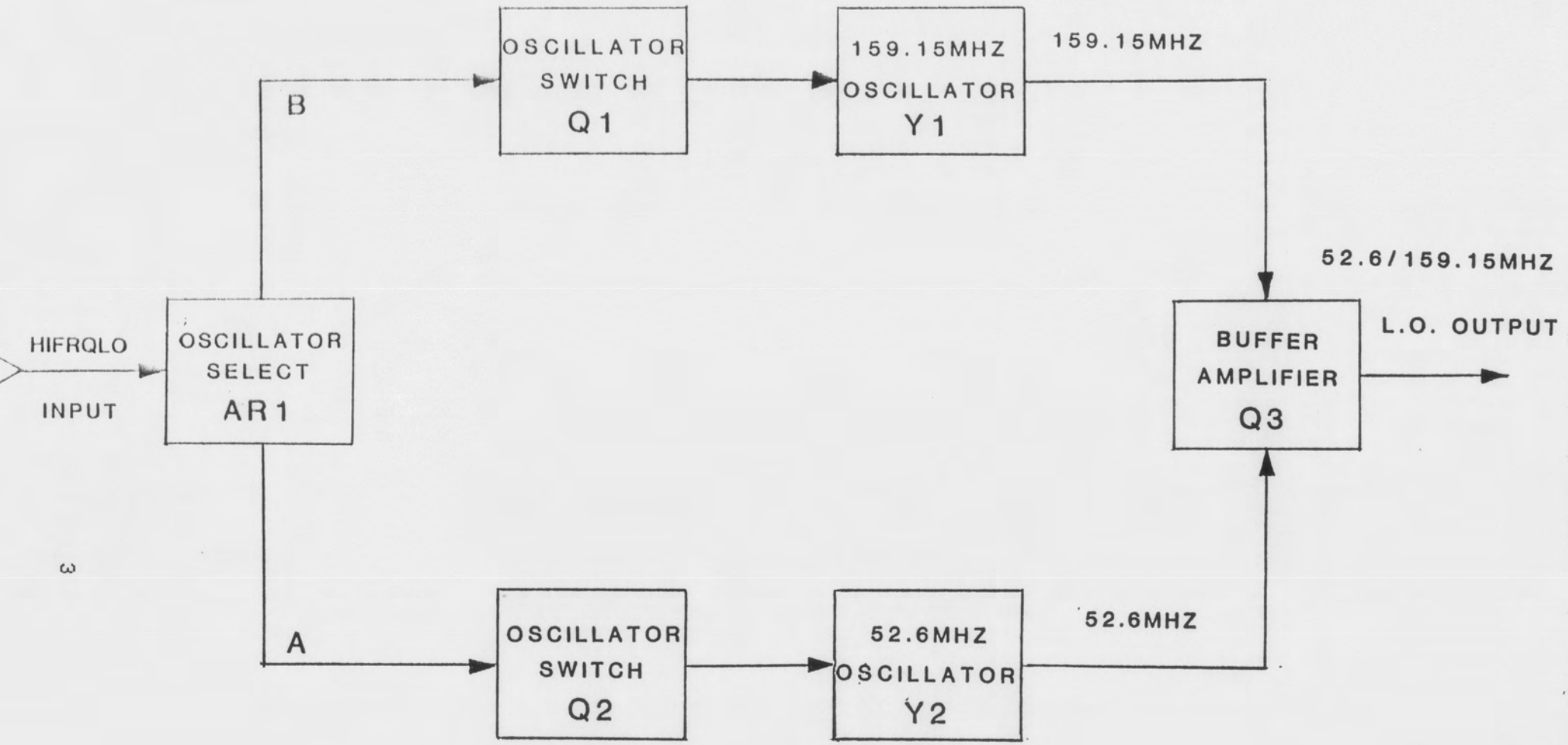
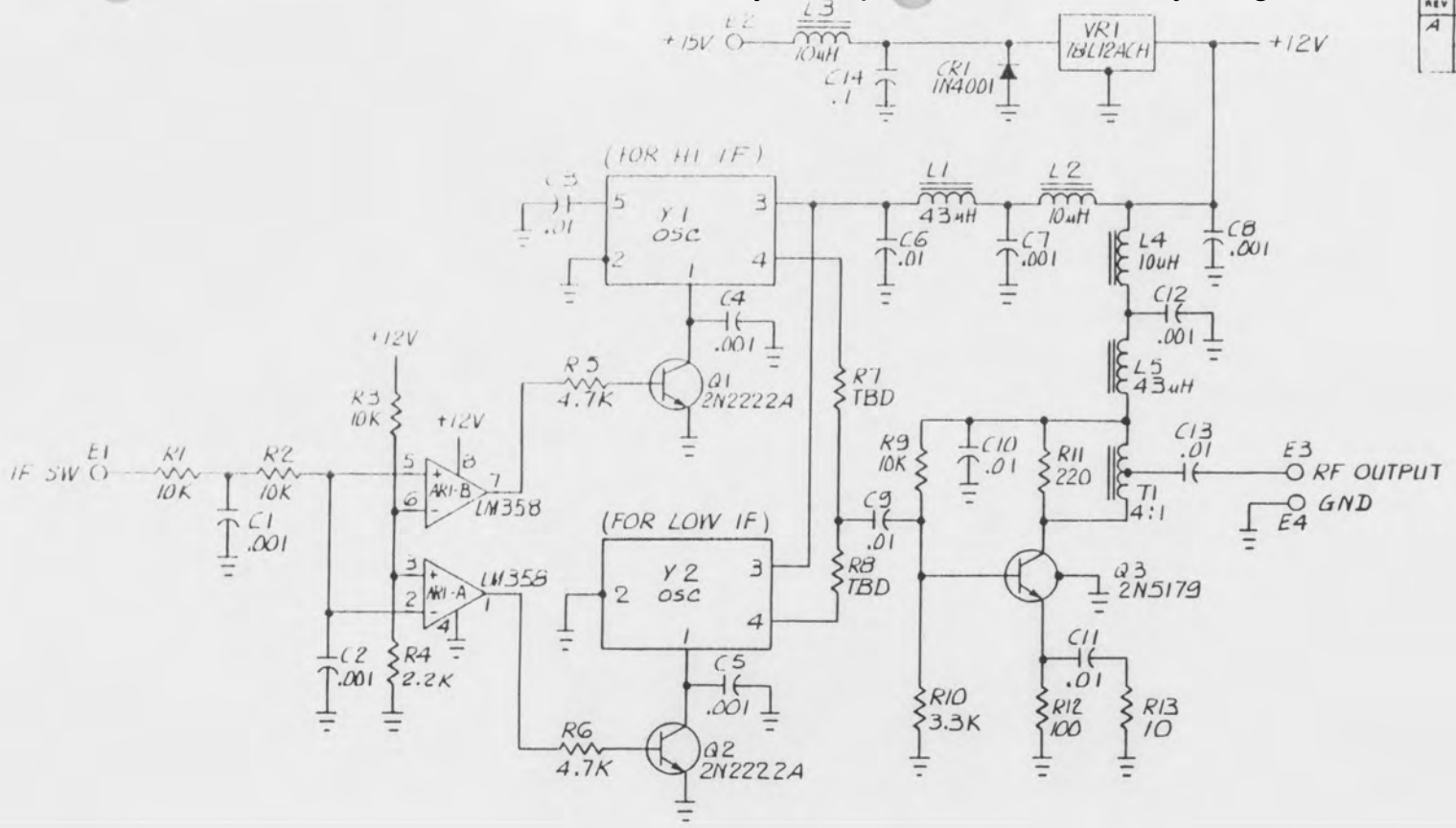


Figure 1. Block Diagram, Panoramic Local Oscillator

REV	DESCRIPTION	DATE	APPROVAL
A	ADDED C3 EFF: S/N 001 & ON R4 WAS 10K CREATED - 3 W 9-19 BA	10/4/84	R BADINER



- -1 STD FOR OAR3045
  Y1 = 159.15MHz
  Y2 = 52.60MHz
- -2 SAME AS -1 EXCEPT
  Y1, Y2 ARE 7100351-1 (OMIT C3)
- -3 STD FOR OAR2040
  Y1 = 132.10MHz
  (3) Y2 & SWITCH CKT OMITTED
  Y1 PIN 1 GROUNDED

(3) COMPONENTS OMITTED FOR -3: AR1, C1-5, R1-6, R8, Q1,2 & Y2.
2. RESISTORS ARE ¼W, RESISTANCE VALUES ARE IN OHMS ±5%.
1. CAPACITORS ARE 50WVDC, CAPACITANCE VALUES ARE IN MF.

NOTE: UNLESS OTHERWISE SPECIFIED

-1	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
QTY PER ASSY					

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30' DECIMAL .X ± .1, .XX ± .03, .XXX ± .010 SURFACE √ MDCE SIZES PER ANSI B32.7

DRAFT	Lindberg	8/31/84
CHECK	R BADINER	9/6/84
APP'D	[illegible]	10/3/84
APP'D	[illegible]	10/3/84
RELEASE	[illegible]	10/2/84
		10-17-84

7100349
NEXT OR ASSOC ASSEMBLY

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

SCHEMATIC
PAN LOCAL OSC

SIZE C | PECM NO. 06994 | DWG NO. 7100549 | REV A

SCALE — | SHEET 1 OF 1

7100549 A

BITE GENERATOR

ASSEMBLY: 396-307

SCHEMATIC: 396-507

SECTION I

DESCRIPTION

1.1 General

The built-in test equipment (BITE) generator is an oscillator which provides an RF test signal for the antenna circuits when switched into the input. The BITE generator simulates the X, Y and Z antenna inputs. Switching circuitry in the antenna inputs disconnects the antennas during BITE testing.

1.2 Circuit Description.

Refer to schematic diagram 396-507 during the following discussion.

When the BITE CONTROL input at J1 is high, transistor Q1 is switched on. This forward biases Q2 providing +15V power to the oscillator, Q3.

Transistor Q3 is a crystal controlled Colpitts oscillator, providing a 10.24 MHz output to a class C amplifier, Q4. The output of Q4 is rich in harmonics, providing an RF signal at 10.24 MHz intervals across the receiver range.

The output of Q4 is shaped and attenuated, then input to a differential transformer, T1. One output of T1 is impedance matched by T2 and provides an X+Y testing output at J2. The Z testing output is delayed by coax W1, and attenuated, then output to the antenna circuits at J3.

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL [illegible]	DATE 6/20/84	TITLE	PARTS LIST 7100344
	APPVD [illegible]	DATE 6/18/84	BEARING PROCESSOR II	SHEET 1 OF 7 REV D
	CHECK M. Helm	DATE 6/19/84		MWO
	DRAWN Dan Duong	DATE 6/13/84		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	240-410	345-410		
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD	1. CD4011SE, RCA, MAY BE SUBSTITUTED, CD4011BE IS PREFERRED.				
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION			APPVD	DATE
A	CHANGE REF DESIGNATORS	CDK	7/27/84	B. BODIKER	7/30/84
B	INCORP ECN 5696 EFF: S/N 001 & ON	CDK	7/27/84	B. BODIKER	7/30/84
C	INCORP ECN 5770 EFF: S/N 001 & ON	KD	8/27/84	B. BODIKER	9/4/84
D	INCORP ECN 6136, EFF: 4-62603 & ON.	MAR	3-12-86	L. CHAVEZ	3/17/86

FORM 161 A

7100344 SH 2 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	BRG PROC II		X						
2										
3										
4										
5	7100244-1	PWB		1						
6	7100544	SCHEMATIC		REF						
7										
8	7100705-1	CRYSTAL UNIT		1						Y1
9										
10										
11	LF347N	OPER AMPL	NATIONAL	4						AR1,4,6,7,
12	LF398N	OPER AMPL	NATIONAL	4						AR2,5,8,9
13	LM358N	OPER AMPL	NATIONAL	1						AR3
14										
15										
16	DM5CC220J	CAP MICA 22PF	ELMENCO	1						C1
17	DM5CC100J	CAP MICA 10PF	ELMENCO	1						C2
18	C320C104K5R5CA	CAP, CER, .1µF	KEMET OR EQ	37	C3-12,14-17,20,21,24-28,30-32,35,36, 41-43,48-50,54,58,61,62,64					
19	T350A105K035AS	CAP, TA 1µF	KEMET	2						C13, 29
20	BA2B333	CAP, MYL, .033µF	IMB	5						C18, 19, 33, 34, 44
21	C315C102K2R5CA	CAP, CER, .001µF	KEMET	8						C22, 23, 37, 65 38, 39, 40, 56
22	A2B473	CAP, MYL, .047µF	IMB	1						C45

7100344 SH 3 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23	BA2B103	CAP, MYL, .01µF	IMB	1						C46
24	T350E106K025AS	CAP TA 10µF 25V	KEMET	1						C47
25	230B1B474K	CAP MYL, .47µF	ELECTRO CUBE	4						C51, 52, 57, 59
26	BA2B104	CAP MYL, .1µF	IMB	4						C53, 55, 60, 63
27	106RLR025M	CAP, ALEL 10µF	ILLINOIS CAP	8						C66-71, 74, 75
28	226RLR016M	CAP. ALEL 22µF	ILLINOIS CAP	2						C72, 73
29										
30										
31										
32										
33										
34	IN4148	DIODE		48						CR1-9, 11-49
35	5082-4494	DIODE	H.P.	1						CR10
36	IN4001	DIODE		9						CR50-58
37										
38										
39										
40										
41	609-1627	CONN	T&B ANSLEY	1						J2
42	609-2027	CONN	T&B ANSLEY	1						J3
43	1-102584-0	CONN	AMP	1						P1
44										

7100344
SH 4 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
45										
46										
47	MPS6521	TRANSISTOR	MOTOROLA	2						Q1, 2
48	LM176	TRANSISTOR	NATIONAL	3						Q3, 4, 5
49										
50										
51										
52										
53	100K	RES. CARB FILM 1/8 W 5%		17					R1-3, 6-9, 15, 20, 29, 33 44, 47, 60, 93, 96, 110	
54	1M			5						R4, 22, 27, 53, 112
55	100Ω			1						R5
56	10K			11					R10, 28, 36, 39, 56, 63, 75, 92, 106, 117, 121	
57	18K			1						R11
58	47K			2						R12, 43
59	20K			4						R13, 14, 45, 46
60	130K			2						R16, 48
61	22K			6						R17, 18, 25 49, 50, 55
62	150K			1						R19
63	33K	RES. CARB FILM 1/8 W 5%		7						R21, 31, 32, 40 51, 58, 59
64	RN55C2003F	RES, 200K 1%		5						R23, 52, 68, 69, 105
65	RN55C4021F	RES, 4.02K 1%		2						R24, 54
66	62W-1-104	RES, VAR, 100K	BOURNS	6						R26, 87, 94 103, 114, 115

FORM 102

7100344
SH 5 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
67	2.2 M	RES, CARB FILM 1/8 W 5%		2						R30,57
68	3262W-1-103	RES, VAR POT 10K	BOURNS	2						R34,61
69	6.8K	RES, CARB FILM 1/8 W 5%		2						R35,62
70	220Ω	↕		6						R37,38,64 65,111,122
71	18K	↕		1						R41
72	2.2K	RES, CARB FILM 1/8 W 5%		1						R42
73	RN55C1003F	RES, 100K, 1%		8						R66,67,97,98 107,108,118,119
74	330Ω	RES, CARB FILM 1/8 W 5%		13						R70-74, 77-84
75	4310R-101-104	RES, NETWORK 100K	BOURNS	1						R76
76	68K	RES, CARB FILM 1/8 W 5%		1						R85
77	200K	RES, CARB FILM 1/8 W 5%		1						R86
78	RN55C4022F	RES, 40.2K, 1%		2						R88,91
79	470K	RES, CARB FILM 1/8 W 5%		1						R89
80	RN55C1962F	RES, 19.6K 1%		1						R90
81	3.3M	RES, CARB FILM 1/8 W 5%		3						R95,104,116
82	RN55C1002F	RES, 10.0K, 1%		4						R99, 100, 101, 102
83	RN55C5622F	RES, 56.2K, 1%		2						R109,120
84	RN55C2213F	RES, 221K, 1%		1						R113
85	RN55C1210F	RES, 121Ω 1%		1						R123
86	RN55C8450F	RES. 845Ω 1%		1						R124
87										
88										

7100344 SH 6 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -/					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
89														
90														
91	MC14094BCP	INT CKT	MOTOROLA	3										U1, 2, 3
92	CD4023BE		RCA ONLY	1										U4
93	MC14024BCP		MOTOROLA	1										U5
94	MC14093BCP		MOTOROLA	1										U6
95	CD40163BE		RCA	6										U7-9, 12-14
96	MC14077BCP		MOTOROLA	1										U10
97	MC14013BCP			1										U11
98	MC14536BCP			1										U15
99	MC14046BCP		MOTOROLA	2										U16, 17
100	CD40116E ▷1		RCA	2										U18, 19
101	MC14016BCP		MOTOROLA	1										U20
102	MC14054BCP	INT CKT	MOTOROLA	1										U21
103														
104														
105														
106														
107	MC78L12ACP	VOLTAGE RGLTR	MOTOROLA	1										VR1
108	MC78L05ACP			2										VR2, 5
109	MC79L12ACP			1										VR3
110	MC79L05ACP	VOLTAGE RGLTR	MOTOROLA	1										VR4

7100344

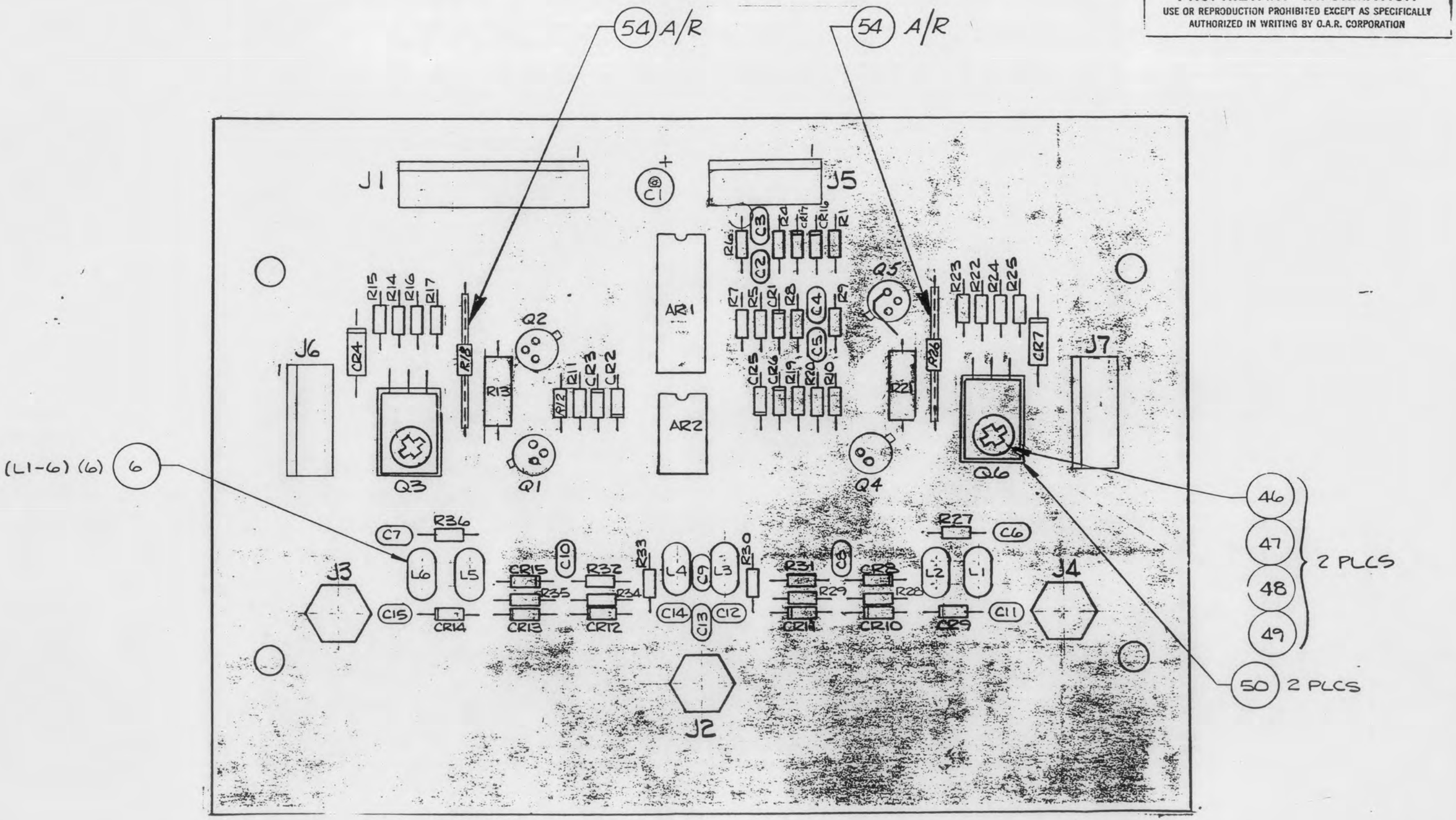
SH 7 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -/					REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
111	LM217H	VOLTAGE RGLTR	MOTOROLA	1										VR6
112	IN 7606	REF DIODE 10V		1										VR7
113														
114														
115	7117-30AP	TRANSIPAD	THERMALLOY	1										
116	S203	EJECTOR	SCANBE	2										
117														
118														
119														
120														
121														
121														
122														
123														
124														
125														
126														
127														
128														
129														
130														
131														

RF AND POWER SWITCH BOARD

ASSEMBLY: 396-300

SCHEMATIC: 396-500



RF and Power Switch

396-300

DWG NO. 7100544 SH 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
A	DIRECT DWG CHANGE: REASSIGN REF DESIGN CDK 7/10/84	7/30/84	R.ZOOKER
A#1	ADDED PI GND NOTATIONS. NO HDWR CHANGE KD 2/4/85	2/15/85	R.ZOOKER

3. UNMARKED DIODES ARE IN4148.
2. RESISTORS ARE 1/8W ±5%, RESISTANCE IS IN OHMS.
1. CAPACITANCE IS IN MICRO-FARADS

NOTE: UNLESS OTHERWISE SPECIFIED

QTY PER ASSY	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √ HOLE SIZES PER AN010387

7100344

NEXT OR ASSOC ASSEMBLY

DWN BY: Ahed 6.8.84
CHECK: M. Herm 6/19/84
APVD: R. Brown 6/17/84
APVD: T. Hamm 12 ec 6/19/84
RLSE: 6/19/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

BEARING PROCESSOR II

SIZE D | FSCM NO. 06994 | DWG NO. 7100544 | REV A

SCALE | SHEET 1 OF

7100544 A

DWG NO. 7100544 SH 2

P1: MOD 40, DATA 60, A GND 37, A GND 38

P1: RCVR, VIDEO 28, AGND 32, PLL VIDEO 30, A GND 31

C39 .001, C40 .001, R66 100K 1%, R67 100K 1%, R68 200K 1%, R69 200K 1%

CR17 CR18 CR19 CR20 CR21 CR22

Q3 J176, Q4 J176, Q5 J176

B C41 .1, C C42 .1, A C43 .1

CW R85 68K, R86 200K, R87 100K, R88 40.2K 1%, R89 470K, -12V

C44 .033 MYL, R90 19.6K 1%, C45 .047 MYL, R91 40.2K 1%, C46 .01 MYL, +C47 10/25V, R92 10K, R93 100K

AR6-B LF347, AR6-A LF347, AR7-B LF347

R94 100K CW -5V, R95 3.3M, +12V C48 .1, AR7-A LF347

-5V D+5V C49 .1, C50 .1

R96 100K, R97 100K 1%, R98 100K, R99 10K 1%, R100 10K 1%, R101 10K 1%, R102 10K 1%

U20 4016B

A +5V U10,12 14,16, U21 4054B, -5V

F G H J

J2: DIR 13, WRT 11, A2 9, A1 7, AØ 5, N/C 14, DGND 15, DGND 16, DBØ 12, DB1 10, DB2 8, DB3 6, DB4 4, DB7 3, DB5 2, DB6 1

U18 CD4016, U19 CD4016

D+5V R75 10K, CR33

CR23 CR24 CR25 CR26 CR27 CR28 CR29 CR30 CR31 CR32

R70 R71 R72 R73 330 x4, R74 330

CR34 CR35 CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR43 CR44 CR45 CR46 CR47 CR48 CR49

R76 100K x4, R77 R78 R79 R80 330 x4, R81 R82 R83 R84 330 x4

+10V

J3: +15V 19, MOD 11, DATA 3, HTONE 9, VTONE 13, -15V 1, DIR 8, WRT 17, A2 15, A1 4, A0 2, D0 12, D1 16, D2 20, D3 18, D4 14, D5 5, D6 10, D7 6, GND 7

ANT

HTONE, VTONE, -15V

R103 100K CW -5V, R104 3.3M, C51 .47 MYL, R105 200K 1%, R106 10K

AR7-C LF347, R107 100K 1%, R108 100K 1%, C53 .1 MYL, R109 5.62K 1%, AR6-D LF347, R110 100K, C52 .47 MYL

R111 220, C56 .001, P1: VERT DC.

+12V C54 .1, C55 .1 MYL, NC, AR8 LF398, -12V

R112 1M, R113 221K 1%, R114 100K 45° CAL ADJ, C57 .47 MYL

A +5V R115 100K CW -5V, R116 3.3M, AR7-D LF347, R117 10K, C58 .1, -12V

R118 100K 1%, R119 100K 1%, C60 .1 MYL, C59 .47 MYL, R120 5.62K 1%, AR6-C LF347, R121 10K, C61 .1, C62 .1, -12V

NC +12V, C63 .1 MYL, AR9 LF398, R122 220, C65 .001, C64 .1, -12V

P1: HORIZ DC, A GND

D/4 K (T&H)

+15V CR51 IN4001, VR1 78L12ZA, VR2 78L05A, +12V, A+5V

CR50 IN4001, C66 10/25V, C67 10/25V, CR52 IN4001, C68 10/25V

-15V CR54 IN4001, VR3 79L12ZA, VR4 79L05A, -12V, -5V

CR53 IN4001, C69 10/25V, C70 10/25V, CR55 IN4001, C71 10/25V

GND GND +8V +8V, CR57 IN4001, VR5 78L05A, D+5V

CR56 IN4001, C72 22/16V, C73 22/16V

+15V CR58 IN4001, VR6 LM217H, +10V

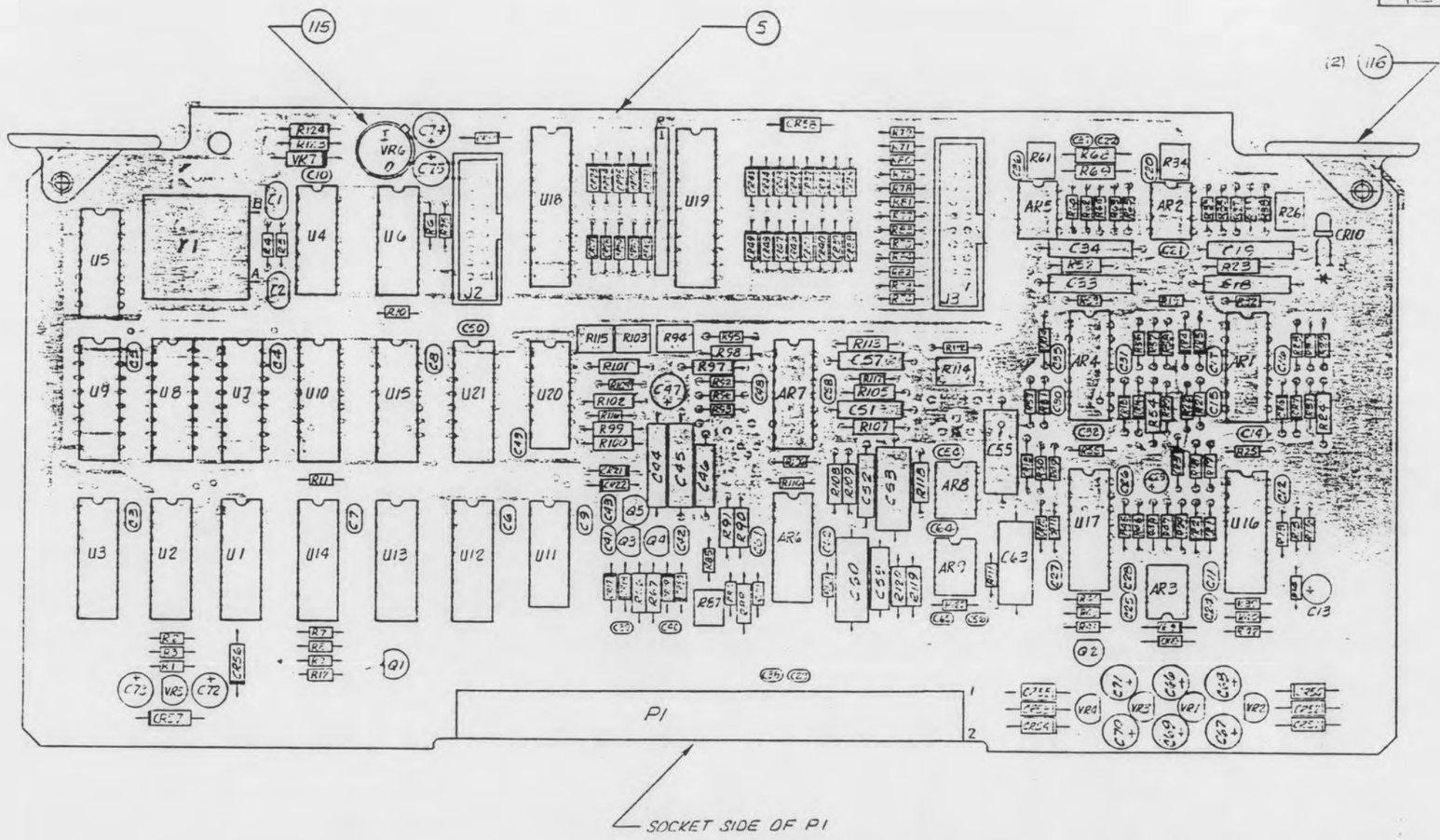
C74 10/25V, R123 121 1%, VR7 IN4766, C75 10/25V, R124 845 1%

LAST REF DES USED									
AR	C	CR	J	P	Q	R	U	VR	
9	75	58	3	1	5	124	21	7	
REF DES NOT USED									
			/						

SIZE	FSCM NO.	DWG NO.	REV
D	06994	7100544	A
SCALE:		SHEET	

7100544 A

DWG NO 7100344		SH 1	
REV	REVISIONS	DATE	APPROVAL
A	DIRECT DRIVING CHANGE, CHANGE PER DESIGN. DRC CDK 7-12-84	7/30/84	B.BUDNER
B	INCORP ECN 5696 EFFSN 001 & CN CDK 7/30/84	7/30/84	B.BUDNER
C	INCORP ECN 5770. EFFECTION #3 12/7/84	9/4/84	B.BUDNER
D	INCORP ECN 6136. MAR. EFF: 2-7/2-86	3/17/86	L.CHAVEZ



-1 BEARING PROCESSOR II

SEE SEPARATE PARTS LIST

3. BAG & TAG WITH P/N 7100344, DASH NO. & REVLTR.
2. FOR SCHEMATIC DIAGRAM SEE 7100544.
1. MOUNT ALL COMPONENTS FLUSH WITH BOARD SURFACE

ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR SPECIFICATION	QTY PER ASSY

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0° 30' DEC MAX ± .XX SURFACE √

NEXT ASSY	USED ON	QTY
345-410		

MATERIAL	FINISH
KE-DURAY	CLEAR

DRAWN	DATE
M. NELM	9/17/84

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

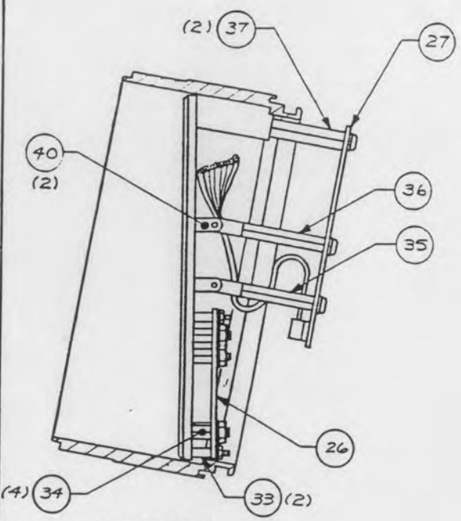
CAD

BEARING PROCESSOR II

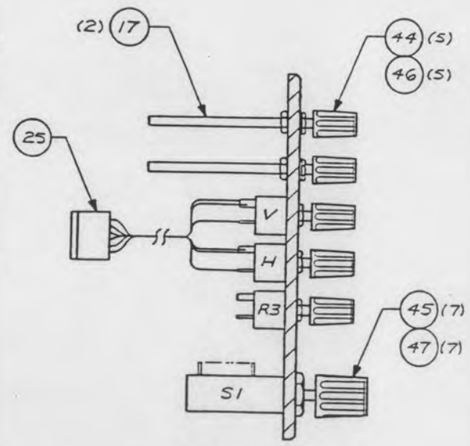
SIZE 004 7100344

DWG NO. 7100400 SH 1 J

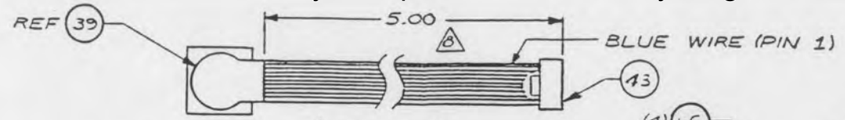
REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
H	INCORP ECN 6008 EFF: 3045 SW001&CN; 2040 SW001&CN: PREVIOUS RELEASE P.L. ONLY KD4-10-85	4/10/85	B. BODIKER
J	INCORP ECN 6155 EFF: 001 & CIJ JT 7/24/85	7/24/85	B. BODIKER



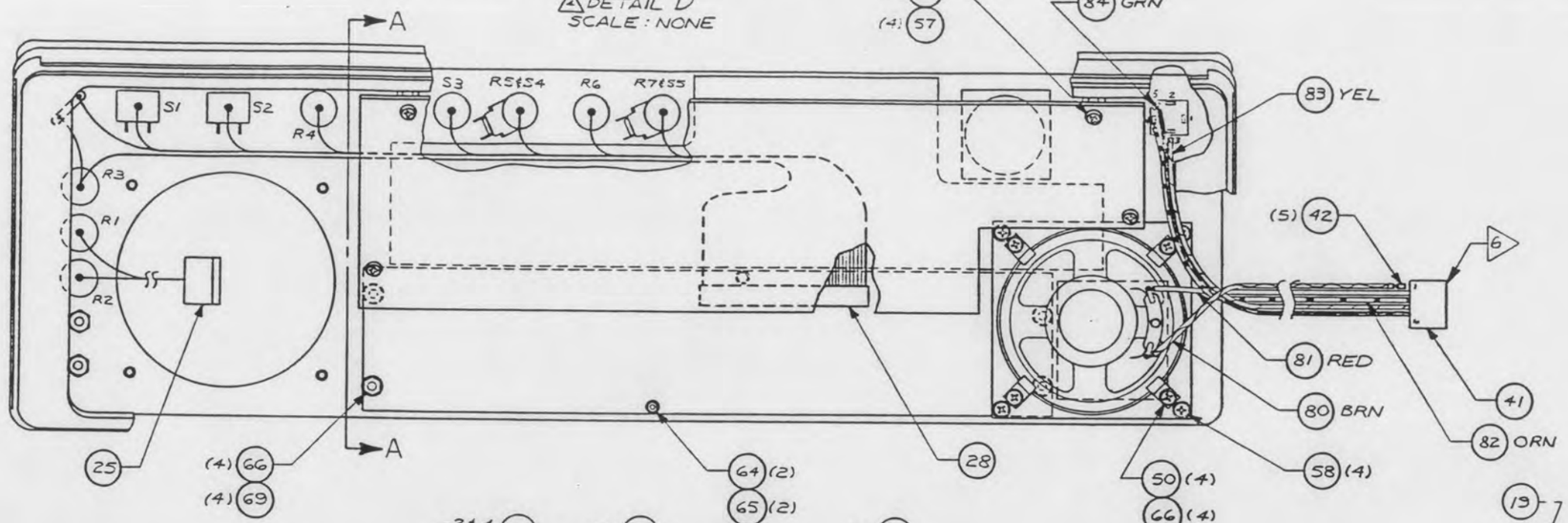
SECTION A-A

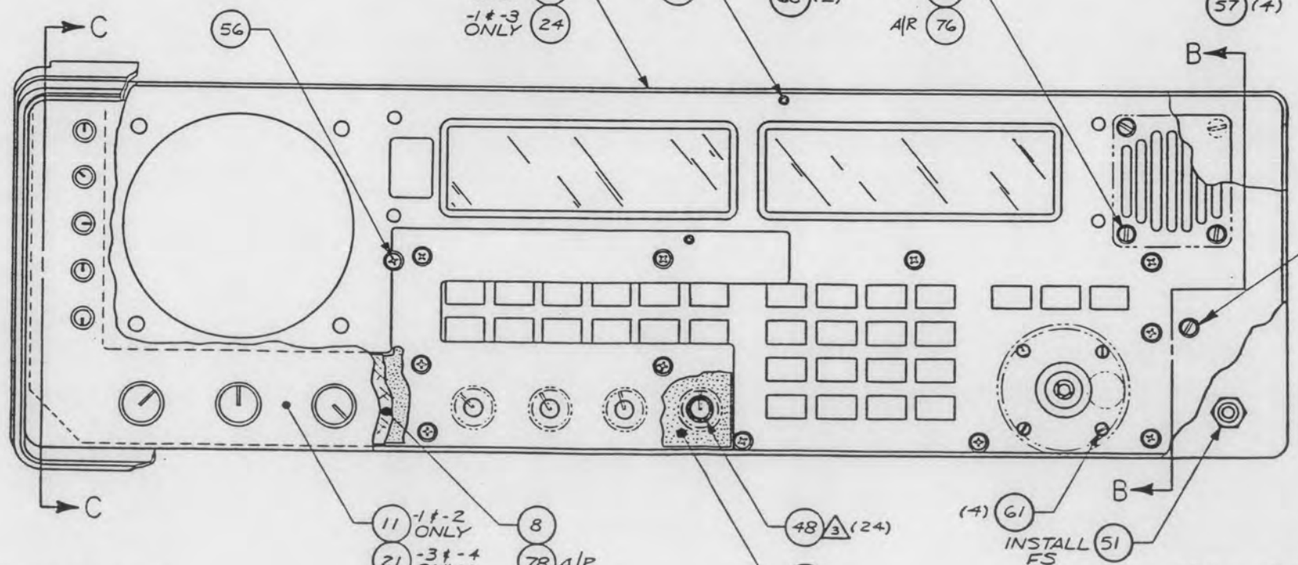


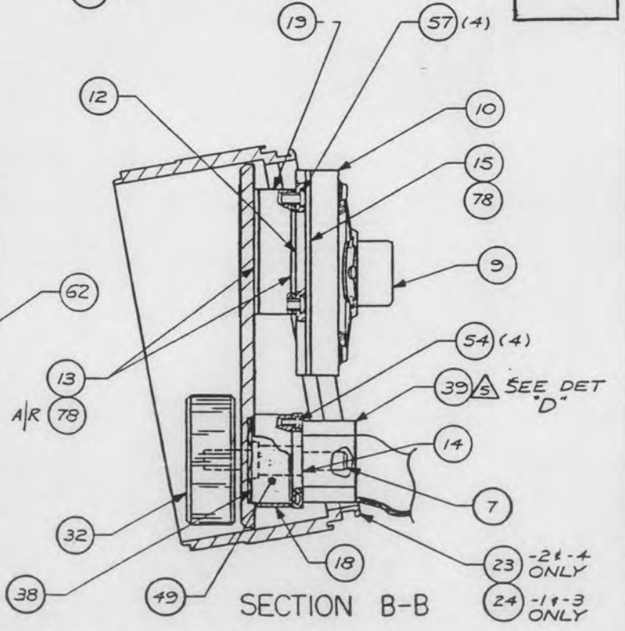
SECTION C-C
(BEZEL REMOVED FOR CLARITY)



△4 DETAIL D
SCALE: NONE







SECTION B-B

SEE SEPARATE PARTS LIST

QTY PER ASSY	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
			LIST OF MATERIAL		

△8 CUT CABLE SUPPLIED TO DIM SHOWN & INSTALL ITEM 43.
7. USE SHRINK TUBING ITEM 79 AT WIRE TERMINATIONS WHERE APPLICABLE.
△6 CABLE LENGTH TO BE APPROX 7.50 LONG.
△5 ASSEMBLE OPTICAL ENCODER (ITEM 39) PER PROCEEDURE 7100936
△4 PRIOR TO ASSEMBLY OF OPTICAL ENCODER (ITEM 39) CUT CONNECTOR STRIP TO SIZE INDICATED. SEE DETAIL D.
△3 INSTALL WASHER BETWEEN E.L. SHIM & E.L. STRIP. SECOND WASHER MAY OR MAY NOT BE USED.
2. APPLY ITEM 75 LOCTITE TO ALL SCREWS WHERE RETAINING HARDWARE IS NOT USED.
1. IDENTIFY BY BAGGING AND TAGGING WITH PART NO. AND REV LTR.
NOTE: UNLESS OTHERWISE SPECIFIED

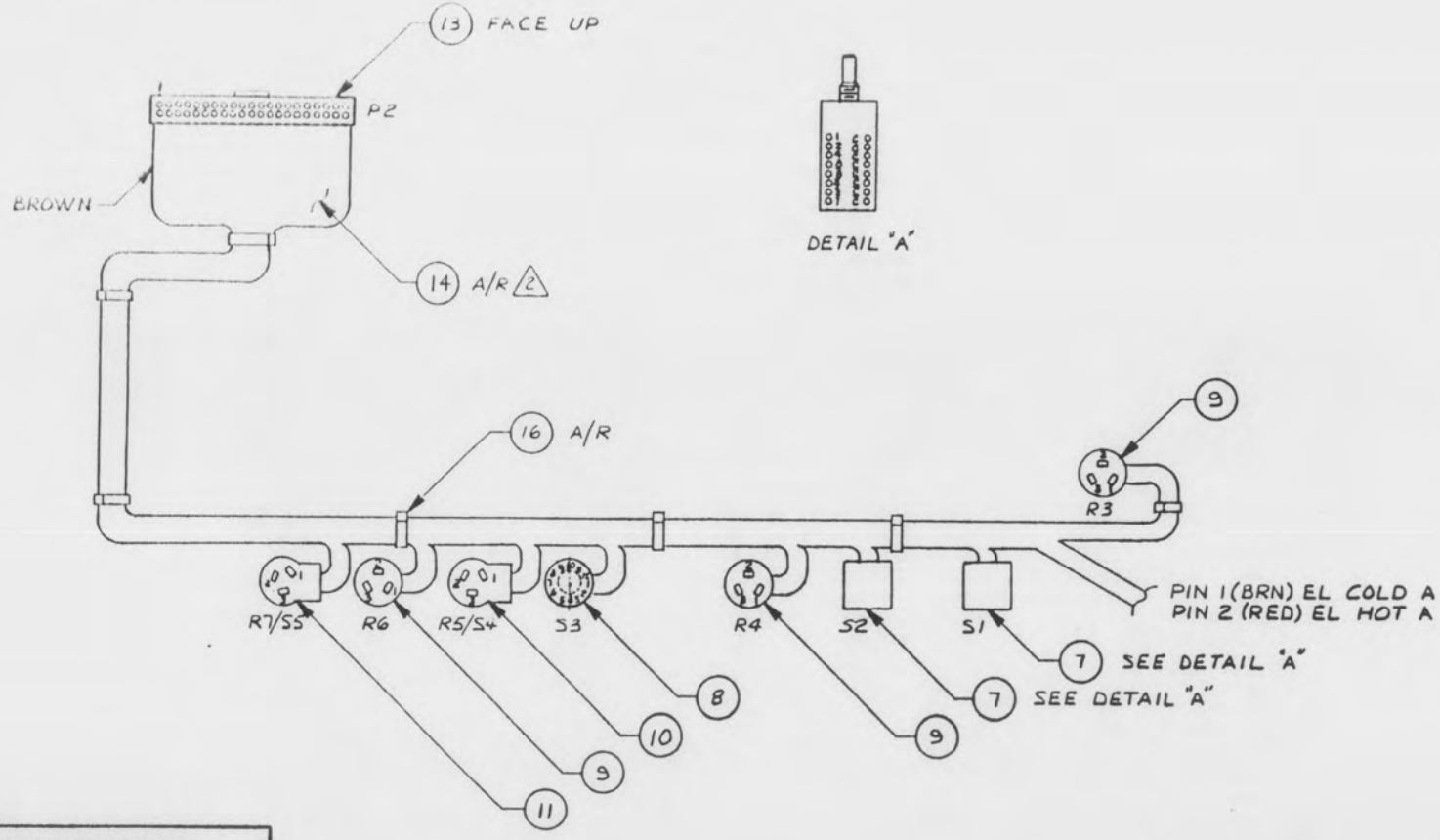
345-410	
240-410	
NEXT OR ASSOC ASSEMBLY	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: ANGLES ± 0°-30' DECIMAL .X = ±.1, .XX = ±.03, .XXX = ±.010 SURFACE √
HOLE SIZES PER AN010387

DWN BY: A. ORUELAS	4/26/84	OCEAN APPLIED RESEARCH CORP (OAR) A DIVISION OF GENERAL INDICATOR CORP
CHECK: B. BODIKER	4/10/85	FRONT PANEL OAR 2040 & 3045
APVD: E. [illegible]	5/2/85	
APVD: T. Mahaffey	5/1/85	
[illegible]	5/2/85	
RLSE		SIZE D FSCM NO. 06994 DWG NO. 7100400 REV J
		SCALE - / / SHEET 1 OF 2

7100400 J

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL



SEE SEPARATE PARTS LIST

3. BAG & TAG WITH PART NO. DASH NO. & REV LTR.
2. ROUTE WIRES TO CONTROLS USING HARNESS BOARD 7100613.
1. WIRE CABLE PER SCHEMATIC 7100522.

NOTE: UNLESS OTHERWISE SPECIFIED

QTY PER ASSY	ITEM	PART NUMBER	DESCRIPTION	MATERIAL OR MANUFACTURER	NOTE
	-1		LIST OF MATERIAL		

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES, TOLERANCES: ANGLES ± 0°30' DECIMAL .X = ±.1 .XX = ±.03 .XXX = ±.010 SURFACE √ HOLE SIZES PER ANSI B32.1

7100400
NEXT OR ASSOC ASSEMBLY

DRAFT	J TAPLEY	7/8/85
CHECK	B. BODIKER	9/9/85
APP'D	D. May	9/11/85
APP'D	[illegible]	9/10/85
	[illegible]	9/10/85
RELEASE	[illegible]	7/11/85

OCEAN APPLIED RESEARCH CORP
A DIVISION OF GENERAL INDICATOR CORP

CABLE, ANALOG CONTROL

SIZE	FSCM NO.	DWG NO.	REV
C	06994	7100464	

SCALE ~ SHEET 1 OF 1

7100464

4 3 2 1

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL Cordis	DATE 9/10/85	TITLE CABLE, ANALOG CONTROL	PARTS LIST 7100464
	APPVD D. Mag	DATE 9/11/85		SHEET 1 OF 2 REV
	CHECK B. BODIKER	DATE 9/6/85		MWO
	DRAWN J TAPLEY	DATE 7/8/85		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100400	7100465		
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE

7100464
SH 2 OF 2

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	CABLE, ANALOG CONTROL		X						
2										
3	7100613	HARNESS BOARD		REF						
4	7100522	SCHEMATIC		REF						
5										
6										
7	7100752-1	SWITCH		2						S1, S2
8	SIMD30-01-1-AJN	SWITCH	GRAYHILL	1						S3
9	GA4T032S103UA	RES, VAR 10K	A-B	3						R3, 4, 6
10	GH4T032S103UA	RES, VAR W/SW 10K	A-B	1						R5/S4
11	GS4T032S103AA	RES, VAR W/SW 10K	A-B	1						R7/S5
12										
13	609-4030	CONNECTOR	ANSLEY	1						P2
14	3581/40	RIBBON CABLE 40 LINE	ALPHA OR EQ	A/R						18"
15										
16	T18S	TY-WRAP	TYTON	A/R						
17										
18										
19										
20										
21										
22										

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL Cindy	DATE 9/23/85	TITLE FRONT PANEL INTERFACE BD	PARTS LIST 7100315
	APPVD	DATE		SHEET 1 OF 4 REV D
	CHECK B. BODIKER	DATE 3/21/84		MWO
	DRAWN MW	DATE 1/2/84		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	7100400			
QTY REQUIRED THIS RELEASE	FINAL ASSY	240-410	345-410		
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION		APPVD DATE
A	SEE QTY CHG ITEMS 9, 12, 42 & 45. SEE P/N CHG ITEM 41. ADDED ITEMS 15, 16, 20, 53, 57 & 58.	MW 1-2-84	
B	INCORP ECN 5469	KD 3/14/84	B. BODIKER 3/21/84
C	INCORP ECN 5518	MW 4/10/84	B. BODIKER 4/10/84
CR2	INCORP ECN 5533 EFF: 001 & ON		
D	INCORP ECN 5588 EFF: 001 & ON	SJ 6/4/85	B. BODIKER 9/18/85

7100315 SH 2 OF D

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	INTERFACE BD		X						
2										
3	7100515	SCHEMATIC		REF						
4	7100215-1	PWB		1						
5										
6	7100433-1	CABLE (40)		1						J1/W1
7	7100433-2	CABLE (20)		1						J4/W2
8										
9	C320C104K5R5CA	CAP, CER 0.1μF	KEMET OR EQ	23						C1,3,5-17,19,24-26,28,29,34,36
10	337RMR025M	CAP, AL 330μF/25V	ILLINOIS OR EQ	3						C30,33,37
11	107RMR025M	100μF/25V		2						C32,35
12	226RLR016M	22μF/16V		3						C2,4,23
13	105RLR050M	CAP, AL 1μF/50V	ILLINOIS OR EQ	2						C18,20
14	BA2C224	CAP, MYL .22μF	IMB	1						C31
15	106RMR025M	CAP, AL 10μF/25V	ILLINOIS OR EQ	3						C21,22,38
16	C315C182K1R5CA	CAP, CER, 1800pF	KEMET OR EQ	1						C27
17	609-1027	CONNECTOR	ANSLEY OR EQ	1						J5
18	609-2027	CONNECTOR	ANSLEY OR EQ	1						J6
19	609-4027	CONNECTOR	ANSLEY OR EQ	1						J2
20	22-11-2062	CONNECTOR	MOLEX	1						J3
21										
22										

7100315 SH 3 OF 0

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23	LM358N	IC OAER AMPL	NAT OR EQ	2						AR2, AR3
24	CD4555BE	IC REGISTER	RCA OR EQ	1						U8
25	CD4013BE	IC FF	RCA OR EQ	1						U9
26	CD4516BE	IC UP/DN	RCA OR EQ	2						U10, 11
27	MM74C244N	IC BUFFER	Nat. or EQ	3						U4, 5, 12
28	MM74C922N	IC ENC		2						U6, 7
29	MM74C138N	IC DECOD		1						U1
30	LM383T01	IC AMPL		1						AR1
31	ADC0805CCN	IC A-D		1						U3
32	MM74C02N	IC GATES	Nat. or EQ.	1						U2
33	MC78L05ACP	IC V REG	MOTA or EQ	1						VR1
34	E613-E0003	DC-AC CONV	ENDICOTT RESEARCH	2						A1, A2
35										
36										
37	MJE 800	XSTR	MOTOROLA	2						Q1, 2
38	IN4001	DIODE		3						CR1-3
39										
40										
41	4308R-101-104	100K NETWORK	BOURNS OR EQ	4						R1-4
42	100K	RES, 1/8W 5%	CARBON FILM	4						R24, 25, 28, 30
43	22K	RES, 1/8W 5%	CARBON FILM	2						R21, 26
44	270Ω	RES, 1/8W 5%	CARBON FILM	1						R27

FORM 102

7100315 SH 4 OF 10

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
45	1K	RES 1/8W 5%	CARBON FILM	3						R13,23,29
46	10K	↑ ↑	↑	10						R5,7,8,12,14-17, 32,33
47	3.3K			2						R9,10
48	6.8K			1						R6
49	10Ω	1/8W 5%	↓	1						R19
50	270Ω	1/2W 5%	CARBON FILM	1						R18
51	1.0Ω G-3	RES 1Ω 2¼W, 5%	DALE OR EQ	1						(RW80) R31
52	3262X-1-103	RES, VAR, 10K POT	BOURNS OR EQ	1						R11
53	TBD	RES, 1/8W, 5%	CARBON FILM	2						R20,22
54										
55										
56										
57	6073B	HEATSINK	THERMALLOY	3						
58	60-11-8302-1674	INSULATOR	CHOMERICS	3						
59										
60	4-40 x 3/8	SCREW	PAN HD PHILLIPS	3						
61	B52200F003	COMP WASHER	MOTOROLA	3						
62	NO. 4	LOCK	SPLIT	3						
63	4-40	NUT	SMALL PATTERN	3						
64										
65	KIT-1C	ADHESIVE	HYSOL	A/R						
66										

OCEAN APPLIED RESEARCH CORPORATION San Diego, Cal. 92121	REL	DATE	TITLE	PARTS LIST 7100400
	APPVD [illegible]	DATE 5/18/84	FRONT PANEL OAR 2040 & 3045	SHEET 1 OF 5 REV J
	CHECK B BODIKER	DATE 5/18/84		MWO
	DRAWN TRUCHAN	DATE 5/17/84		

MANUFACTURING WORK ORDER NO.	NEXT ASSY	240-410	345-410		
QTY REQUIRED THIS RELEASE	FINAL ASSY				
RELEASE DATE MTL REQD					
TOTAL PARTS COST THIS RELEASE					

REV	DESCRIPTION	APPVD	DATE
E	REWRITTEN WITH CHANGE (DIR DWG CHNG) REVISED ITEM NOS DELETING PANEL SUBASSY PARTS AND ADDING PANEL SUBASSY NOS. (SEE OBSOLETE REV C FOR WAS COND) DISPN: NONE EFF: 1 & ON (NO REWORK REQUIRED)	UKA BXH	5/17/84 5/18/84
F	INCORP ECN 5671 EFF 001 & ON KD 4-10-85	B. BODIKER	4/10/85
G	INCORP ECN 5916; EFF: 3045 S/N 031 & ON; 2040 S/N 016 & ON KD 4-10-85	B. BODIKER	4/10/85
H	INCORP ECN 6008 EFF: 3045 S/N 001 & ON; 2040 S/N 001 & ON KD 4-10-85	B. BODIKER	4/10/85
J	INCORP ECN 6155 EFF: 001 & ON JT 7/24/85	B. BODIKER	7/24/85

7100400 SH 2 OF J

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
1	-1	FRONT PANEL		X									PROD (2040)
2	-2	FRONT PANEL			X								PRE PROD (2040)
3	-3	FRONT PANEL				X							PROD (3045)
4	-4	FRONT PANEL					X						PRE PROD (3045)
5	7100936	PROCEDURE FOR ASSY OF OPTICAL ENCODER		REF	REF	REF	REF						
6	7100800	DIAGRAM		REF	REF	REF	REF						
7	7100013-1	ENCODER SHAFT		1	1	1	1						
8	7100014-1	EL SHEET		1	1	1	1						
9	7100016-1	SPEAKER		1	1	1	1						
10	7100017-1	SPKR HOUSING		1	1	1	1						
11	7100020-1	OVERLAY		1	1	-	-						(2040 BLK)
12	7100030-1	SPKR BASE PLT		1	1	1	1						
13	7100031-1	GSKT, SMALL		2	2	2	2						
14	7100032-1	MTG BASE		1	1	1	1						
15	7100047-1	GSKT, LARGE		1	1	1	1						
16													
17	7100081-1	BUSHING		2	2	2	2						
18	7101007-1	BEARING BLOCK		1	1	1	1						
19	7101008-1	SPKR BLOCK		1	1	1	1						
20													
21	7101033-1	OVERLAY		-	-	1	1						(3045 BLK)
22	7101034-1	EL SHIM		1	1	1	1						

7100400 SH 3 OF J

ITEM NO	PART NO	DESCRIPTION	MATERIAL OR MANUFACTURER	QTY PER ASSEMBLY -1	-2	-3	-4	REL QTY REQ	QTY ISSD	BAL REQ	UNIT COST	TOTAL LINE COST	REMARKS
23	7100444-1	PNL SUBASSY		-	1	-	1						(MACH BEZEL)
24	7100447-1	PNL SUBASSY		1	-	1	-						(CAST BEZEL)
25	7100434-1	VER/HORIZ CABLE		1	1	1	1						
26	7100314-1	DISPLAY		1	1	1	1						
27	7100315-1	FP INTERFACE		1	1	1	1						
28	7100464-1	ANALOG CONT		1	1	1	1						
29													
30													
31													
32	KN-175185-1/4	KNOB	ALCO	1	1	1	1						
33	8003-55-0800	STANDOFF	AMATOM	2	2	2	2						1/8 DIA X 5/16 0-80 THD
34	8102-55-0440	STANDOFF	AMATOM	4	4	4	4						3/16 HEX X 1/4 4-40 THD
35	8111-55-0440	STANDOFF	AMATOM	1	1	1	1						3/16 HEX X 1 4-40 THD
36	8113-55-0440	STANDOFF	AMATOM	1	1	1	1						3/16 HEX X 1 1/8 4-40 THD
37	9743-55-0440	M/F STANDOFF	AMATOM	2	2	2	2						1/4 HEX X 1 4-40 M/F
38	W1159-013	SPRING WSHR	ASSOC SPRING	1	1	1	1						
39	HEDS-5000-A06	OPTICAL ENCODER	HEWLETT PACKARD	1	1	1	1						
40	333	M/F HINGE	KEYSTONE	2	2	2	2						3/16 DIA X .625 4-40 M/F
41	22-01-3067	CONNECTOR	MOLEX	1	1	1	1						
42	08-55-0102	CONTACT	MOLEX	5	5	5	5						
43	609-1030	CONNECTOR	ANSLEY	1	1	1	1						
44	26-10-31-3	KNOB	PWR DYNAMICS	5	5	5	5						