HF/VHF/UHF Receiver

RA 1794A

Technical Manual

Racal Communications Limited

Western Road, Bracknell, RG12 1RG, England
Tel: Bracknell (0344) 483244 Telex: 848166

Prepared by Group Technical Handbooks Department, Racal Group Services Limited

RACAL

The Electronics Group

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LETHAL VOLTAGE WARNING

VOLTAGES WITHIN THIS EQUIPMENT ARE SUFFICIENTLY HIGH TO ENDANGER LIFE.

COVERS MUST NOT BE REMOVED EXCEPT BY PERSONS QUALIFIED AND AUTHORISED TO DO SO AND THESE PERSONS SHOULD ALWAYS TAKE EXTREME CARE ONCE THE COVERS HAVE BEEN REMOVED.

RESUSCITATION

TREATMENT OF THE NON-BREATHING CASUALTY

1 SHOUT FOR HELP. TURN OFF WATER, GAS OR SWITCH OFF ELECTRICITY IF POSSIBLE

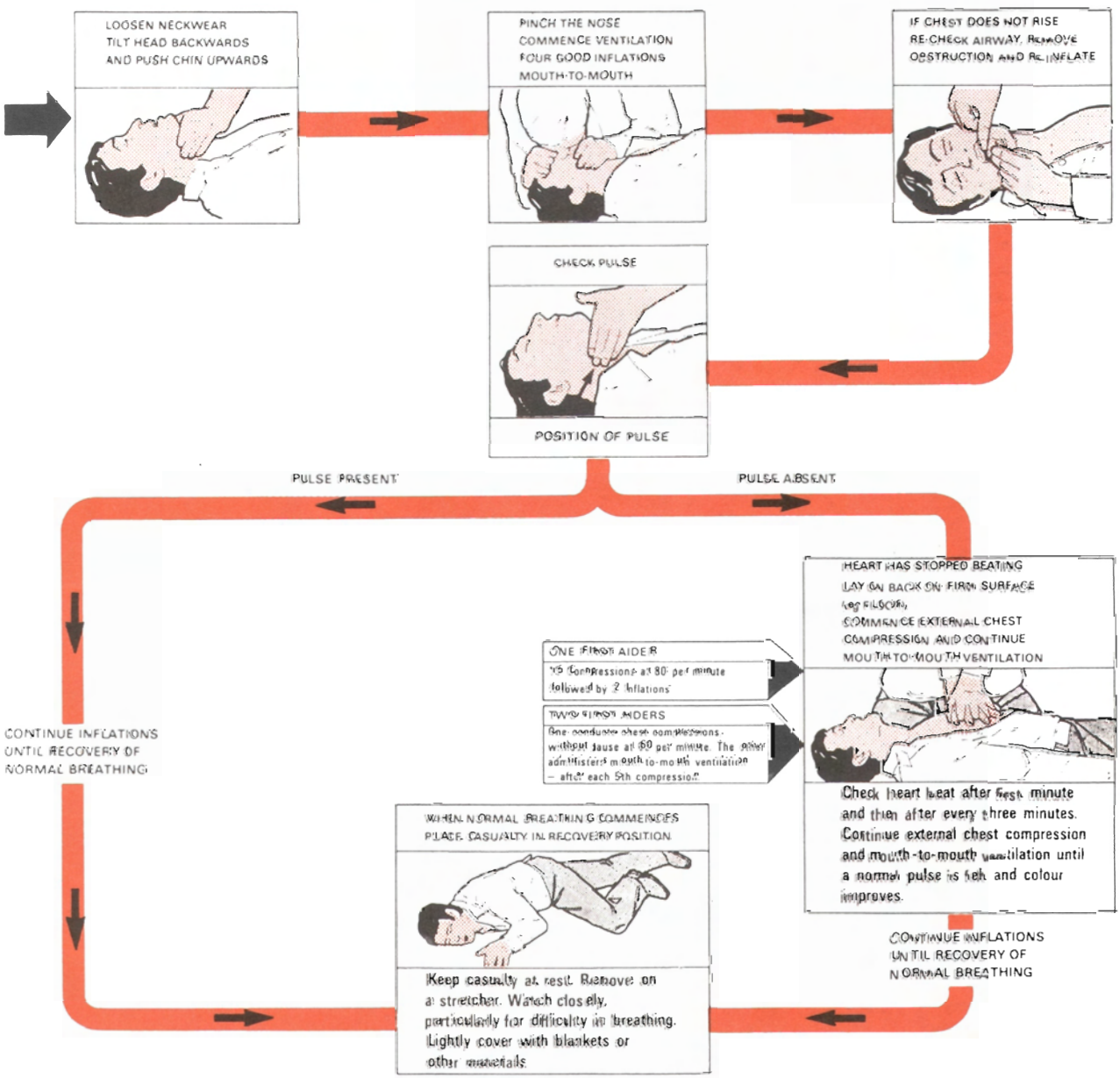
Do this immediately. If not possible don't waste time searching for a tap or switch.

2 REMOVE FROM DANGER: WATER, GAS, ELECTRICITY, FUMES, ETC.

Safeguard yourself when removing casualty from hazard. If casualty still in contact with electricity, and the supply cannot be isolated, stand on dry non-conducting material (rubber mat, wood, linoleum).
Use rubber gloves, dry clothing, length of dry rope or wood to pull or push casualty away from the hazard.

3 REMOVE OBVIOUS OBSTRUCTION TO BREATHING

If casualty is not breathing start ventilation at once.



SEND FOR DOCTOR AND AMBULANCE

DOCTOR	AMBULANCE	HOSPITAL	Nearest First Aid Post
TELEPHONE	TELEPHONE	TELEPHONE	

HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

'POZIDRIV" SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trade mark of G.K.N. Screws and Fastners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

RACAL COMMUNICATIONS LTD

RA1794A HF/VHF/UHF RECEIVER

TH2449/3

Amendment 1 - Issue 10 - February 1992

CR 81248 - CR 81629

CHAPTER 11

Components 5

R7: Amend 4k7 and 913490 to read:

5k6 and 918128

Components 7

D4: Amend BZX70C24 and 926830 to read:

BZT03C24 and 947780

Figure 17.4

R7: Amend Value to read: 5k6

Diode Table amend D4 to read: BZT03C24

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RA1794A HF/VHF/UHF RECEIVER

TH2449/3

Amendment 2 - Issue 10 - September 1992

CR 84072

Remove and Destroy		Insert	
Chapter 21			
Pages	11/12	Pages	11/12
	13/14		13/14
	15/16		15/16
	17/18		17/18
	29/30		29/30
	35/36		35/36
	43/44		43/44

ROM Devices & Test Switch Buffer

34. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(3) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(4) Set the front panel POWER switch to ON.

(5) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- C690/H
0V	-	Negative end of C8	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(6) Connect the signature analyser probe, in turn, to the points given in table 2 and check that correct signatures are obtained.

RAM and EAROM Devices

35. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

Table 2: ROM Device and Test Switch Buffer Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC pin No.)					
		ML6	ML10	ML11	PD1	PD2/3	ML14
A0	9270	25	1	-	8	8	-
A1	71H0	26	2	-	7	7	-
A2	1AF5	27	-	1	6	6	-
A3	HF6A	28	-	2	5	5	-
A4	825P	29	3	3	4	4	-
A5	U801	30	4	4	3	3	-
A6	C9HC	31	15	16	2	2	-
A7	1511	32	-	-	1	1	-
TPA	0000(F)	34	17	17	-	-	-
$\overline{MRD}$	0000(F)	7	5,6	-	-	-	-
$\overline{MWR}$	C690/H	35	-	6	-	-	-
$\overline{AV}$	0000(F)	-	-	5	-	-	-
0V	0000/L	20	9,14	9,14	12	12	8
+5V	C690/H	16,40	16,18	18	21,24	21,24	16
A8	178U	-	7	-	23	23	-
A9	U9U7	-	8	-	22	22	-
A10	0548	-	-	7	19	19	-
A11	HAA7	-	-	8	18	18	-
$\overline{CS0}$	P254	-	13	-	20	-	-
$\overline{CS1}$	H6AA	-	12	-	-	20(PD2)	-
$\overline{CS2}$	34UP	-	11	-	-	20(PD3)	-
$\overline{CS3}$	C690(F)	-	10	-	-	-	1
D0	U08P	15	-	-	-	-	-
*D1	33H6	14	-	-	-	-	-
*D2	4H7H	13	-	-	-	-	-
*D3	210A	12	-	-	-	-	-
*D4	SU5P	11	-	-	-	-	-
*D5	H7H2	10	-	-	-	-	-
*D6	599P	9	-	-	-	-	-
*D7	H313	8	-	-	-	-	-

* These signatures are dependant upon the software fitted in the equipment. If these signatures are required, they can be provided from analysis of a known working receiver having the same program number and software issue. The signatures relate to P82892 Issue 02.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- 755U/H
0V	-	Negative end of C8	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 3 and check that correct signatures are obtained.

Table 3: RAM and EAROM Device Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC PIN No.)								
		ML6	ML10	ML11	ML4	ML5	ML12	ML14	ML2	ML3
0V	0000/L	20	9,14	9,14	8	8	7	8	9	9
5V	755U/H	16,40	16,18	18	-	-	14	16	22	22
A0	H335	25	1	-	4	4	-	-	16	16
A1	C113	26	2	-	3	3	-	-	17	17
A2	7050	27	-	1	2	2	-	-	18	18
A3	0772	28	-	2	1	1	-	-	19	19
A4	C4C3	29	3	3	21	21	-	-	20	20
A5	AA08	30	4	4	5	5	-	-	21	21
A6	7211	31	15	16	6	6	-	-	3	3
A7	A3C1	32	-	-	7	7	-	-	4	4
$\overline{TPA}$	0000(F)	34	17	17	-	-	-	-	-	-
$\overline{MRD}$	0000(F)	7	5,6	-	18	18	-	-	-	-
$\overline{MWR}$	755U/H	35	-	6	20	20	-	-	-	-
AV	0000(F)	-	-	5	-	-	-	-	-	-
A8	7707	-	7	-	-	-	-	-	5	5
A9	577A	-	8	-	-	-	-	-	6	6
A10	HH86	-	-	7	-	-	-	-	7	7
A11	89F1	-	-	8	-	-	-	-	8	8
$\overline{CS0}$	A207	-	-	13	-	-	-	14	-	-
$\overline{CS1}$	H6A3	-	-	12	-	-	-	12	-	-
$\overline{CS2}$	755U/H	-	-	11	-	-	-	-	-	-
$\overline{CS3}$	H24U	-	-	10	19	19	-	-	-	-
$\overline{CLEAR}$	755U/H	3	-	-	17	17	-	-	-	-
$\overline{DMAOUT}$	0000/L	37	-	-	-	-	6	-	-	-
D1S	755U/H	-	-	-	-	-	8	15	-	-
OUT5	755U/H	-	-	-	-	-	-	13	14,15	-
OUT6	755U/H	-	-	-	-	-	-	11	-	14,15
+5VB	755U/H	-	-	-	22	22	-	-	-	-

Self-Test Switches

36. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- 826P/H
OV	-	Negative end of C8	- 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 4 and check that correct signatures are obtained.

Table 4: Self-Test Switch Signatures

SIGNAL	SIGNATURE/ TIP STATE	SWITCH SETTINGS						TEST POINT	
		F	E	D	C	B	A	ML6	ML14
0V	0000/L	0	0	0	0	C	0	20	8
+5V	826P/H	0	0	0	0	C	0	16,20	16
DIS	0000 *	0	0	0	0	C	0	-	1
IN1	826P/H	0	0	0	0	C	0	-	10
IN1	0000/L	0	0	0	C	C	0	-	10
OUT1	826P *	0	0	0	0	C	0	15	9
OUT1	0000 *	0	0	0	C	C	0	15	9
IN2	826P/H	0	0	0	0	C	0	-	6
IN2	0000/L	0	0	C	0	C	0	-	6
OUT2	826P *	0	0	0	0	C	0	14	7
OUT2	0000 *	0	0	C	0	C	0	14	7
IN3	826P/H	0	0	0	0	C	0	-	4
IN3	0000/L	0	C	0	0	C	0	-	4
OUT3	826P *	0	0	0	0	C	0	13	5
OUT3	0000 *	0	C	0	0	C	0	13	5
IN4	826P/H	0	0	0	0	C	0	-	2
IN4	0000/L	C	0	0	0	C	0	-	2
OUT4	826P *	0	0	0	0	C	0	12	3
OUT4	0000 *	C	0	0	0	C	0	12	3
$\overline{EF1}$	826P/H	0	0	0	0	C	0	24	-
$\overline{EF1}$	0000/L	0	0	0	0	C	C	24	-

* = May or may not be flashing.
0 = OFF
C = ON

Address Valid Circuit

37. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST PUSHBUTTON	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor board and check that correct signatures are obtained.

+5V - ML6 pin 40 - C690/H
OV - Negative end of C8 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 5 and check that correct signatures are obtained.

Table 5: Address Valid Circuit Signatures

SIGNAL	SIGNATURE/ TIP STATUS	TEST POINT (IC Pin No.)				
		ML6	ML7	ML20	ML19	ML12
+5V	C690/H	-	14	16,15	5,14	14
OV	0000/L	-	7	8,6	6,7	7
CK	C690(F)	1	3	-	-	-
$\overline{CK}$	0000(F)	-	4	9	-	-
MRD	0000(F)	7	-	7	-	13
MRDD	0000(F)	-	-	10	3	-
$\overline{AV}$	0000(F)	-	-	14	2	-
$\overline{MWR}$	C690/H	35	-	-	-	2
MRD.MWR	0000/L	-	-	1	-	1
AR	0000(F)	-	-	13	4	-

CPU, Address Bus & Address Decoder

38. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton IN (negative edge)
STOP pushbutton IN (negative edge)

CLOCK pushbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	ML6 pin 32
STOP	ML6 pin 32
CLOCK	ML6 pin 34
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained:

+5V - ML6 pin 40 - 0001/H
0V - Negative end of C8 - 0000/L

(7) Connect the signature analyser probe, in turn, to the points given in table 6 and check that correct signatures are obtained.

Table 6: CPU, Address Bus & Address Decoder Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT		
		ML6	ML10	TP
0V	0000/L	20	9,14	
+5V	0001/H	16,40	16,18	
CK	0000(F)	1	-	
$\overline{\text{WAIT}}$	0001/H	2	-	
$\overline{\text{CLEAR}}$	0001/H	3	-	
$\overline{\text{DMA IN}}$	0001/H	38	-	
$\overline{\text{DMA OUT}}$	0000/L	37	-	
TPA	0000(F)	34	17	
MA0	HC89	25	1	
MA1	2H70	26	2	
MA2	HPP0	27	-	
MA3	1293	28	-	
MA4	HAP7	29	3	
MA5	3C96	30	4	
MA6	3827	31	15	
MA7	755U	32	-	
$\overline{\text{MRD}}$	0000(F)	7	5	
$\overline{\text{CS0}}$	822A	-	13	TP4
$\overline{\text{CS1}}$	A169	-	12	
$\overline{\text{CS2}}$	C5U3	-	11	
$\overline{\text{CS3}}$	AP96	-	10	TP5

(5) Connect the signature analyser leads as follows:

START	TP5)	
STOP	TP5)	Processor card
CLOCK	TP1)	
GROUND	Any convenient OV point (chassis).	

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following signatures are obtained.

+5V - ML16 pin 39 - P254/H
OV - ML16 pin 24 - 0000/L

NOTE: If the correct +5V sig is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 15 and check that correct signatures are obtained.

Table 15: Synthesizer Board Signatures 1

SIGNAL	SIGNATURE/ TIP STAT	TEST POINT	
		PL39	ML16
OV	0000/L	5,6	24
+5V	P254/H	8,10	39
* +15V	P254/H	7	-
+9V	P254/H	-	38
STB1	366U	15	17
I00	2P0A	11	22
I01	4F62	13	21
I02	PP2C	12	20
I03	P246	14	19
I04	HAPP	16	18
CTL1	F378	-	15,34

(*+15V - use potential divider.
See Figure 21c on page 21-32)

(9) Set the front panel POWER switch to OFF.

(10) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Connect the signature analyser leads to the following points on the synthesizer board.

START	ML16 pin 2
STOP	ML16 pin 2
CLOCK	ML16 pin 17
GROUND	ML16 pin 24

(12) Set the front panel POWER switch to ON.

(13) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained:

+5V - ML16 pin 39 - 494P/H
0V - ML16 pin 24 - 0000/L

(14) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 16 and check that correct signatures are obtained.

(15) Set the front panel POWER switch to OFF. Disconnect the signature analyser leads. Replace the cover of the synthesizer compartment. Position the unit upright.

(10) Transfer the signature analyser leads to the following points on the demodulator card:

START	ML10 pin 13
STOP	ML10 pin 13
CLOCK	ML10 pin 17
GROUND	ML10 pin 24

(11) Set the front panel POWER switch to ON.

(12) Connect the signature analyser probe, in turn, to the following points on the demodulator card and check that correct signatures are obtained:

+8V	- ML10 pin 39	-	494P/H
0V	- ML10 pin 24	-	0000/L

(13) Connect the signature analyser probe, in turn, to the points on the demodulator card given in table 19 and check that correct signatures are obtained.

(14) Set the front panel POWER switch to OFF.

(15) Disconnect the signature analyser leads.

(16) Remove the extender card and replace the demodulator card into slot 5.

Table 19: Demodulator Card Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)			
		ML10	ML15	ML3	ML8
0V	0000/L	24	8	8	7,4
+8V	494P/H	38,39	1,7,10,16	16	14
CI	0000/L	36	-	-	-
CK.IN	0000(F)	37	-	-	-
CK1	(F)	40	-	-	- *
D0	6PC4	22	-	-	-
D1	04UP	21	-	-	-
D2	3017	20	-	-	-
D3	3UUC	19	-	-	-
D4	H416	18	-	-	-
$\overline{W}$	0000(F)	17	-	-	-
C0	0000/L	16	-	-	-
CTL2	4946	34,14	-	-	-
DIV1	6929	13	3	-	-
DIV2	846C	12	4	-	-
DIV3	9481	11	5	-	-
DIV4	7290	10	6	-	-
DIV5	PHFA	9	-	-	-
DIV6	3HC9	8	-	-	-
DIV7	P7C7	7	-	-	-
DIV8	CFU6	6	-	-	6
DIV9	PAU3	5	-	11	-
DIV10	CH5P	4	-	10	-
DIV11	37AC	3	-	9	-
DIV12	86U5	2	-	-	-

(F) denotes flashing probe tip.
* May be unstable

AGC Card (ST 85491)

46. (1) Set the front panel POWER switch to OFF.

(2) Mount the AGC card onto the extender card (inserted into slot 6).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

Table 25: SCORE Interface Card Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)								
		EC	ML16	ML10	ML14	ML9	ML5	ML3	ML1	ML2
0V	0000/L	1,64	4	7	4	7	8	7	5,7,9	7
+5V	P254/H	2,63	1	14	8	14	10,16	14	14	14
INT.CK	P955	44	-	-	-	6	-	-	-	-
CK.IN	0000/L	35	5	-	-	-	-	-	-	-
CK.RTN	0000/L	46	6	-	-	-	-	-	-	-
$\overline{\text{CK.IN}}$	0000/L	-	3	11	-	13	-	-	-	-
CK.IN	P254/H	-	-	10	6	-	-	-	-	-
CK.D	0000/L	-	-	-	7	-	-	-	-	-
CK.E	P254/H	-	-	-	5	1,2	-	-	-	-
EXT.P	0000/L	-	-	1	-	3,12	-	-	-	-
$\overline{\text{EXT.P}}$	P254/H	-	-	2	-	5	-	-	-	-
EXT.SEL	P254/H	-	-	-	-	9,11	-	-	-	-
INT.SEL	0C01	-	-	-	-	8,4	-	-	-	-
SCORE.CK	P955	-	-	13	-	10	9	-	-	-
$\overline{\text{SCORE.CK}}$	0C01	-	-	12	-	-	-	-	3	-
Q4	0000(F)	-	-	-	-		14	1	-	-
SAS	8U10	-	-	-	-	-	-	2	-	-
$\overline{\text{Q4}}$	6H44	-	-	-	-	-	-	3	-	-
STB13	0000/L	7	-	-	-	-	-	-	4,8	-
SIS	0000/L	-	-	-	-	-	-	-	13	9
$\overline{\text{SIS}}$	P254/H	-	-	-	-	-	-	-	12	13
$\overline{\text{SYNC}}$	P254/H	-	-	-	-	-	-	-	-	10,5
SET	8U10	-	-	-	-	-	-	-	6	4
LOAD	9HH1	-	-	-	-	-	-	-	11,1	-
$\overline{\text{LOAD}}$	7U85	-	-	-	-	-	-	-	2	12
RESET	9HH1	-	-	-	-	-	15	-	-	11

Table 26: SCORE Interface Card Signatures 4

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC PIN No.)						
		ML12	ML7	ML10	ML2	ML3	ML8	ML15
$\overline{FIFO}$	U5PA	-	2 *	9 *	-	-	-	-
DOR	300C	-	14	-	-	-	-	-
LOAD	9HHI	-	-	-	1	-	-	-
$\overline{SO}$	3AIC	-	-	-	3	5,6	-	-
SO	H84U	15	15	-	-	4	9	-
P1	F64H	-	13	-	-	-	7	-
P2	P4H5	-	12	-	-	-	6	-
P3	C6FA	-	11	-	-	-	5	-
P4	4301	-	10	-	-	-	4	-
P5	943A	13	-	-	-	-	13	-
P6	9132	12	-	-	-	-	14	-
P7	UFC6	11	-	-	-	-	15	-
P8	2396	10	-	-	-	-	1	-
CK	0C01	-	-	-	-	-	10	-
Q8	F0U1	-	-	-	-	-	3	3

* ML10 Pin 9 is P254(F) on earlier Boards.

(12) Link the pins of a 26-way plug (para. 2) as listed below and connect to the CONTROL socket on the receiver front panel

Pin D to pin R
Pin H to pin a
Pin K to pin c
Pin M to pin b
Pin P to pin Z

(13) Set the front panel POWER switch to ON.

(14) Connect the signature analyser probe, in turn, to the following points on the SCORE interface and check that correct signatures are obtained.

+5V - Positive end of C4 - CC34/H
0V - Negative end of C4 - 0000/L

(15) Connect the signature analyser probe, in turn, to the points on the SCORE interface card given in table 27 and check that correct signatures are obtained.

(16) Set the front panel POWER switch to OFF.

RA 1794A HF/VHF/UHF RECEIVER

TECHNICAL MANUAL

CONTENTS

TECHNICAL SPECIFICATION

Frequency range	2MHz to 512MHz
Tuning	Numerical frequency entry. Frequency can also be stepped in pre-programmed steps or fine-tuned with UP/DOWN pushbuttons.
Frequency Standard	Internal 9420 Standard (optional) Frequency: 5MHz Ageing rate: 5×10^{10} per day Warm-up time: 20 minutes Initial accuracy ±4.2 parts in 10^8 over the temperature range. External: Operators from any sub-multiple of 20MHz, from 5MHz down to and including 100kHz. Input level 0dBm ±5dB into 50 ohms.
Modes of Operation	CW (A1A) MCW (A2A) AM (A3E) FM (F3E) SSB (R3E, H3E, J3E, R2A, H2A, J2A)
Antenna Input	(a) Input impedance 50 ohms (b) VSWR 3:1 maximum
Noise Figure	15dB maximum over the frequency range 10MHz to 512MHz.
Audio Output	(a) 200mW for connection to an external 8 ohm loudspeaker. (b) Line output, 1mW into 600 Ohms, balanced. Output level adjustable by internal preset control. (c) Phone output, 1mW into 600 Ohms.

IF Output	(a) 21.4MHz (IF2), 3MHz wide, level dependent on received signal strength and receiver AGC characteristic. (b) 1.4MHz (IF3), filtered, 100mV r.m.s. into 50 ohms not applicable in SSB mode.
Video Output	1 volt peak-to-peak into 75 ohms.
Video Response	Within 6dB from 100Hz to 150KHz.
Hum and Noise	At least 35dB S+N/N ratio for 70% modulated AM signal.
Re-radiation	Not greater than 10µV across a 50 ohm termination at the antenna input, up to 1GHz.
Carrier Operated Relay	Operating threshold adjustable by IF GAIN control.
Audio Squelch	Audio output is muted when signal falls below pre-determined level.
Selectivity	The following nominal filter bandwidths are available as standard: 300Hz 1.2kHz 3kHz (always selected for SSB) 8kHz 15kHz 30kHz 300kHz
AGC	(a) Range: An increase in antenna input of 100dB shall produce an output change of less than 3dB.

	(b) Time constants (nominal): automatically selected with MODE, as follows: AM and FM: Attack 30ms Decay 300ms SSB and CW: Attack 5ms Delay before hang 100ms Hang 2 seconds Delay 1 second
Gain Control	Control range 100dB. AGC is operative when the manual IF GAIN control is in use but only operates on signals above the level set by the IF GAIN control. This setting also controls the threshold of COR and squelch functions.
Audio Muting	Reduces audio line output to less than -40dBm by earthing a control line.
BFO	Programmable off-set for CW. Tuneable in 10Hz steps from front panel over the range ±7.79kHz.
Intermodulation Products	Third-order intercept point 0dBm. (10MHz to 512MHz)
Power Supply	24V nominal
Power Consumption	Typically 40 watts
Environmental Requirements	Def. Stan. 07-55 as applicable to wheeled and tracked vehicles, trailers and shelters, for use anywhere in the world.
Temperature	$-10^{o}C$ to $+70^{o}C$ operating $-40^{o}C$ to $+70^{o}V$ storage
Reduced Specification	$-10^{o}C$ to $+45^{o}C$ to achieve specified frequency stability when an internal standard is fitted.

Relative Humidity	95% at 35°C 12 hours cycling to 20°C 6 hours saturation.
Vibration	5 to 13Hz 6mm displacement 11 to 500Hz 1.5g peak acceleration. Duration 6 hours in vertical axis only.
Dimensions	Height: 204mm (8 in) Width: 254mm (10 in) Depth: 381mm (15 in)
Weight	14kg (30 lb) maximum

CHAPTER 1

GENERAL DESCRIPTION

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Illustrations

CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1. The RA 1794A is a synthesized HF/VHF receiver designed for use in EW, surveillance and DF systems. It covers the frequency range 2 MHz to 512 MHz in 10 Hz increments and provides reception facilities for LSB/USB (R3E, H3E, J3E, R2A, H2A, J2A), MCW (A2A), CW (A1A), AM (A3E) and FM (F3E). An optional control facility using SCORE (Serial Control of Racal Equipment) is available for extended or remote control purposes.

2. The receiver is housed in a 1 ATR configuration cast metal case with all controls and connections mounted on the front panel. It has an internal DC power supply unit which operates from a nominal DC input voltage of 24V.

BRIEF TECHNICAL DESCRIPTION

3. For explanation purposes, the receiver is divided into two sections, namely the RF/IF/AF section and the control and display section. These sections are described in the following paragraphs in conjunction with the block diagrams given in figs 1.1 and 1.2 at the end of the chapter.

RF/IF/AF Section (fig 1.1)

4. The signal induced into the antenna is applied via a 512 MHz low-pass filter to the first mixer/VCO board, where it is up-converted to produce the first IF of 661.4 MHz. The 661.4 MHz to 1173.4 MHz first local oscillator signal is produced by a single-loop synthesizer where the voltage controlled oscillator (VCO) is located on the first mixer board. The output signal from the first mixer is amplified and then fed via a 661.4 MHz band-pass filter (3 dB bandwidth of 3 MHz) to the second mixer/640 MHz board. Here it is applied to mixer 2 via a gain-controlled (AGC1) amplifier and is mixed with a 640 MHz second local oscillator injection signal to produce the second IF at 21.4 MHz.

5. The 640 MHz second local oscillator signal is derived from a 640 MHz VCO which is phase-locked to a 20 MHz reference signal; this signal is produced on the 20 MHz reference board and is phase-locked to either the optional internal 5 MHz frequency standard or to an external frequency standard.

6. The 21.4 MHz output signal from the second mixer is amplified before application to the IF filter card, and to the 21.4 MHz IF output amplifier.

7. The IF filter board contains up to seven symmetrical filters, 21.4 MHz and 1.4 MHz gain-controlled IF amplifiers, and mixer 3. Note that sideband filters are not fitted; for USB or LSB, FL3 is normally selected, and the synthesized first local oscillator and BFO signals are displaced in

frequency by the required amount. Filter selection is accomplished using PIN diodes controlled by latched data from the AGC card. When one of the narrow bandwidth 1.4 MHz filters (FL1 to FL4) is selected, the 21.4 MHz filter FL5 is also selected. When one of the wide bandwidth 21.4 MHz filters (FL5, FL6, or FL7) is selected, the 1.4 MHz wideband (300 kHz) condition is selected.

8. The filtered and amplified 21.4 MHz IF signal is combined in mixer 3 with the 20 MHz reference signal, and the difference frequency output signal, at 1.4 MHz, is applied to the AGC card and the demodulator card via the selected 1.4 MHz filter, the 1.4 MHz gain-controlled IF amplifier, a 300 kHz band-pass filter and an emitter-follower buffer stage.

9. The AGC card contains the AGC detector, the AGC distribution stages and the 1.4 MHz IF output amplifer. Parallel data from the control section conveying filter selection and AGC time constant selection information is stored in a set of latches and is then applied to the IF filter card and the AGC detector. The IF gain voltage, which is dependent on the setting of the front panel IF GAIN control, is used to set the COR (carrier operated relay) threshold level. When SQUELCH is selected, the IF GAIN control is also used to set the AGC threshold and the audio mute threshold for the FM mode.

10. The demodulator card contains a synthesized BFO (centre frequency 1.4 MHz), three detector circuits with associated selection circuitry, an audio pre-amplifier followed by a 150 kHz low-pass filter, and three audio output amplifiers. The synthesized BFO produces a 1.4 MHz plus or minus 7.79 kHz output signal, tunable in 10 Hz increments. It uses an LSI device to control a programmable divider which forms part of a phase-locked loop. The applied 20 MHz reference signal is divided by ten and then by two to produce a 1 MHz reference input for the LSI device. The 2 MHz output from the decade divider is also applied to the control and display section where it is used as the CPU clock signal.

11. Two FM detectors are provided, one for wideband and one for narrow band FM signals. The third detector is for the AM, CW and SSB modes. For the AM mode, a limited carrier output from the narrow-band FM detector is applied, together with the 1.4 MHz IF signal, to an envelope detector. For the SSB and CW modes, the BFO signal is applied, together with the 1.4 MHz IF signal, to a product detector. The detected audio signal is then applied to a pre-amplifier, which is followed by a 150 kHz low-pass filter and three output amplifier stages. One of these provides a 600 ohm balanced audio line output, a separate amplifier provides the output for the phones, the internal loudspeaker, and an external loudspeaker, whilst the remaining amplifier provides a wide-band video output. The video amplifier also feeds an audio peak detector, the output of which is used for audio metering purposes.

Control and Display Section

12. The control and display section of the receiver is based on a micro-computer assembly located on the processor card. It comprises an 8-bit C-MOS central processing unit (CPU), 8k bytes of read-only memory (ROM), in which is stored the operating program and a number of test programs,

256 bytes of random access memory (RAM), 1 k byte of electrically alterable read only memory (EAROM) and a programmable input/output (PIO) device. The 256 byte RAM is used by the CPU for temporary data storage, whilst the EAROM is used to store channel information as well as the current receiver settings so that they may be recalled when power is restored following a power failure.

13. The PIO device has two high-speed 8-bit I/O ports. One of these is used to produce a number of data strobe signals and to control a 16-line multiplex circuit; this is used in conjunction with a digital-to-analogue (D to A) converter to monitor a variety of analogue signals, such as the regulated voltage supplies, the IF GAIN control setting, and phase-locked loop varactor monitor lines. The remaining PIO port is the main communications link between the CPU and remainder of the receiver.

14. The keyboard is arranged as a 4-row by 6-column matrix; this is scanned once every 8 milliseconds (approximately) and the content of each six-bit column is temporarily stored in RAM (on the processor card). A multiplexed display system is used where the data to be displayed is stored in RAM (located on the display driver card). A multiplex counter is used to simultaneously address RAM for the required segment data and to produce the correct one-of-16 decoder output for the appropriate display common cathode.

15. The 20 MHz reference board accepts the output from the optional internal 5 MHz frequency standard or the output from an external frequency standard (which may be any sub-multiple of 5 MHz down to and including 100 kHz). When an external frequency standard is connected to the receiver, it automatically overrides the internal frequency standard (if fitted). The 20 MHz reference signal, which is produced using a voltage controlled oscillator (VCO) within a phase-locked loop, is applied to the second mixer/640 MHz board, mixer 3 on the IF filter card, the synthesizer board (para 16) and the BFO circuitry on the demodulator card.

16. The synthesizer board contains the first local oscillator single-loop synthesizer circuity, apart from the 661.4 MHz to 1173.4 MHz VCO, which is located on the first mixer/VCO board. An output signal from this VCO is applied to a programmable divide-by-N stage, where the value of N is determined by the most significant digits of the required operating frequency. The least significant digits of the required operating frequency (those below the sampling frequency of 1 MHz) are used to compute a phase offset control voltage which is fed into the loop (via a digital-to-analogue converter) as an extra input. The loop adjusts the VCO phase to be the sum of the reference phase (i.e. that resulting from the comparison between the 1 MHz reference and the output signal from the divide-by-N stage) and the computed phase.

17. The optional SCORE interface card allows for extended control (hard-wired cables) or full remote control (data modems), using a control unit such as the MA 1113, or another receiver. The SCORE system is based on a number of 48-bit synchronous frames, each of which contains a 16-bit preamble

(synchronisation, word number identification, etc.) followed by a 32-bit data word. Separate lines are used for both data and clock signals travelling in each direction. These comply with CCITT V10 and are thus compatible with a wide variety of data modems.

18. The user functions provide for up to four earth connections applied to a receiver to be reproduced at the remote or extended control unit unit via the serial revertive data, and up to four earth connections applied to the control unit to be reproduced at the receiver via the serial control data. The two systems are completely independent and may be used for a variety of applications. For further details see Chap. 16.

INDENTIFICATION OF VARIANTS

19. In order to identify the optional facilities fitted to a particular receiver, an option label is attached to the top face of the front panel assembly, adjacent to the type/serial number plate. The meanings of the option label codes are as follows:

First Character: Alphabetical identification of filters fitted to the IF filter card. Code HA denotes standard filters of 0.3, 1.2, 3, 8, 15, 30 and 300 kHz.

Second Character: Frequency standard.
0 indicates no internal frequency standard fitted; receiver operates from an external frequency standard.

S2 indicates type 9442 fitted.

S3 indicates type 9420 fitted.

Third Character: SCORE interface

0 indicates not fitted (standard)

S indicates is fitted.

ANTENNA

512 MHz

FIRST MIXER/VCO BOARD

MIXER 1

661·4MHz TO 1173·4 MHz VCO

661·4MHz

SECOND MIXER/ 640 MHz BOARD

21·4MHz IF OUT

MIXER 2

AGC 1

21·4 MHz

640 MHz VCO

÷ 64

÷ 2

IF FILTER CARD

FL5 (15 KHz)

FL6 (30KHz)

FL7 (300 KHz)

FILTER SELECT

FILTER SELECT

AGC 2

MIXER 3

1·4MHz

FL1 (300 Hz)

FL2 (1KHz)

FL3 (3KHz)

FL4 (7·5KHz)

WIDEBAND (300 KHz)

FILTER SELECT

FILTER SELECT

AGC 3

300 KHz

DEMODULATOR CARD

WBFM DET

NBFM DET

AM/ CW/ SSB DET

DETECTOR SELECT

3

150 KHz

AUDIO LINE OUT

PHONES/ LOUDSPEAKE

VIDEO OUT

AUDIO PEAK DET

BFO

NOTE: IF FILTER BANDWIDTHS SHOWN ARE TYPICAL.

AGC CARD

AGC DIST

AGC DET

LATCHES

1·4MHz IF OUT

IF GAIN VOLTAGE

20MHz REFERENCE OUT

FREQUENCY STANDARD

EXTERNAL REF IN

CONTROL AND DISPLAY (SHEET 2)

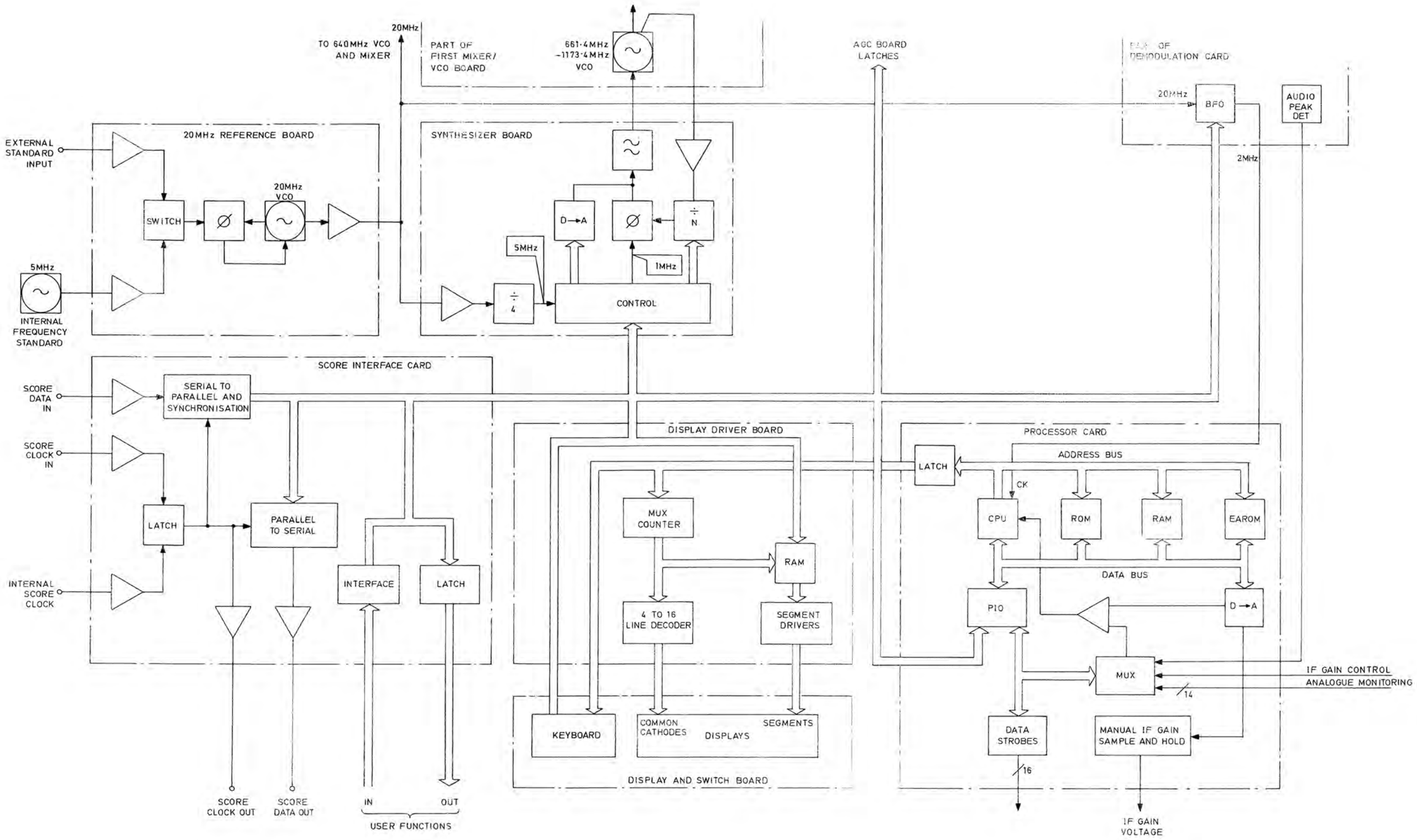
2MHz

ANALOGUE MONITORING

AUDIO METERING

RACAL TH 2449

Block Diagram: RA1794 (Sheet 1) Fig.1.1



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TH 2449

Block Diagram: RA1794 (Sheet 2) Fig.1.2

CHAPTER 2

INSTALLATION

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CHAPTER 2

INSTALLATION

INTRODUCTION

1. As the RA 1794A is designed as a tactical systems receiver, it generally forms part of a larger system and is supplied complete with prefabricated cable and connector assemblies tailored to suit a particular system. It may, however, be required to operate the receiver divorced from the system (in a workshop, for example), or it may be required to re-install this equipment in a different configuration. To facilitate these requirements, this chapter provides the necessary installation information.

POWER CONNECTOR

2. The receiver operates from a nominal 24 V DC supply which is normally provided by a vehicle battery (negative earth). The mating socket for the POWER connector is an Amphenol type 62GB-56T-8-4S (Racal number 935040) with a backshell (Racal number 939539). Use a 2-core screened cable with a conductor size of 1 square mm (Racal number 938290). The connection details are as follows:

PIN	CONNECTION
A and B	Positive (Brown)
C and D	Negative (Blue)

POWER FUSE

3. The applied power input is routed to the internal power supply board via the POWER switch and a 6.3 ampere fuse (mounted on the front panel). Check that a serviceable fuse of the correct rating is fitted (replacement part number 922454).

CONTROL CONNECTOR

4. This is a 26-way connector (mating plug Amphenol 62GB-56T-16-26P, Racal 939099, with backshell, Racal 939543). The connections are given in table 1.

AUDIO CONNECTORS

5. The mating plug type for the parallel-connected AUDIO 1 and AUDIO 2 sockets is Amphenol 62GB-56T-12-10P, Racal 931611, with backshell, Racal 939541. The connection details are given in table 2.

ANTENNA CONNECTION

6. The antenna socket is of the coaxial N-type, and is 50 ohms impedance. The type of mating plug is dependent on the type of coaxial antenna feeder in use, and examples are given below. Alternatively, an N-to-BNC adaptor, male-to-female, Racal 930569, may be used to allow the use of a 50 ohm BNC plug (Racal 900038) for the antenna connection.

Cable URM 43 (RG58C/U) - N Connector type Racal 927694
Cable URM 67 (RG213/U) - N Connector type Racal 932547

Table 1: Control Connector

PIN	FUNCTION
A	Spare 1
B	AGC Level IN/OUT
C	Spare 2
D	SCORE Data In
E	Spare 3
F	SCORE Clock In
G	Spare 4
H	OUT User Function W
J	Spare 5
K	OUT User Function X
L	SCORE Data IN return
M	OUT User Function Y
N	SCORE Clock IN return
P	OUT User Function Z
R	SCORE Data Out
S	Carrier Operated Relay (COR)
T	SCORE Clock OUT
U	Mute
V, W, X, Y	0 V
Z	D
a	A
b	C — User Functions IN
c	B

Table 2: AUDIO 1 and 2 Connectors

PIN	FUNCTION
A	AGC Level IN/OUT
B	Carrier Operated Relay (COR)
C	Loudspeaker
D	Loudspeaker earth
E	Headphones earth
F	Line Output
G	Balanced
H	0 V
J	Mute
K	Headphones

BNC CONNECTORS

7. Connections to the BNC connectors (IF2, IF3, VIDEO, EXT. STD) may be made using 50 ohm BNC coaxial plugs, Racal Part Number 900038.

DESICCATOR

8. The desiccator fitted to the front panel is designed to reduce the humidity within the sealed case. The colour of the indicator is blue when the humidity is below 40% and changes to pink when above 50%. Provided the receiver case is effectively sealed, the relative humidity will be maintained and the indicator will remain blue. If however, moisture is allowed to permeate the case seal, the humidity will rise and the indicator will eventually turn pink. The desiccator must then be replaced and the case resealed.

9. A saturated desiccator body may be reactivated in an oven, which has a controlled temperature of approximately 120 degrees centigrade, for a period of two hours. A stream of heated air should be allowed to pass over the desiccator body and away to the atmosphere. This will ensure that the liberated water vapour is cleared from the desiccant. The reactivated desiccator should be placed in a sealed container until required for use.

Desiccator Removal

10. The desiccator comprises two main assemblies, the humidity indicator head, which screws into the receiver front panel, and the desiccator body, which screws into the humidity indicator head. With the front panel assembly removed from the case, the desiccator body may be unscrewed from the rear. Alternatively, the complete desiccator assembly can be unscrewed from the front of the unit.

EARTH TERMINAL

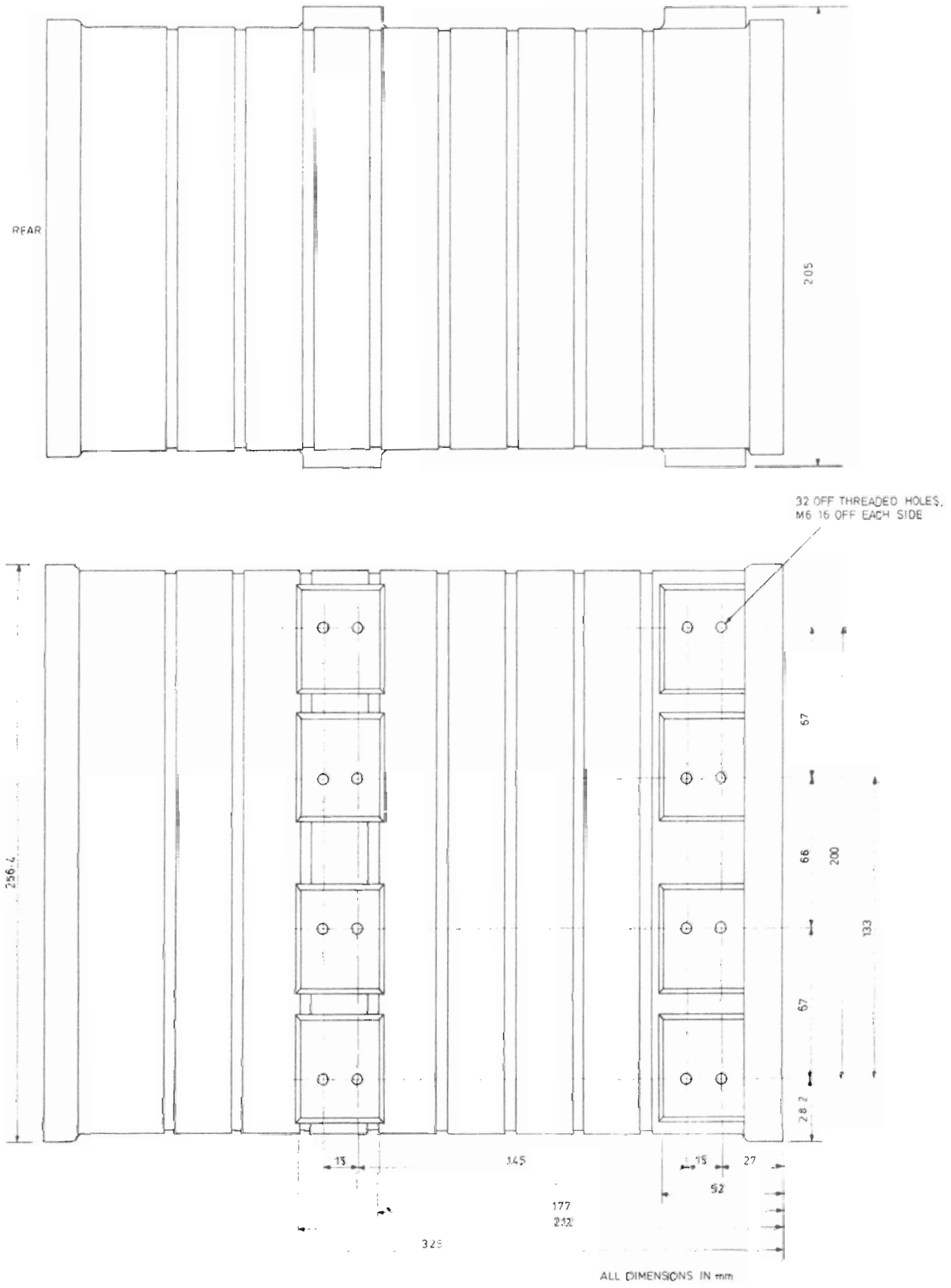
11. The earth terminal, at the bottom right-hand corner of the front panel, should be connected to a suitable earthing point using heavy-duty copper braid.

RECEIVER MOUNTING

12. The receiver is mounted in a 1ATR configuration cast metal case which is fitted with mounting bosses on both the top and bottom surfaces (fig. 2.1). These bosses have a number of tapped holes (thread size M6) to suit a number of different mounting arrangements.

RECEIVER MOUNTING KIT

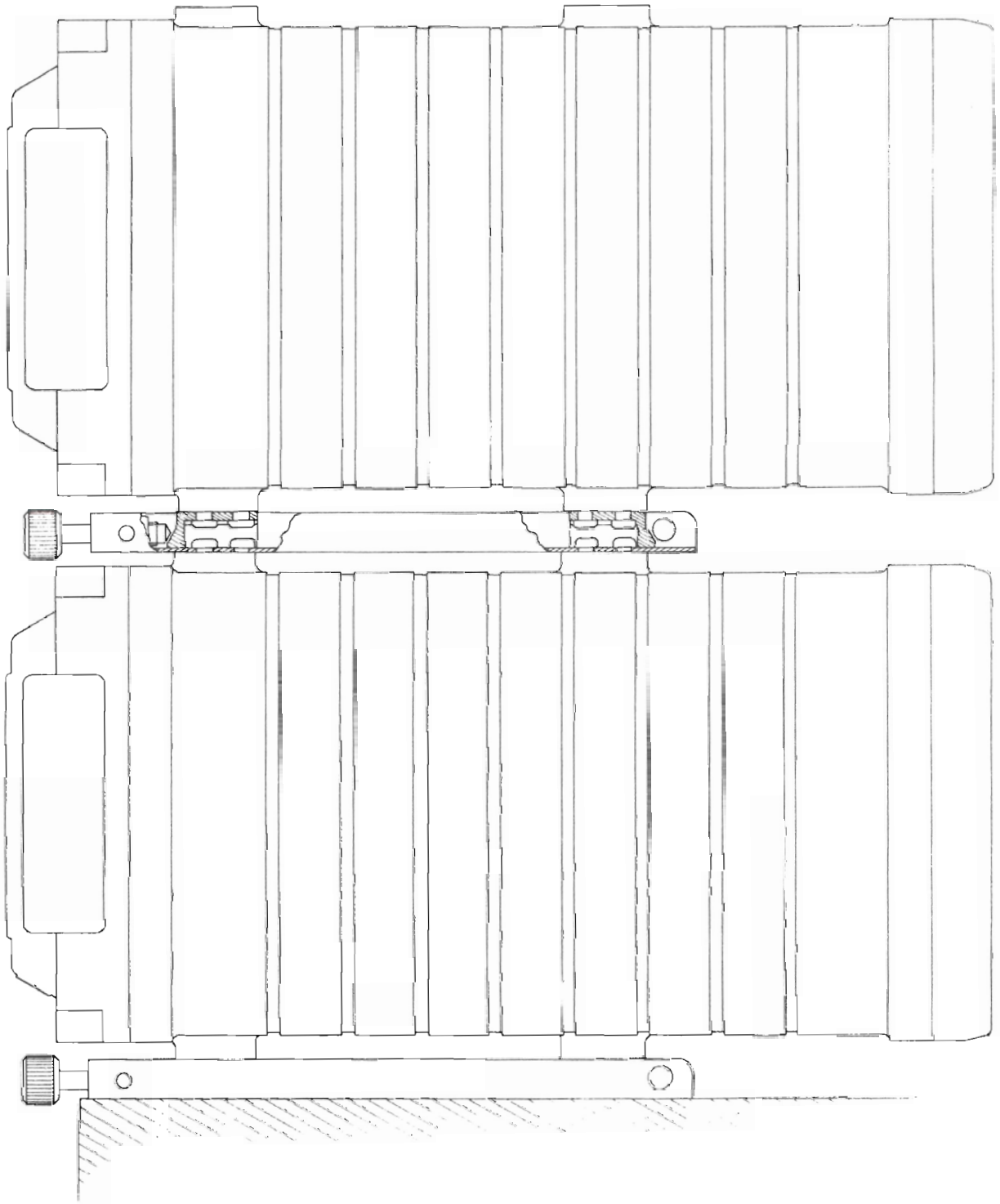
13. A mounting kit (Racal ST 790356) is available which allows for the mounting of a single receiver or the mounting of one receiver above another (fig. 2.2). A number of kits may be used to assemble a variety of equipment types provided each is fitted into a suitable case. Each mounting kit comprises a pair of channels, two pairs of mounting blocks (which are bolted to the receiver case), the retaining screw assemblies and all the necessary fixing hardware.



RACAL
TH2449

Case Details

Fig. 2.1



RACAL TH2449

Mounting Kit Details

Fig. 2.2

CHAPTER 3

OPERATING INSTRUCTIONS

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CHAPTER 3

OPERATING INSTRUCTIONS

INTRODUCTION

1. This chapter provides general operating instructions for the RA 1794A receiver. It is assumed that the receiver has been correctly installed in accordance with the instructions given in Chapter 2 and/or the appropriate system manual.

FUNCTION OF CONTROLS

2. The function of each front panel control is described in the following paragraphs; these should be read in conjunction with fig 3.1 at the end of the chapter.

3. (1) POWER on/off Switch: Toggle switch, up for ON

(2) IF GAIN: Rotary control which is used to set the AGC thresholds, the COR (carrier operated relay) threshold, and the audio squelch threshold (dependent on selected function and/or MODE)

(3) VOLUME: Rotary Control used to adjust the level of the audio signal at the loudspeaker and phones outputs.

(4) UP and DOWN Keys: Used to increment or decrement the displayed frequency (TUNE & STEP), BFO and Channel number.

(5) MODE Key: Used to select the second function of numeric Keys 0 to 6, i.e. TEST, USB, AM, CW, LSB, FM and SQLCH respectively.

(6) Numeric Keys (0 - 9) Used in conjunction with other Keys to select: detector, squelch status, self test status, frequency entry, tune rate, step size, BFO tune rate, channel number and test number.

(7) TUNE Key: Selects the tune mode, where the numeric keys are used to select the tune rate, and the UP/DOWN keys are used to increment/decrement the receiver frequency.

(8) STEP Key: Selects the step mode where the numeric keys are used to select the step size, and the UP/DOWN Keys are used to control the direction of the frequency steps.

(9) BFO Key: When the CW mode is selected, this Key selects the BFO tune mode, where the numeric Keys are used to select the BFO tune rate and the UP/DOWN Keys are used to increment or decrement the BFO frequency.

(10) REMOTE Key: Pressed to select remote control, pressed a second time to select local control.

(11) BW+ and BW- Keys: Used to select filters of wider or narrower bandwidth.

(12) STORE Key: To store the displayed setting, the STORE key is held depressed whilst the required channel number (00 to 99) is selected, using the numeric Keys. The STORE operation occurs when the STORE key is released.

(13) RCL Key: When the receiver is in the display - only mode (flashing CHANNEL display - see para 5), pressing the RCL (recall) key causes the actual receiver settings to be displayed.

(14) ENTER Key: When the receiver is in the display - only mode (flashing CHANNEL display - see para 5), pressing the ENTER key causes the receiver to be set to the displayed settings.

(15) FREQ Key: When the key is pressed, the receiver enters the display-only mode (para 5) and the numeric Keys are enabled to allow a specific frequency to be displayed.

(16) CHAN Key: When this Key is pressed, the receiver enters the display-only mode (para 5) and allows the channel settings to be displayed without affecting the actual receiver settings.

FRONT PANEL INDICATORS

4. (1) CHANNEL: Indicates the channel number when in the channel mode, or the test number when in the self-test mode. When in the display-only mode, the CHANNEL digits flash and give the display - only channel number (CHAN mode enabled) or (CHAN mode not enabled)

(2) FREQUENCY: Indicates the frequency in MHz or the fault number when in the self-test mode.

(3) METER: Denotes the RF signal strength (in decibels).

(4) BW kHz — Indicates the filter bandwidth in kHz

(5) BFO kHz — Indicates the BFO offset frequency in kHz

(6) MODE: — The selected mode, ie. USB, LSB, AM, FM, or CW, is displayed.

(7) FAULT: — Flashes to indicate a fault condition.

(8) SQLCH: — FM Mode: Indicates that audio squelch is operational.
Other Modes: Indicates that threshold AGC is operational.

(9) REM — Illuminates when the receiver has been set to the remote control mode.

DISPLAY ONLY MODES

5. Before attempting to operate the receiver it is important to note that when the CHANNEL display (which consists of a channel number in the range 00 to 99 or ==) is flashing, the front panel displays may not indicate the actual receiver settings. These conditions are known as the display-only modes (as opposed to the normal 'receiver' mode) and are entered whenever the FREQ key, the CHAN key or the STORE key is pressed and released. When the FREQ key is pressed and released, the flashing channel display == occurs to denote the normal display-only mode. When the CHAN Key or the STORE key is pressed and released, the flashing channel number denotes the channel display - only mode. If, when in the channel display-only mode, the FREQ, MODE, BW+, BW-, TUNE, STEP, BFO or SQLCH key is pressed, the flashing channel number display is repalced with the flashing== display, and the receiver enters the normal display-only mode.

6. When the receiver is in either of the two display-only modes, the actual receiver control settings in force prior to the entry of the display-only mode remain unchanged, allowing normal uninterrupted receiver operation. Press the RCL key to display the actual receiver settings and exit from the display-only mode. Press the ENTER key to set the receiver to the displayed settings.

FREQUENCY SELECTION

7. The receiver frequency may be set either by using the numeric keys or by using the UP/DOWN keys in conjunction with the TUNE key. The frequency may also be stepped using the STEP key.

Numeric Key Frequency Selection

8. (1) Press and release the FREQ key. The receiver enters the normal display-only mode, as denoted by the flashing channel display . The frequency display is set to zero and a _ prompt signal appears at the 100 MHz digit position.

(2) If a numeric key in the range 1 to 5 is pressed, the digit is displayed in the 100 MHz position and the prompt moves to the 10 MHz digit position. If the 0 numeric key is pressed, the 100 MHz digit is blanked and the prompt moves to the 10 MHz digit position (leading zero suppression is operative at all times on the 100 MHz and 10 MHz frequency digits). If a numeric key in the range 6 to 9 is pressed, the key press is ignored since numeral 5 is the highest allowable digit to occupy the 100 MHz digit position.

(3) Further numeric key presses cause successive digits to be displayed and the prompt to move to the right after each numeral is entered. Note that if the 100 MHz digit is set to numeral 5, then the 10 MHz digit may only be set to either 0 or 1 (maximum receiver operating frequency is 511.999 99 MHz.

(4) When eight digits have been entered correctly, the prompt disappears and further numeric entries are ignored. If a non-numeric key is pressed during the frequency entry, a zero is entered into the prompt position and the frequency entry mode is terminated. If an error is made whilst entering the frequency, press the FREQ key and start again.

(5) When the required operating frequency is displayed (Note that trailing zeros need not be entered), press and release the ENTER key. The flashing== channel display is extinguished and the receiver is set to the displayed frequency.

TUNE key Frequency Selection

9. (1) Press and release the TUNE key. This enables the UP/DOWN keys for tuning purposes and enables the numeric keys for selection of the required tuning rate. The function of the UP/DOWN and numeric keys may be modified if the MODE, STEP, BFO, STORE, FREQ or CHAN key is subsequently pressed. Note that the function of the numeric keys may be modified without changing the function of the UP/DOWN keys. For example, if the TUNE key is pressed, the required tuning rate is selected using the numeric keys (table 1), and the required operating frequency is obtained using the UP and DOWN keys, the MODE key may then be pressed in order to change the MODE. Thus the function of the numeric keys is changed but the UP and DOWN keys when pressed will still increment or decrement the frequency at the last selected tuning rate.

(2) When TUNE is selected, the slowest tune rate available is automatically selected (table 1). Use the numeric keys to select the required tune rate, and press the UP or DOWN key, as appropriate, to achieve the desired frequency. As the desired frequency is approached, select a slower tune rate.

Table 1 : Tuning Rates

NUMERIC KEY	TUNING RATE (per second)
1	39 Hz
2	625 Hz
3	3.75 KHz
4	13.75 KHz
5	18.75 KHz
6	37.5 KHz
7	125 KHz
8	625 KHz
9	2.5 MHz

STEP Key Frequency Selection

10. (1) Press and release the STEP key. This enables the UP/DOWN keys to step the receiver frequency and enables the numeric keys for the selection of the required step size (table 2).

(2) Press and release the appropriate numeric key to select the required step size, as given in table 2. Note that when the STEP key is pressed, a step size of zero is automatically selected; a step size must therefore be selected.

(3) Press the UP or DOWN Key to increase or decrease the receiver frequency, in steps of the selected size, at a rate of approximately two steps per second.

(4) When STEP is selected, the function of the UP, DOWN and numeric keys may be modified if the MODE, TUNE, BFO, STORE, FREQ or CHAN Key is subsequently pressed. Note that the function of the numeric keys may be modified without changing the function of the UP/DOWN keys. For example, if the STEP key is pressed, the required step size is selected using the numeric keys, and the operating frequency is incremented or decremented using the UP or DOWN keys, the MODE key may then be pressed to allow the selection of a different mode. Thus the function of the numeric keys is changed but the UP and DOWN keys when pressed will still increment or decrement the frequency, at the last selected step size.

Table 2 : Step Size Selection

NUMERIC KEY	STEP SIZE SELECTED
1	9 kHz
2	6.25 kHz
3	12.5 kHz
4	25 kHz
5	50 kHz

MODE SELECTION

11. (1) Press and release the MODE key: This causes the numeric keys 0 to 6, when pressed, to select the modes marked in green on the key tops, i.e. TEST, USB, AM, CW, LSB, FM and SQLCH respectively.

(2) Press the required detector mode key. The selected mode is displayed, together with the last bandwidth selected in that mode. For the CW mode, the last BFO setting is also displayed.

(3) The SQLCH indicator toggles between on and off each time the SQLCH key is pressed. When SQLCH is not illuminated, the receiver is in the full AGC mode where the IF GAIN control is used solely to set the COR level. When SQLCH is illuminated, the receiver is in a threshold AGC mode where both the AGC threshold and the COR level are set by the IF GAIN control. If the FM mode and SQLCH are both selected, the audio output is muted when the received signal level is below the AGC/COR threshold.

(4) If the MODE and TEST keys are pressed simultaneously, the receiver enters the self-test mode (para 24). The receiver operating conditions are preserved in memory and are returned when the self-test mode is cancelled (by again pressing MODE and TEST).

BANDWIDTH SELECTION

12. To increase or decrease the receiver bandwidth press the BW+ or BW- key respectively. This causes the displayed filter bandwidth to increment or decrement to the next available filter bandwidth for the selected mode. When the widest or narrowest filter bandwidth is displayed, further presses of the BW+ or BW- keys have no effect. (Not operative for the USB and LSB modes).

BFO TUNING

13. Provided the CW mode is selected, the BFO freqency may be set to any frequency in the range plus and minus 7.79 kHz, as follows:

14. (1) Press and release the BFO key. This enables the UP/DOWN keys for BFO tuning purposes, and enables the numeric keys for the selection of the required BFO tuning rate (table 3).

(2) Select the required BFO tuning rate using the numeric keys 1, 2 or 3, as given in table 3.

(3) Increase or decrease the BFO frequency, as required, by pressing the UP or DOWN key.

Table 3: BFO Tuning Rates

NUMERIC KEY	TUNING RATE (per second)
1	39 Hz
2	625 Hz
3	3.75 KHz

CHANNEL SELECTION

15. The receiver may be set to any one of the 100 channels as follows:

16. (1) Press and release the CHAN key. The receiver is now in the channel display-only mode, denoted by a flashing channel number display, where the number is that of the last channel previously accessed. The UP/DOWN keys are enabled, to increment or decrement the displayed channel, and the numeric keys are enabled, to allow selection of a particular channel number.

(2) Then either:

(a) Use the numeric keys to select the required channel number (00 to 99) starting with the 10's digit, or
(b) Press and hold the UP key or the DOWN key, as appropriate, until the required channel is displayed (the displayed channels are incremented or decremented at a rate of approximately two channels per second).

(3) Press and release the ENTER key to set the receiver to the displayed settings. Note that the UP, DOWN and numeric keys are still enabled allowing channelized operation and 'on-air' channel tuning. If the receiver operating conditions (frequency, mode, bandwidth, BFO or squelch) are subsequently modified, the channel number is blanked and the normal receiver mode is entered.

17. CHANNEL LOADING

Each of the 100 channels may be preset to a particular frequency and operating mode, without affecting receiver operation, as follows:

18. (1) Press and release the FREQ key.

(2) Enter the desired frequency using the numeric keys. If an error is made, repeat the procedure starting at (1).

(3) When the required frequency is correctly displayed, press the MODE key followed by the required mode key. Select SQLCH if required.

(4) Select the required bandwidth (using the BW+ or BW- keys) and set the BFO frequency, if required, as detailed in para 14.

(5) Verify the selected parameters by observing the display. If correct, press and hold the STORE key. The CHANNEL display is set to '-' and the numeric keys are enabled to allow selection of the required channel number.

(6) Using the numeric keys, select the required channel number, starting with the 10's digit.

(7) Release the STORE key. The frequency and mode data displayed on the front panel is now stored in the memory location for the selected channel.

(8) To display the actual receiver setting, press and release the RCL key.

Note: AT any time while operating the receiver, the current operating parameters may be stored using the above procedure commencing at step (5).

CHANNEL MEMORY CHECK

19. The contents of the channel memory may be checked at any time simply by pressing the CHAN key and then either the UP/DOWN keys or the numeric keys to display the channels. This procedure does not affect the operation of the receiver.

20. When the receiver is in the channel display-only mode, the content of a particular displayed channel may be modified at any time without affecting normal receiver operation. Note however, that modification to the frequency, mode, bandwidth, BFO or squelch causes the receiver to leave the channel display-only mode (flashing channel number) and to enter the normal display-only mode (flashing == channel display). The number of the modified channel is therefore lost and should be noted if reinstatement is required.

CHANEL MEMORY TRANSFER

21. The contents of one channel memory location may be transferred to a different location as follows.

22. (1) Press and release the CHAN key

(2) Use the UP/DOWN keys or the numeric keys to display the channel to be transferred.

(3) Press and hold the STORE key.

(4) Use the numeric keys to enter the new channel number (10's digit first).

(5) Release the STORE key.

REMOTE CONTROL

23. Pressing the REM key causes the REM display to toggle on and off. When illuminated, it indicates that the receiver is under remote (SCORE) control, where all front panel controls except the REM key are effectively disabled. When REM is not illuminated, the receiver is under local control from the front panel and any incoming SCORE data is ignored.

SELF-TEST MODE

24. The receiver contains a number of self-test routines which can be used to assist in the localisation of a fault. The self-test mode is entered by pressing simultaneously the MODE and TEST keys. This initiates a confidence display check where the displays are illuminated one at a time and then extinguished one at a time. This routine continues indefinately until further tests are initiated by the pressing of various key combinations, or until the self-test mode is terminated by again pressing simultaneously the MODE and TEST keys. For a detailed description of the self-test routines, refer to Chapter 19.

AGC TIME CONSTANT

25. When the receiver leaves the factory, the AGC time constants for each of the available detector modes are pre-programmed, as listed below. Thus under normal operating conditions, the appropriate pre-programmed AGC time constant is selected automatically when the MODE is selected, no manual control of the AGC time constant is available, and the selected AGC time constant is not displayed.

Table 4: AGC Time Constant Selection

MODE	AGC
AM	SHORT
FM	SHORT
CW	LONG
USB	LONG
LSB	LONG

26. To facilitate receiver testing and alignment, the AGC time constant may be set using certain front panel controls, as follows,

27. (1) Press and hold the MODE key, press the TEST key, and then release both keys together to set the receiver to the self-test mode.

(2) Press and release the CHAN key and then select channel 99 (press the numeral 9 key twice).

(3) Press and hold the MODE key, press the TEST key, and then release both keys together to exit from the self-test mode.

(4) Press and release the MODE key.

(5) The 7, 8 and 9 numeral keys may now be used to select short, medium or long time constants respectively, and manual gain control may be selected, either on its own or with long, medium or short, by pressing and releasing the SQLCH key.

(6) The selected AGC time constant is displayed, under BW, as follows:

SHORT:	5
MEDIUM:	n
LONG:	L
MANUAL:	.

28. To return the receiver to the normal operating mode (where AGC time constant selection is automatic), set the receiver to the self-test mode and then exit from the self-test mode without first selecting channel 99 i.e. perform steps (1) and (3) only of para. 27.

DF AGC MODE

29. The DF AGC mode (DAM) is designed for use with either the MA1110 or MA1122 Direction Finding Processors, both of which provide external AGC control of the receiver. In this mode the receiver IF gain is set to maximum in all modes, irrespective of the position of the IF GAIN control. The IF GAIN control can, however, still be used to set the squelch level in the FM mode and the COR threshold.

30. To enter the DAM proceed as follows:

(1) Press and hold the MODE key.

(2) Press and release the SQLCH key.

(3) Press the SQLCH key, and release the SQLCH and MODE keys together.

31. When the receiver is in the DAM the symbol d. is displayed between BW and BFO. The following points apply to this mode:

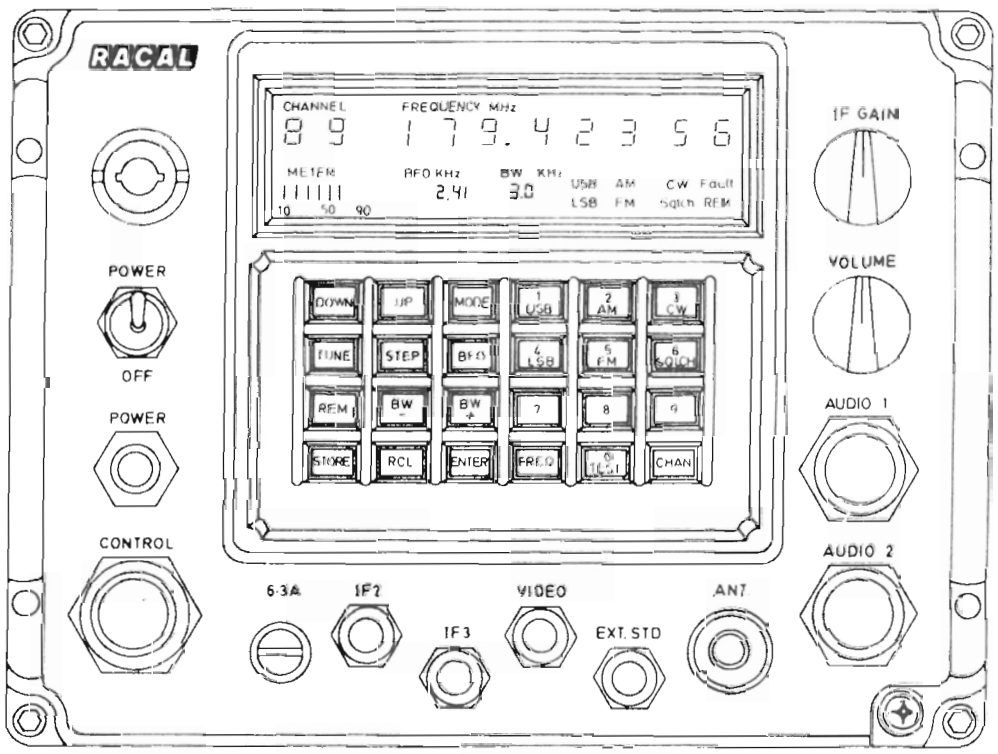
(1) The COR operates without the 5 second delay.

(2) The DAM is remembered during BITE routines and while the power is switched off.

(3) The DAM cannot be stored in the channel store. If storage is attempted the manual gain mode will be stored. If the AGC mode is enabled when the channel is recalled the receiver will be set to manual gain. If the AGC mode is not enabled the receiver will default to the appropriate AGC time constant.

(4) The DAM cannot be set on a receiver operating under remote control using the SCORE system. For remote DF applications manual gain must be sent to the receiver. In master-slave systems, where two receivers are linked together, the receiver in local control should be set to the DAM. The slave receiver will follow the local receiver, but will display manual gain instead of DAM.

32. To leave the DAM repeat the procedure given in paragraph 30.



RACAL MH 249

Front Panel Controls and Indicators Fig.3.1

CHAPTER 4

DISMANTLING AND RE-ASSEMBLY

CONTENTS

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CHAPTER 4

DISMANTLING AND RE-ASSEMBLY

INTRODUCTION

1. This Chapter provides instructions for gaining access to the printed circuit cards, printed circuit boards, sub-assemblies and chassis-mounted components. In general, the re-assembly is the reversal of the dismantling procedure. When re-assembling, ensure that all screws are replaced complete with the washers provided. Refer to figs 4.1 to 4.3 (at the end of the Chapter) for component location information.

O-RING SEALS

2. The receiver case assembly is fitted with four O-ring seals to prevent the ingress of moisture. One O-ring is fitted between the front panel bezel assembly (containing the display window and the keypad) and the front panel, one is fitted between the front panel assembly and the receiver case, one is fitted between the rear panel and the receiver case, and the last is fitted between the power supply assembly and the rear panel. To achieve the required degree of sealing, all four O-rings are lightly smeared with silicone grease (Racal 905486), the four screws securing the front panel bezel to the front panel are tightened to a torque of 15 lb. in. (1.7 Nm) whilst the socket-headed screws securing the receiver to the case (four at the front panel, ten at the rear panel) are tightened to a torque of 36 lb. in (4.1 Nm).

3. A further rubber seal is fitted between the red display window and the front panel bezel. Do not apply silicone grease to this seal as damage to the window may result.

4. Additional torque figures are given in table 1 for the various front-panel components. Should it be necessary to replce any of these components, the securing nuts should be tightened to the torque figures given. Note that an O-ring seal is fitted to each of the front panel connectors.

Table 1 : Torque Figures

ITEM	TORQUE FIGURES			
	MIN		MAX	
	lb.in.	Nm	lb.in.	Nm
IF GAIN	40	4.5	54	6.1
VOLUME	40	4.5	54	6.1
EXT STD	40	4.5	54	6.1
VIDEO	40	4.5	54	6.1
IF3	40	4.5	54	6.1
IF2	40	4.5	54	6.1
POWER	40	4.5	54	6.1
POWER SWITCH	50	5.7	66	7.5
AUDIO 1	60	6.8	78	8.9
AUDIO 2	60	6.8	78	8.9
ANT	50	5.7	66	7.5
CONTROL	70	7.9	90	10.2
FUSE HOLDER	4	0.45	4	0.45
DESICCATOR				

SCREENING COVERS

5. The screening covers, for the synthesizer board, 20 MHz board, first mixer/VCO board and the second mixer/640 MHz board are fitted with gaskets. When a cover is replaced, ensure that all screws are fully tightened so that the gasket is compressed to form an effective RF screen. For optimum results the gasket should be replaced each time a cover is removed.

SEMI-RIGID COAXIAL CONNECTORS

6. The low pass filter connections between the first mixer/VCO board and the front panel ANTENNA socket are made using short lengths of semi-rigid coaxial cable, terminated with coaxial plugs (PL49, PL50 and PL59). When re-assembling these connectors a torque wrench (Racal 940824) should be used to tighten the 8 mm nuts (an internal ratchet releases when a nut has been tightened to a torque figure between 7 lb.in and 10 lb.in or 0.8 Nm and 1.2 Nm).

RECEIVER CASE REMOVAL

7. (1) Disconnect all cables from the front of the unit.

(2) Place the unit on its rear panel on a flat clean working surface.

(3) Using a 4 mm key, remove the four socket-headed screws, one at each corner of the front panel.

(4) Turn the receiver over so that it rests on the front panel handles.

(5) Remove the six captive socket-headed screws securing the case to the power supply assembly.

(6) Carefully slide the case upwards until it is clear of the receiver.

PRINTED CIRCUIT CARD REMOVAL

8. The mother board contains seven edge connectors to accommodate the printed circuit cards, as listed in table 2. Note that the SCORE interface card (edge connector number 2) is an optional item.

CAUTION: DO NOT REMOVE OR INSERT A CARD WITH THE POWER APPLIED.

9. The edge connectors are numbered (front to back) from 1 to 7, and the coresponding number is printed in a circle on each card. Take care to insert the cards into the correct positions. To remove a card, release the self-captive screws and slide the card upwards. The display driver card (in socket 1) is also connected via ribbon cable connectors SK28 and SK29 to the front panel-mounted display board.

Table 2 : Printed Circuit Cards

CARD	SOCKET NUMBER
Display Driver	1
SCORE Interface	2
Processor	3
Extender	4
Demodulator	5
AGC	6
IF Filter	7

REMOVAL OF SECOND MIXER (640 MHz MODULE)

10. Remove the two screws, each with a crinkle washer, securing the module to each of the two chassis side panels. Disconnect coaxial connectors SK12, SK14, SK15 and SK16, together with ribbon cable connector SK6, and remove the module. To gain access to the second mixer (640 MHz board, release the ten captive screws securing the module cover, and remove the cover. To remove the board from the module, disconnect coaxial connectors SK59, SK60, SK61 and SK70, disconnect ribbon cable connector SK38, and then release the two captive screws securing the board to the module.

REMOVAL OF POWER SUPPLY MODULE

11. (1) Remove the four self-captive screws securing the module to the rear of the receiver.

(2) Remove the ribbon cable connector from PL27, the supply connectors from PL62 and PL63, and remove the module.

(3) Should it be necessary to remove the power supply board, note the wire insulation colours before unsoldering the wires from the board pins. Then remove the ten securing screws, each with a spring washer and a flat washer.

(4) To gain access to the 5.5 V and 15 V modules, remove the cover assembly attached to the heat sink by twelve screws. The modules are each attached to the cover by two screws.

FREQUENCY STANDARD REMOVAL

12. (1) Remove the two screws, each with a crinkle washer, securing the frequency standard bracket to the left-hand chassis side member.

(2) Release the two captive screws securing the frequency standard bracket to the cast chassis.

(3) Disengage the frequency standard module, complete with mounting bracket, from the B7G connector.

FRONT PANEL ASSEMBLY REMOVAL

13. (1) Place the receiver underside uppermost to gain access to the rear of the front panel ANTENNA socket.

(2) Using an 8 mm spanner, release the nut securing PL59 (low-pass filter connection) to the antenna socket.

NOTE: A torque wrench should be used when re-assembling this connector (see paragraph 6).

(3) Turn the receiver over and position such that the front panel assembly overhangs the work surface.

(4) Remove the three screws through the front edge of each of the two chassis side members securing the front panel assembly.

(5) Carefully ease the front panel assembly forward until it is clear of the reciever chassis assembly. The front panel assembly may now be lowered to 'hinge' on the connecting cableforms, to rest on the handles.

(6) To completely remove the front panel assembly, disconnect coaxial connectors SK12 from the first mixer/640 MHz module, SK8 and SK9 from the motherboard, and SK30 from the chassis assembly.

(7) Disconnect ribbon cable connectors SK4 and SK66 from the mother board and SK28 and SK29 from the display driver card.

(8) Finally, separate the push-on supply connections located on the inner front face of the left-hand chassis side member.

MOTHER BOARD REMOVAL

14. (1) Remove the second mixer/640 MHz module (para 10).

(2) Remove the front panel assembly (para 13).

(3) Disconnect coaxial connectors SK10 and SK11 from the mother board (the other end of the SK10 cableform should also be free as it mates with PL14 on the previously removed second mixer/640 MHz module).

(4) Disconnect ribbon cable connectors SK5 and SK7 from the mother board.

(5) Release the nine captive securing screws and remove the mother board.

FIRST MIXER/VCO BOARD REMOVAL

15. (1) Remove the compartment cover secured with eight captive screws.

(2) Use an 8 mm spanner to release the nut securing PL50 to the low-pass filter.

NOTE: A torque wrench should be used when re-assembling this connector (see paragraph 6).

(3) Disconnect coaxial connectors SK25 and SK26.

(4) Disconnect ribbon cable connector SK41.

(5) Release the two captive securing screws and remove the board.

20 MHz REFERENCE BOARD REMOVAL

16. (1) Remove the compartment cover secured with eight captive screws.

(2) Disconnect coaxial connectors SK20 to SK24 inclusive and ribbon cable connector SK40.

(3) Release the four captive securing screws and remove the board.

SYNTHESIZER BOARD REMOVAL

17. (1) Remove the compartment cover secured with ten captive screws.

(2) Disconnect coaxial connectors SK18 and SK19, and disconnect ribbon cable connector SK39.

(3) Release the two captive securing screws and remove the board.

DISPLAY AND SWITCH BOARD REMOVAL

18. (1) Lower the front panel assembly so that it rests on the handles (para. 13). It may be found necessary to disconnect ribbon cable connectors SK4 and SK66 from the motherboard, and also SK28 and SK29 from the display driver card.

(2) Disconnect ribbon cable connectors SK2 and SK3 from the display and switch board.

(3) Remove the nine screws, each with a crinkle washer, securing the display and switch board. Note that the three screws nearest to the bottom edge of the front panel are also used to secure the cable clamp.

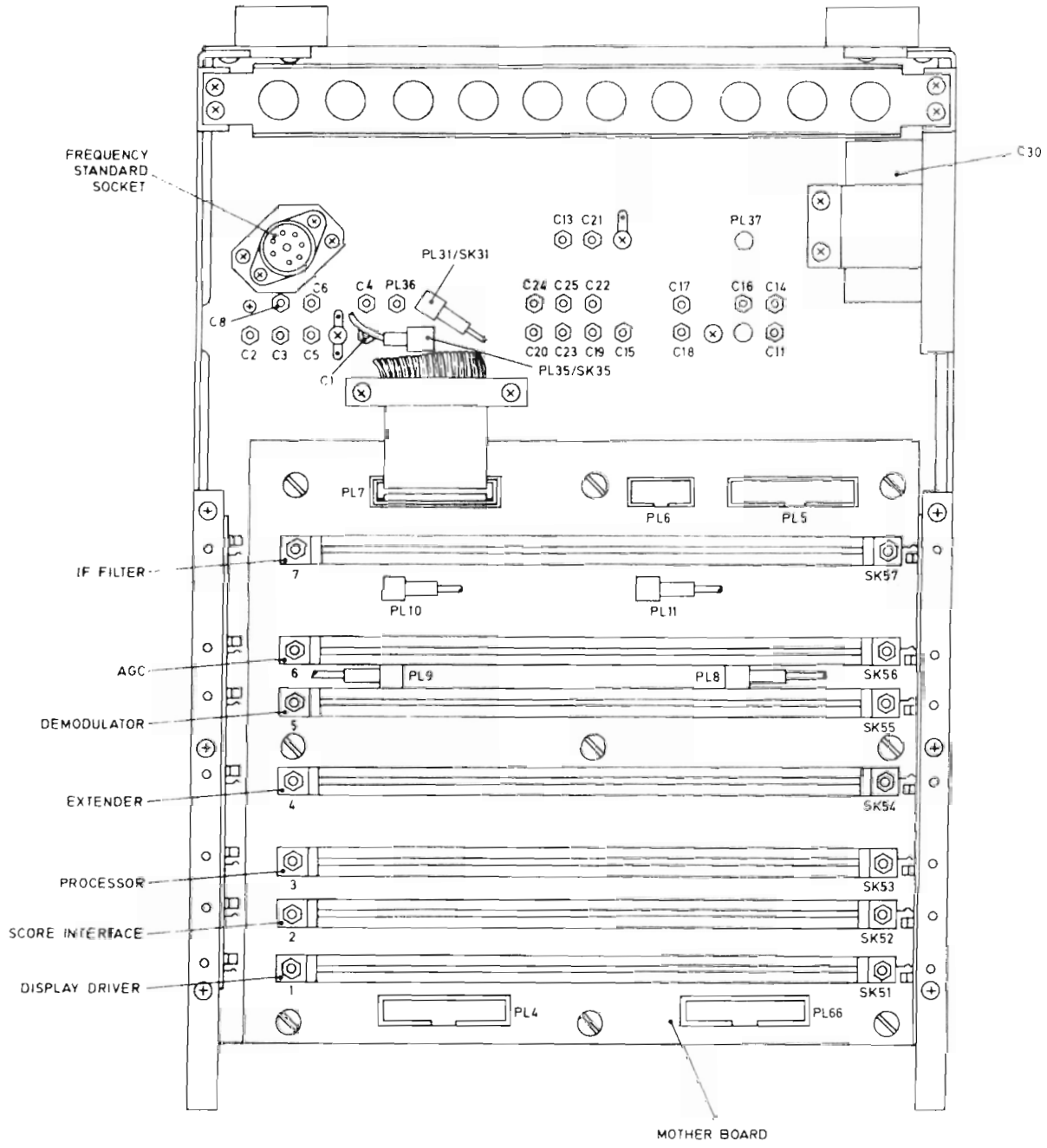
(4) Lift out the board.

FRONT PANEL BEZEL ASSEMBLY REMOVAL

19. (1) Lower the front panel assembly (para 13).

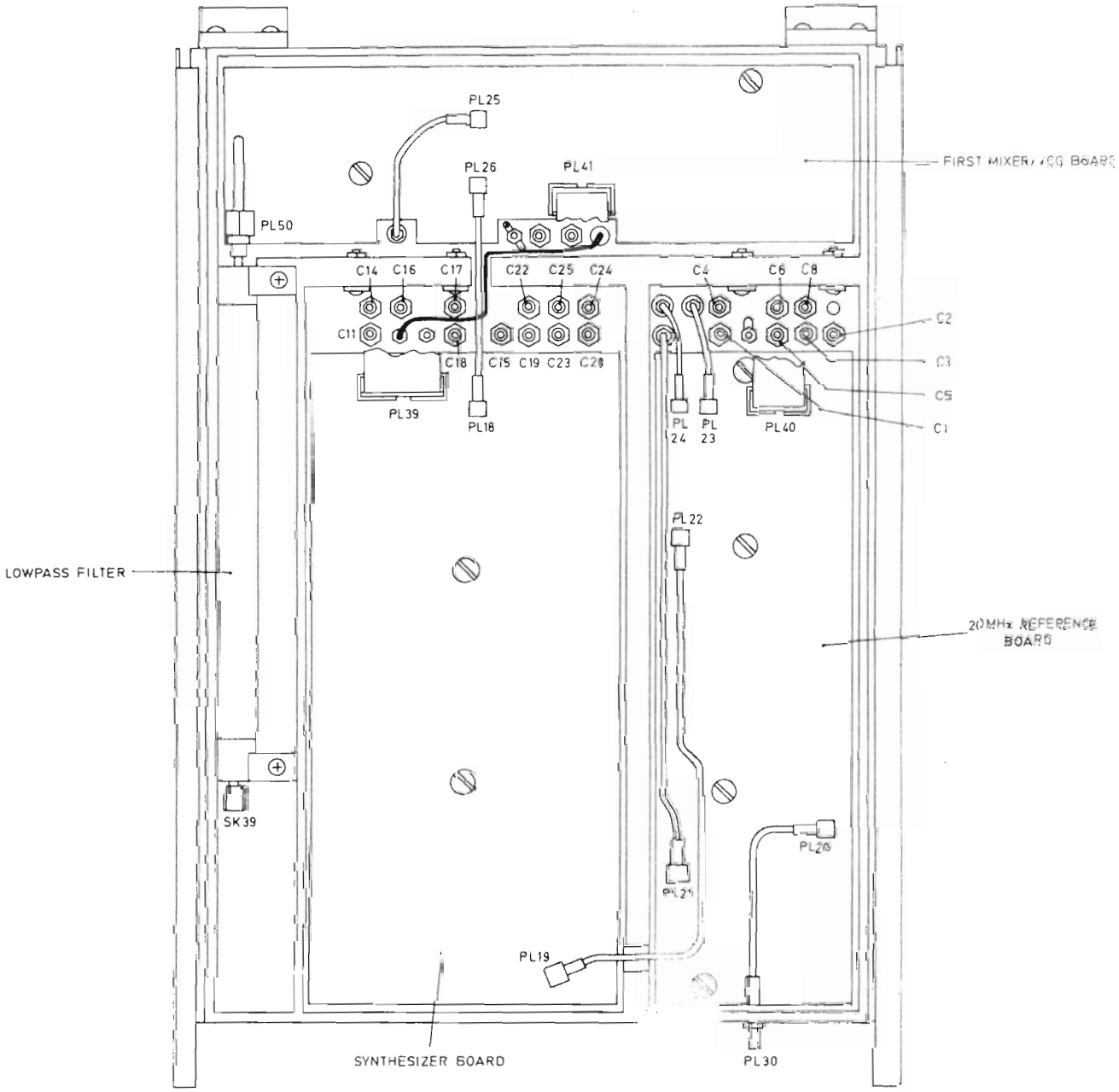
(2) Remove the display and switch board (para 18).

(3) Remove the four screws, each with a crinkle washer, securing the front panel bezel, one at each corner.



RACAL TM2449

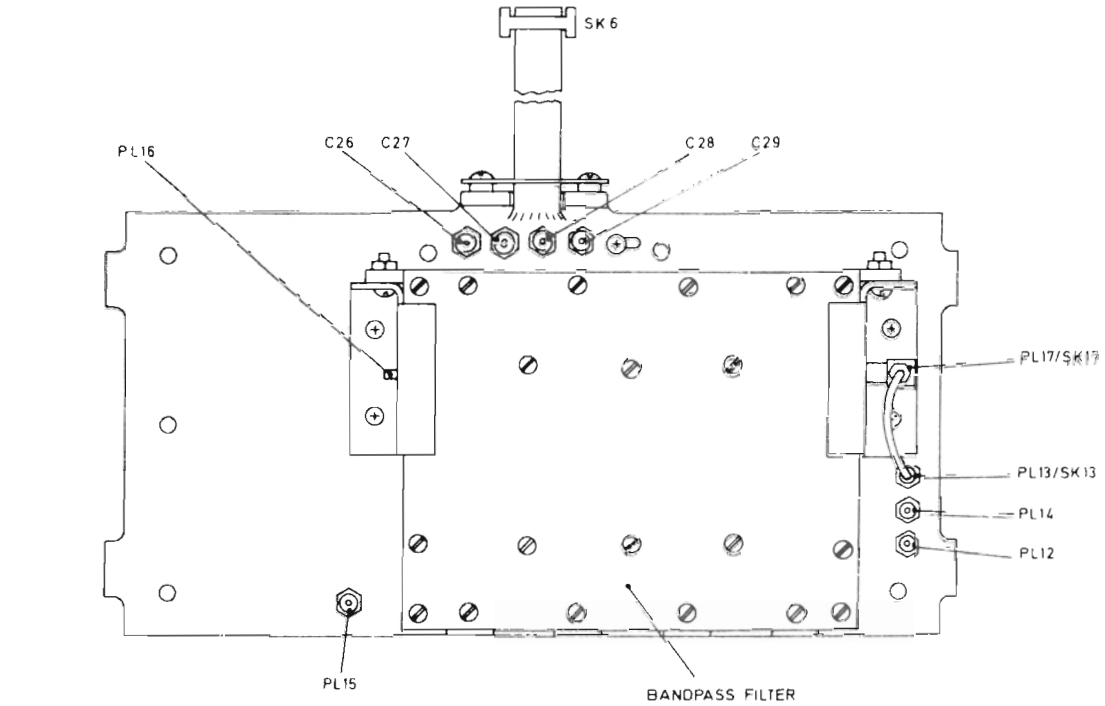
Layout: Main Chassis Assembly - Top View Fig.4.1

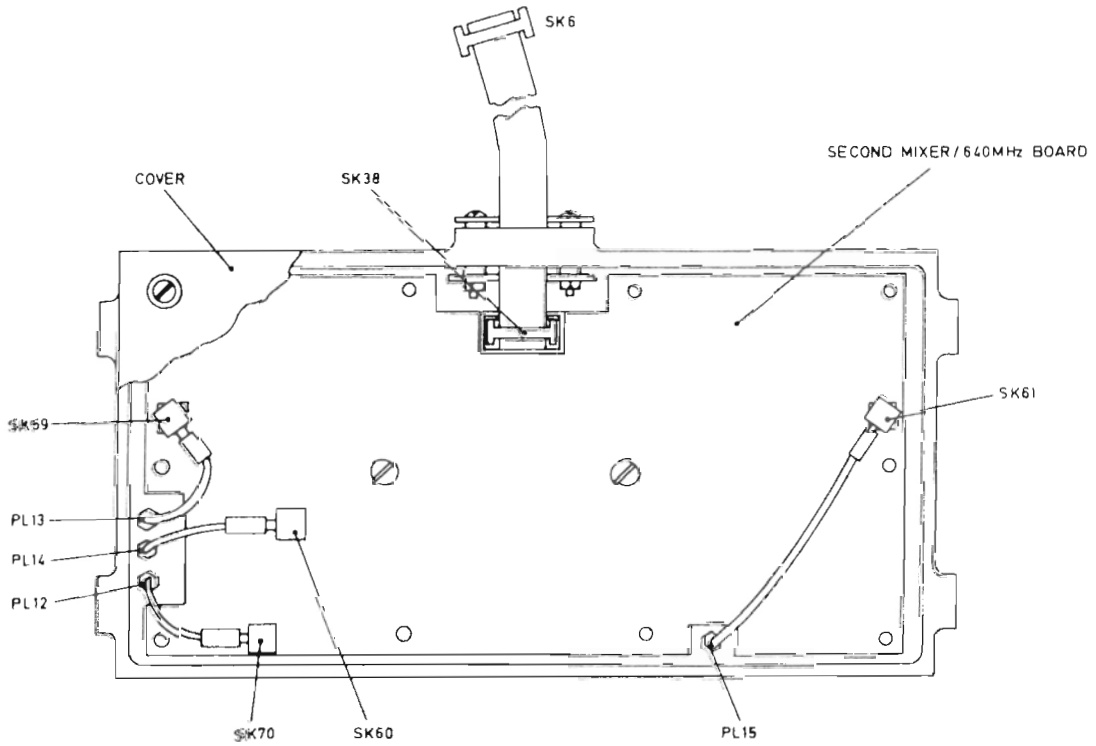


RACAL TH 2449

Layout: Main Chassis Assembly - Underside View

Fig.4.2





RACAL TH2449

Layout: Second Mixer/640MHz Module Fig.4.3

CHAPTER 5

DISPLAY AND SWITCH BOARD

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At end of chapter

CHAPTER 5

DISPLAY AND SWITCH BOARD

INTRODUCTION

1. The display and switch board is mounted on the inner face of the front panel bezel, and houses the LED displays and the 24 key-switches. Electrical connections are made via two ribbon cable and connector assemblies which mate with the display driver card (Chapter 6).

KEY SWITCHES

2. Each of the 24 key switches consists of a snap dome assembly fitted over a single pair of gold-plated pads on the printed circuit board. When finger pressure is applied to the actuating rubber key, the spring-steel dome 'snaps' and bridges the two pads, thus performing a single-pole push-to-make switching action.

CIRCUIT DESCRIPTION (Fig. 5.1)

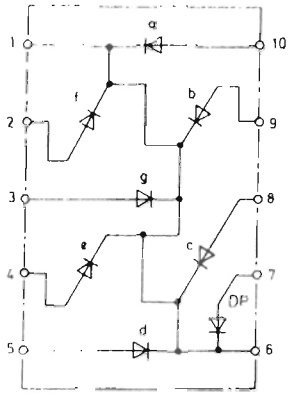
3. A time-sequential strobing type display system is used, where eleven strobe signals, designated digit 0 to digit 10, are used to sequentially display up to 16 bits of display data per strobe pulse. A 10 kHz clock signal is used (on the display driver card) to generate the strobe signals, and since 11 strobes are produced (table 1), the repetition rate is approximately 900 Hz.

Table 1: Display Strobes

STROBE	DISPLAYS	
DIGIT 0	10 Hz & 100 Hz	FREQUENCY DIGITS
DIGIT 1	1 kHz & 10 kHz	
DIGIT 2	100 kHz & 1 MHz	
DIGIT 3	10 MHz & 100 MHz	
DIGIT 4	CHANNEL, MSD & LSD	
DIGIT 5	BFO FREQUENCY	
DIGIT 6	DIGITS AND	
DIGIT 7	BANDWIDTH	
DIGIT 8		
DIGIT 9	METER	
DIGIT 10	MODE, SQUELCH FAULT AND REMOTE	

Channel and Frequency Displays

4. The channel and frequency displays (ML1 to ML10) are high-efficiency, 0.3 inch, seven-segment, common cathode devices, each with a right-hand decimal point (fig. 5(a)). They are operated in pairs by applying the strobe signal to the interconnected common cathode pins of two devices and simultaneously applying the a to h and A to H display data to the anode pins to illuminate the appropriate segments.

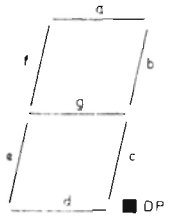


PIN	CONNECTION
1	COMMON CATHODE
2	ANODE f
3	ANODE g
4	ANODE e
5	ANODE d
6	COMMON CATHODE
7	DP ANODE
8	ANODE c
9	ANODE b
10	ANODE a

Fig. 5(a) 7-Segment Display HP5082-7613

BFO Frequency and BW Displays

These displays are provided by two 0.11 inch 4-digit 7-segment devices, ML12 and ML13; these are designed for strobed operation in that the four sets of segments are connected in parallel and the four individual common cathodes are brought out to separate pins for strobing purposes (Fig. 5(b)).



PIN	CONNECTION	PIN	CONNECTION
1	CATHODE 1	7	ANODE g
2	ANODE e	8	ANODE d
3	ANODE c	9	ANODE f
4	CATHODE 3	10	CATHODE 2
5	DP ANODE	11	ANODE b
6	CATHODE 4	12	ANODE a

Fig. 5(b) 4-Digit 7-Segment Display HP5082-7414

Meter Display

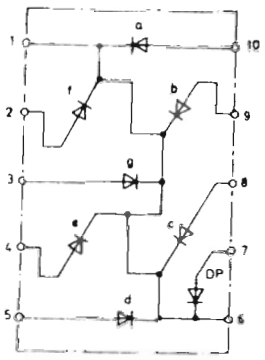
6. The bar graph-type meter scale is produced using a ten-element linear display device ML11. The individual cathode connections (C1 to C10) are connected in parallel and are controlled by the digit 9 strobe signal.

Mode, Squelch, Fault and Remote Displays

7. The remaining displays are illuminated using four twin light-bar modules ML14 to ML17. Each module contains two pairs of light emitting diodes; the two diodes forming each pair are externally connected in parallel and are illuminated to display the associated legend on the inner face of the red display filter.

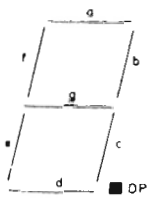
Key Switches

8. The key switches are connected as a four-row by six-column matrix. The matrix is scanned by sequentially applying a 0 V signal to the four row lines and then reading the six column lines to see whether a key is pressed.



PIN	CONNECTION
1	COMMON CATHODE
2	ANODE f
3	ANODE g
4	ANODE e
5	ANODE d
6	COMMON CATHODE
7	DP ANODE
8	ANODE c
9	ANODE b
10	ANODE a

Fig. 5(a) 7-Segment Display HP5082-7613



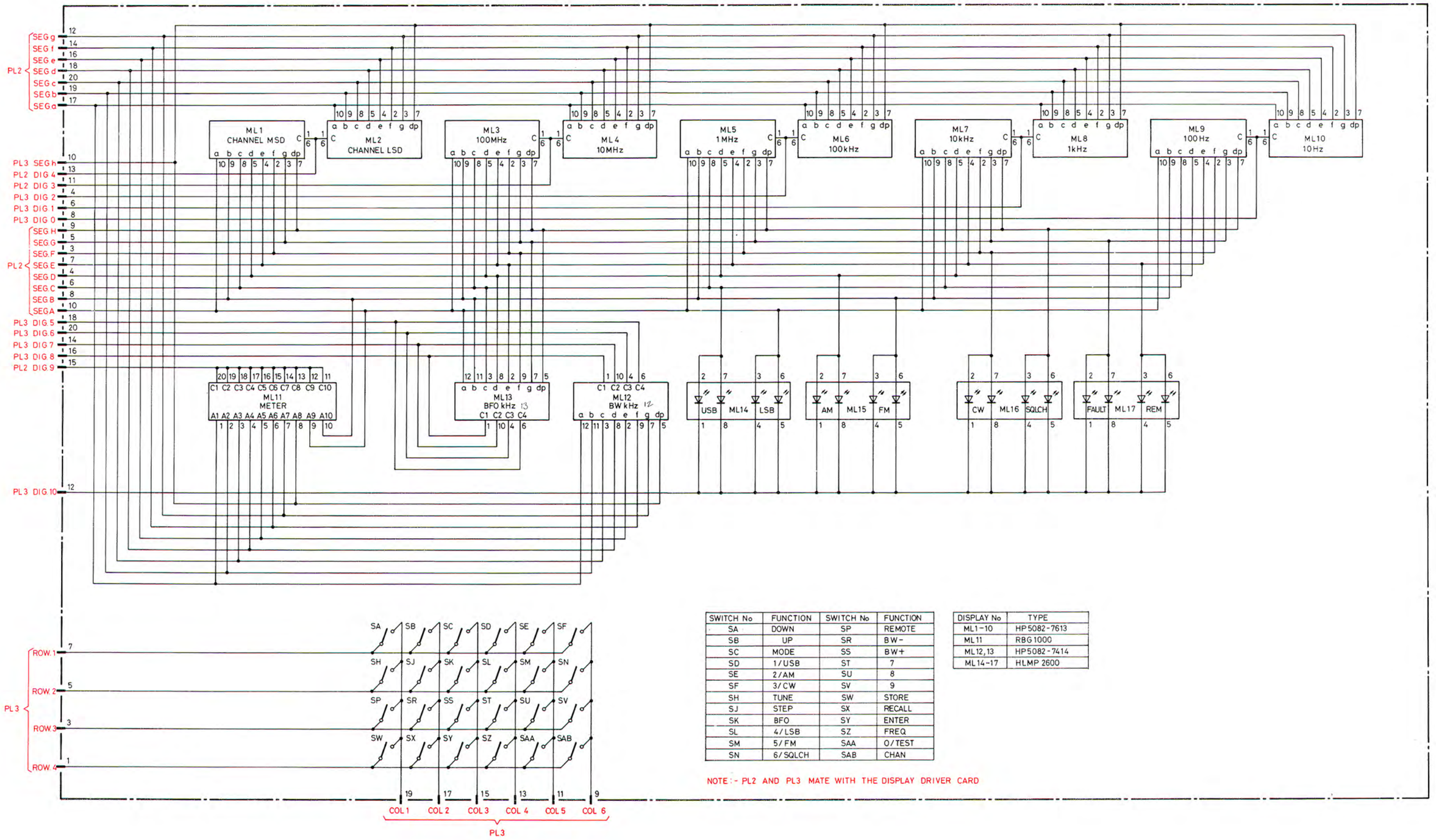
PIN	CONNECTION	PIN	CONNECTION
1	CATHODE 1	7	ANODE g
2	ANODE e	8	ANODE d
3	ANODE c	9	ANODE f
4	CATHODE 3	10	CATHODE 2
5	DP ANODE	11	ANODE b
6	CATHODE 4	12	ANODE a

Fig. 5(b) 4-Digit 7-Segment Display HP5082-7414

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		DISPLAY AND SWITCH BOARD (ST 79806)			
		Connectors			
PL2		Plug, 20-way			938861
PL3		Plug, 20-way			938861
		Integrated Circuits			
ML1		7-segment Display HP 5082-7613			938870
ML2		7-segment Display HP 5082-7613			938870
ML3		7-segment Display HP 5082-7613			938870
ML4		7-segment Display HP 5082-7613			938870
ML5		7-segment Display HP 5082-7613			938870
ML6		7-segment Display HP 5082-7613			938870
ML7		7-segment Display HP 5082-7613			938870
ML8		7-segment Display HP 5082-7613			938870
ML9		7-segment Display HP 5082-7613			938870
ML10		7-segment Display HP 5082-7613			938870
ML11		Bar Display RBG 1000			938871
ML12		4 x 7-segment Display HP 5082-7414			938869
ML13		4 x 7-segment Display HP 5082-7414			938869
ML14		Light Bar Display HLMP 2600			938889
ML15		Light Bar Display HLMP 2600			938889
ML16		Light Bar Display HLMP 2600			938889
ML17		Light Bar Display HLMP 2600			938889
		Miscellaneous			
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			946979

NOTE

Switches SA to SA8 are manufactured as part of the printed circuit board and are thus non-repairable.



SWITCH No	FUNCTION	SWITCH No	FUNCTION
SA	DOWN	SP	REMOTE
SB	UP	SR	BW−
SC	MODE	SS	BW+
SD	1/USB	ST	7
SE	2/AM	SU	8
SF	3/CW	SV	9
SH	TUNE	SW	STORE
SJ	STEP	SX	RECALL
SK	BFO	SY	ENTER
SL	4/LSB	SZ	FREQ
SM	5/FM	SAA	0/TEST
SN	6/SQLCH	SAB	CHAN

DISPLAY No	TYPE
ML1−10	HP5082-7613
ML11	RBG1000
ML12,13	HP5082-7414
ML14−17	HLMP 2600

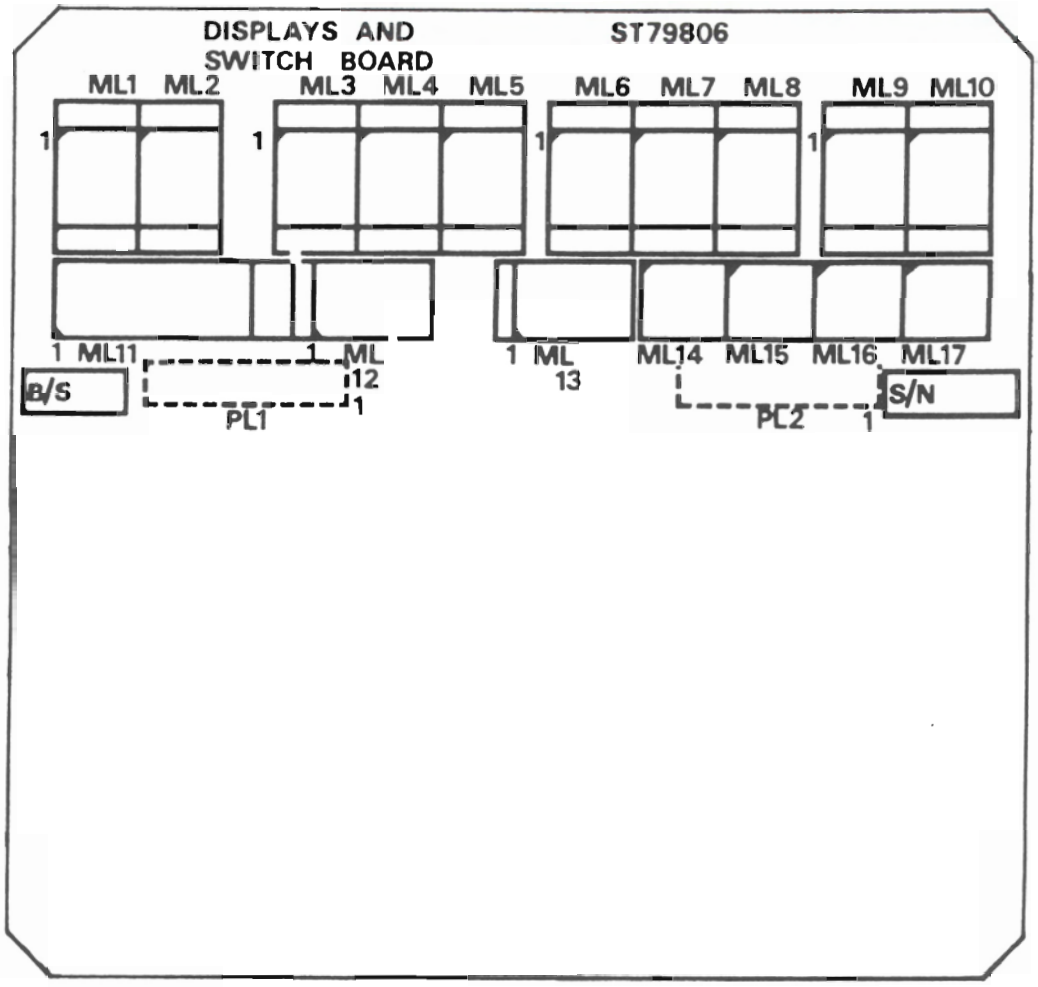
NOTE:- PL2 AND PL3 MATE WITH THE DISPLAY DRIVER CARD

RACAL

TH2449	DC79806	5.1
1		1/2

TH2449	DC79806	5.1
1		2/2

Circuit: Display and Switch Board Fig.5.1



ED 79805/4 [1]

Layout: Display Board Fig. 5.2

CHAPTER 6

DISPLAY DRIVER CARD

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At end of Chapter

CHAPTER 6

DISPLAY DRIVER CARD

INTRODUCTION

1. This card interfaces the front panel key switches to the processor card and produces the drive signals for the front panel displays. The circuit diagram is given in fig. 6.1 at the end of the Chapter.

CIRCUIT DESCRIPTION

Key Switch Interface

2. The front panel key switches are scanned once every 32 milliseconds (approximately) by the CPU. A positive-going strobe pulse (strobe 8) from the processor card (at PL51 pin 42) is inverted by ML11a and applied to:

   (1) The enable input ('0' to enable) of a binary to 1-of-4 inverting decoder ML11b (table 1).

   (2) The disable inputs ('1' to disable) of a hex tri-state buffer ML10.

3. The levels present on the A0 and A1 address bus lines (binary 0, 1, 2 or 3) are decoded by ML11b to produce a '0' at the appropriate keyboard row (input) line, and the resulting keyboard column (output) signals are applied to the processor board via ML10 and the I/O bus.

Table 1: Binary to 1-of-4 Decoder Truth Table

INPUTS			OUTPUTS							
ENABLE	SELECT		NON INVERTING (4555)				INVERTING (4556)			
E	B	A	Q3	Q2	Q1	Q0	$\overline{Q3}$	$\overline{Q2}$	$\overline{Q1}$	$\overline{Q0}$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X denotes 0 or 1

Display Data Memory

4. The display data is held in RAM on the processor card and is periodically transferred to the RAM on the display driver card. This transfer occurs regularly every half second and additionally every time the data changes.

5. The four RAM devices on the display driver card (ML6 to ML9) are of the C-MOS type and are 16-word by 4-bit organised. Each device has four address input lines (A,B,C and D), four data input lines (DI1 to DI4), a write enable ($\overline{WE}$) input, a memory enable ($\overline{ME}$) input, and four tri-state data outputs (DO1 to DO4). For writing data to the memory, the devices are connected in pairs (ML9, ML6 and ML8, ML7) and 22 bytes of data are loaded in from the I/O bus. This data is subsequently read from RAM organised as eleven by 16-bit words.

RAM Write Sequence

6. The processor write-to-RAM sequence is initiated by setting the display control signal, at PL51 pin 36, to a '1'. This is routed to:

(1) The enable ($\overline{EN}$) input of the clock pulse generator ML2a, as a disable signal.

(2) The B input of a binary to 1-of-4 non-inverting decoder ML2b.

(3) NOR gate G2, forcing the output to a '0'; this is routed to NOR gates G3 and G4, and to NAND gates G6 to G16 to prevent generation of digit outputs 0 to 10.

(4) The preset enable (PE) input of binary up-counter ML17 (up/down input permanently at '1'). The levels present on the A1 to A4 address bus lines are then routed through ML17 to the parallel-connected address lines of the four RAM devices.

7. The positive-going strobe 7 pulse, at PL51 pin 38, now occurs; this is inverted by ML11a (table 1), ML2b is enabled, and the level present at the A0 address bus line is decoded to produce a '1' at the Q2 output (A0 = '0') or a '1' at the Q3 output (A0 = '1'). The effect of this is to produce a '0' at the output of G5, which is applied to the write enable ($\overline{WE}$) inputs of all four RAM devices, and a '0' at the output of either G3 or G4 to enable RAM device pair ML8, ML7, or RAM device pair ML9, ML6, dependent on the state of the A0 address bus line. Bytes of data are thus written alternately into each pair of RAM devices.

RAM Read Sequence

8. One 16-bit word of display data is read from the RAM approximately every 100 microseconds except when the processor is writing data into the RAM. A nominal 10 kHz clock signal from the processor card, at PL51 pin 35, is applied direct to the B input, and via delay components R1, C2 to the A input of binary to 1-of-4 non-inverting decoder ML2a. Provided a '0' is present at PL51 pin 36, then ML2a is enabled, and nominal 2 microsecond

positive-going pulses are produced at the Q2 output (table 1). These pulses are routed to:

(1) NAND gate G1 which forms part of the display brilliance control circuit (para. 10).

(2) The clock input of up-counter ML17; the counter is incremented, and this in turn increments the 4-bit address applied to the RAM.

(3) NOR gate G2; the resulting negative-going output pulses are routed to:

(a) NAND gates G6 to G16 to blank the displays until the next 16 bits of display data have been read from RAM.

(b) NOR gates G3 and G4; the negative-going transition of the resulting prositive-going pulses at the outputs of G3 and G4, which are applied to the memory enable ($\overline{ME}$) inputs of the RAM devices, are used to latch the address, and the addressed data appears at the data output (DO) pins.

Digit Strobe Outputs

9. The eleven sequential digit strobe signals, Digit 0 to Digit 10, are produced by a 4-line to 16-line decoder ML14, NAND gates G6 to G16, and emitter-follower driver transistors TR1 to TR11. The truth table for the applicable states of ML14 is given in table 2. Note that when the up-counter ML17 reaches a count of 11 (A, B and D inputs of ML14 at '1'), ML17 is reset to zero by the '1' at the Q11 output of ML14, and a '1' occurs at the Q0 output of ML14.

Table 2: 4-line to 16-line Decoer Truth Table

INPUTS						OUTPUT
STROBE	INHIBIT	D	C	B	A	AT '1'
1	0	0	0	0	0	Q0
1	0	0	0	0	1	Q1
1	0	0	0	1	0	Q2
1	0	0	0	1	1	Q3
1	0	0	1	0	0	Q4
1	0	0	1	0	1	Q5
1	0	0	1	1	0	Q6
1	0	0	1	1	1	Q7
1	0	1	0	0	0	Q8
1	0	1	0	0	1	Q9
1	0	1	0	1	0	Q10
1	0	1	0	1	1	Q11
1	1	X	X	X	X	All at '0'

Display Brilliance

10. The display brilliance control circuit comprises inverting NAND gate G1 and a comparator ML3. It acts as a monostable where the mark-to-space ratio (duty cycle) of the Square wave output signal is set by R6. Since this output signal is applied to the inhibit input ('1' to inhibit) of ML14, the setting of R6 determines the period of time during each 100 microsecond clock period that drive is applied to the common cathode of the appropriate display device. The waveforms applied to the inhibit input of ML14 for two settings of R6 are shown in fig. 6(a).

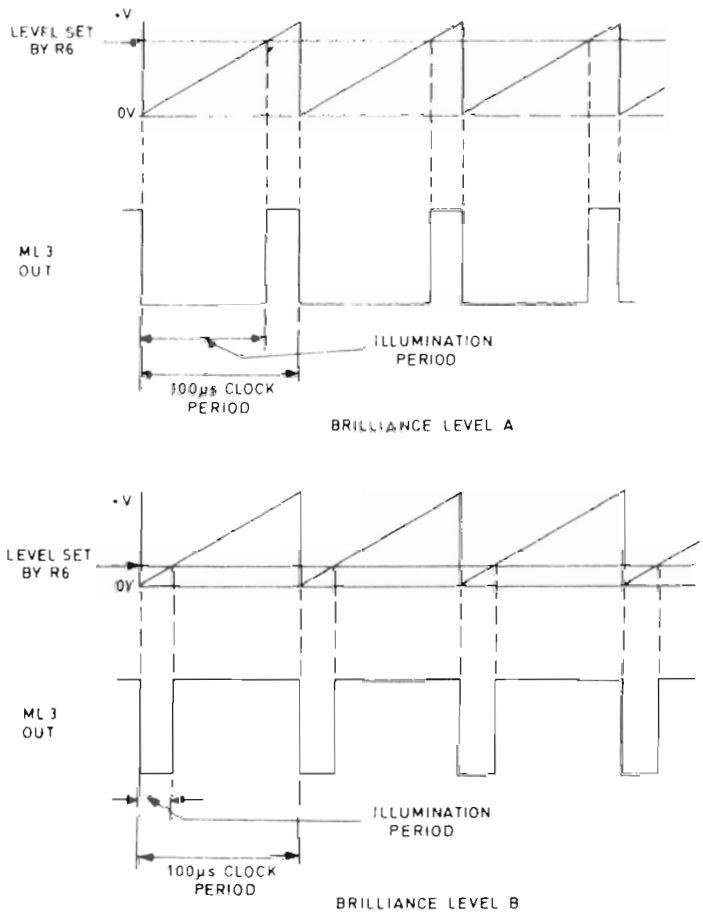
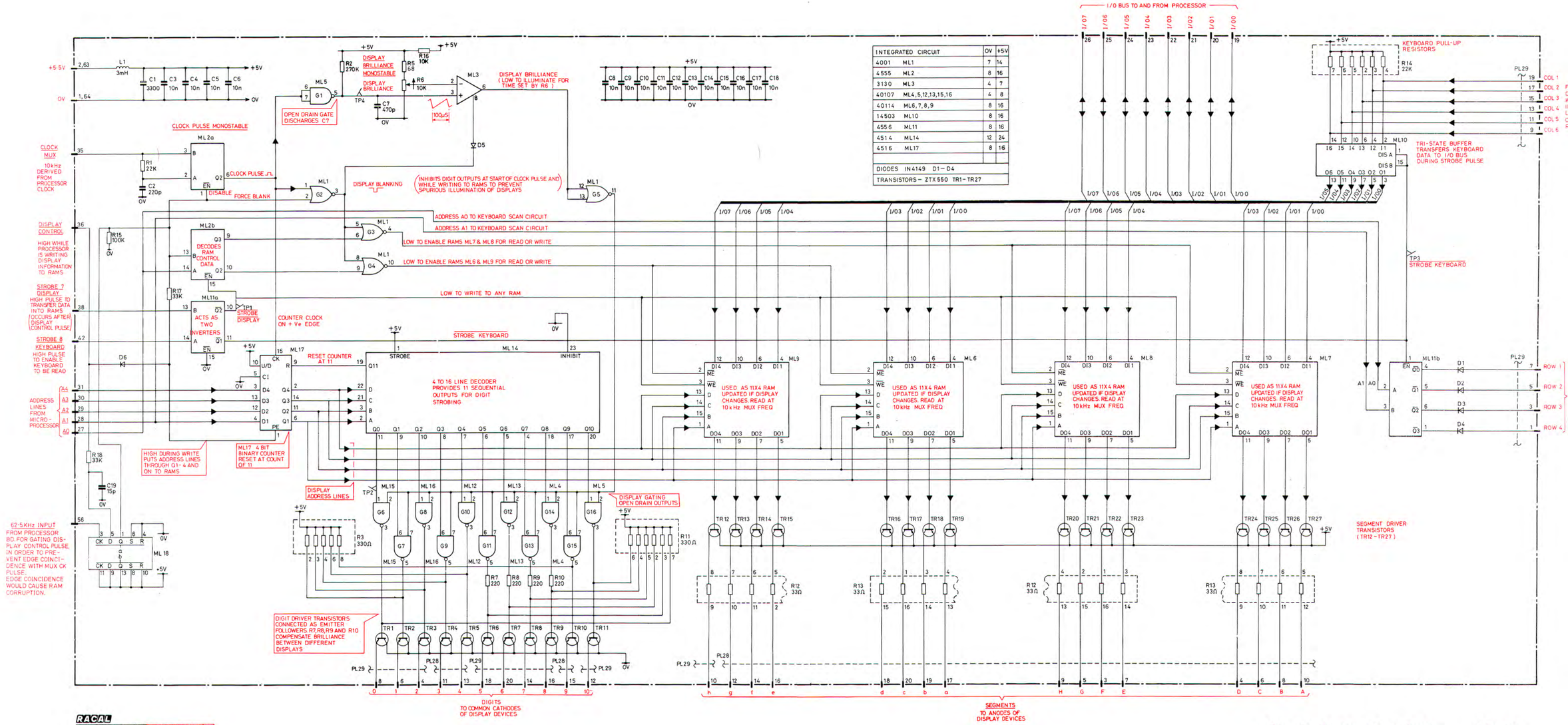


Fig. 6(a) Timing Diagram:Brilliance Level Waveform

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		DISPLAY DRIVER CARD (ST 79784)			
	Resistors				
R1	18 k	Metal Oxide		2	900944
R2	270 k	Metal Oxide		2	923598
R3	330	7-Resistor SIL Network		2	939168
R4	270 k	Metal Oxide		2	923598
R5	12 k	Metal Oxide		2	917952
R6	10 k	Variable, Preset		20	939328
R7	220	Metal Oxide		2	910390
R8	220	Metal Oxide		2	910390
R9	220	Metal Oxide		2	910390
R10	220	Metal Oxide		2	910390
R11	330	7-Resistor SIL Network		2	939168
R12	33	8-Resistor DIL Network		2	939171
R13	33	8-Resistor DIL Network		2	939171
R14	22 k	9-Resistor SIL Network		2	935012
R15	22 k	Metal Oxide		2	913493
R16	22 k	Metal Oxide		2	913493
R17	33 k	Metal Oxide		2	913495
R18	33 k	Metal Oxide		2	913495
	Capacitors		V		
C1	3300	Electrolytic	10	+50 -10	939329
C2	220p	Ceramic Disc	500	10	940308
C3	10n	Ceramic Disc	250	+40 -20	900067
C4	10n	Ceramic Disc	250	+40 -20	900067
C5	10n	Ceramic Disc	250	+40 -20	900067
C6	10n	Ceramic Disc	250	+40 -20	900067
C7	470p	Ceramic Disc	500	10	917453
C		Ceramic Disc	250	+40 -20	900067
C9	10n	Ceramic Disc	250	+40 -20	900067
C10	10n	Ceramic Disc	250	+40 -20	900067
C11	10n	Ceramic Disc	250	+40 -20	900067
C12	10n	Ceramic Disc	250	+40 -20	900067
C13	10n	Ceramic Disc	250	+40 -20	900067
C14	10n	Ceramic Disc	250	+40 -20	900067
C15	10n	Ceramic Disc	250	+40 -20	900067

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C16	10n	Ceramic Disc	250	+40 -20	900067
C17	10n	Ceramic Disc	250	+40 -20	900067
C18	10n	Ceramic Disc	250	+40 -20	900067
C19	15p	Ceramic Disc	500	10	940295
C20	47p	Ceramic Disc	500	10	917418
	Inductors				
L1	3 mH	Choke		10	AT 82475
	Connectors				
PL28		Plug, 20-way			938861
PL29		Plug, 20-way			938861
	Diodes				
D1		Silicon 1N 4149			914898
D2		Silicon 1N 4149			914898
D3		Silicon 1N 4149			914898
D4		Silicon 1N 4149			914898
D5		Silicon 1N 4149			914898
D6		Silicon 1N 4149			914898
	Transistors				
TR1-TR27		PNP Silicon ZTX550			931489

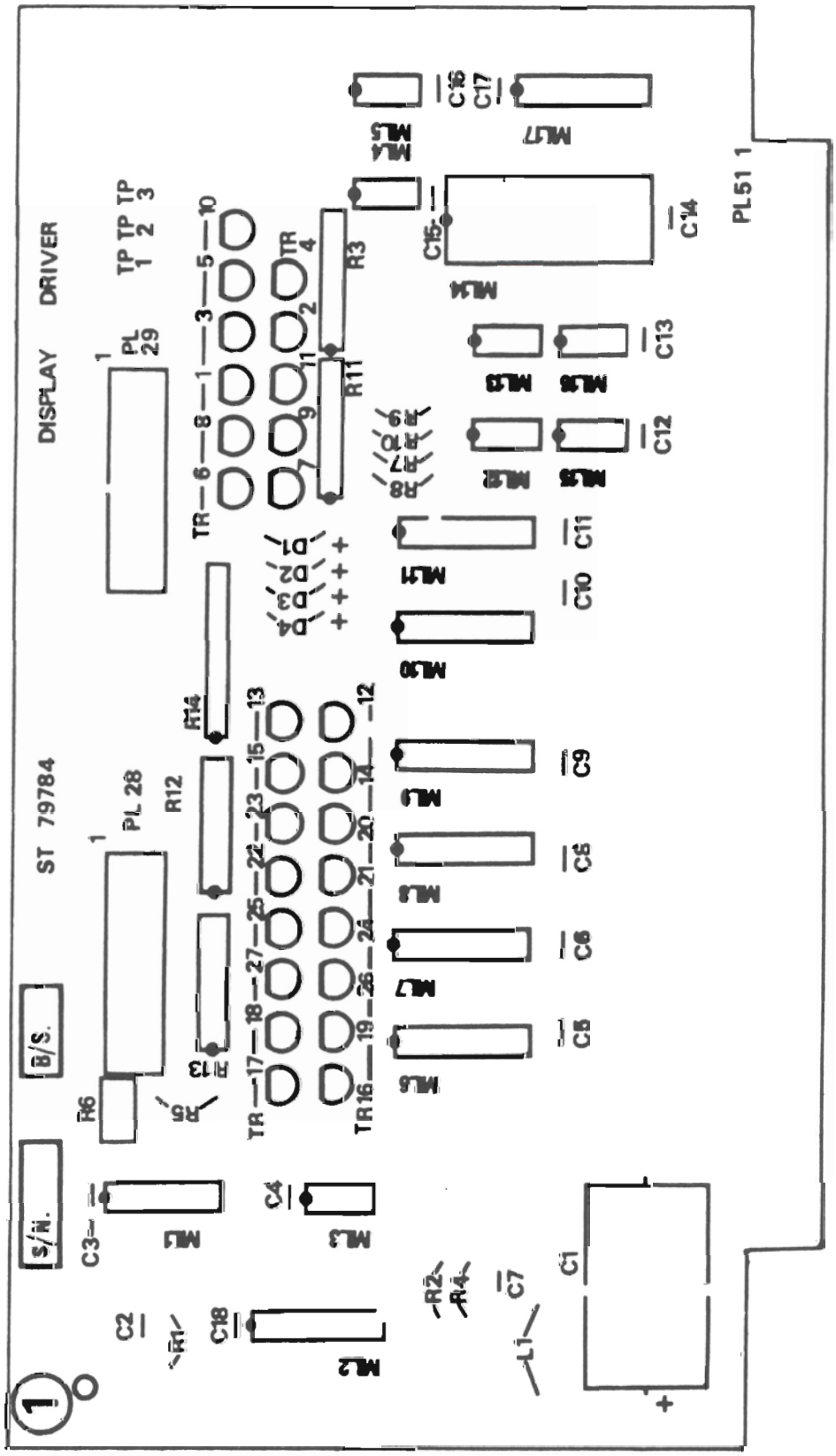
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Integrated Circuits			
ML1		Quad 2-input NOR gate 4001			930027
ML2		Dual Binary to 1-of-4 decoder 4555			928189
ML3		Operational Amplifier 3130			939327
ML4		Dual 2-input NAND buffer 40107			931052
ML5		Dual 2-input NAND buffer 40107			931052
ML6		16 x 4-bit RAM 40114			931647
ML7		16 x 4-bit RAM 40114			931647
ML8		16 x 4-bit RAM 40114			931647
ML9		16 x 4-bit RAM 40114			931647
ML10		Hex Tri-state Buffer 14503			931004
ML11		Dual Binary to 1-of-4 inverter 4556			929333
ML12		Dual 2-input NAND buffer 40107			931052
ML13		Dual 2-input NAMD buffer 40107			931052
ML14		4 to 16 line Decoder 4514			931010
ML15		Dual 2-input NAND buffer 40107			931052
ML16		Dual 2-input NAND buffer 40107			931052
ML17		Binary up/down counter 4516			929329
ML18		IC Type 4013			926860
		Miscellaneous			
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		24-pin DIL IC socket			930609
		Test Point			936148
		Board Stiffener			BD 79561
		Captive Screw M3 x 10 mm			AD 81976



RACAL

TH 2449	DC79784	6.1	TH2449	DC79784	6.1
1	1/2		1	2/2	

Circuit: Display Driver Card Fig. 6.1



Layout: Display Driver Card Fig. 6.2

CHAPTER 7

PROCESSOR CARD, ST83771

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CHAPTER 7

PROCESSOR CARD, ST83771

INTRODUCTION

1. The control circuits of the RA 1794A receiver uses four devices from the 1800 microprocessor family. These are located on the processor card. The CDP 1802 C-MOS Central Processing Unit (CPU) is an 8-bit register-orientated device which, in this application, uses a pair of CDP 1868 memory latch and decoder devices to interface with the memory devices (ROM, RAM, and EAROM) fitted to the processor card. The remaining device of the 1800 family is a CDP 1851 programmable input/output (PIO) interface device, which has two high-speed 8-bit I/O parts. One of these is used to produce a number of data strobe signals and to control a 16-line analogue multiplex circuit, whilst the other forms the main communications link between the CPU and the remainder of the receiver. The circuit diagram of the card is given in Fig 7.1 (at the end of the chapter).

NOTE:
The earlier ST79794 Processor Card is covered in Appendix 1. The associated Fault Finding is covered in Appendix 2.

Power On Reset

2. When the power is switched on C7 charges quickly to +2.56 V from the reference output at ML9 pin 7, while C6 charges slowly via R11 from the +5V A supply rail. This ensures that ML1d pin 5 is held negative with respect to ML1d pin 4 for a short period after switching on, holding the $\overline{\text{CLEAR}}$ line at ML1d pin 2 at logic '0'. Both the microprocessor, ML6, and the programmable input/output interface (PIO) ML13, are reset. Once C6 has charged to more than +2.56 V the $\overline{\text{CLEAR}}$ line goes to logic '1', putting ML6 to the run state and releasing ML13 ready for programming.

Address Bus Operation

3. Since the microprocessor has only eight address lines, the memory addresses occupy two bytes. The high-order byte (of which only seven bits are used) is put onto the address bus first, and is latched into ML10 or ML11 in synchronism with the timing pulse from ML6 pin 34. Note that, due to the connections at ML10 and ML11 pins 14, 15 and 16, the data on address lines A4 and A5 enter ML10 for addresses having address line A6 at logic '0' and ML11 for addresses having line A6 at logic '1'.

4. The high-order address byte is decoded by ML10 and ML11 into the required logic levels for address lines A8 and A9 (ML10) address lines A10 and A11 (ML11) and seven chip-select lines. The logic levels for lines A8 to A11 appear at the output immediately, but the decoded chip-select levels occur only when the memory read ($\overline{\text{MRD}}$) or the memory write ($\overline{\text{MWR}}$) inputs are taken to logic '0'.

Read-Only Memory Operation

5. To read from the read-only memory (ROM) the microprocessor puts the required address onto the address bus as described in paragraphs 3 and 4. According to the address a logic '0' will occur at either ML10 pin 13, ML10 pin 12 or ML10 pin 11, to select PD1, PD2 or PD3 when ML6 pin 7 ($\overline{MRD}$) is put to logic '0'. The data from the addressed location is then put onto the data bus and read by the microprocessor.

Electrically-Alterable ROM Operation

6. ML2 and ML3 are 1K by 4-bit, non-volatile electrically alterable read-only memory (EAROM) devices. They are used for the storage of pre-programmed channel information (channels 00 to 99), as well as the storage of the latest front panel setting information so that the receiver returns to these same settings when switched on again after a period of non-usage (the stored front panel control setting data is updated at one-minute intervals).

7. The functioning of the EAROM is controlled by the two control lines C0 and C1, which select the operating mode in accordance with Table 1. The EAROM is a comparatively slow operating system (the write cycle is 1ms and the erase cycle 10ms). For these functions the microprocessor sets the address, data and control code required, and these are latched into the appropriate device by the chip enable signal. The EAROM then processes the information independently of the microprocessor.

Table 1: EAROM Mode Control

C1	C0	Mode
0	0	Read
0	1	Write
1	1	Word erase

8. When the EAROM devices are in the write or the erase mode the timing requirements are such that the chip-select signals, decoded from the address bus signals in ML11, must occur before the $\overline{MWR}$ output from ML6 pin 35. To generate a negative-going enable signal for ML11 at the correct time, the positive going trailing edge of the $\overline{MRD}$ pulse from the previous microprocessor cycle is delayed and inverted (the previous cycle will have been a 'fetch' cycle, so the $\overline{MRD}$ pulse will always occur).

9. The trailing edge of the $\overline{MRD}$ pulse is fed to pin 7 of the shift register, ML20a. A positive-going transition occurs at ML20a pin 10 after a delay of four cycles of the clock waveform applied at ML20a pin 9. The positive-going edge clocks ML19a pin 2 to logic '0', and provides the required enabling signal for ML11. (Note that the internal structure of ML11 is such that the chip-select signal required for a write operation will be obtained even though the enabling signal is applied at the $\overline{MRD}$ input, pin 5).

10. The negative-going output from ML19a pin 2 is applied to ML20b pin 14, releasing ML20b from the reset condition. At the point in the cycle where the $\overline{MRD}$ and $\overline{MWR}$ outputs from ML6 pins 7 and 35 are both at logic '1', a logic '1' level is applied to ML20b pin 1, via ML12a, and ML20b pin 14 is clocked to logic '1'. This resets ML19a, terminating the chip-enable input to ML11 and resetting ML20b. Resetting ML20b releases ML19a, and the circuit is returned to the initial state.

11. The EAROM chip-select signals are connected to the devices via the tri-state buffer, ML14a. This provides protection of the EAROM when SB is closed for signature analysis, or under software control via ML13 pin 23.

Random-Access Memory Operation

12. The random-access memory (RAM) comprises two 256 x 4 bit devices connected as a single 256 x 8 bit store. To address the RAM the microprocessor puts the required address onto the address bus as described in paragraphs 3 and 4. The read or write mode is selected according to the logic level present at ML6 pin 35 ($\overline{MWR}$).

13. The RAM devices have two chip-select inputs. The first, $\overline{CS1}$, is decoded in ML11 from the high order address byte. The second, CS2, is derived from the $\overline{CLEAR}$ line. This is normally at logic '1', but goes to logic '0' if the +5V A supply falls below +4.75 V. The RAM is therefore automatically deselected during power failure, so protecting it against spurious inputs which might occur at such times.

14. The power supply for the RAM is maintained by means of a high value capacitor (C8) for approximately one minute after supply failure. This prevents the RAM contents being lost due to short duration interruptions in the supply.

Analogue Measurement

15. Provision is made for the microprocessor to monitor a number of analogue signal levels. These are connected to the 16-way multiplexer, ML17. When a measurement is to be made the microprocessor selects the required input by latching the appropriate multiplexer address at ML13 pins 18, 19, 21 and 22. The required signal level is then present at ML17 pin 1 and at pin 11 of the comparator, ML1a.

16. The microprocessor next addresses the digital-to-analogue converter (DAC) ML9, and puts a binary number on the data bus. (The chip-select signal for ML9 is decoded from the high-order address byte in ML11. Note that, due to the internal construction of ML11, the enable signal occurs when ML11 pin 6, not pin 5, goes to logic '0'). The analogue output of the DAC is applied to ML1a pin 10 via ML8.

17. The microprocessor now varies the binary input to the DAC in steps, examining the state of event flag line $\overline{EF3}$ at each stage. When the logic level on the event flag line changes the binary input to the DAC is a measure of the analogue voltage.

18. During normal operation only the IF GAIN WIPER and AGC MONITOR inputs are measured, the other inputs being measured during the self-test routines only. After each measurement is made the binary number corresponding to the IF GAIN WIPER level is latched into ML9. The multiplexer is inhibited and ML12b is closed by a logic '1' level, set at ML13 pin 24 by the microprocessor. The DAC output is then fed to the AGC board via PL53 pin 43. The capacitor C4 maintains this voltage during the periods when measurements are being made and ML12b is open.

Strobe Output and Data Transfer

19. Data transfer between the microprocessor and other parts of the receiver takes place via an input/output bus and port A of the programmable input/output interface (PIO) ML13. The instruction to read data from or put data onto the input/output bus is given by one of sixteen strobes. These are generated in the decoder, ML18, in response to a binary address sent by the microprocessor via port B of the PIO.

20. Chip selection and port selection in ML13 are exercised by the microprocessor by means of the N0, N1 and N2 control outputs.

21. The transfer of data into and out of ML13 and the duration of the strobe pulses from ML18 are controlled by ML19b. When port A of ML13 is in the input mode the following action occurs.

(1) The microprocessor latches the required strobe address at pins 18, 19, 21 and 22 of ML13.

(2) The TPA timing pulse is applied to ML19b pin 11. Since ML19b pin 9 is at logic '1', pin 13 goes to logic '1' and pin 12 to logic '0'.

(3) The logic '0' level applied to ML18 pin 23 enables the addressed strobe output. The logic '1' level at ML13 pin 35 prepares the input registers of ML13 to receive the data sent in response to the strobe pulse.

(4) The TPB timing pulse from the microprocessor resets ML19b. The strobe output is inhibited by a logic '1' level at ML18 pin 23, and the data is latched into ML13 by a high-to-low transition at ML13 pin 35.

(5) The data in ML13 is read by the microprocessor.

22. The action of ML19b when port A of ML13 is set to the output mode is similar. The microprocessor loads data into ML13, after which ML19b is clocked by timing pulse TPA. The strobe is enabled in the normal manner, and the logic '1' at ML13 pin 35 loads the data onto the input/output bus. The system is reset by the TPB timing pulse.

Clock Divider

23. The TPB clock signal from the CPU (ML6 pin 33) is applied to the clock input of a 12-stage binary counter ML15. This produces a nominal 16 millisecond period squarewave signal at the Q12 output (used by the CPU for timing various events), a 7.8 kHz signal at the Q5 output (SCORE interval clock and display multiplexer), and a 62.5 kHz signal at the Q2 output (used by the power supply generation circuit).

Program Running Indicator

24. The logic level at ML6 pin 4 is set under software control. The output is made to flash the LED D1 when the program is running.

Power Supplies

25. Two supply rails, +5 V A and +5 V B, are fed from the +5.5 V input at PL53 pin 63. The +5 V B supply is used only for the RAM, ML4 and ML5. On switching on ML1c pin 8 is held at a potential lower than that at pin 9 until C13 charges. This delays the switching on of TR3 so that the +5 V B supply is established before the +5 V A supply. This is an operating requirement of ML4 and ML5.

26. In the event of failure of the +5.5 V supply TR1 will be switched off, turning off TR2. The reservoir capacitor C8 maintains the +5 V B supply to the RAM for at least one minute. This prevents loss of the RAM contents during short term power failures. When the +5 V A supply is reduced to +4.75 V, ML16 pin 7 will be more negative than pin 6. As a result C6 will be discharged and ML1d will pull the $\overline{\text{CLEAR}}$ line to logic '0'.

Test Switches

27. Six in-line single-pole switches, labelled SA to SF, are provided to facilitate testing of the processor card. For normal receiver operation, all switches are set to the open position. To test the card, SA is set to the closed position, whilst SB is closed for signature analysis. The remaining four switches, SC to SF, are for the selection of a particular test program (stored in ROM). The state of these switches is periodically checked by the CPU by the application of any address in the range 3000 to 3FFF. This results in a negative-going pulse at the $\overline{\text{CS3}}$ output ML10. The disable condition is momentarily removed from the tri-state buffer ML14b, and the state of the switches is conveyed to the CPU via data bus lines D0 to D3.

Microprocessor Clock

28. An externally generated 2 MHz clock signal enters the board at PL53 pin 32, and is fed to ML6 pin 1.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		PROCESSOR CARD (ST 83771)			
	Resistors				
R1	100 k	9 Resistor SIL Network			938049
R2	4 k7	Metal Oxide		2	913490
R3	2 k2	Metal Oxide		2	916546
R4	100 k	Metal Oxide		2	915190
R5	3 k3	Metal Oxide		2	910111
R6	22 k	Metal Oxide		2	913493
R7	22 k	Metal Oxide		2	913493
R8	50 k	Variable preset			939322
R9	27 k	Metal Oxide		2	913494
R10	100 k	Metal Oxide		2	915190
R11	100 k	Metal Oxide		2	915190
R12	390	Metal Oxide		2	916331
R13	82 k	Metal Oxide		2	915189
R14	50 k	Variable, Preset			939322
R15	82 k	Metal Oxide		2	915189
R16	10 k	Metal Oxide		2	914042
R17	22 k	Metal Oxide		2	913493
R18	22 k	Metal Oxide		2	913493
R19	100 k	Metal Oxide		2	915190
R20	68 k	Metal Oxide		2	916478
R21	22 k	Metal Oxide		2	913493
R22	150 k	Metal Oxide		2	917954
R23	3 k3	Metal Oxide		2	910111
R24	82 k	Metal Oxide		2	915189
R25	6 k8	Metal Oxide		2	910112
R26	82 k	Metal Oxide		2	915189
R27	22 k	Metal Oxide		2	913493
R28	4 k7	Metal Oxide		2	913490
R29	56	Metal Oxide		2	917055
R30	22 k	Metal Oxide		2	913493
R31	82 k	Metal Oxide		2	915189
R32	12 k	Metal Oxide		2	917952
R33	100 k	Metal Oxide		2	915190
R34	100 k	Metal Oxide		2	915190
R35	47	Metal Oxide		2	917063

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	1 R5	Wirewound	1.5 W	5	917139
R37	150 k	Metal Oxide		2	917954
R38	100 k	Metal Oxide		2	915190
R39	220	Metal Oxide		2	910390
R40	120 k	Metal Oxide		2	915373
R41	10 k	9 Resistor SIL Network			934506
R42	6 k8	Metal Oxide		2	910112
R43	Not used				
R44	22 k	Metal Oxide		2	913493
R45	22 k	Metal Oxide		2	913493
R46	10 k	Metal Oxide		2	914042

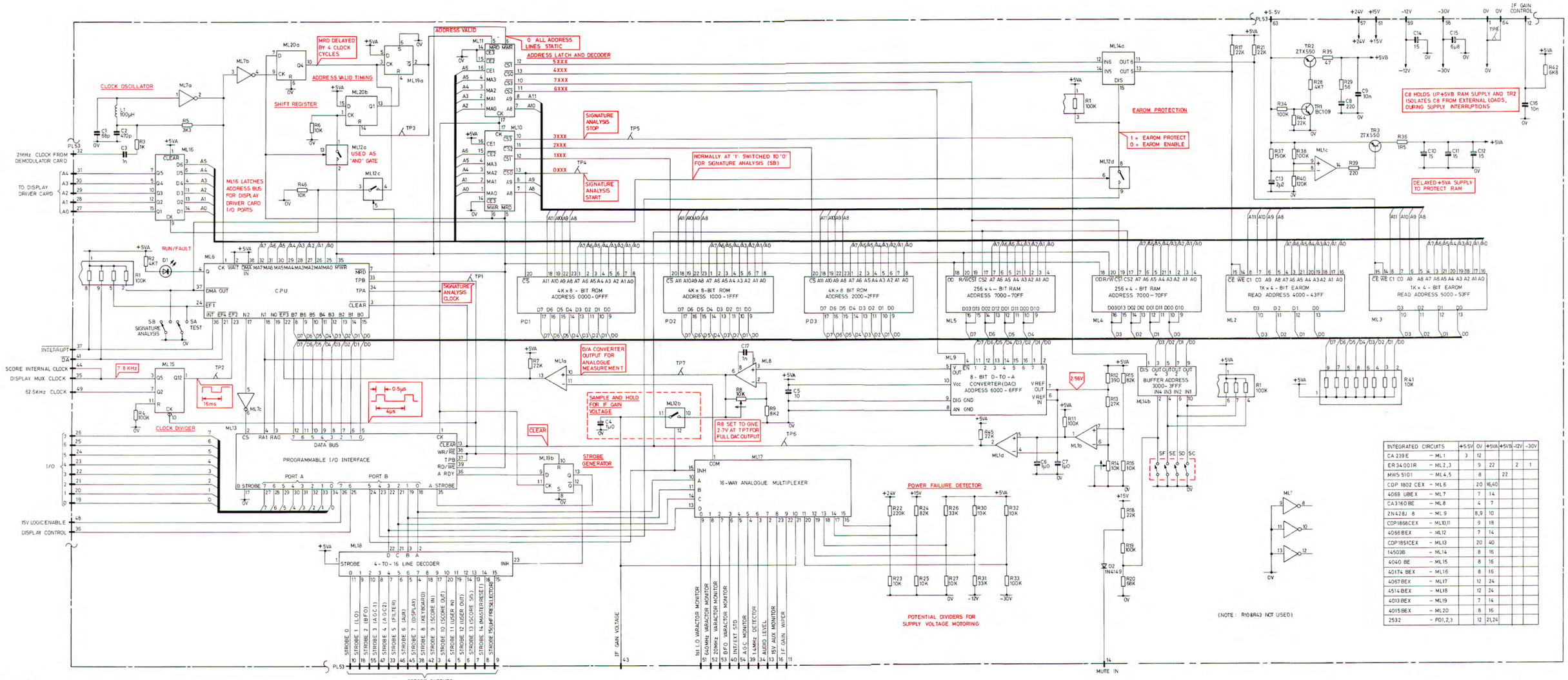
	Capacitors		V		
C1	68 p	Silver Mica	400	1 p	939325
C2	470 p	Silver Mica	100	2	939326
C3	1 n	Disc Ceramic	500	20	915243
C4	1 µ0	Tantalum Bead	35	20	923571
C5	10 µ	Tantalum Bead	35	20	921256
C6	1 µ0	Tantalum Bead	35	20	923571
C7	1 µ0	Tantalum Bead	35	20	923571
C8	220 µ	Tantalum Tubular	10	20	938988
C9	10 n	Disc Ceramic	250	+40 -20	900067
C10	15 µ	Tantalum Bead	10	20	923566
C11	15 µ	Tantalum Bead	10	20	923566
C12	15 µ	Tantalum Bead	10	20	923566
C13	2 µ2	Tantalum Bead	35	20	923572
C14	15 µ	Tantalum Bead	25	20	922516
C15	6 µ8	Tantalum Bead	50	20	939324
C16	10 n	Disc Ceramic	250	+40 -20	900067
C17	1 n	Disc Ceramic	500	20	915243

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Inductors			
L1	100 µ H	Choke		10	939161
		Diodes			
D1		LED, red			931291
D2		Silicon 1N 4149			914898
		Transistors			
TR1		Silicon PNP ZTX 550			931489
TR2		Silicon NPN BC109			923234
TR3		Silicon PNP ZTX550			931489
		Integrated Circuits			
ML1		Quad Comparator CA 239E			938962
ML2		1K x 4 EAROM ER3400IR			938886
ML3		1K x 4 EAROM ER3400IR			938886
ML4		CMOS Static RAM MWS5101			939180
ML5		CMOS Static RAM MWS5101			939180
ML6		CPU CDP 1802CEX			939301
ML7		Hex. Inverter 4049UBEX			930999
ML8		CA3130BE			933314
ML9		D/A Converter ZN428J-8			938903
ML10		Memory Address Latch CDP1868CEX			939182
ML11		Memory Address Latch CDP1868CEX			939182
ML12		Quad Analogue Switch 4066BEX			930148
ML13		PIO CDP1851CEX			939181
ML14		Hex Tri-state Buffer 14503B			931004
ML15		12-Bit Counter 4040BE			936673

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML16		Hex D-type flip-flop 40174BEX			931060
ML17		16-way Analogue Multiplexer 4067BEX			930998
ML18		4-to-16 Line Decoder 4514BEX			931010
ML19		Dual D-type flip-flop 4013BEX			926860
ML20		Dual 4-bit Shift Register 4015BEX			930973
PD1,PD2		TMS 2532A-45-JSP4			946080

Miscellaneous

		Switch, 2-way DIL			932881
		Switch, 4-way DIL			933738
		8-Pin DIL IC Socket			940901
		14-Pin DIL IC Socket			940902
		16-Pin DIL IC Socket			940903
		18-Pin DIL IC Socket			930607
		22-Pin DIL IC Socket			930608
		24-Pin DIL IC Socket (ML17, ML18)			930609
		24-Pin DIL IC Socket (PD1, PD2)			933813
		40-Pin DIL IC Socket			933814
		Test Point			936148
		Board Stiffener			BD79561
		Captive Screw M3 x 10 mm			AD 79561



INTEGRATED CIRCUITS		+5.5V	0V	+5VA	+5VB	-12V	-30V
CA 239 E	- ML 1	3	12				
ER 34001R	- ML 2,3		9	22		2	1
MW5 5101	- ML 4,5		8		22		
CDP 1802 CEX	- ML 6		20	16,40			
4069 UBE X	- ML 7		7	14			
CA 3160 BE	- ML 8		4	7			
ZN 428J 8	- ML 9		8,9	10			
CDP1868CEX	- ML10,11		9	18			
4066 BEX	- ML12		7	14			
CDP1851CEX	- ML13		20	40			
14503B	- ML14		8	16			
4040 BE	- ML15		8	16			
40174 BEX	- ML16		8	16			
4067 BEX	- ML17		12	24			
4514 BEX	- ML18		12	24			
4013 BEX	- ML19		7	14			
4015 BEX	- ML20		8	16			
2532	- PD1,2,3		12	21,24			

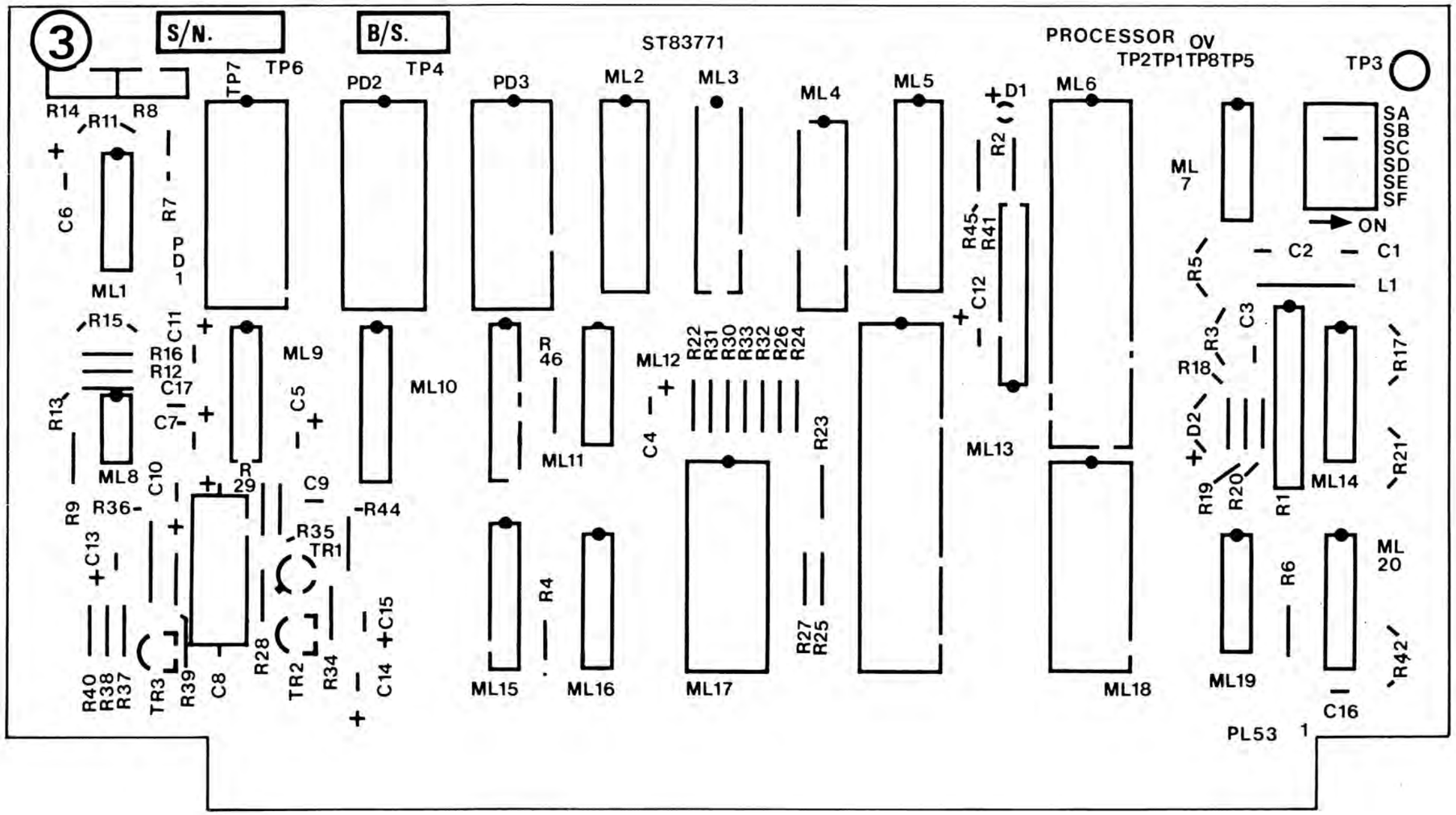
RACAL

TH 2449/3	DC83771/1	TH 2449/3	DC83771/2
1	2	1	

CHAP 7 RA1794 CHAP 7

Circuit: Processor Board

Fig. 7.1



RACAL

TH 2449/3 | DA83770

4

CHAP 7

Layout: Processor Board

Fig.7.2

CHAPTER 8

FREQUENCY STANDARD

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CHAPTER 8

FREQUENCY STANDARD

INTRODUCTION

1. One of two types of 5 MHz frequency standard may be fitted to the receiver (dependent upon the degree of frequency stability required) as an option. The two types of frequency standard are described below. Note that either type may be retrospectively fitted to a receiver by ordering the approriate kit of parts (ST 81218 for the 9420 kit, ST 81219 for the 9442 kit).

FREQUENCY STANDARD TYPE 9442

2. The Racal 9442 frequency standard is a fast warm-up crystal oscillator of small physical size which provides a high degree of accuracy and long term stability with low power consumption (table 1). The crystal is housed in a temperature controlled oven which, together with the maintaining circuit and a buffer amplifier, is fitted in a metal can with polyurethane foam to provide heat insulation. Access may be gained to the internal trimmer capacitor after removal of a small rubber plug. Adjustment procedures are given in Chapter 20. Connections are made via a B7G base, with pin connections as given in table 2.

FREQUENCY STANDARD TYPE 9420

3. The Racal 9420 frequency standard is a compact crystal oscillator similar in construction to the 9442. It contains a high-quality crystal which is operated in the third overtone mode. Like the 9442, the metal can contains polyurethane heat for best insulation and a removeable rubber plug allows access to the internal multi-turn trimmer capacitor. For finer adjustment, a potentiometer is fitted to the 20 MHz reference board which sets the voltage applied to an internal varactor diode. Adjustment instructions are given in Chapter 20. Pin connections are given in table 3.

Table 1: Frequency Standard Specifications

	UNITS	9442	9420
Frequency	MHz	5	5
Daily Ageing Rate on Delivery		1×10^{-8}	2×10^{-9}
Daily Ageing Rate after 3 months		3×10^{-9}	5×10^{-10}
Short Term Stability over 1 Second		5×10^{-10}	1×10^{-10}
Warm-up time for 1×10^{-7} accuracy	Minutes	4	20
Retrace Characteristics		4×10^{-8} in 24 hours	2×10^{-8} in 24 hours
Temperature Operating Range	^{o}C	-10 to +60	-10 to +60
Stability with Temperature Change	Per ^{o}C	3×10^{-9}	6×10^{-10}
Stability with supply voltage change	For 10% change	4×10^{-8}	5×10^{-9}
Minimum Output Level	mV r.m.s.	250 into 50 Ω	250 into 50 Ω
Trim Range		-6 +3 parts in 10^6	-8 +2 parts in 10^7
Supply Voltage	V	12	12
Typical Supply Current at $25^{o}C$	mA	60	120
Size	cm in	5 x 5 x 5 2 x 2 x 2	5 x 5 x 9.5 2 x 2 x 3.75
Base		B7G	B7G

Table 2 : 9442 Pin Connections

1 5 MHz output relative to pin 7
2 Not used
3 Not used
4 +12 V supply
5 Not used
6 Not used
7 0V (also connected to can)

REPAIR

4. If the specified performance of either type of frequency standard cannot be obtained, users are advised to return the faulty module to Racal Communications Limited for servicing, since select-on-test components and precise assembly techniques are employed to ensure the specified performance.

Table 3 : 9420 Pin Connections

1	5 MHz Output relative to pin 7
2	Internally stabilized +5.6 V varactor diode control voltage
3	+7.5 V stabilized monitor output
4	+12 V supply
5	Internally stablized +2.8 V output
6	Varactor diode connection
7	0 V (also connected to can).

CHAPTER 9

20 MHz REFERENCE BOARD

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At end of Chapter

CHAPTER 9

20 MHz REFERENCE BOARD

INTRODUCTION

1. The 20 MHz reference board accepts the reference frequency from either an internal or external frequency standard and produces three 20 MHz output signals, all locked to the frequency standard. An automatic switching circuit removes the operating supply from an internal frequency standard when an external standard is connected to the front panel EXT. STD.

CIRCUIT DESCRIPTION (fig 9.1)

EXTERNAL STANDARD INPUT STAGE

2. The output signal from an external frequency standard, applied to the front panel EXT. STD socket, may be any of 20 MHz between 100 KHz and 5 MHz e.g. 200 KHz, 400 KHz, 500 KHz etc. It is coupled by transformer T1 to a wideband amplifier/limiter circuit which uses three sections of a quad line receiver ML6a, ML6b and ML6c. This is an ECL (emitter coupled logic) device and contains a Vbb supply generator which is used to set the input and output threshold levels (table 1).

EXTERNAL STANDARD DETECTOR

3. The remaining section of ML6 (ML6d) is used as an external standard detector circuit. When an external standard signal is present, the clock output signal from Schmitt trigger ML6b is applied via C4 to the non-inverting input ML6d; the resulting positive output from ML6d holds C5 in the discharged state, and also results in the following:

   (1) A high level at the output of comparator ML2a to gate the external standard signal to the phase comparator.

   (2) A high level at the output of comparator ML2b to switch off the +12 V supply for the internal standard (if fitted).

   (3) A low level at the output of comparator ML2c which effectively switches off the internal standard amplifier/limiter ML1.

4. When an external standard is not connected to the receiver, the output from ML6d falls to approximately 3.5 V, and the output signals from comparator stages ML2a, ML2b and ML2c assume the opposite states, as follows:-

   (1) The low level at the output of ML2a causes a low level at the output of ML6c and effectively isolates the external standard amplifier/limiter stage from the phase comparator stage.

(2) The low level at the output of ML2b switches on TR1, the +15 V supply is applied via TR2 to the input of three terminal +12 V regulator ML9, and the +12 V output is applied to the internal frequency standard. The low level at the output of ML2b is also routed via diode D1 and pin 1 of PL40 to the processor card to indicate operation from an internal standard.

Table 1 : Quad Line Receiver Truth Table

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	Vbb	L
H	Vbb	H
Vbb	H	L
Vbb	L	H

INTERNAL STANDARD INPUT STAGE

This wideband amplifier/limiter stage uses three sections of an ECL quad line receiver ML1a, ML1b and ML1c. Provided an external standard is not connected to the receiver, then a high level at the output of ML2c gates the amplified signal to the phase comparator, and a low level at the output of ML2b switches on the +12 V supply for the internal frequency standard. R51 is used to set the varactor voltage applied to the internal frequency standard (type 9420 only). For further details see Chap. 8.

20 MHz OSCILLATOR

6. TR5 is connected as a 20 MHz voltage controlled crystal oscillator. The varactor diode D5 is in series with the 20 MHz crystal XL1, and is used to shift the phase of the oscillator signal until is becomes locked to the phase of the signal derived from the frequency standard. An increase in the varactor voltage causes a decrease in capacitance and hence an increase in oscillator frequency, and vice-versa.

PHASE-LOCK RANGE DETECTOR

7. The 20 MHz output signal from ML5a is applied to a phase-shifting stage ML4a, R39, C21, which introduces a phase difference of approximately 90 degrees (fig 9 (a), Waveforms 1 and 2). Provided the positive-going edge of the signal derived from the frequency standard occurs during the positive excursion of the 20 MHz quadrature signal i.e. the phase-lock window, then the Q2 output of ML7a is maintained at a '1', the $\overline{Q2}$ output is maintained at a '0', TR3 and TR4 are held off, and the phase detector stage ML3a, ML3b, is effectively enabled.

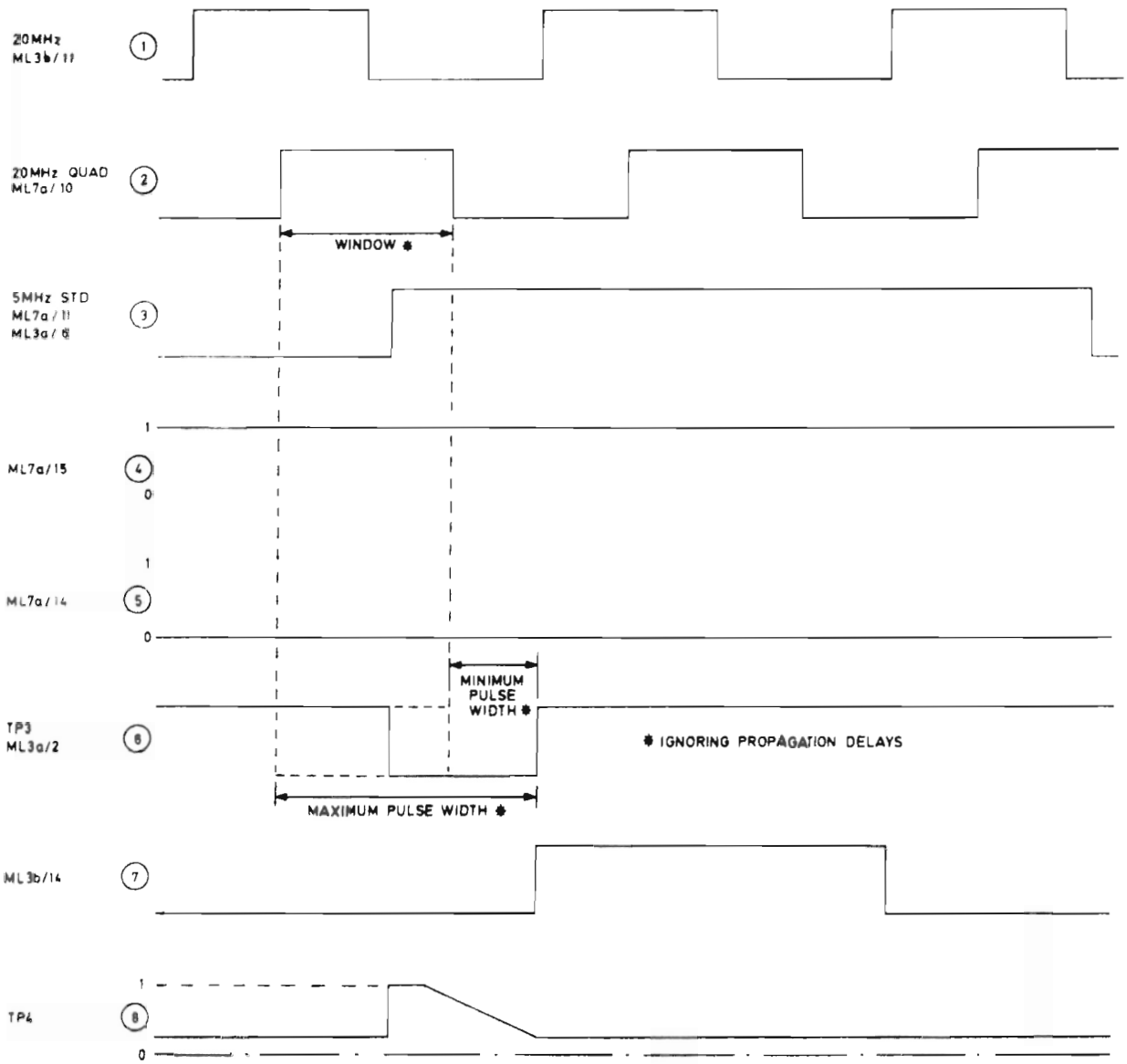


Fig. 9(a) Timing Diagram: In-Lock with 5MHz Standard

8. If the positive-going edge of the signal derived from the frequency standard occurs outside the phase-lock window, then the fast lock circuit is brought into operation and the phase detector is effectively inhibited.

PHASE DETECTOR

9. Provided the $\overline{Q2}$ output from the phase-lock range detector ML7a is at '0', then the 20 MHz signal from ML5a is applied to the clock input (CK2) of D-type flip-flop ML3b, to sample the signal derived from the frequency standard. This results in a negative-going pulse at TP3 for every positive-going transition of the frequency standard signal, where the duration of the pulse is proportional to the phase difference between the two signals.

SAMPLE AND HOLD STAGE

10. This stage (ML4b) stores a voltage in C16, the amplitude of which is proportional to the length of the pulse at TP3. When the level at TP3 goes low, the output from ML4b goes high for a short period (determined by C15, R26, R27 and R28) to discharge C16. This capacitor then charges via D3 and R29 until the level at TP3 goes high again (fig 9(a), waveform 8). The voltage held in C16 is then applied to inverting integrator C18, R30, ML8 to produce the varactor voltage.

FAST LOCK CIRCUIT

11. If the 20 MHz VCO frequency is either too high or too low for the lock-range of the phase detector, i.e. the rising edge of the signal derived from the frequency standard occurs outside the phase-lock window (fig 9(a), waveform 2), then a '1' is clocked through to the $\overline{Q2}$ output of ML7a, with the following results.

(1) A '1' is applied to the D1 input of ML3a, and this prevents the generation of the negative-going sampling pulse at TP3 i.e. the phase comparator is effectively inhibited.

(2) The '1' from the $\overline{Q2}$ output of ML7a clocks ML7b, and the level present at the D1 input ('0' for a high oscillator frequency, '1' for a low oscillator frequency) is transferred to the $\overline{Q1}$ output to switch on the appropriate fast-lock transistor, as follows:-

(a) If the 20 MHz oscillator frequency is too high, the '0' at the D1 input of ML7b results in a '1' at the $\overline{Q1}$ output. Since, for this condition, the Q2 output of ML7a is at a '0', TR4 is turned on, current is fed into the inverting integrator, and the varactor voltage is reduced. This causes an increase in the varactor diode capacitance and hence a reduction in the oscillator frequency.

(b) If the 20 MHz oscillator frequency is too low, the '1' at the D1 input of ML7b results in a '0' at the $\overline{Q1}$ output. This time TR3 is turned on, current is drawn from the inverting integrator, the varactor voltage level is increased and this results in an increase in the oscillator frequency.

20 MHz OUTPUT STAGES

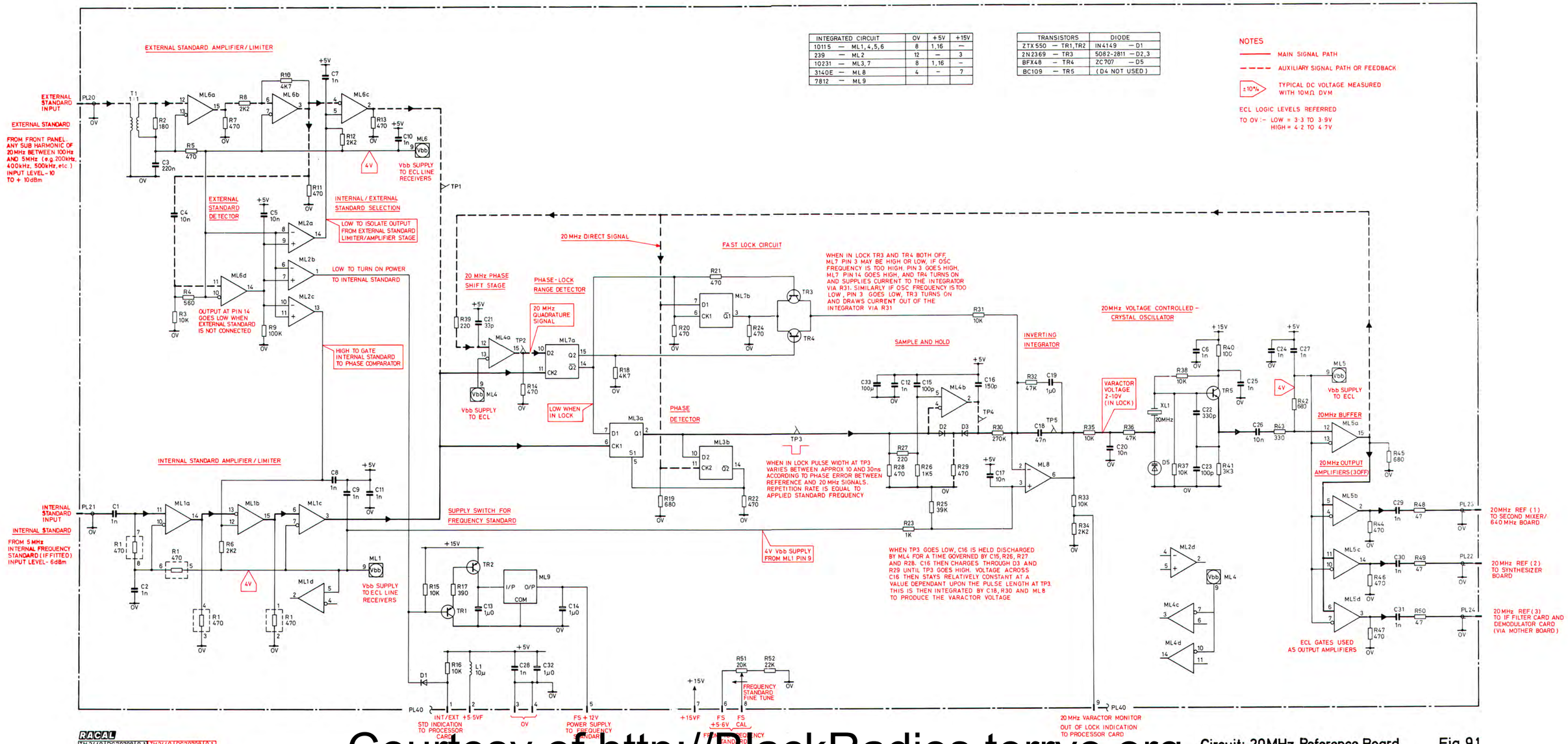
12. The 20 MHz output signal from buffer stage ML5a is applied to three identical ECL output amplifier stages ML5b, ML5C and ML5d. Resistors R44, R46 to R50, and capacitors C29, C30 and C31 are for impedance matching and output short-circuit protection.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		20 MHz REFERENCE BOARD (ST 79798)			
	Resistors				
R1	470	4-resistor network, SIL			939302
R2	180	Metal Oxide		2	915465
R3	10 k	Metal Oxide		2	914042
R4	560	Metal Oxide		2	917061
R5	470	Metal Oxide		2	920758
R6	2 k2	Metal Oxide		2	916546
R7	470	Metal Oxide		2	920758
R8	2 k2	Metal Oxide		2	916546
R9	100 k	Metal Oxide		2	915190
R10	4 k7	Metal Oxide		2	913490
R11	470	Metal Oxide		2	920758
R12	2 k2	Metal Oxide		2	916546
R13	470	Metal Oxide		2	920758
R14	470	Metal Oxide		2	920758
R15	10 k	Metal Oxide		2	914042
R16	10 k	Metal Oxide		2	914042
R17	390	Metal Oxide		2	916331
R18	4 k7	Metal Oxide		2	913490
R19	680	Metal Oxide		2	910113
R20	470	Metal Oxide		2	920758
R21	470	Metal Oxide		2	920758
R22	470	Metal Oxide		2	920758
R23	1 k	Metal Oxide		2	913489
R24	470	Metal Oxide		2	920758
R25	39 k	Metal Oxide		2	900993
R26	1 k5	Metal Oxide		2	911166
R27	220	Metal Oxide		2	910390
R28	470	Metal Oxide		2	920758
R29	470	Metal Oxide		2	920758
R30	270 k	Metal Oxide		2	923598
R31	10 k	Metal Oxide		2	914042
R32	47 k	Metal Oxide		2	913496
R33	10 k	Metal Oxide		2	914042
R34	2 k2	Metal Oxide		2	916546
R35	10 k	Metal Oxide		2	914042

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	47 k	Metal Oxide		2	913496
R37	10 k	Metal Oxide		2	914042
R38	10 k	Metal Oxide		2	914042
R39		Not Used			
R40	100	Metal Oxide		2	910388
R41	1 k2	Metal Oxide		2	911179
R42	330	Metal Oxide		2	915690
R43	680	Metal Oxide		2	910113
R44	470	Metal Oxide		2	920758
R45	680	Metal Oxide		2	910113
R46	470	Metal Oxide		2	920758
R47	470	Metal Oxide		2	920758
R48	47	Metal Oxide		2	917063
R49	47	Metal Oxide		2	917063
R50	47	Metal Oxide		2	917063
R51	20 k	Variable, preset			939302
R52	22 k	Metal Oxide		2	913493
	Capacitors		V		
C1	1 n	Disc ceramic	500	20	915243
C2	1 n	Disc ceramic	500	20	915243
C3	220 n	Polyester	100	20	931161
C4	10 n	Disc ceramic	250	+40 -20	900067
C5	10 n	Disc ceramic	250	+40 -20	900067
C6	1 n	Disc ceramic	500	20	915243
C		Disc ceramic	500	20	915243
C8	1 n	Disc ceramic	500	20	915243
C9	1 n	Disc ceramic	500	20	915243
C10	1 n	Disc ceramic	500	20	915243
C11	1 n	Disc ceramic	500	20	915243
C12	1 n	Disc ceramic	500	20	915243
C13	1 µ0	Tantalum Bead	35	20	923571
C14	1 µ0	Tantalum Bead	35	20	923571
C15	100 p	Disc ceramic	500	10	917417
C16	220 p	Disc ceramic	500	10	931148
C17	10 n	Disc ceramic	250	+40 -20	900067
C18	47 n	Polyester	400	20	931167
C19	1 µ0	Polyester	100	20	931163
C20	10 n	Disc ceramic	250	+40 -20	900067

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C21	68 p	Disc ceramic	500	10	917737
C22	330 p	Disc ceramic	500	10	917738
C23	100 p	Disc ceramic	500	10	917417
C24	1 n	Disc ceramic	500	20	915243
C25	1 n	Disc ceramic	500	20	915243
C26	10 n	Disc ceramic	250	+40 -20	900067
C27	1 n	Disc ceramic	500	20	915243
C28	1 n	Disc ceramic	500	20	915243
C29	1 n	Disc ceramic	500	20	915243
C30	1 n	Disc ceramic	500	20	915243
C31	1 n	Disc ceramic	500	20	915243
C32	1 µ0	Tantalum Bead	35	20	923671
		Inductors			
L1	10 µH	Choke	10		922364
T1		Transformer assembly			AT81941
		Diodes			
D1		Silicon 1N4149			914898
D2		Schottky 5082-2811			941092
D3		Schottky 5082-2811			941092
D4		Not used			
D5		Varactor ZC706			920266
		Connectors			
PL20		Plug coaxial PCB			935268
PL21		Plug coaxial PCB			935268
PL22		Plug coaxial PCB			935268
PL23		Plug coaxial PCB			935268
PL24		Plug coaxial PCB			935268
PL40		Plug, 10-way			938859

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Crystals			
XL1	20 MHz	Quartz			AD85549/001
		Transistors			
TR1		PNP Silicon ZTX550			931489
TR2		PNP Silicon ZTX550			931489
TR3		NPN Silicon 2N2369			939306
TR4		PNP Silicon BFX48			915231
TR5		NPN Silicon BC109			923234
		Integrated Circuits			
ML1		Quad ECL Line Receiver 10115			935262
ML2		Quad Comparator LM 239N			938962
ML3		Dual ECL Flip-flop 10231			935264
ML4		Quad ECL Line Receiver 10115			935262
ML5		Quad ECL Line Receiver 10115			935262
ML6		Quad ECL Line Receiver 10115			935262
ML7		Dual ECL Flip-flop 10231			935264
ML8		Operational Amplifier CA 3140E			932204
ML9		+12 V Regulator 7812			938879
		Miscellaneous			
		Test Point			936148
		8-pin DIL IC Socket			940901
		14-pin DIL IC Socket			940902
		16-pin DIL IC Socket			940903
		Captive panel fastener			930396



INTEGRATED CIRCUIT		OV	+5V	+15V
10115	ML1,4,5,6	8	1,16	—
239	ML2	12	—	3
10231	ML3,7	8	1,16	—
3140E	ML8	4	—	7
7812	ML9			

TRANSISTORS		DIODE	
ZTX550	TR1,TR2	IN4149	D1
2N2369	TR3	5082-2811	D2,3
BFX48	TR4	ZC707	D5
BC109	TR5	(D4 NOT USED)	

NOTES

MAIN SIGNAL PATH

AUXILIARY SIGNAL PATH OR FEEDBACK

±10% TYPICAL DC VOLTAGE MEASURED WITH 10MΩ DVM

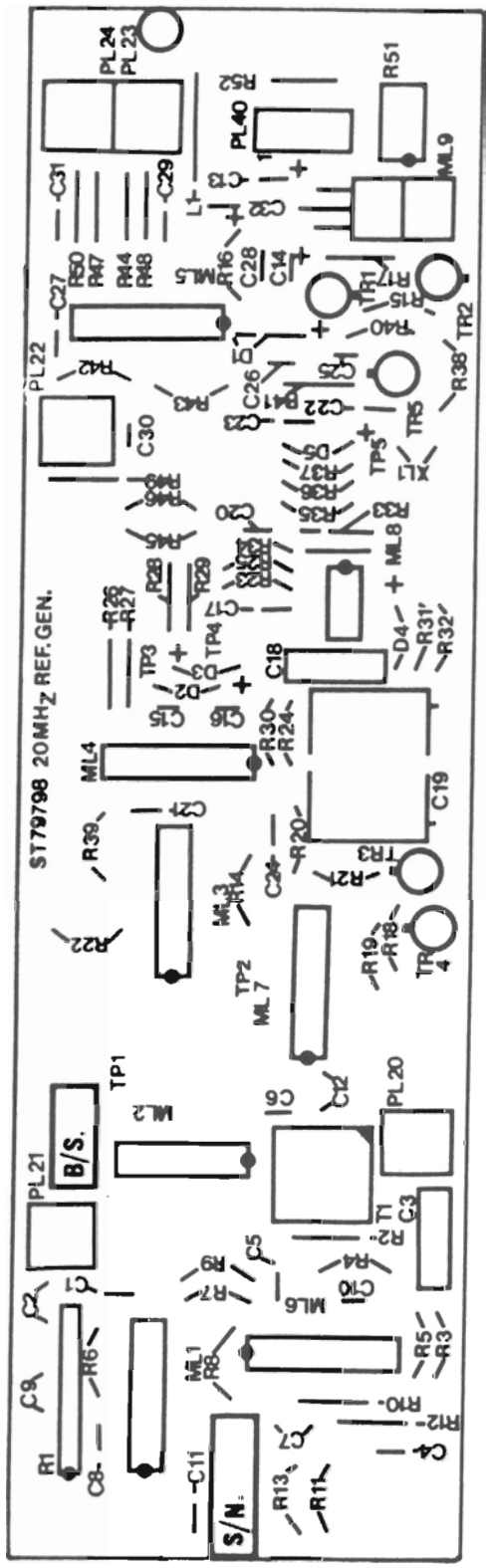
ECL LOGIC LEVELS REFERRED TO 0V :- LOW = 3·3 TO 3·9V HIGH = 4·2 TO 4·7V

RACAL

TH 2449	DC 79798	9.1	1
TH 2449	DC 79798	9.1	2/2

Circuit: 20MHz Reference Board

Fig. 9.1



Layout: 20MHz Reference Board Fig. 9.2

CHAPTER 10

SYNTHESIZER BOARD

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Tables

Illustrations

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At end of Chapter

CHAPTER 10

SYNTHESIZER BOARD

INTRODUCTION

1. A single-loop synthesizer is used to control the first local oscillator frequency, in 10Hz increments, over the range 661.40000 MHz to 1173.40000 MHz. It makes use of an LSI device (ML16) which contains the synthesizer control circuitry. A simplified block diagram of this device is given in fig. 10(a)

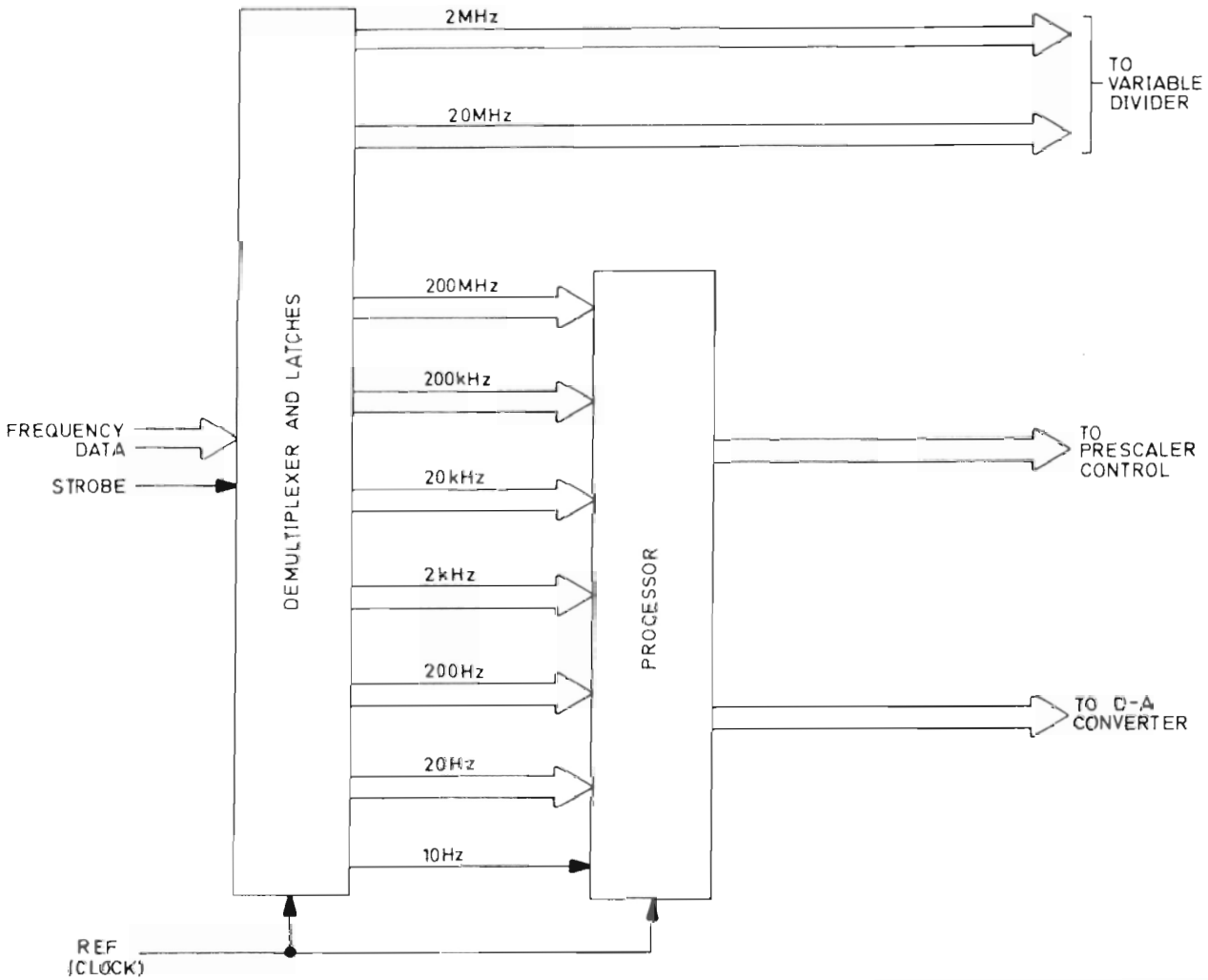


Fig. 10 (a) Block Diagram : Synthesizer Control Device ML16

FUNCTIONAL DESCRIPTION

2. In the block diagram of the synthesizer board given in fig. 10(b), the main signal flow is denoted by the heavy lines. The 661.4 MHz to 1173.4 MHz signal from the first local oscillator (located on the first mixer/VCO board) is applied to a phase comparator via a programmed divider comprising a divide-by-20/divide-by-22 prescaler and a variable divider

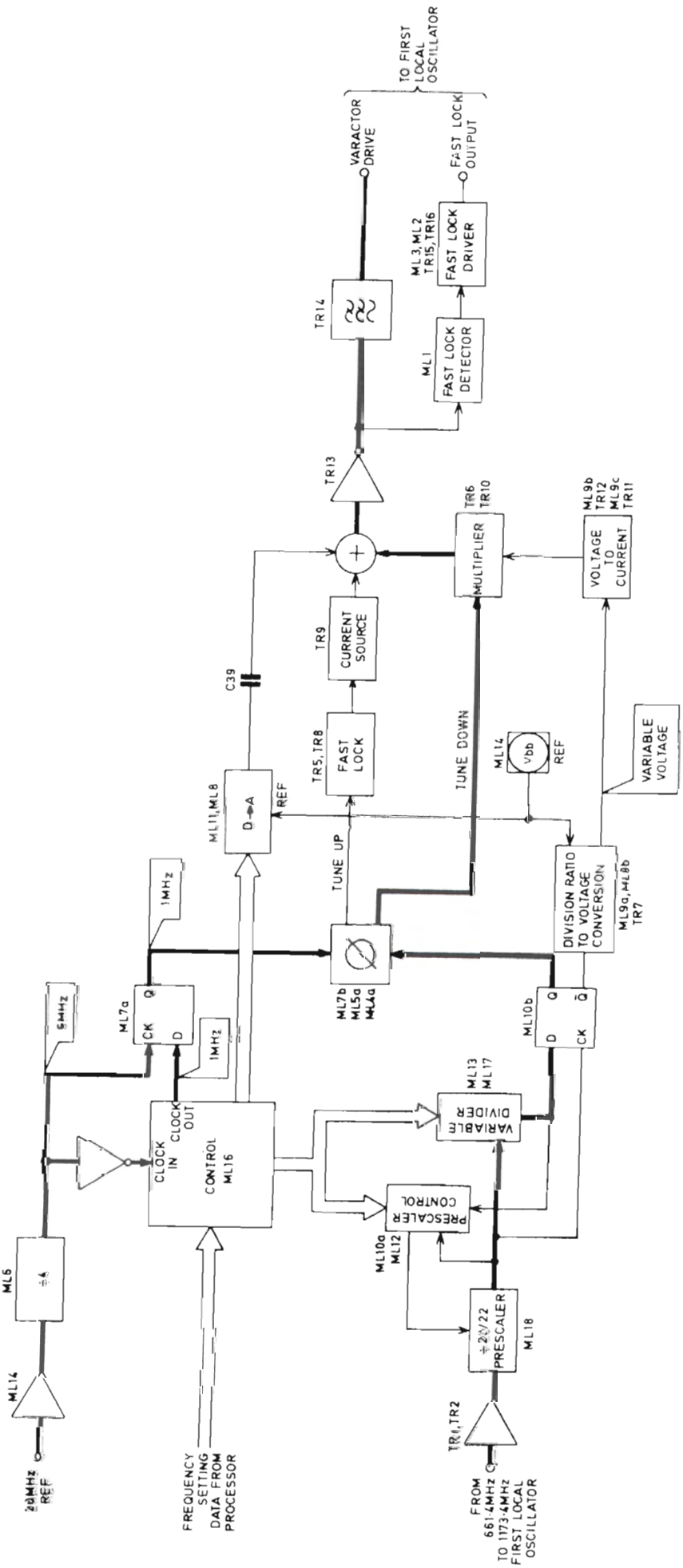


Fig.10(b) Block Diagram: Synthesizer Board

RACAL TH 2449

RA 1794A
FD 72A

(both controlled by ML16) together with output buffer stage ML10b. A 1 MHz reference signal from the control stage ML16 is first resynchronised to a 5 MHz signal derived from the 20 MHz reference signal, and is then applied as the second input to the phase comparator. The main output signal from the phase comparator is then applied, via a current multiplier (para. 4), a summing node, inverting buffer TR13 and loop filter TR14, to the first local oscillator.

3. Thus, the phase comparator output signal drives the first local oscillator (VCO) until its frequency, when divided by the programmed divider, is equal to the 1 MHz reference frequency, and phase lock is then achieved.

4. The division ratio to voltage conversion stage is fed from the $\overline{Q}$ output of buffer stage ML10b, and produces an output voltage which is proportional to the programmed divider division ratio. This is then converted to a current to produce, at the output of the multiplier stage, a current which is a product of the tune-down output current from the phase comparator and that derived from the division ratio to voltage converter. The circuit is included to increase the effective phase comparator gain with an increasing division ratio and so maintain a constant loop bandwidth.

5. The fast lock circuit provides additional current only when the loop is out of lock. The current is summed with that from the current multiplier and also that from a digital-to-analogue converter with differentiating capacitor C39. This latter stage is included to control the phase of the oscillator frequency and further reduce spurious levels.

6. The output from buffer stage TR13 is applied via a low-pass filter to the varactor diodes of the first local oscillator, and is also applied to a fast lock detector. This stage is used to detect a change in the receiver frequency setting and then rapidly drives the first local oscillator, either up or down, as necessary, to bring about a rapid return to the locked condition.

CIRCUIT DESCRIPTION (fig. 10.1)

20 MHz Reference Buffer Amplifier

7. The 20 MHz reference signal at PL19 is coupled by C1 to a wideband amplifier/limiter stage which uses all four sections of a quad line receiver ML14. This is an ECL (emitter coupled logic) device and contains a Vbb supply generator which is used to set the input and output threshold levels (table 1).

Table 1: Quad Line Receiver Truth Table

NON-INVERTING INPUT	INVERTING INPUT	OUTPUT
L	H	L
H	L	H
L	Vbb	L
H	Vbb	H
Vbb	H	L
Vbb	L	H

Divide-by-four Stage

8. The 20 MHz output signal from ML14d is applied to a divide-by-four stage consisting of an ECL high-speed dual D-type flip-flop ML6a, ML6b. The 5 MHz signal at the Q output of ML6b is converted to 9V C-MOS levels by TR4 before application to the digiphase synthesizer control stage ML16, whilst a 5 MHz output signal at ECL levels (from the $\overline{Q}$ output of ML6b) is applied to the 1 MHz reclocking stage ML7a.

9V C-MOS Supply

9. This is derived from the +15V(A) supply (R15, D2) and is routed to the supply pins (VDD) of C-MOS devices ML16 and ML11. In the event of a +15V supply failure, the +5.5V supply is routed via D4 to the Vdd pin of ML16 for protection purposes.

Programmed Divider

10. The 661.4 MHz to 1173.4 MHz first local oscillator signal at PL18 is applied via buffer amplifier stage TR1, TR2 to the programmed divider comprising divide-by-20/divide-by-22 prescaler ML18, prescaler control stage ML12, ML10a, and main variable divider ML13, ML17.

11. The prescaler stage ML18 is an ECL UHF programmable divider which divides by 20 when either or both of the $\overline{PE}$ control inputs is at logic '1', and divides by 22 when both $\overline{PE}$ inputs are at logic '0'. The prescaler control stage ML12 is an ECL four-stage binary counter where the mode of operation is determined by the state of the S1, S2 and $\overline{CIN}$ (carry-in) inputs (table 2). Since the S2 input is taken to 0V, the stage can only be preset or set to the count down mode, as determined by the wired-OR connected outputs from ML17. Table 2 also shows that counting-down can only take place when the $\overline{CIN}$ input is at '0'; since this comes from the $\overline{Q}$ output of ML10a, and since the wired-OR connected outputs from ML12 are applied to the D input of ML10a, when ML12 counts down to 1 the counting action is inhibited until after the next preset.

Table 2: ML12, ML13 and ML17 Truth Table

$\overline{CIN}$	S1	S2	MODE
0	0	0	PRESET
0	0	1	COUNT UP
0	1	0	COUNT DOWN
0	1	1	HOLD
1	X	X	COUNT INHIBIT

12. The main variable divider consists of ECL decade counter ML13 and ECL binary counter ML17. Both are set to the count down mode (S2 inputs at '0'); ML13 counts down from a preset number to zero and then starts again at nine, whilst ML17 counts down from a preset number until zero is reached at which time both counters, together with ML12, are again preset. Note that ML13 and ML17 are cascaded by connecting the carry-out of one to the carry-in of the other.

Phase Comparator

13. The phase comparator uses two high-speed ECL D-type flip-flops, ML7b and ML5a, together with NOR gate ML4a. The D inputs of the two flip-flops are taken to OV, the 1 MHz clock output from ML16, resynchronised to the 5 MHz reference signal by ML7a, is used to clock ML7b, whilst ML5a is clocked from the buffered output signal (ML10b) from the variable divider. Thus when the positive-going edge of the 1 MHz signal at TP6 clocks ML7b, the '0' at the D input results in a '0' at Q output, and this is applied to one input of ML4a. Similarly, when the positive-going edge of the variable divider signal at TP7 clocks ML5a, the '0' at the D input results in a '0' at the Q output, and this is applied to the remaining input of ML4a. When both inputs of ML4a are at '0', a '1' is produced at the output and this is used to set both ML7b and ML5a.

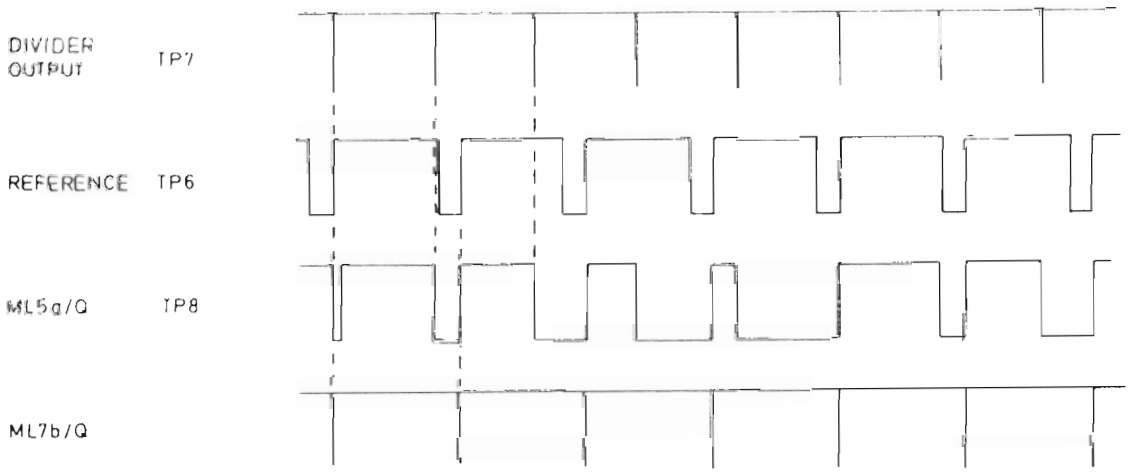


Fig.10(c) Timing Diagram: Divider Frequency High

14. The timing diagram given in fig. 10(c) shows the situation where the first local oscillator frequency, and hence the divider output frequency, is too high. The resulting waveform at the Q output of ML5a is applied to the base of TR6, whilst the inverse of this waveform, at the $\overline{Q}$ output of ML5a, is first delayed by R42, C42, and is then applied to the base of TR10. The result of this is a decrease in the collector current of TR10, a corresponding decrease in the varactor voltage at the emitter of TR13, and hence a reduction of the first local oscillator frequency.

15. The very narrow pulses at the Q and $\overline{Q}$ outputs of ML7b are applied to TR5, but the time constant preset by R40 and C40 is sufficient to prevent the conduction of TR8. Thus under the conditions depicted in fig. 10(c), and also under the phase-locked condition, the fast lock-up circuit is inactive and TR9 simply supplies a fixed level of current to the summing node (TP10).

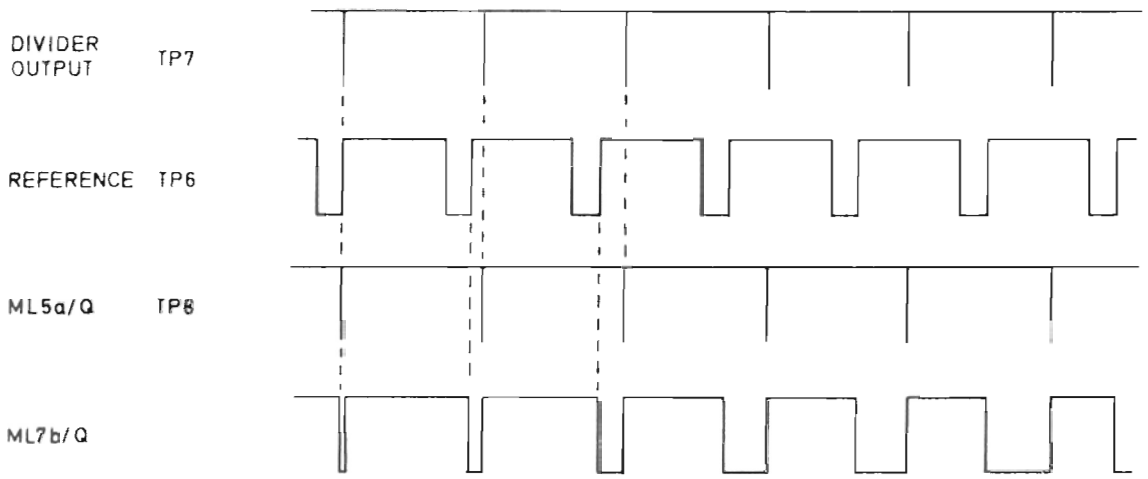


Fig.10(d) Timing Diagram: Divider Frequency Low

16. The situation where the divider frequency is low is depicted in fig. 10(d). This time the wider pulses at the Q and $\overline{Q}$ outputs of ML7b cause the conduction of TR8, the shunting of R46 causes an increase in the collector current of TR9 and the resulting increased voltage at the emitter of TR13 causes a corresponding increase in the first local oscillator frequency.

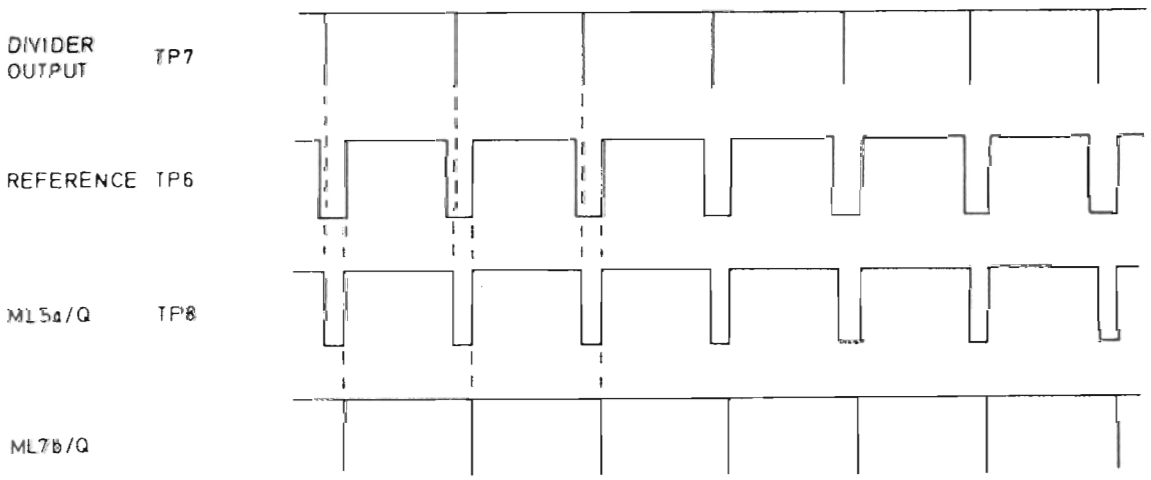


Fig.10(e) Timing Diagram: Divider and Reference in Phase

17. Fig. 10(e) depicts the in-lock condition, where the two signals are equal in frequency, and where the phasing in such that the duration of the pulses at TP8 is approximately equal to eight times the duration of the pulses at the Q output of ML7b (60 nanoseconds and 7 nanoseconds respectively). This slight difference in phase is necessary to offset the fixed level of current injected into the loop by TR9.

Division Ratio to Voltage Converter

18. This comprises ML9a, TR7 and shottky diodes D5 and D6. The feedback loops around operational amplifier ML9a (ac feedback via C38, dc feedback via inverting transistor TR7) continually strive to maintain the non-inverting input at the Vbb reference level from ML14 (approximately +4V) which is

applied to the inverting input. Since the output signal from ML10b is applied via D5, the higher the mark:space ratio the greater the current pulsed by TR7 to maintain equilibrium, and the greater the voltage developed across R41. ML9d and TR12 are connected as a current mirror to shift the level of the voltage developed across R41 to one that rises from 0V, and this voltage is used to control the current source stage ML9c, TR11.

Fast Lock Detector

19. This circuit, comprising ML1a, ML1b, ML1c and ML2a to ML2d, comes into operation following an abrupt change in the receiver frequency setting. At all other times, the voltages from potential divider R53 to R56 ensure that a '1' is present at the outputs of both ML1a and ML1b (pull-up voltage from R60); this results in a voltage of approximately +24V at the junction of R66 with D9 (ML1a, b and c have open-collector outputs), and the quad transmission gate (analogue switch) device ML2 is held disabled (ML2 is designed to be operated from plus and minus 15V supplies. In this application however, the minus supply connection is taken to 0V, the 0V connection is taken to +15V, and the +15V connection is taken to +24V. This means that, as far as ML2 is concerned, a level of +24V at a control input is regarded as a logic '1', to inhibit switch operation, whilst a level of +15V is regarded as a logic '0', to enable switch operation).

20. When a change of receiver frequency occurs, the voltage at the emitter of TR13 is abruptly taken high for an increase in frequency, or low for a decrease in frequency. This abrupt change is sensed by the limit comparator formed by ML1a and ML1b such that if the level at the junction of C44 with R57 exceeds +8.2V or falls below +6.8V, then the output from either ML1a or ML1b is pulled down to 0V. This results in a '0' at the output of ML1c and this is translated to a level of approximately +15V to enable quad transmission gate ML2. ML2a and ML2b close to increase the bandwidth of the loop filter, whilst ML2c and ML2d bring the fast lock power amplifier stage ML3, TR15, TR16 into operation, and so bring about a rapid return to the phase-locked condition.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SYNTHESIZER BOARD (ST 79782)			
	Resistor				
R1	68	Metal Oxide		2	916476
R2	390	Metal Oxide		2	916331
R3	470	Metal Oxide		2	920758
R4	22	Metal Oxide		2	920743
R5	470	9 Resistor SIL network		2	939166
R6	100 k	Metal Oxide		2	915190
R7	680	Metal Oxide		2	910113
R8	47	Metal Oxide		2	917063
R9	100 k	Metal Oxide		2	915190
R10	680	Metal Oxide		2	910113
R11	22	Metal Oxide		2	920743
R12	22 k	Metal Oxide		2	913493
R13	4 k7	7 Resistor SIL network		2	939169
R14	470	Metal Oxide		2	920758
R15	220	Metal Oxide		2	910390
R16	470	Metal Oxide		2	920758
R17	100	Metal Oxide		2	910388
R18	4 k7	5 Resistor SIL network		2	939649
R19	10 k	Metal Oxide		2	914042
R20	2 k2	Metal Oxide		2	916546
R21	470	Metal Oxide		2	920758
R22	1 k	Metal Oxide		2	913489
R23	470	Metal Oxide		2	920758
R24	470	Metal Oxide		2	920758
R25	2 k2	Metal Oxide		2	916546
R26	470	Metal Oxide		2	920758
R27	Not used				
R28	2 k2	Metal Oxide		2	916546
R29	100	Metal Oxide		2	910388
R30	470	Metal Oxide		2	920758
R31	470	Metal Oxide		2	920758
R32	150	Metal Oxide		2	910389
R33	2 k2	Metal Oxide		2	916546
R34	22 k	Metal Oxide		2	913493
R35	470	5 Resistor SIL network		2	939648
R36	20 k	Variable, Preset			934266
R37	4 k7	Metal Oxide		2	913490
R38	10 k	Metal Oxide		2	914042
R39	100	Metal Oxide		2	910388
R40	5 k6	Metal Oxide		2	918128

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R41	680	Metal Oxide		2	910113
R42	3 k3	Metal Oxide		2	910111
R43	3 k3	Metal Oxide		2	910111
R44	4 k7	Metal Oxide		2	913490
R45	1 k	Metal Oxide		2	913489
R46	27k	Metal Oxide		2	913494
R47	330	Metal Oxide		2	915690
R48	5 k6	Metal Oxide		2	918128
R49	1 k	Metal Oxide		2	913489
R50	10 k	Metal Oxide		2	914042
R51	20 k	Variable, Preset			934266
R52	120 k	Metal Oxide		2	915373
R53	4 k7	Metal Oxide		2	913490
R54	470	Metal Oxide		2	920758
R55	470	Metal Oxide		2	920758
R56	4 k7	Metal Oxide		2	913490
R57	100 k	Metal Oxide		2	915190
R58	4 7k	Metal Oxide		2	913496
R59	1 k8	Metal Oxide		2	914042
R60	10 k	Metal Oxide		2	914042
R61	3 k3	Metal Oxide		2	910111
R62	47 k	Metal Oxide		2	913496
R63	100 k	Metal Oxide		2	915190
R64	10 k	Metal Oxide		2	914042
R65	10 k	Metal Oxide		2	914042
R66	10 k	Metal Oxide		2	914042
R67	10 k	Metal Oxide		2	914042
R68	3 k3	Metal Oxide		2	910111
R69	100	Metal Oxide		2	910388
R70	47 k	Metal Oxide		2	913496
R71	2 k2	Metal Oxide		2	916546
R72	15 k	Metal Oxide		2	920645
R73	1 k	Metal Oxide		2	913489
R74	100	Metal Oxide		2	910388
R75	100	Metal Oxide		2	910388
	Capacitors		V		
C1	1 n	Ceramic Disc	500	20	915243
C2	4 µ7	Tantalum Tubular	10	20	905388
C3	1 n	Ceramic Disc	500	20	915243
C4	15 p	Ceramic Plate	100	2	939140
C5	15	Tantalum Tubular	50	20	938985

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C6	1 µ0	Tantalum Tubular	40	10	931177
C7	4 µ7	Tantalum Tubular	10	20	905388
C8	1 µ0	Tantalum Tubular	40	10	931177
C9	0 µ1	Ceramic Block	50	20	938857
C10	0 µ1	Ceramic Block	50	20	938857
C11	0 µ1	Ceramic Block	50	20	938857
C12	0 µ1	Ceramic Block	50	20	938857
C13	1 n	Ceramic Disc	500	20	915243
C14	33 p	Ceramic Plate	100	2	938994
C15	0 µ1	Ceramic Disc	50	20	938857
C16	5 o6	Ceramic Plate			925414
C17	0 µ1	Ceramic Block	50	20	938857
C18	33 p	Ceramic Plate	100	2	938994
C19	0 µ1	Ceramic Block	50	20	938857
C20	1 µ0	Tantalum Tubular	40	10	931177
C21	0 µ1	Ceramic Block	50	20	938857
C22	4 p7	Ceramic Plate	100	0.25 p	923955
C23	0 µ1	Ceramic Block	50	20	938857
C24	1 n	Ceramic Chip	50	10	939101
C25	1 n	Ceramic Chip	50	10	939101
C26	4 µ7	Tantalum Tubular	10	20	905388
C27	0 µ1	Ceramic Block	50	20	938857
C28	0 µ1	Ceramic Block	50	20	938857
C29	0 µ1	Ceramic Block	50	20	938857
C30	10 n	Ceramic Disc	250	+40 -20	900067
C31	1 n	Ceramic Disc	500	20	915243
C32	1 n	Ceramic Chip	50	10	939101
C33	10 n	Ceramic Disc	250	+40 -20	900067
C34	22 p	Ceramic Disc	500	5	921624
C35	0 µ1	Ceramic Block	50	20	938857
C36	0 µ1	Ceramic Block	50	20	938857
C37	10 n	Ceramic Disc	250	+40 -20	900067
C38	0 µ1	Ceramic Block	50	20	938857
C39	10 p	Ceramic Disc	500	5	921270
C40	1 p8	Ceramic Plate	100	0.25 p	938992
C41	0 µ1	Ceramic Block	50	20	938857
C42	0 µ1	Ceramic Block	50	20	938857
C43	330 p	Ceramic Disc	500	10	917738
C44	10 n	Ceramic Disc	250	+40 -20	900067
C45	10 n	Ceramic Disc	250	+40 -20	900067

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C46	47 n	Ceramic Block	50	20	939307
C47	2 n2	Ceramic Disc	500	25	917438
C48	1 n	Ceramic Disc	500	20	915243
C49	2 n2	Ceramic Disc	500	25	917438
C50	1 n	Ceramic Disc	500	20	915243
C51	1 µ0	Polyester	100	20	931163
C52	1 n	Ceramic Disc	500	20	915243
C53	1 n	Ceramic Disc	500	20	915243

Inductors

L1	1 mH	Choke	10	938956
L2	1 mH	Choke	10	938956
L3	1 mH	Choke	10	938956
L4	1 µH	Choke	10	938966
L5	1 µ5H	Choke	10	938967
L6	2 µ2H	Choke	10	922459
L7	4 µ7H	Choke	10	925362
L8	4 µ7H	Choke	10	925362
L9	1 mH	Choke	10	938956
L10	1 µH	Choke	10	938966
L11	2 µ2H	Choke	10	922459
L12	0 µ33H	Choke	10	938965
L13	47 µH	Choke	10	939160
L14	1 µ5H	Choke	10	938967

Connectors

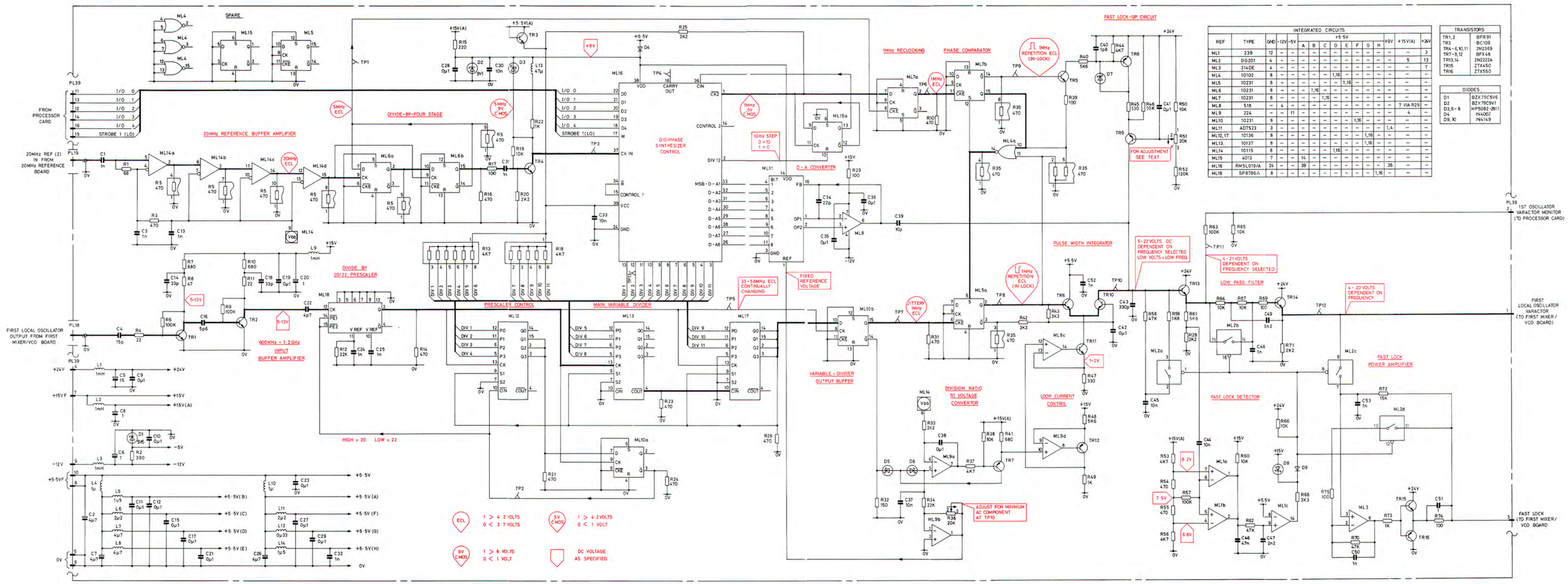
PL18	Plug, coaxial, 50 ohms	935268
PL19	Plug, coaxial, 50 ohms	935268
PL39	Plug, 16-way	938860

Cct. Ref.	Value Description	Rat	Tol %	Racal Part Number
	Diodes			
D1	Zener, 5 V6, 400 mW, BZX79C5V6			921749
D2	Zener, 9V1, 400 mW, BZX79C9V1			921751
D3	Schottky, HP5082-2811			941092
D4	Rectifier, 1N4002			923564
D5	Schottky HP5082-2811			941092
D6	Schottky HP5082-2811			941092
D7	Schottky HP5082-2811			941092
D8	Schottky HP5082-2811			941092
D9	Silicon 1N4149			914898
	Transistors			
TR1	NPN Silicon BFR91			938866
TR2	NPN Silicon BFR91			938866
TR3	NPN Silicon BC109			923234
TR4	NPN Silicon 2N2369			939306
TR5	NPN Silicon 2N2369			939306
TR6	NPN Silicon 2N2369			939306
TR7	PNP Silicon BFX48			915231
TR8	PNP Silicon BFX48			915231
TR9	PNP Silicon BFX48			915231
TR10	NPN Silicon 2N2369			939306
TR11	NPN Silicon 2N2369			939306
TR12	PNP Silicon BFX48			915231
TR13	NPN Silicon 2N2222A			923217
TR14	NPN Silicon 2N2222A			923217
TR15	NPN Silicon ZTX450			933099
TR16	PNP Silicon ZTX 550			931489
	Integrated Circuits			
ML1	Quad Comparator 239			938962
ML2	Quad Analogue Switch 201			938974
ML3	Operational Amplifier CA 3140E			932204
ML4	ECL Quad 2-input OR gate 10102P			935265
ML5	ECL Dual D-Type flip-flop 10231P			935264

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML6		ECL Dual D-Type flip-flop 10231P			935264
ML7		ECL Dual D-Type flip-flop 10231P			935264
ML8		Operational Amplifier AD5185S			938882
ML9		Quad Operational Amplifier 224			938978
ML10		ECL Dual D-type flip-flop 10231P			935264
ML11		8-Bit D to A Converter AD7523			938883
ML12		ECL Binary Counter 10136P			938875
ML13		ECL BCD Counter 10137P			938876
ML14		ECL Quad Line Receiver 10115P			935262
ML15		Dual D-type flip-flop 4013			926860
ML16		Digiphase Control RMSL019/A			AD80763/A
ML17		ECL Binary Counter 10136P			938875
ML18		ECL 20/22 Prescaler SP8786M			938888

Miscellaneous

8-pin DIL IC Socket	940901
14-pin DIL IC Socket	940902
16-pin DIL IC Socket	940903
40-pin DIL IC Socket	933814
Test Points	936148
Captive Panel fastener	930396



INTEGRATED CIRCUITS														
REF	TYPE	GND	-12V	-5V	+5·5V							+9V	+15V(A)	+24V
					A	B	C	D	E	F	G	H		
ML1	239	12	–	–	–	–	–	–	–	–	–	–	–	3
ML2	DG201	4	–	–	–	–	–	–	–	–	–	–	5	13
ML3	314DE	4	–	–	–	–	–	–	–	–	–	–	–	7
ML4	10102	8	–	–	–	–	1,16	–	–	–	–	–	–	–
ML5	10231	8	–	–	–	–	–	1,16	–	–	–	–	–	–
ML6	10231	8	–	–	1,16	–	–	–	–	–	–	–	–	–
ML7	10231	8	–	–	–	–	1,16	–	–	–	–	–	–	–
ML8	518	–	4	–	–	–	–	–	–	–	–	–	7 VIA R29	–
ML9	224	–	–	11	–	–	–	–	–	–	–	–	4	–
ML10	10231	8	–	–	–	–	–	–	–	–	1,16	–	–	–
ML11	AD7523	3	–	–	–	–	–	–	–	–	–	–	1,4	–
ML12,17	10136	8	–	–	–	–	–	–	–	–	–	1,16	–	–
ML13	10137	8	–	–	–	–	–	–	–	–	–	1,16	–	–
ML14	10115	8	–	–	–	–	–	–	–	–	1,16	–	–	–
ML15	4013	7	–	–	14	–	–	–	–	–	–	–	–	–
ML16	RMSL0191A	24	–	–	39	–	–	–	–	–	–	–	38	–
ML18	SP8786A	8	–	–	–	–	–	–	–	–	–	1,16	–	–

TRANSISTORS	
TR1,2	BFR91
TR3	1BC109
TR4-6,10,11	2N2369
TR7-9,12	BFX48
TR13,14	2N2222A
TR15	ZTX450
TR16	ZTX550

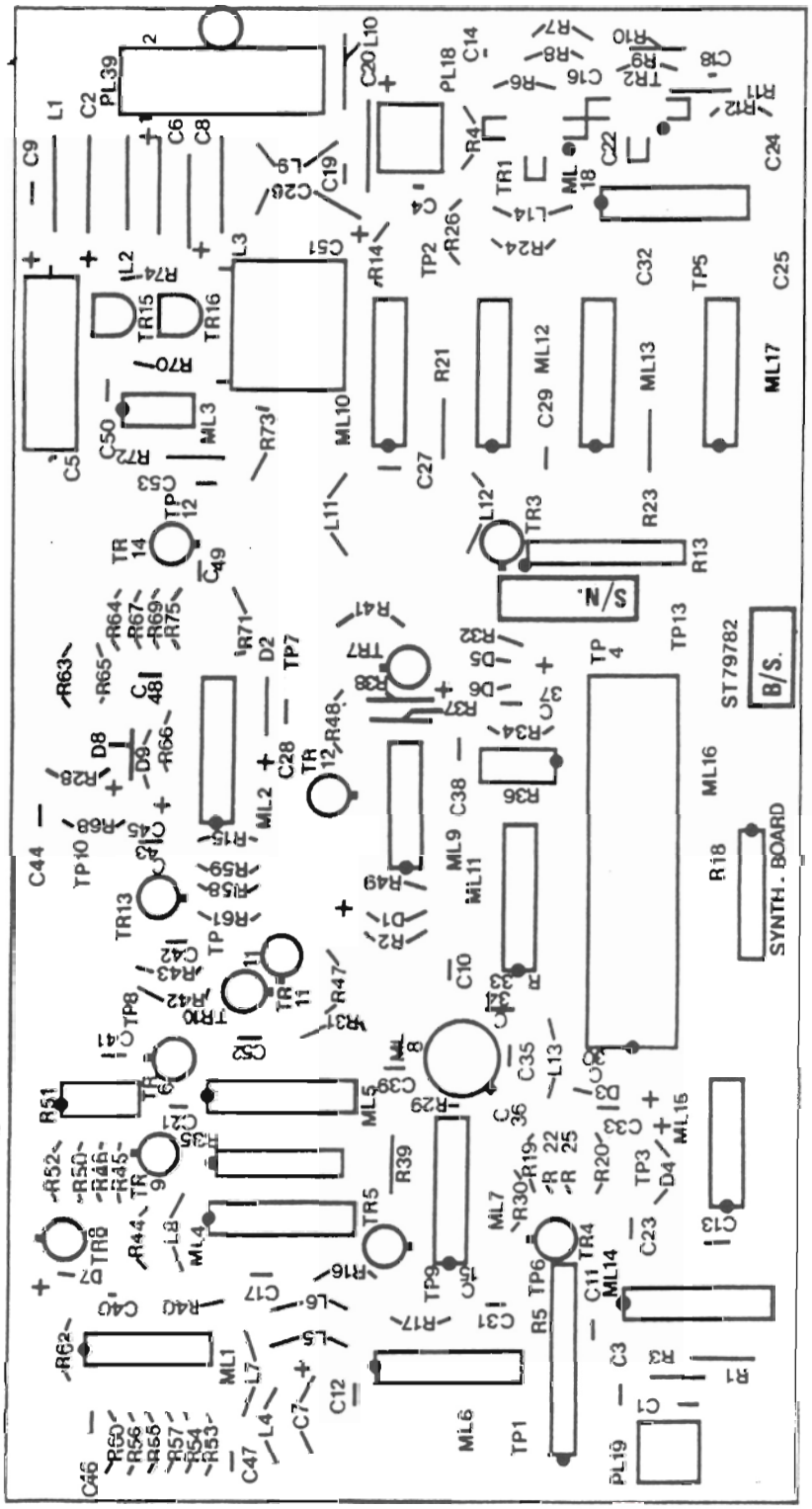
DIODES	
D1	BZX79C5V6
D2	BZX79C9V1
D3,5-8	HPS082-2811
D4	IN4002
D9, 10	IN4149

RACAL

TH 2449 DC79782 10.1	TH 2449 DC79782 10.1
1 (6) 7	1 / 2

Circuit: Synthesizer Board

Fig.10.1



Layout: Synthesizer Board Fig. 10.2

CHAPTER 11

FIRST MIXER/VCO BOARD

Illustrations

CHAPTER 11

FIRST MIXER/VCO BOARD

INTRODUCTION

1. This board is mounted in an under-chassis compartment at the rear of the receiver. It contains the 661.4 MHz to 1173.4 MHz VCO (controlled by the synthesizer board circuitry - Chap 10), the output from which is first amplified and then mixed with the received signal from the 512 MHz low-pass filter. The 661.4 MHz output signal from the mixer stage is then amplified before application to the second mixer board via the 661.4 MHz band-pass filter unit.

CIRCUIT DESCRIPTION (fig 11.1)

Voltage Controlled Oscillator

2. This uses NPN T-package transistor TR1, a tuned circuit comprising a tuned line/coupler DL1 with varactor diodes D2 to D5, and feedback varactor diode D1. Note that the tuned line/coupler DL1 is formed by accurately dimensioned and positioned strips of track on the printed circuit board (DL2 is similarly fabricated). The varactor line and fast lock input voltage signals from the synthesizer board are applied to the varactor diodes via filter components R5, R7, R8, C4, C5, L1 and L2.

Broadband Amplifier

3. The output signal from the VCO is coupled by C7 to a broadband amplifier TR3, TR4. This acts as a buffer between the oscillator and mixer stages and also provides the correct drive level to the first mixer. The overall gain of the amplifier is approximately 14 dB.

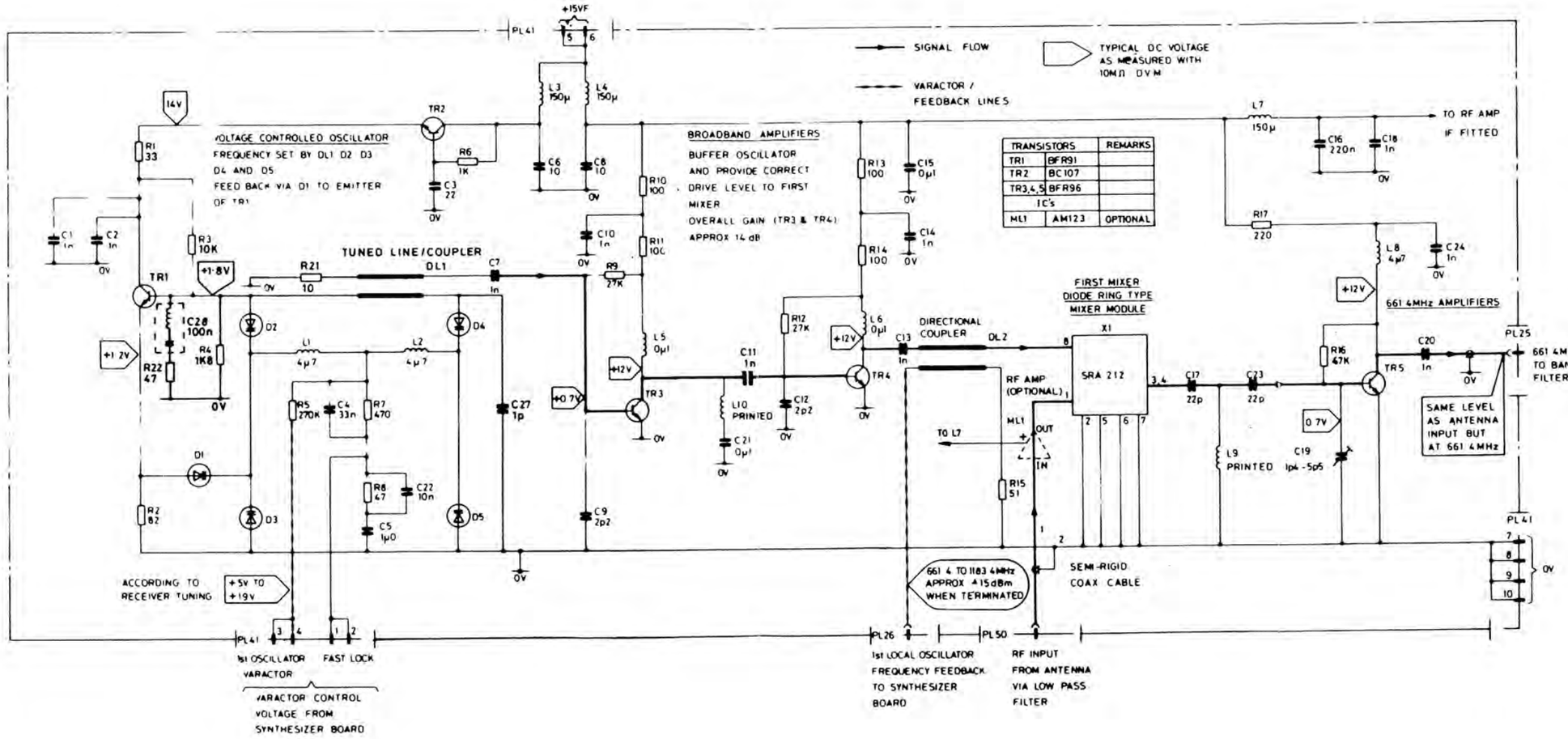
First Mixer Stage

4. X1 is an encapsulated switching balanced-ring type of mixer. The 661.4 MHz output signal from the VCO is applied to the switching input (pin 8), the received signal from the low-pass filter module is applied to the signal input (pin 1), and the 661.4 MHz difference frequency output is taken from pins 3 and 4. C17 couples the output signal from the mixer to amplifier stage TR5, and the final output at PL25 is applied to the second mixer/640 MHz board via the 661.4 band-pass filter unit. Trimmer capacitor C19 is set from maximum signal level at the output of the 661.4 band-pass filter unit, with a 500 MHz signal applied to the receiver antenna socket.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		FIRST MIXER/VCO BOARD (ST 85169)			
	Resistors				
R1	33	Metal Film	0.25	2	917060
R2	82	Thick Film	0.125	2	943877
R3	10 k	Metal Film	0.25	2	914042
R4	1 k8	Metal Film	0.25	2	911148
R5	270 k	Metal Film	0.25	2	923598
R6	1 k	Metal Film	0.25	2	913489
R7	470	Metal Film	0.25	2	920758
R8	47	Metal Film	0.25	2	917063
R9	27 k	Metal Film	0.25	2	913494
R10	100	Metal Film	0.25	2	910388
R11	100	Metal Film	0.25	2	910388
R12	27 k	Metal Film	0.25	2	913494
R13	100	Metal Film	0.25	2	910388
R14	100	Metal Film	0.25	2	910388
R15	51	Metal Film	0.25	2	917056
R16	47 k	Metal Film	0.25	2	913496
R17	20	Metal Film	0.25	2	910390
R18-R20		NOT USED			
R21	10	Thick Film	0.125	2	943865
R22	47	Metal Film	0.25	2	917063
	Capacitors		V		
C1	1 n	Ceramic Chip	50	10	939101
C2	1 n	Ceramic Disc	500	20	915243
C3	22	Electrolytic	25	+50 -10	943072
C4	33 n	Polyester	400	20	939184
C5	1 µ0	Polycarbonate	63	10	940389
C6	10	Tantalum Bead	35	20	921256
C7	1 n	Ceramic Chip	50	10	939101
C8	10	Tantalum Bead	35	20	921256
C9	2 p2	Ceramic Plate	100	0.25p	943470
C10	1 n	Ceramic Disc	500	20	915243
C11	1 n	Ceramic Disc	500	20	915243
C12	2 p2	Ceramic Plate	100	0.25p	943470
C13	1 n	Ceramic Disc	50	10	939101
C14	1 n	Ceramic Disc	500	20	915243
C15	0 µl	Polyester	100	20	931130

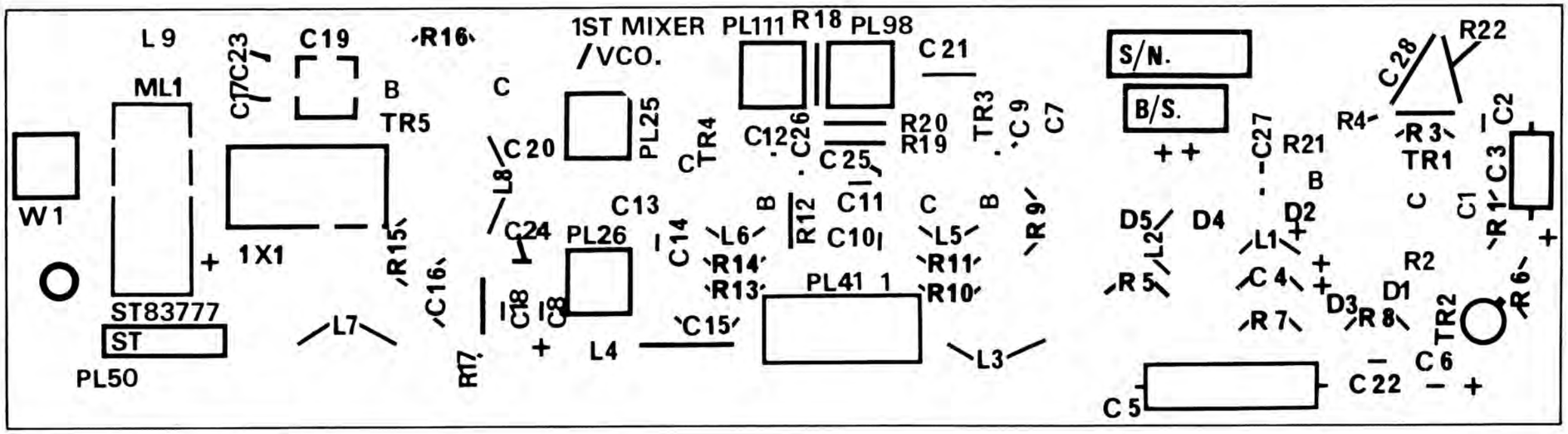
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C16	220 n	Polyester	100	20	931161
C17	22 p	Ceramic	100	20	943474
C18	1 n	Ceramic Disc	500	20	915243
C19	1p4-5p	Variable, Preset			926274
C20	1 n	Ceramic Disc	500	20	915243
C21	0 µ1	Polycarbonate	100	20	931130
C22	10 n	Ceramic Disc	40	+50 -25	926360
C23	22 p	Ceramic	100	20	943474
C24	1 n	Ceramic Disc	500	20	915243
C25 - C26	NOT USED				
C27	1 p	Ceramic Disc	50	0.25	946204
C28	100 n	Ceramic Plate	50	20	940318
	Inductors				
L1	4 µ7H	Choke		10	925362
L2	4 µ7H	Choke		10	925362
L3	150 µH	Choke		10	939162
L4	150 µH	Choke		10	939162
L5	0 µ1H	Choke		10	939847
L6	0 µ1H	Choke		10	939847
L7	150 µH	Choke		10	939162
L8	4 µ7H	Choke		10	925362
	Connectors				
PL25		Plug, coaxial, SMB, 50 Ω			935268
PL26		Plug, coaxial, SMB, 50 Ω			935268
PL41		Plug, 10-way			938859
PL50		Plug and cable assembly			BA81838
		Comprising:			
		Plug, coaxial, SMA, 50 Ω			939653
		Cable, coaxial, semi-rigid			939652
	Diodes				
D1		Varactor BB205B			939650
D2		Varactor BB205B			939650
D3		Varactor BB205B			939650
D4		Varactor BB205B			939650
D5		Varactor BB205B			939650

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Transistors			
TR1		NPN Silicon BFR91			938866
TR2		NPN Silicon BC107			911929
TR3		NPN Silicon BFR96			938867
TR4		NPN Silicon BFR96			938867
TR5		NPN Silicon BFR96			958867
		Miscellaneous			
X1		Mixer Module SRA 220			938865
W1		Cable Assembly, Rigid, Co-axial			BA81838
	NOTE:	Lines DL1 and DL2 consist of accurately dimensioned and positioned tracks on the PCB.			
		Captive Panel Fastener			930396



RACAL
TH2449 | DC85169
3

Circuit: 1st Mixer / VCO Board Fig 11.1



RACAL
TH2449 DA83776
4

Layout: 1st Mixer/VCO Board Fig 11.2

CHAPTER 12

SECOND MIXER/640 MHz BOARD

CONTENTS

Illustrations

CHAPTER 12

SECOND MIXER/640 MHz BOARD

INTRODUCTION

1. For description purposes, this board is divided into four main sections, namely (1) the 640 MHz generator and phase-locked loop, (2) the 661.4 MHz IF amplifier (together with the external 661.4 MHz band-pass filter) and the variable attenuator, (3) the second mixer, and (4) the 21.4 MHz IF amplifiers. (fig. 12(a)).

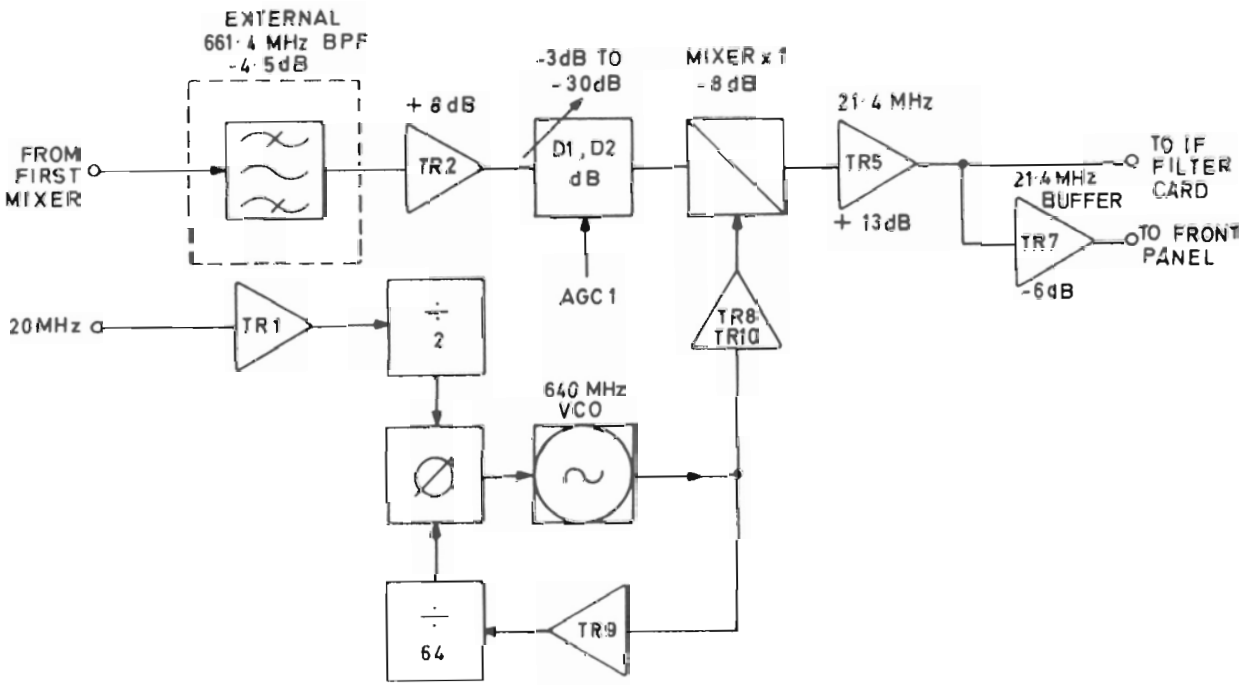


Fig.12(a) Block Diagram: Second Mixer / 640 MHz Board

CIRCUIT DESCRIPTION (Fig 12.1)

640 MHz GENERATOR AND PHASE-LOCKED LOOP

2. The 640 MHz VCO is built around TR5; the tuned circuit comprises the quarter wavelength coaxial line DL4 terminated by trimmer capacitor C35, C36, C40 and varactor diode D3. Positive feedback is provided by C42. The circuit is designed to oscillate at 640 MHz and is pulled into synchronism with the 20 MHz reference by the phase-locked loop circuit.

3. Two outputs are taken from the source of TR6 (via relatively high impedance capacitors (C44 and C45) to minimise loading), and two 640 MHz amplifier stages are thus provided to compensate for the reduction in the signal level. TR8 and TR10 form a broadly tuned amplifier to provide the required drive to the mixer, whilst TR9 amplifies the signal routed to divide-by-64 stage ML1.

4. The phase locked loop circuit comprises a phase-sensitive detector ML2a, ML2b, NAND gate ML4, and varactor driver stage TR3, TR4. The 640 MHz output signal from TR9 is divided down to 10 MHz by the emitter-coupled logic (ECL) divider ML1 and is then applied to the clock input of ML2a, whilst the 20 MHz reference input at PL61 is applied to the clock input of ML2b via amplifier stage TR1 and divide-by-two stage ML3b.

5. A timing diagram of the phase-sensitive detector is given on the circuit diagram, fig. 12.1. A positive-going transition of the VCO derived 10 MHz signal at the clock input of ML2a transfers the '1' at the D input to the Q output; similarly, a positive-going transition of the 10 MHz reference signal at the clock input of ML2b transfers the '1' at the D input to the Q output. When both Q outputs are at logic '1', both sections of ML2 are reset by the '0' output from ML4. Negative-going pulses are thus produced at the $\overline{Q}$ output of ML2a, where the pulse width is proportional to the phase error between the two 10 MHz signals. These pulses are used to switch TR4 on for short periods of time.

6. TR3 and TR4 are both constant current genrators with outputs in the ratio 1 to 7 (set by the values of R18 and R19). C28 is thus charged constantly by TR3 and is discharged by the conduction of TR4 to produce an average voltage proportional to phase error. This voltage is used to control the varactor diode D3 and is adjusted by C35 to give a level of approximately 5.5 V at TP4 for the in-lock condition.

7. Potential divider R20, R21 is included to produce a sample of the varactor line voltage (approximately 0.8 V for 5.5 V at TP4) which is routed to the processor card via PL38 pins 9 and 10 for receiver self-test purposes. Phase lock is normally achieved with a varactor voltage in the range 2.5 V to 8.5 V (0.35 V to 1.25 V at PL38 pins 9 and 10); any voltage outside these limits is normally interpreted as an out-of-lock condition.

661.4 MHz IF STAGES

8. The output signal from the first mixer/VCO board is routed to the second mixer/640 MHz board via the band-pass filter unit. This is a passive device with 50 ohm input and output impedances, an insertion loss of approximately 4.5 dB, a ±3 dB bandwidth of ±1.5 MHz, and a -60 dB bandwidth of ±10 MHz, centred on 661.4 MHz. It is a non-repairable item and the internal adjustment screws must NOT be disturbed.

9. After filtering, the 661.4 MHz IF signal is matched by C9 and DL1 to amplifier stage TR2, which has a gain of approximately 8 dB. C9 is adjusted for maximum sensitivity at low signal levels.

10. The amplifier stage is followed by a variable attenuator, which uses two PIN diodes, D1 and D2. Two coupled parallel tuned lines, DL2 and DL3 tuned by C17 and C20 respectively, are made to resonate at 661.4 MHz.

Since a PIN diode is effectively connected across each tuned circuit (via C19 and C21), and since the impedance of a pin diode is inversely proportional to the current flowing through the diode, a high voltage level at PL38 pins 3 and 4 (10 V to 15 V) results in little or no diode forward current and thus minimum attenuation of the signal. In the presence of a strong received signal, the level of the AGC 1 voltage (from the AGC card) is reduced, this results in an increase in diode current, a subsequent decrease in the impedance of each diode, and the Q of each tuned circuit is damped thereby increasing the attenuation. A maximum attenuation figure of approximately 40 dB is achieved with an AGC1 voltage level of approximately 4 V (2.5 mA through R11). With a 10 to 15 V level at the AGC1 input, no current is drawn through the diodes and a loss of approximately 3 dB results. C17 and C20 are adjusted for maximum sensitivity at low signal levels with the AGC1 line at a high level.

SECOND MIXER

11. X1 is a non-repairable diode ring mixer module with input and output impedances of 50 ohms. The 661.4 MHz output signal from DL3 is mixed with the 640 MHz output signal from TR10 to produce the 21.4 MHz second IF at a level approximately 8 dB below the level of the 661.4 MHz input signal.

21.4 MHz IF STAGES

12. The 21.4 MHz difference frequency output signal from the mixer is coupled by C29 to common base amplifier stage TR5. Negative feedback is applied via T1. This stage provides a matched power gain of about 13 dB and has input and output impedances of 50 ohms; these parameters are governed by the transformer turns ratio and are relatively independent of transistor characteristic variations.

13. A sample of the amplified IF signal is developed across R28 and is fed to a further amplifier stage, TR7, which provides the 21.4 MHz IF output signal available at a front panel connector. The level of this output signal is approximately 6 dB below the level applied to the IF filter card via PL60.

POWER SUPPLIES

14. AS low-level RF signals are present on this board, extensive power supply decoupling is provided to minimise interference from other high-level signals generated elsewhere within the receiver. L,C or R,C filters are fitted to most stages, with ceramic chip-type capacitors being used in the UHF section. A power supply noise filter, L18, C59, C60, reduces incoming noise on the 15 V supply up to around 100 KHz, whilst TR11 acts as a ripple filter for the 14 V supply rail. Note that current limiting is not provided for TR11 and care must be taken to prevent accidental shorting of the +14 V supply to earth with test probes etc, otherwise TR11 will be damaged.

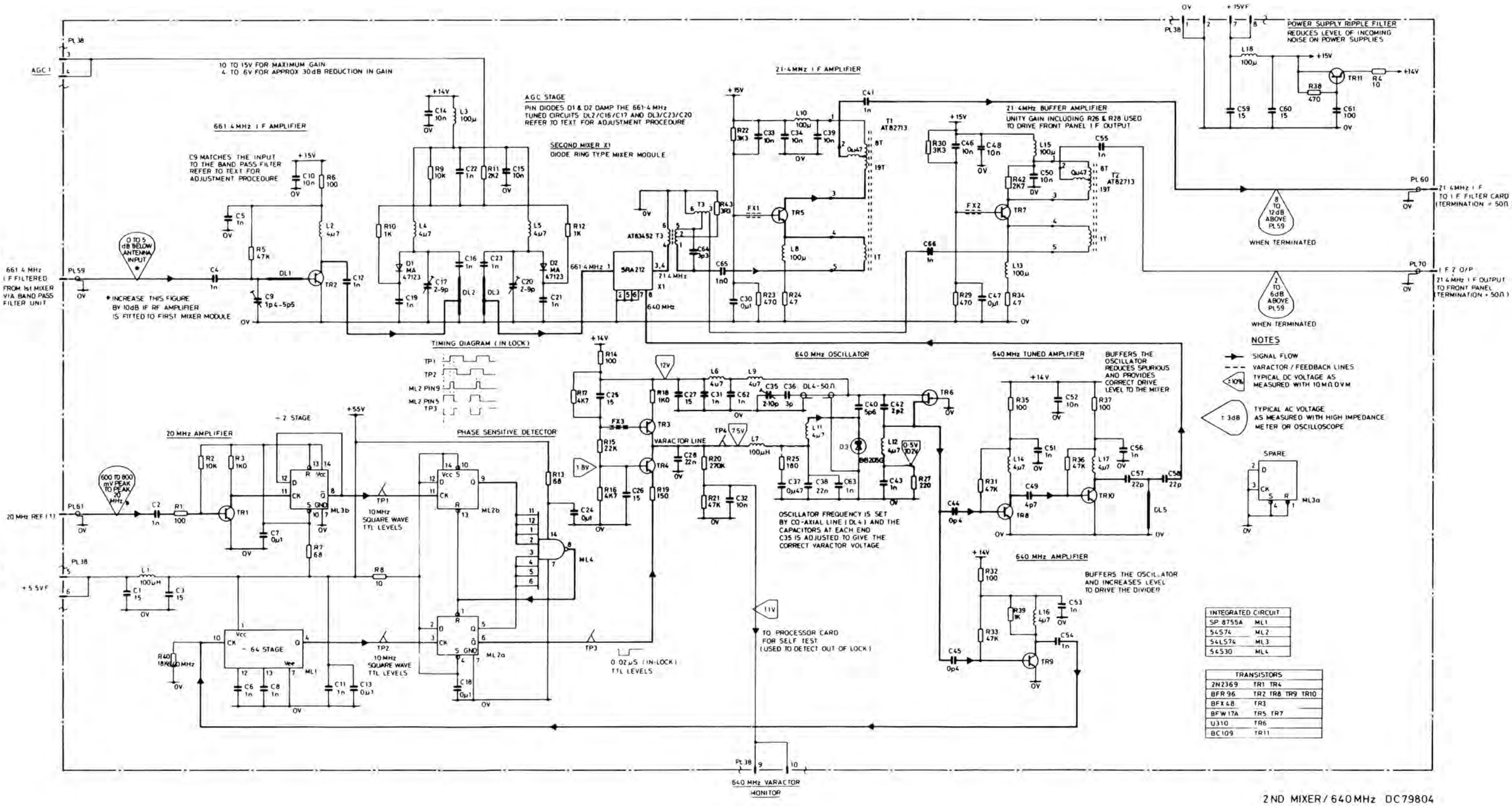
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SECOND MIXER/640 MHz BOARD (ST 79804)			
	Resistors				
R1	100	Metal Oxide		2	910388
R2	10 k	Metal Oxide		2	914042
R3	1 k	Metal Oxide		2	913489
R4	10	Metal Oxide		2	920736
R5	47 k	Metal Oxide		2	913496
R6	100	Metal Oxide		2	910388
R7	68	Metal Oxide		2	916476
R8	10	Metal Oxide		2	920736
R9	10 k	Metal Oxide		2	914042
R10	1 k	Metal Oxide		2	913489
R11	2 k2	Metal Oxide		2	916546
R12	1 k	Metal Oxide		2	913489
R13	68	Metal Oxide		2	916476
R14	100	Metal Oxide		2	910388
R15	22 k	Metal Oxide		2	913493
R16	4 k7	Metal Oxide		2	913490
R17	4 k7	Metal Oxide		2	913490
R18	1 k	Metal Oxide		2	913489
R19	150	Metal Oxide		2	910389
R20	270 k	Metal Oxide		2	923598
R21	47 k	Metal Oxide		2	913496
R22	3 k3	Metal Oxide		2	910111
R23	470	Metal Oxide		2	920758
R24	47	Metal Oxide		2	917063
R25	180	Metal Oxide		2	915465
R26	Not used				
R27	220	Metal Oxide		2	910390
R28	Not used				
R29	470	Metal Oxide		2	920758
R30	3 k3	Metal Oxide		2	910111
R31	47 k	Metal Oxide		2	913496
R32	100	Metal Oxide		2	910388
R33	47 k	Metal Oxide		2	913496
R34	47	Metal Oxide		2	917063
R35	100	Metal Oxide		2	910388
R36	47 k	Metal Oxide		2	913496
R37	100	Metal Oxide		2	910388
R38	470	Metal Oxide		2	920758
R39	1k	Metal Oxide		2	913489
R40	18k	Metal Oxide		2	900994
R41	3R3	Metal Oxide		2	941981
R42	2k7	Metal Oxide		2	916548

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
	Capacitors		V		
C1	15	Tantalum Bead	25	20	922516
C2	1 n	Ceramic Disc	500	20	915243
C3	15	Tantalum Bead	25	20	922516
C4	1 n	Ceramic Chip	50	10	939101
C5	1 n	Ceramic Chip	50	10	939101
C6	1 n	Ceramic Chip	50	10	939101
C7	0 µ1	Polyester	100	20	930801
C8	1 n	Ceramic Chip	50	10	939101
C9	2-9p	Variable, Preset			926274
C10	10 n	Ceramic Disc	250	+40 -20	900067
C11	1 n	Ceramic Chip	50	10	939101
C12	1 n	Ceramic Chip	50	10	939101
C13	0 µ1	Polyester	100	20	930801
C14	10 n	Ceramic Disc	250	+40 -20	900067
C15	10 n	Ceramic Disc	250	+40 -20	900067
C16	1 n	Ceramic Chip	50	10	939101
C17	2-9p	Variable, Preset			923004
C18	0 µ1	Polyester	100	20	930801
C19	1 n	Ceramic Chip	50	10	939101
C20	2-9p	Variable, Preset			923004
C21	1 n	Ceramic Chip	50	10	939101
C22	1 n	Ceramic Disc	500	20	915243
C23	1 n	Ceramic Chip	50	10	939101
C24	0 µ1	Polyester	100	20	930801
C25	15	Tantalum Bead	25	20	922516
C26	15	Tantalum Bead	25	20	922516
C27	15	Tantalum Bead	25	20	922516
C28	22 n	Polyester	400	20	931166
		Not used			
C30	0 µ1	Polyester	100	20	930801
C31	1 n	Ceramic Chip	50	10	939101
C32	10 n	Ceramic Disc	250	+40 -20	900067
C33	10 n	Ceramic Disc	250	+40 -20	900067
C34	10 n	Ceramic Disc	250	+40 -20	900067
C35	2-10p	Variable, Preset			943718
C36	3p	Porcelain Chip	500	0.25p	938856
C37	0 µ47	Tantalum Bead	35	20	939267
C38	22 n	Polyester	400	20	931166
C39	10 n	Ceramic Disc	250	+40 -20	900067
C40	3p	Porcelain Chip	500	0.25p	900067

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C41	1 n	Ceramic Disc	500	20	915243
C42	2 p2	Porcelain Chip	500	0.25p	940653
C43	1 n	Ceramic Chip	50	10	939101
C44	0p4	Porcelain Chip	500	0.1p	938854
C45	0p4	Porcelain Chip	500	0.1p	938854
C46	10 n	Ceramic Disc	250	+40 -20	900067
C47	0 µ1	Polyester	100	20	930801
C48	10 n	Ceramic Disc	250	+40 -20	900067
C49	4p7	Ceramic Disc	500	5	917741
C50	10 n	Ceramic Disc	50	10	939101
C51	1 n	Ceramic Chip	50	10	939101
C52	10 n	Ceramic Disc	250	+40 -20	900067
C53	1 n	Ceramic Chip	50	10	939101
C54	1 n	Ceramic Chip	50	10	939101
C55	1 n	Ceramic Disc	500	20	915243
C56	1 n	Ceramic Chip	50	10	939101
C57	22p	Ceramic Disc	500	5	940026
C58	22p	Ceramic Disc	500	5	940026
C59	15	Tantalum Bead	25	20	922516
C60	15	Tantalum Bead	25	20	922516
C61	100	Electrolytic	25	+50 -10	921546
C62	1 n	Ceramic Chip	50	10	939101
C63	1n	Ceramic Chip	50	10	939101
C64	3 p3	Ceramic Disc	500		917744
C65	1n	Ceramic Disc	500	20	915243
C66	1n	Ceramic Disc	500	20	915243
	Inductors				
L1	100 µH	Choke		10	939161
L2	4 µ7H	Choke		10	925362
L3	100 µH	Choke		10	939161
L4	4 µ7H	Choke		10	925362
L5	4 µ7H	Choke		10	925362
L6	4 µ7H	Choke		10	925362
L7	100 µH	Choke		10	939161
L8	100 µH	Choke		10	939161
L9	4 µ7H	Choke		10	925362
L10	100 µH	Choke		10	939161
L11	4 µ7H	Choke		10	925362
L12	4 µ7H	Choke		10	925362
L13	100 µH	Choke		10	925361
L14	4 µ7H	Choke		10	925362
L15	100 µH	Choke		10	939161

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
L16	4 µ7H	Choke		10	925362
L17	4 µ7H	Choke		10	925362
L18	100 µH	Choke		10	939161
		Transformers			
T1		Transformer Assembly			AT82028
T2		Transformer Assembly			AT82028
T3		Transformer Assembly			AT83542
		Connectors			
PL38		Plug, 10-way			938859
PL59		Plug, Coaxial, 50 Ω			935268
PL60		Plug, Coaxial, 50 Ω			935268
PL61		Plug, Coaxial, 50 Ω			935268
PL70		Plug, Coaxial, 50 Ω			935268
		Diodes			
D1		PIN MA 47123			938862
D2		PIN MA 47123			938862
D3		Varactor BB205B			939650
		Transistors			
TR1		NPN Silicon 2N2369			939306
TR2		NPN Silicon BFR96			938867
TR3		PNP Silicon BFX48			915231
TR4		NPN Silicon 2N2369			939306
TR5		NPN Silicon BFW17A			920012

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
TR6		N-Channel FET U310			932518
TR7		NPN Silicon BFW17A			920012
TR8		NPN Silicon BFR 96			938867
TR9		NPN Silicon BFR 96			938867
TR10		NPN Silicon BRF 96			938867
TR11		NPN Silicon BC109			923234
		Integrated Circuits			
ML1		Divide by 64 SP8755A			938887
ML2		Dual D-type flip-flop 54S74J			939472
ML3		Dual D-type flip-flop 54LS74J			938312
ML4		8-input NAND gate 54S30J			939471
		Miscellaneous			
X1		Mixer Module SRA212			938865
FX1		Ferrite Bead			907488
FX2		Ferrite Bead			907488
FX3		Ferrite Bead			907488
		Test Point			936148
		14-pin DIL IC Socket			940902
		Heatsink (for TR5, TR7)			939473
	Note	Delay lines DL1, DL2, DL3, and DL5 consist of accurately dimensioned and positioned tracks on the PCB. DL4 is fabricated from a short length of semi-rigid coaxial cable.			
		Captive Panel Fastener			930396



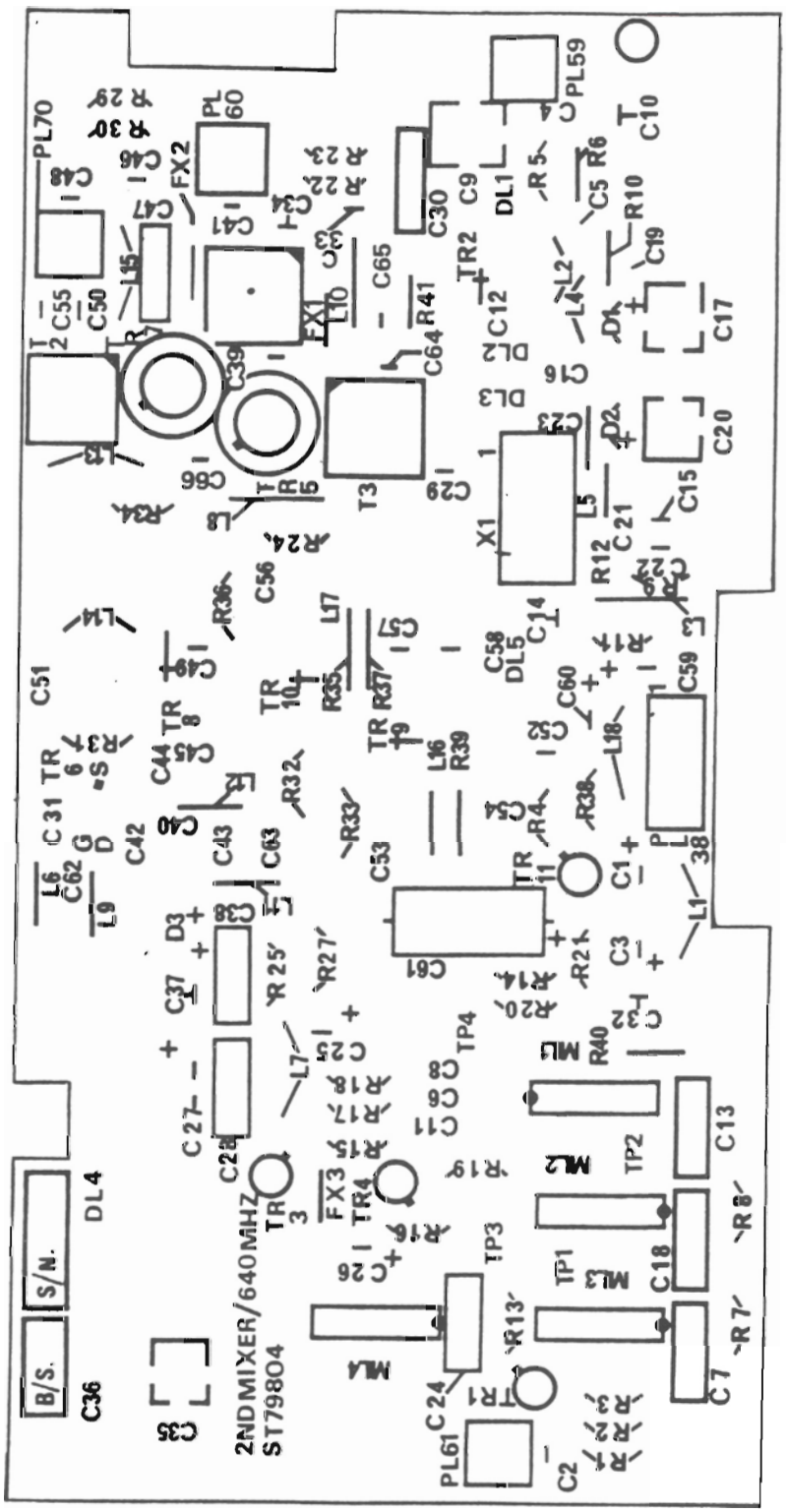
2ND MIXER / 640MHz DC79804

RACAL

TH2449/3	DC79804
9	

Circuit Diagram:
2nd Mixer / 640 MHz

Fig.12.1



Layout: Second Mixer/640MHz Board Fig. 12.2

CHAPTER 13

IF FILTER CARD

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Tables

Illustrations

CHAPTER 13

IF FILTER CARD

INTRODUCTION

1. The IF filter card provides most of the receiver IF gain and selectivity. It contains the 21.4 MHz IF filters, a gain-controlled 21.4 MHz IF amplifier, the third mixer stage, the 1.4 MHz IF amplifiers, and the 1.4 MHz IF filters.

CIRCUIT DESCRIPTION (Fig 13.1)

IF Filter Selection

2. IF filter selection data from the processor card is routed to the IF filter card (edge connector pins 29 to 32) via a 4-bit latch on the AGC card. The decoder circuit, which uses a dual binary to 1-of-4 decoder device ML4a, ML4b, is so arranged that when one of the 1.4 MHz IF filters (FL1 to FL4) is selected, 21.4 MHz IF filter FL5 is also selected. The 1.4 MHz filter condition is set to wideband when one of the 21.4 MHz filters (FL5, FL6 or a 300 KHz L-C filter) is selected as the operational bandwidth.

3. PIN diodes (D1 to D9) are used for 21.4 MHz filter selection, whilst general purpose switching diodes (D13 to D22) are used for 1.4 MHz filter selection. The table on the circuit diagram (fig 13.1) shows that when a filter in the range 1 to 4 is selected, the f3 select line (edge converter pin 29) is held at a '0', ML4b is enabled, and the levels present at the f1 and f0 select lines are decoded to produce the required 1-of-4 output. The '0' at the enable input of ML4 also causes conduction of D17, the voltage at the junction of R50 and D17 falls to approximately 2 V, and this causes D22 to become reverse biased and so isolate the IF signal from C63. The '1' at the appropriate Q output of ML4b reverse biases diode D13, D14, D15 or D16, whilst diode D10, D19, D20 or D21 becomes forward biased for the output signal from the selected filter.

4. The table on fig 13.1 also shows that the f2 select line (edge connector pin 30) is at a '1' for a selected filter in the range 1 to 4. This holds ML4a in the disabled state, causes conduction of D1 (via R13 and R2), and reverse biases D4; this in turn allows conduction of D7 and the 21.4 MHz IF signal from T1 is routed via FL5. A '1' at the enable input of ML4a forces the Q1 and Q2 outputs to a '0' to isolate FL6 and the 300 KHz L-C filter (diodes D2, D8, D3 and D9 reverse biased, diodes D5 and D6 forward biased).

5. When filter 5, 6 or 7 (300 KHz L-C filter) is selected, the f3 select line is set to a '1' to select the 1.4 MHz wideband condition, and the levels present on the f0, f1 and f2 lines select the appropriate 21.4 MHz filter.

21.4 MHz IF Amplifier

6. The output signal from the selected 21.4 MHz IF filter is coupled by C25 to a low noise FET common gate amplifier TR1. The gain of this stage is controlled by PIN diode D10 which is fed from the AGC2 signal from the AGC

card (Chap 14). The output signal from tuned circuit L7, C32, C33 is applied to a 21.4 MHz cascode amplifier TR2, TR3, and is then applied to the signal input pin of the third mixer device ML3.

Third Mixer

7. A switching type of integrated circuit mixer, ML3, is used to produce the final IF output signal at 1.4 MHz. The 21.4 MHz IF signal is applied to the signal input (pins 1 and 4), the 20 MHz reference signal is a applied to the switching (carrier) input (pins 8 and 10), and the difference frequency output is taken from pins 6 and 12. This is applied to a 1.4 MHz 300 kHz bandwidth LC filter before application to a 1.4 MHz If amplifier stage ML5. This is a wideband amplifier with differential input and output. The gain is determined by the value of resistor R38, which is connected across the gain select pins G1a and G1b. The amplified output signal is applied via C50 in parallel to the input of each 1.4 MHz filter, and is also applied via R39 to a level detector R40, C48, C49, D11, D12. The positive and negative-going output signals (Y and Z) from this detector are applied to a gain control distribution stage on the AGC card to reduce the gain of the first and second IF amplifier stages (via AGC1 and AGC2) for strong signals outside the 1.4 MHz bandwidth.

1.4 MHz IF Amplifier

8. The output signal from the selected 1.4 MHz filter is coupled by C70 to a dual voltage-controlled(AGC3) amplifier stage ML2. This is followed by a 1.4 MHz 300 KHz bandwidth L-C filter which feeds the emitter-follower output buffer stage TR4. A +12 V supply for ML2 is provided by three-terminal regulator ML1.

IF Filters

9. The standard filter option for the RA 1794A receiver comprises seven symmetrical filters. Three of these are 21.4 MHz filters (one 300 KHz L-C filter and two crystal filters) whilst the remaining four are 1.4 MHz crystal filters. Normally one of the 1.4 MHz crystal filters is shifted within the IF passband to be used as both an upper sideband and a lower sideband filter. The standard filter arrangement is as shown in table 1.

Table 1: Standard Filter Option

FILTER CODE	CIRCUIT REF	BANDWIDTH KHz	FILTER OFFSET KHz (BFO)
0	FL1	0.3	-
1	FL2	1.2	-
2	FL3	3.0	-
3	FL4	8.0	-
4	FL5	15	-
5	FL6	30	-
6	FL7	300	-
USB	FL3	3.0	+1.80
LSB	FL3	3.0	-1.80

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		IF FILTER CARD (ST 80453)			
	Resistors				
R1	6 k8	Metal Oxide		2	910112
R2	6 k8	Metal Oxide		2	910112
R3	6 k8	Metal Oxide		2	910112
R4	6 k8	Metal Oxide		2	910112
R5	100	Metal Oxide		2	910388
R6	220	Metal Oxide		2	910390
R7	6 k8	Metal Oxide		2	910112
R8	6 k8	Metal Oxide		2	910112
R9	6 k8	Metal Oxide		2	910112
R10	470	Metal Oxide		2	910758
R11	47	Metal Oxide		2	917063
R12	470	Metal Oxide		2	920758
R13	470	Metal Oxide		2	920758
R14	6 k8	Metal Oxide		2	910112
R15	3 k3	Metal Oxide		2	910111
R16	3 k3	Metal Oxide		2	910111
R17	3 k 3	Metal Oxide		2	910111
R18	220	Metal Oxide		2	910390
R19	100	Metal Oxide		2	910388
R20	47	Metal Oxide		2	917063
R21	10 k	Metal Oxide		2	914042
R22	1 k	Metal Oxide		2	913489
R23	220	Metal Oxide		2	910390
R24	100	Metal Oxide		2	910388
R25	100	Metal Oxide		2	910388
R26	4 k7	Metal Oxide		2	913490
R27	100	Metal Oxide		2	910388
R28	10	Metal Oxide		2	920736
R29	6 k8	Metal Oxide		2	910112
R30	2 k2	Metal Oxide		2	916546
R31	4 k7	Metal Oxide		2	913490
R32	150	Metal Oxide		2	910389
R33	220	Metal Oxide		2	910390
R34	10 k	Metal Oxide		2	914042
R35	10 k	Metal Oxide		2	914042

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	33	Metal Oxide		2	917060
R37	4 k7	Metal Oxide		2	913490
R38	1 k5	Metal Oxide		2	911166
R39	1 k	Metal Oxide		2	913489
R40	1 k5	Metal Oxide		2	911166
R41	1 k	Metal Oxide		2	913489
R42	1 k	Metal Oxide		2	913489
R43	1 k	Metal Oxide		2	913489
R44	1 k	Metal Oxide		2	913489
R45	1 k	Metal Oxide		2	916546
R46	5 k6	Metal Oxide		2	918128
R47	5 k6	Metal Oxide		2	918128
R48	5 k6	Metal Oxide		2	918128
R49	5 k6	Metal Oxide		2	918128
R50	5 k6	Metal Oxide		2	918128
R51	470	Metal Oxide		2	920758
R52	470	Metal Oxide		2	920758
R53	470	Metal Oxide		2	920758
R54	470	Metal Oxide		2	920758
R55	470	Metal Oxide		2	920758
R56	1 k8	Metal Oxide		2	911148
R57	50 k	Variable, Preset		2	935105
R58	2 k2	Metal Oxide		2	916546
R59	6 k8	Metal Oxide		2	910112
R60	2 k	Metal Oxide		2	932939
R61	47	Metal Oxide		2	917063
R62	4 k7	Metal Oxide		2	913490
R63	47	Metal Oxide		2	917063
R64	10 k	Metal Oxide		2	014042
R65	10 k	Metal Oxide		2	914042
R66	1 k2	Metal Oxide		2	911179
R67	220	Metal Oxide		2	910390

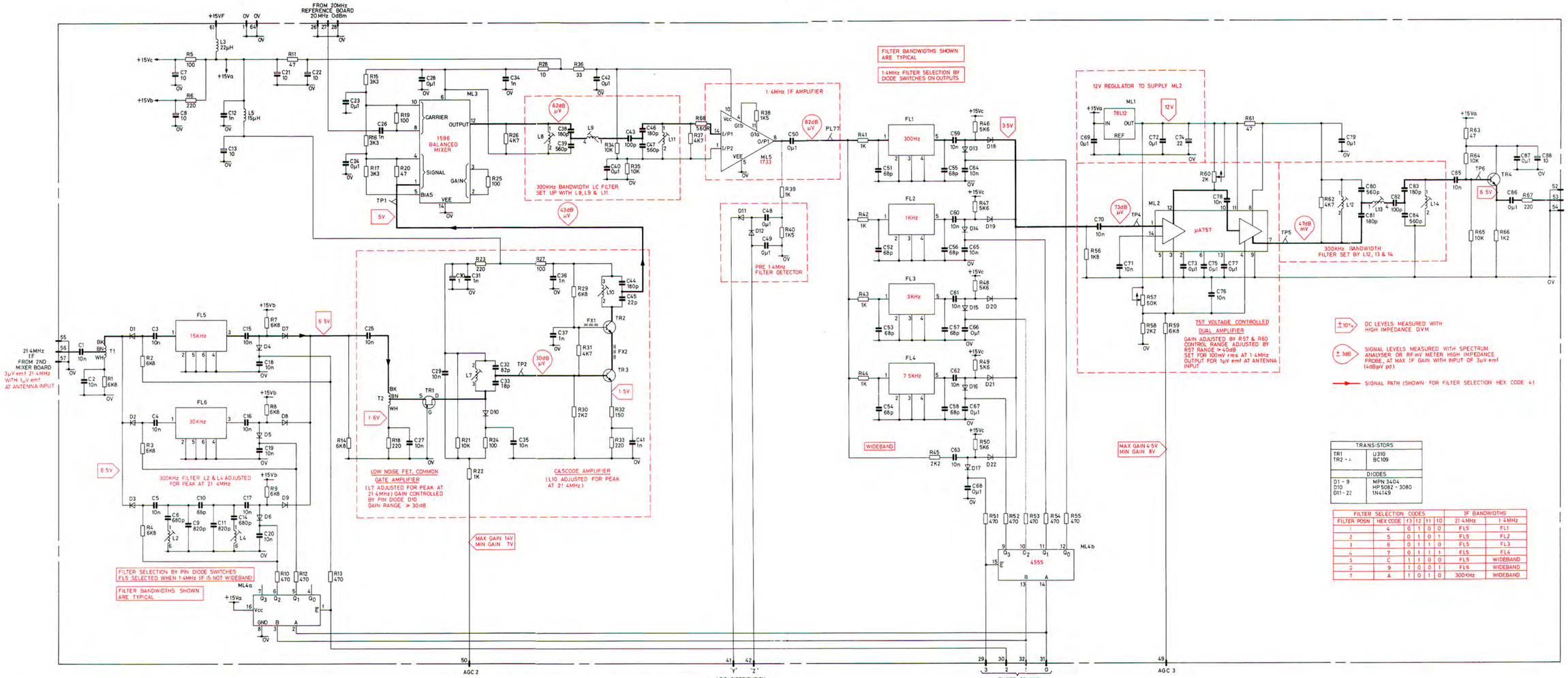
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
	Capacitors		V		
C1	10 n	Ceramic Disc	250	+40 -20	916187
C2	10 n	Ceramic Disc	250	+40 -20	916187
C3	10 n	Ceramic Disc	250	+40 -20	916187
C4	10 n	Ceramic Disc	250	+40 -20	916187
C5	10 n	Ceramic Disc	250	+40 -20	916187
C6	680 p	Silver Mica	100	2	93910
C7	10	Tantalum Bead	35	20	921256
C8	10	Tantalum Bead	35	20	921256
C9	820 p	Silver Mica	100	2	917737
C10	68 p	Ceramic Disc	500	10	917737
C11	820 p	Silver Mica	100	2	931735
C12	1 n	Ceramic Disc	500	20	915243
C13	10	Tantalum Bead	35	20	921256
C14	680 p	Silver Mica	100	2	939100
C15	10 n	Ceramic Disc	250	+40 -20	916187
C16	10 n	Ceramic Disc	250	+40 -20	916187
C17	10 n	Ceramic Disc	250	+40 -20	916187
C18	10 n	Ceramic Disc	250	+40 -20	916187
C19	10 n	Ceramic Disc	250	+40 -20	916187
C20	10 n	Ceramic Disc	250	+40 -20	916187
C21	10	Tantalum Bead	35	20	921456
C22	10	Tantalum Bead	35	20	921256
C23	0 µl	Ceramic Disc	50	20	938857
C24	0 µl	Ceramic Disc	50	20	938857
C25	10 n	Ceramic Disc	250	+40 -20	916187
C26	1 n	Ceramic Disc	500	20	915243
C27	10 n	Ceramic Disc	250	+40 -20	916187
C28	0 µl	Ceramic Disc	50	20	938857
C29	10 n	Ceramic Disc	250	+40 -20	916187
C30	1 µ0	Tantalum Bead	35	20	923571
C31	1 n	Ceramic Disc	500	20	915243
C32	82 p	Silver Mica	400	1 p	935524
C33	22 p	Silver Mica	400	1 p	930803
C34	1 n	Ceramic Disc	500	20	915243
C35	10 n	Ceramic Disc	250	+40 -20	916187

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C36	1 n	Ceramic Disc	500	20	915243
C31	1 n	Ceramic Disc	500	20	915243
C38	180 p	Silver Mica	100	2	938997
C39	560 p	Silver Mica	100	2	938999
C40	0 µl	Ceramic Disc	50	20	938857
C41	1 n	Ceramic Disc	500	20	915243
C42	0 µl	Ceramic Disc	50	20	938857
C43	100 p	Silver Mica	400	2	931736
C44	180 p	Silver Mica	100	2	938997
C45	22 p	Silver Mica	400	1 p	930803
C46	180 p	Silver Mica	100	2	938997
C47	560 p	Silver Mica	100	2	938999
C48	0 µl	Ceramic Disc	50	20	938857
C49	0 µl	Ceramic Disc	50	20	938857
C50	0 µl	Ceramic Disc	50	20	938857
C51	68 p	Ceramic Disc	500	10	917737
C52	68 p	Ceramic Disc	500	10	917737
C53	68 p	Ceramic Disc	500	10	917737
C54	68 p	Ceramic Disc	500	10	917737
C55	69 p	Ceramic Disc	500	10	917737
C56	68 p	Ceramic Disc	500	10	917737
C57	68 p	Ceramic Disc	500	10	917737
C58	68 p	Ceramic Disc	500	10	917737
C59	10 n	Ceramic Disc	250	+40 -20	916187
C60	10 n	Ceramic Disc	250	+40 -20	916187
C61	10 n	Ceramic Disc	250	+40 -20	916187
C62	10 n	Ceramic Disc	250	+40 -20	916187
C63	10 n	Ceramic Disc	250	+40 -20	916187
C64	10 n	Ceramic Disc	250	+40 -20	916187
C65	10 n	Ceramic Disc	250	+40 -20	916187
C66	0 µl	Ceramic Disc	50	20	938857
C67	0 µl	Ceramic Disc	50	20	938857
C68	0 µl	Ceramic Disc	50	20	938857
C69	0 µl	Ceramic Disc	50	20	938857
C70	10 n	Ceramic Disc	250	+40 -20	916187
C71	10 n	Ceramic Disc	250	+40 -20	916187
C72	0 µl	Ceramic Disc	50	20	938857
C73	0 µl	Ceramic Disc	50	20	938857
C74	22	Tantalum Bead	16	20	938857
C75	0 µl	Ceramic Disc	50	20	938857

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C76	10 n	Ceramic Disc	250	+40 -20	916187
C77	0 µl	Ceramic Disc	50	20	938857
C78	10 n	Ceramic Disc	250	+40 -20	916187
C72	0 µl	Ceramic Disc	50	20	938857
C80	560 p	Silver Mica	100	2	938999
C81	180 p	Silver Mica	100	2	938997
C82	100 p	Silver Mica	400	2	931736
C83	180 p	Silver Mica	100	2	938997
C84	560 p	Silver Mica	100	2	938999
C85	10 n	Ceramic Disc	250	+40 -20	916187
C86	0 µl	Ceramic Disc	50	20	938857
C87	0 µl	Ceramic Disc	50	20	938857
C88	10	Tantalum Bead	35	20	921256
	Inductors				
L1	Not used				
L2		Coil Assembly			AT 81917
L3	22 µH	Choke		10	939164
L4		Coil Assembly			AT 81917
L5	15 µH	Choke		10	938955
L6	Not used				
L7		Coil Assembly			AT 81915
L8		Coil Assembly			AT 81912
L9		Coil Assembly			AT 81911
L10		Coil Assembly			AT 81916
L11		Coil Assembly			AT 81912
L12		Coil Assembly			AT 81912
L13		Coil Assembly			AT 81911
L14		Coil Assembly			AT 81912
	Transformers				
T1		Transformer Assembly			AT 81913
T2		Transformer Assembly			AT 81914

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Diodes			
D1		PIN MPN 3404			938863
D2		PIN MPN 3404			938863
D3		PIN MPN 3404			938863
D4		PIN MPN 3404			938863
D5		PIN MPN 3404			938863
D6		PIN MPN 3404			938863
D7		PIN MPN 3404			938863
D8		PIN MPN 3404			938863
D9		PIN MPN 3404			938863
D10		PIN HP5082-3080			921200
D11		Silicon 1N4149			914898
D12		Silicon 1N4149			914898
D13		Silicon 1N4149			914898
D14		Silicon 1N4149			914898
D15		Silicon 1N4149			914898
D16		Silicon 1N4149			914898
D17		Silicon 1N4149			914898
D18		Silicon 1N4149			914898
D19		Silicon 1N4149			914898
D20		Silicon 1N4149			914898
D21		Silicon 1N4149			914898
D22		Silicon 1N4149			914898
		Transistors			
TR1		N-Channel FET U310			932518
TR2		NPN Silicon BC109			923234
TR3		NPN Silicon BC109			923234
TR4		NPN Silicon BC109			923234

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		Integrated Circuits			
ML1		+12V Regulator 78L12			938880
ML2		Gain controlled IF Amplifier µA 757			922574
ML3		Balanced Mixer 1596			939261
ML4		Dual Binary to 1-of-4 decoder 4555			928189
ML5		Video Amplifier MC 1733L			938964
		Filters			
		1.4 MHz - 0.3 kHz			BD 81071
		1.4 MHz - 1.2 kHz			BD 81072
		1.4 MHz - 3.0 kHz			BD 81073
		1.4 MHz - 8.0 kHz			BD 81074
		21.4 MHz - 15 kHz			BD 81075
		21.4 MHz - 30 kHz			BD 81076
		Miscellaneous			
FX1, FX2		Ferrite Bead			907488
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		Test Point			936148
		Board Stiffener			BO 79561
		Captive Screw M3 x 10 mm			AD 81976
PL77		Vertical PCB Mounting			935268



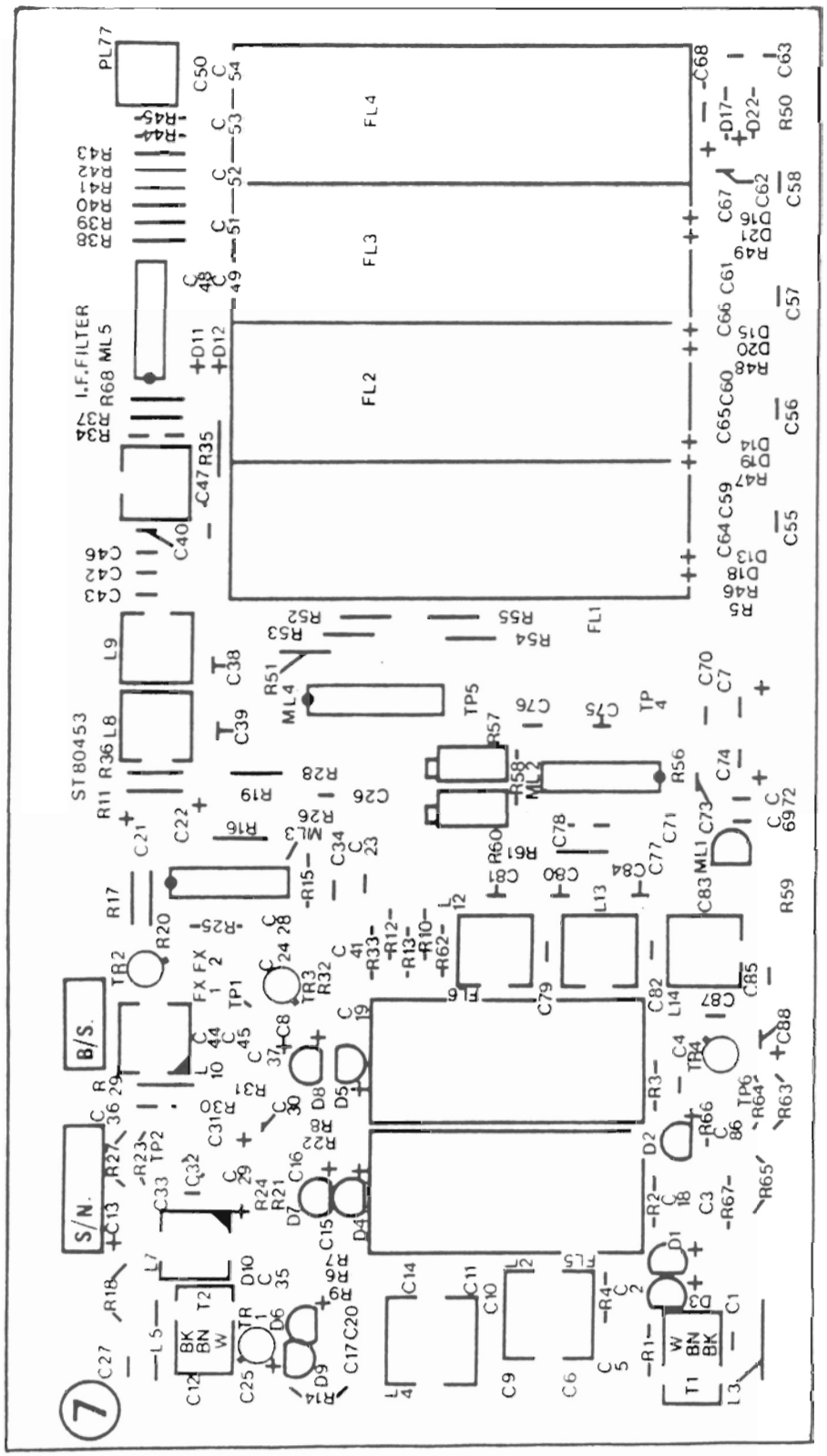
TRANSISTORS	
TR1	U310
TR2 - 4	BC109
DIODES	
D1 - 9	MPN 3404
D10	HP 5082 - 3080
D11 - 22	1N4149

FILTER SELECTION CODES						IF BANDWIDTHS	
FILTER POSN	HEX CODE	f3	f2	f1	f0	21·4MHz	1·4MHz
1	4	0	1	0	0	FL5	FL1
2	5	0	1	0	1	FL5	FL2
3	6	0	1	1	0	FL5	FL3
4	7	0	1	1	1	FL5	FL4
5	C	1	1	0	0	FL5	WIDEBAND
6	9	1	0	0	1	FL6	WIDEBAND
7	A	1	0	1	0	300KHz	WIDEBAND

RACAL
TH 2449 IDC80453 13.1 1/2 | TH2449 IDC80453 13.1 2/2

Circuit: IF Filter Card

Fig. 13.1



Layout: IF Filter Card Fig. 13.2

CHAPTER 14

AGC CARD

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AGC CARD - ST85491

INTRODUCTION

1. The main purpose of the AGC card is to control the receiver gain so as to maintain the 1.4 MHz IF signal applied to the AGC card at a level of 100 mV rms for any signal at the antenna socket in the range 0 to 100 dBμV. To achieve this, the applied IF signal is amplified, detected and then compared with a reference voltage; the voltage resulting from this comparison is then used to control the levels of three AGC voltage signals which are used to control the gains of the first, second and third IF amplifier stages (AGC1, AGC2 and AGC3).

2. AGC status is controlled by the processor card; data conveyed via a 4-bit I/O bus is first converted from 5 V levels to 15 V (C-MOS) levels and is then clocked into a latch by the appropriate strobe signal. Other latches are used for filter selection and COR (carrier operated relay) data, which is also conveyed to the AGC card via the 4-bit I/O bus.

CIRCUIT DESCRIPTION (fig 14.1)

1.4 MHz IF Output

3. The 1.4 MHz IF input, at edge connector pin 53, is coupled via C2 to the AGC detector (para 4) and is also coupled via C1 to IF output amplifier ML8b, TR1. ML8 (ML6 is a similar device) consists of five general-purpose silicon NPN transistors, where two of the transistors share a common emitter connection (pin 3) for use as a differentially connected pair. In this application, each transister is used individually, and for ease of drawing, the pin 3 connection is shown twice on the circuit diagram. TR1 is connected as an emitter follower and produces an output to the front panel (IF3) at a nominal impedance of 50 ohms.

AGC Detector

4. The 1.4 MHz IF signal is amplified by ML8d and then fed to emitter-follower stage ML8c which is temperature compensated for d.c. drift by ML8a (strapped as a diode). The output signal at TP2 is applied to ML5b of the AGC hang circuit (para 12), whilst the outputs from potential divider R17, R18, R19 are applied to the analogue signal monitoring circuitry on the processor card (Chap 7) via edge connector pin 34 and to a peak signal detector ML5a, D1, and thence via FET switch TR9 to AGC integrator ML5c, or via FET switch TR2 direct to ML5c. Peak signal detection is selected ('1' at the Q output of ML10b) for SSB and CW modes, and for the AM and FM modes provided medium or long AGC is selected. Average signal detection is selected ('0' at the Q output of ML10b) when manual only gain control is selected (regardless of selected mode) or for the AM and FM modes when short AGC is selected.

5. A 1 V reference level, derived from potential divider R20, R21, is applied to the non-inverting input of the integrator stage ML5c. Since approximately 1 V is produced at the drain of TR9 and also at the drain of TR2, for a 1.4 MHz IF input level of 100 mV r.m.s. at TP1, the result of a comparison between these two levels represents the change in receiver gain required to restore the IF input level to 100 mV.

6. Apart from the output signal from FET switch TR9 or FET switch TR2, three other input signals can affect the AGC line voltage, as listed below. The input signal to ML5c which represents the lowest receiver gain overrides the other three input signals.

   (1) IF gain control voltage at card edge connector pin 43. This comes from the processor card and represents either the setting of the front panel IF GAIN control (receiver under local control) or a manual IF gain control setting conveyed via SCORE control data (receiver under remote control).

   (2) An external AGC input level, at edge connector pin 38, from, for example, the second receiver in a diversity configuration.

   (3) Manual-only control input.

7. The range of the output voltage from ML5c, at TP3, is between approximately 1 V for minimum IF gain and 10 V for maximum IF gain. The potential divider formed by R40, R41 and R42 reduces the voltage level at the non-inverting input of ML4a to a quarter of the level at TP3, whilst 0 to 2.7 V IF gain voltage is applied to the inverting input of ML4a via voltage follower ML4d. If the level at TP3 is greater than four times the IF gain voltage level, then the output from ML4a goes positive, D9 conducts, and the level at the inverting input of ML5c is raised until the level at TP3 is brought down to equal four times the IF gain voltage level.

8. If an IF signal is present and is at a level greater than 100 mV r.m.s. (measured at TP1), then the proportionately higher level at the inverting input of ML5c causes the level at TP3 to drop and this causes a corresponding reduction in the receiver IF gain. This allows the IF GAIN control to be used to set the AGC threshold i.e. the maximum receiver gain is set by the front panel IF GAIN control. For full AGC operation, the IF gain input voltage is held at 2.7 V to maintain the maximum threshold, and the front panel IF GAIN control is disabled.

9. ML4b is used to compare the level at TP3 with an externally applied voltage on the AGC level IN/OUT line. If the external voltage is lower, the output from ML4a goes positive, D8 conducts and the level applied to ML5c rises until the level at TP3 is brought down to match the AGC IN/OUT level.

10. When manual-only control is selected, transmission gate ML3d is turned on ('1' at the $\overline{Q}$ output of ML11a), FET switch TR9 is turned off ('1' at the $\overline{Q}$ output of ML10b), so that the level at TP3 is solely dependent on the level of the IF gain voltage and the corresponding output from ML4a, D9. Manual gain control can now only be overriden by a lower input on the AGC level IN/OUT line.

Decay Time Constant

11. For peak signal detection (FET switch TR9 turned on), and following a drop in the IF signal level, the integrator capacitor C15 is allowed to discharge through R28, R29 or R30, depending on the state of the Q3 and Q2 outputs from latch ML9. Decay is however, inhibited when a '0' is present at the output of the ML5d (AGC hang circuit), since gates G2, G3 and G4 all have open-drain outputs.

AGC Hang

12. When a signal is present and the receiver is under the control of the AGC circuit, the level at TP2 (emitter of transistor ML8c) is higher than the 1 V reference set by potential divider R20, R21. The level at the non-inverting input of ML5b is thus higher than the level at the inverting input, the positive output voltage charges C9 via D2, and also results in a '1' at the output of ML5d.

13. When the IF signal is removed, the conditions at the input of ML5b are reversed; the '0' at the output reverse biases D2 and also causes the voltage at the non-inverting input of ML5d to become less positive than that at the inverting input (which is held up by the charge stored in C9). The output of ML5d thus changes to a '0' to inhibit AGC decay until C9 has discharged via R27 (long hang) or R26 (short hang) sufficiently to cause ML5d to switch and re-enable the AGC decay select gates. If a short-duration IF signal occurs, C9 only charges partially and the hang time is correspondingly reduced. When hang is not selected ('0' at the Q4 output of latch ML9), D3 holds the inverting input of ML5d at a '0', and a '1' is maintained at the output.

14. AGC hang is enabled for the CW and SSB modes only. The short hang time period is selected when a short AGC time constant is selected, whilst the long hang time is selected when AGC medium or long is selected.

AGC Dump

15. The AGC dump circuit is activated each time the strobe 4 signal occurs (para 26) but the AGC capacitors are only discharged when the level of the IF input signal at TP1 results in a d.c. level at TP2 lower than the 1 V reference established by potential divider R20, R21. Furthermore, the AGC capacitors are only discharged to the level appropriate to the strength of the signal being received. The action of the circuit is as follows.

16. When a signal is being received and the receiver is under the control of the AGC circuit, the level at TP2 is higher than the 1 V reference level. This results in a '1' at the output of ML5b and the dump latch ML10a is held reset. Only when the IF signal is removed and the level at TP2 is lower than the 1 V reference level is the reset removed from ML10a to allow AGC dumping following a change in mode and/or AGC function. When this occurs, the strobe 4 signal at card edge connector pin 33 is applied via translator ML12 to the clock input of ML10a, the '1' at the D input is transferred to the Q output, and this is routed to:

(1) Open-drain inverting gate G1 to discharge C9 via D5 and C15 via D6 and D7.

(2) Transmission gate ML3b to discharge the AGC filter capacitor C19 via R47.

17. If a signal is received before the AGC capacitors are fully discharged, discharging ceases when the level of the IF signal at TP1 causes the d.c. level at TP2 to exceed the 1V reference level, at which point the AGC dump latch ML10a is reset.

AGC Filtering

18. In the peak detect mode, the signal at TP3 is filtered by R47 and C19 before application to the voltage-follower buffer stage ML4c. If the IF signal level is increasing, then D11 is forward biased and R49 shunts R50 to provide a fast attack time constant.

19. In the average detect mode, transmission gate ML3c is enabled ('1' at the $\overline{Q}$ output of ML10b) and the filter is bypasssed by R48.

AGC Distribution

20. To achieve optimum receiver noise performance, attenuation of receiver gain should initially occur at the third intermediate frequency (1.4 MHz IF stage), then, after a 25 dB reduction, at the second (21.4 MHz) IF, and finally, at the first (661.4 MHz) IF. The purpose of the AGC distribution circuit is thus to apportion gain control according to these requirements.

21. At maximum IF gain, TP4 is at 10 V and the output of integrator ML7c is at its upper limit (13 V). Whilst the non-inverting input of ML7d is held constant, this stage acts simply as an inverting amplifier. If the level at TP4 falls, the output of ML7d increases, and this level (AGC3) is used to control the gain of the 1.4 MHz (third IF) amplifier. This action continues as the level at TP4 falls until the rising level at the inverting input of ML7c reaches the reference level at the non-inverting input. The level at the output of ML7c then begins to fall from its upper limit; this is fed back to the non-inverting input of ML7d such that its output level (AGC3) is maintained at the reference level set by R61.

22. A further fall in the AGC level at TP4 causes the voltage level at TP6 to fall to the lower limit of 0.6 V. When this lower limit is reached, ML7d again acts as an inverting amplifier and the AGC3 level begins to rise again.

23. The delay around ML7c ensures that a step change in the signal level at TP1 is first controlled at 1.4 MHz (the third IF); the gain control is then evened-out over all three IF stages.

PIN Diode Drive Amplifier

24. The drive current required by the PIN diode attenuator on the first and second mixer boards is developed as a logarithimic function of the voltage at TP6 by ML7a, ML6a, ML6b for AGC2 and by ML7b, ML6c, ML6d for AGC1. This function is derived using the law of the base-to-emitter junction of a transistor (ML6b, ML6d), thus defining the collector current which becomes the PIN diode forward current. Resistor R58 introduces a slight difference between the reference level at the non-inverting input of ML7a and that at the non-inverting input of ML7b so that attenuation at the second IF starts before that at the first IF.

25. The level of the drive signal at TP7 can be controlled from outside the main AGC loop by the output from a pre 1.4 MHz filter detector on the IF filter board (AGC distribution control inputs Y and Z at edge connector pins 41 and 42). If a large signal is present within the 21.4 MHz IF bandwidth but is outside the 1.4 MHz bandwidth, the positive and negative Y and Z signals from the pre 1.4 MHz filter detector are used to offset the inputs conditions of ML7a. The main AGC loop is unaffected but the overall receiver sensitivity is reduced by the amount of attenuation in the first and second IF stages. Any possible overloading before the third IF stage is thus avoided.

Processor Interface

26. Communication between the processor card and the AGC card is via a 4-bit I/O bus (edge connector pins 19 to 22) together with a 15 V logic enable line (pin 48) and four strobe signals (pins 33, 45, 46 and 47). Whenever a new filter or AGC mode is selected, or whenever the COR (carrier operator relay) threshold is reached, the processor applies a '1' to the 15 V logic enable line (to enable voltage translators ML12 and ML14). The required data is applied to the 4-bit I/O bus and the appropriate strobe line is then pulsed to clock the data into the appropriate latch. The coding of the I/O bus data corresponding to strobes 3, 4 and 5 is given in the following tables. Strobe 6 is applied to the clock input of latch ML15 to energise or de-energise a carrier operated relay (or similar device) via open collector transistor TR2 and pin B of either of the two multiway audio connectors on the receiver front panel.

Table 1 : AGC1 & AGC2 Data (Strobes 3 & 4)

	SSB & CW								AM & FM							
	STROBE 3				STROBE 4				STROBE 3				STROBE 4			
	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
SHORT	1	0	0	1	1	1	1	D	1	0	1	0	0	1	1	D
MEDIUM	0	1	1	1	1	1	1	U	0	1	0	0	1	1	1	U
LONG	0	0	1	1	1	1	1	M	0	0	0	0	1	1	1	M
MAN ONLY	1	0	1	0	0	0	1	P	1	0	1	0	0	0	1	P

Table 2 : IF Filter Select Data (Strobe 5)

I/O BUS					SELECTED
HEX	3	2	1	0	FILTER
4	0	1	0	0	FL1
5	0	1	0	1	FL2
6	0	1	1	0	FL3
7	0	1	1	1	FL4
C	1	1	0	0	FL5
9	1	0	0	1	FL6
A	1	0	1	0	FL7

Transmission Gates and FET Transistors

27. Integrated circuits ML12, ML13 and FET switches TR4-8 are operated only when this AGC card is fitted in other equipments which require different AGC characteristics.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		AGC CARD (ST 85491)			
	Resistors				
R1	22 k	Metal Oxide		2	913493
R2	4 k7	Metal Oxide		2	913490
R3	3 k3	Metal Oxide		2	910111
R4	1 k2	Metal Oxide		2	911179
R5	3 k3	Metal Oxide		2	910111
R6	220	Metal Oxide		2	910390
R7	220	Metal Oxide		2	910390
R8	1 k	Metal Oxide		2	913489
R9	10 k	Metal Oxide		2	914042
R10	10 k	Metal Oxide		2	914042
R11	390	Metal Oxide		2	916331
R12	10 k	Metal Oxide		2	914042
R13	22 k	9 Resistor SIL Network		2	935012
R14	47	Metal Oxide		2	917063
R15	39	Metal Oxide		2	917062
R16	47	Metal Oxide		2	917063
R17	680	Metal Oxide		2	910113
R18	820	Metal Oxide		2	917065
R19	680	Metal Oxide		2	910113
R20	22 k	Metal Oxide		2	913493
R21	1 k5	Metal Oxide		2	911166
R22	47 k	Metal Oxide		2	913496
R23	10 k	Metal Oxide		2	914042
R24	10 k	Metal Oxide		2	914042
R25	47 k	Metal Oxide		2	913496
R26	33 k	Metal Oxide		2	913495
R27	220 k	Metal Oxide		2	921771
R28	47 k	Metal Oxide		2	913496
R29	10 k	Metal Oxide		2	914042
R30	1 k	Metal Oxide		2	913489
R31	22 k	Metal Oxide		2	913493
R32	220 k	Metal Oxide		2	921771
R33	1 k5	Metal Oxide		2	911166
R34	1 k5	Metal Oxide		2	911166
R35	15 k	Metal Oxide		2	920645

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	220 k	Metal Oxide		2	921771
R37	180 k	Metal Oxide		2	920644
R38	10 k	Metal Oxide		2	914042
R39	22 k	Metal Oxide		2	913493
R40	220	Metal Oxide		2	910390
R41	3 k9	Metal Oxide		2	915074
R42	1 k5	Metal Oxide		2	911166
R43	1 k0	Metal Oxide		2	913489
R44	220 k	Metal Oxide		2	921771
R45	1 k	Metal Oxide		2	913489
R46	1 k	Metal Oxide		2	913489
R47	1 k	Metal Oxide		2	913489
R48	1 k0	Metal Oxide		2	913489
R49	3 k3	Metal Oxide		2	910111
R50	22 k	Metal Oxide		2	913493
R51	100 k	Metal Oxide		2	915190
R52	10 k	Metal Oxide		2	914042
R53	47 k	Metal Oxide		2	913496
R54	15 k	Metal Oxide		2	920645
R55	68 k	Metal Oxide		2	916478
R56	18 k	Metal Oxide		2	900994
R57	470 k	Metal Oxide		2	918443
R58	3 k9	Metal Oxide		2	915074
R59	100 k	Metal Oxide		2	915190
R60	18 k	Metal Oxide		2	900994
R61	10 k	Variable, preset			940868
R62	2 k2	Metal Oxide		2	916546
R63	1 k	Metal Oxide		2	913489
R64	2 k2	Metal Oxide		2	916546
R65	1 k5	Metal Oxide		2	911166
R66	2 k2	Metal Oxide		2	916546
R67	100 k	Metal Oxide		2	915190
R68	10 k	Metal Oxide		2	914042
R69	2 k2	Metal Oxide		2	916546
R70	100	Metal Oxide		2	910388

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R71	2 k2	Metal Oxide		2	916546
R72	2 k2	Metal Oxide		2	916546
R73	330k	Metal Oxide		2	920828
R74	2 k2	Metal Oxide		2	916546
R75	10	Metal Oxide		2	920736
R76	10	Metal Oxide		2	920736
R77	270 k	Metal Oxide		2	923598
R78	270 k	Metal Oxide		2	923598

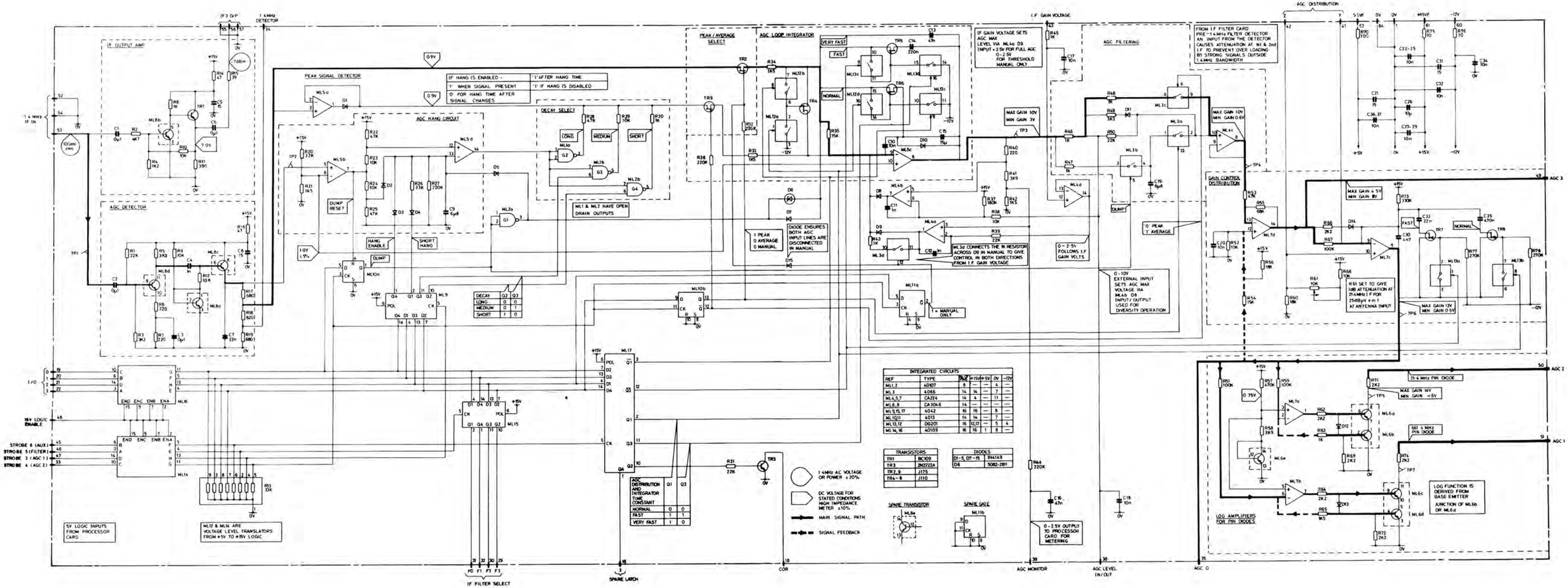
	Capacitors		V		
C1	0 µ1	Polycarbonate	100	10	931130
C2	0 µ1	Polycarbonate	100	10	931130
C3	0 µ1	Polycarbonate	100	10	931130
C4	1 n	Ceramic Plate	50	10	940312
C5	15	Tantalum Bead	25	20	922516
C6	0 µ1	Polycarbonate	100	10	931130
C7	22 n	Polycarbonate	100	10	931137
C8	15	Tantalum Bead	25	20	922516
C9	6 µ8	Tantalum Bead	35	20	923573
C10	10 n	Ceramic Plate	50	10	940315
C11	1 n	Ceramic Plate	50	10	940312
C12	1 n	Ceramic Plate	50	10	940312
C13	47 n	Polycarbonate	100	10	931129
C14	220 n	Polycarbonate	100	10	931131
C15	15 µ0	Tantalum	20	20	935601
C16	47 n	Polycarbonate	100	10	931129
C17	10 n	Polycarbonate	400	10	931136
C18	10 n	Ceramic	50	10	940315
C19	6 µ8	Tantalum Bead	35	20	923573
C20	10 n	Ceramic	50	10	940315
C21	15 µ	Tantalum Bead	25	20	922516
C22	10 n	Ceramic Disc	50	10	940315
C23	10 n	Ceramic Disc	50	10	940315
C24	10 n	Ceramic Disc	50	10	940315
C25	10 n	Ceramic Disc	50	10	940315

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C26	10 µ	Tantalum Bead	35	20	921256
C27	10 n	Ceramic Plate	50	10	940315
C28	10 n	Ceramic Plate	50	10	940315
C29	10 n	Ceramic Plate	50	10	940315
C30	4 n7	Ceramic Plate	50	10	940314
C31	15 µ	Tantalum Bead	25	20	922516
C32	10 n	Ceramic Plate	50	10	940315
C33	22n	Polycarbonate	400	10	931137
C34	10 n	Ceramic Plate	50	10	940315
C35	470 n	Polycarbonate	100	10	931132
C36	10n	Ceramic Plate	50	10	940315
C37	10n	Ceramic Plate	50	10	940315
	Diodes				
D1 - D5		Silicon 1N4149			914898
D6		Schottky diode ZC2811H			941092
D7 - D15		Silicon 1N4149			914898
	Transistors				
TR1	BC109				923234
TR2	J175				933405
TR3	2N2222				923217
TR4	J110				943016
TR5	J110				943016
TR6	J110				943016
TR7	J110				943016
TR8	J110				943016
TR9	J175				933405
	Integrated Circuits				
ML1		Dual 2-input NAND Buffer 40107			931052
ML2		Dual 2-input NAND Buffer 40107			931052
ML3		Quad analogue switch 4066			930148
ML4		Quad Operational Amplifier 224			938978
ML5		Quad OPerational Amplifier 224			938978
ML6		Transistor Array 3046			938975
ML7		Quad Operational Amplifier 224			938978
ML8		Transistor Array 3046			938975
ML9		Quad D-type latch 4042			930861
ML10		Dual D-type flip-flop 4013			926860

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML11		Dual D-type flip-flop 4013			926860
ML12		Analogue Switch, 201			943619
ML13		Analogue Switch, 201			943619
ML14		Quad level translater 40109			931054
ML15		Quad D-type latch 4042			930861
ML16		Quad Level Translator 40109			931054
ML17		Quad D-type Latch 4042			930861

Miscellaneous

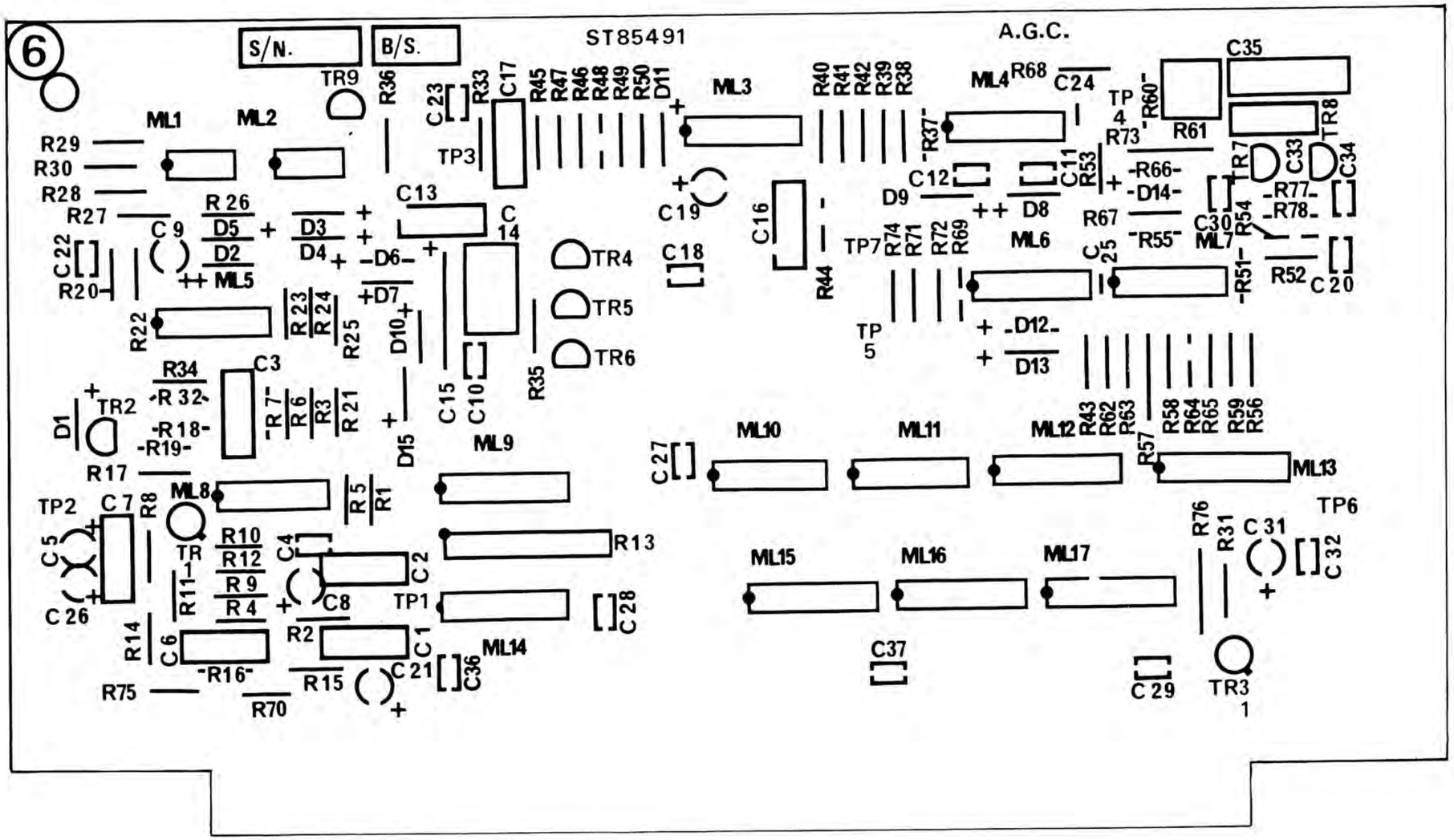
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		Test point			936148
		Screening plate			BA81974
		Board Stiffener			BD79561
		Captive Screw M3 x 10 mm			AD 81976



RACAL

TH 2449/3	DC85491
4	

Circuit: FAR AGC Card Fig.14.1



RACAL

TH 2449	DC 85490
2	

Layout: A.G.C. Card Fig 14·2

CHAPTER 15

DEMODULATOR CARD

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At end of Chapter

CHAPTER 15

DEMODULATOR CARD

INTRODUCTION

1. The demodulator card contains the 1.4 MHz BFO circuit, three demodulator circuits, two audio amplifier stages and a video output amplifier. The circuit diagram is contained on two sheets; sheet 1 (fig 15.1) covers the BFO circuitry, whilst the remaining circuitry is given in Sheet 2 (fig 15.2).

CIRCUIT DESCRIPTION

1.4 MHz BFO (fig 15.1)

2. A 2.8 MHz VCO (D5, G1) is connected into a phase-locked loop circuit comprising a programmable divider ML15, ML8a, a phase sensitive detector ML9a, ML9b, and a loop filter ML7. The division ratio of the programmable divider, and hence the VCO frequency, is controlled by LS1 divice ML10, which is similar to that used on the synthesizer board (Chap 10).

3. ML10 (fig 15 (a)) is controlled by the processor card via the I/O bus and the positive-going strobe 2 signal at PL55 pin 55. It has three input modes, namely address, data and control, as given in table 1. The address mode is used to address one of eight internal 4-bit latches; of these six are used to set the BFO frequency, whilst the remaining two are used for demodulator selection (table 2).

Table 1 : ML10 Mode Control

Mode	I/O4	I/O3	I/O2	I/O1	I/O0	STROBE 2
ADDRESS	1	0	A2	A1	A0	
DATA	0	D3	D2	D1	D0	
CONTROL	1	1	CTL2	CTL1	STROBE	

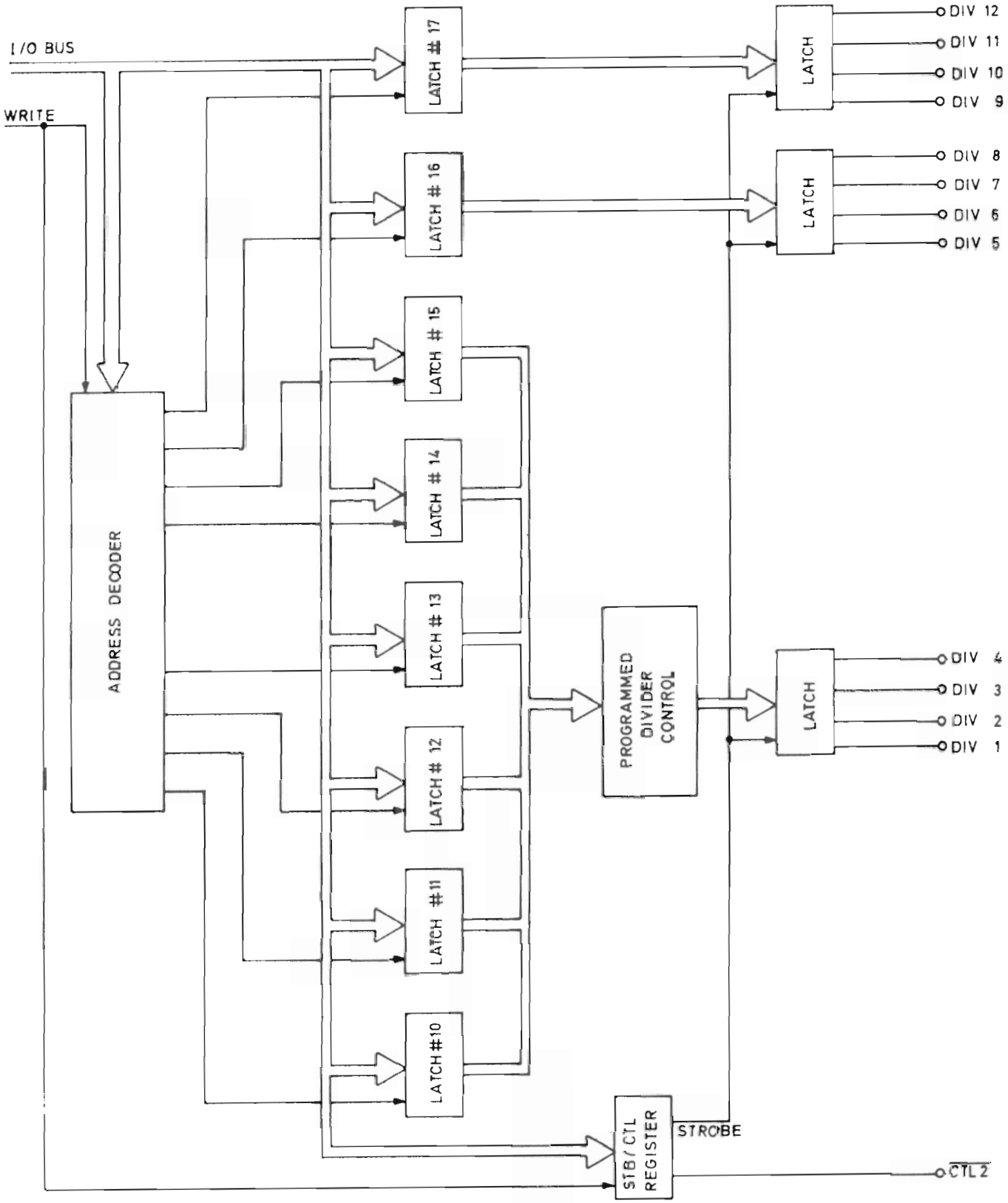


Fig. 15 (a) Functional Diagram: LSI Device ML10

RA 1794A
FD 72A

Table 2 : Latch Addresses

ADDRESS						FUNCTION
Hex	I/O4	I/O3	I/O2	I/O1	I/O0	
10	1	0	0	0	0	1 Hz Data
11	1	0	0	0	1	10 Hz Data — BFO
11	1	0	0	1	0	100 Hz Data — Frequency
13	1	0	0	1	1	1 KHz Data — Setting
14	1	0	1	0	0	10 KHz Data — Data
15	1	0	1	0	1	100 KHz Data
16	1	0	1	1	0	Demodulator 1 Select
17	1	0	1	1	1	Demodulator 2 Select

4. The control mode is used to reset the device (via the $\overline{CT2}$ output) and/or to produce an internal data output strobe. To reset the device, hexadecimal 1C (11100) is applied to the I/O bus; this is loaded into ML10 on the positive-going transition of the strobe 2 pulse, the $\overline{CT2}$ output is set to a '0', and this is used to reset the device (the $\overline{CTL1}$ output is not used). The internal strobe pulse is produced when hexadecimal 19 (11001) is applied to the I/O bus (together with strobe 2) and is used to enable the output latches.

5. The demodulator selection details are given in table 3. This shows that the divide-by-two BFO output stage ML8b is held in the set condition (DIV8 output at '1') for all modes except SSB/CW.

Table 3 : Demodulator Selection

MODE	ADDRESS 17 (DEM2)				ADDRESS 16 (DEM1)	
	I/O3	I/O2	I/O1	I/O0	I/O3	I/O2
	DIV12	DIV11	DIV10	DIV9	DIV8	DIV7
8 KHz FM	1	0	0	1	1	0
15 KHz FM	1	0	1	0	1	0
30 KHz FM	1	0	1	1	1	0
300 KHz FM	0	1	0	0	1	0
AM	1	1	1	0	1	1
CW/SSB	1	1	0	1	0	0
MUTE	1	1	1	1	1	0

ML10 Clock

6. A 1 MHz clock signal for ML10 is derived from the 20 MHz reference input at PL55 pin 27. The output from shaper stage TR1 is applied to decade divider ML14, the resulting 2 MHz output is applied via shaper TR2 to D-type flip-flop ML13a, and the resulting 1 MHz signal at the Q output is applied to the clock input of ML10. The 2 MHz output signal from ML14 is also applied to the processor card where it is used to derive the CPU clock signal.

7. A 200 KHz reference signal is produced by ML10, derived from the applied 1 MHz clock signal. This 200 KHz reference signal is applied to the phase sensitive detector (para 11).

Programmed Divider

8. The programmed divider comprises 4-bit binary counter ML15 together with D-type flip-flop ML8a. With the clear ($\overline{C}$) and enable (PE,TE) inputs of ML15 permanently at '1', the counter counts up from the programmed starting point until a count of 15 is reached. At this point, a positive-going carry-out ($\underline{CO}$) pulse is produced which is clocked through ML8a to produce the next $\underline{LOAD}$ pulse, and the binary number present at the P1 to P4 input pins is loaded in to determine the starting point of the next count sequence.

9. For a fixed BFO frequency of 1.4 MHz, the divider is programmed to start counting at binary 3 i.e. 0011 is present at the P4 to P1 input pins. The timing diagram given in fig 15 (b) shows that this situation gives a division ratio of 14:1, i.e. one CO pulse is produced for every 14 clock pulses. Under phase-locked conditions therefore, with a frequency of 200 KHz at the clock input of ML9b, the output signal from G3 must be equal to 200 KHz x 14 which is 2.8 MHz exactly. For BFO frequencies higher or lower than 1.4 MHz, the programmed starting point for ML15 is continually changing although the mean frequency at the clock input of ML9b (under phase-locked conditions) is still 200 KHz.

10. The frequency range of the BFO is 1.4 MHz plus or minus 7.79 KHz i.e. 1.39221 KHz to 1.40779 KHz in 10 Hz steps, and a negative offset of up to 9.99 KHz may also be introduced (to cater for the SSB condition using a symmetrical filter).

Phase Sensitive Detector

11. The phase sensitive detector uses a dual D-type flip-flop ML9a, ML9b, to compare the phase of the 200 KHz output signal from ML8a with the phase of the 200 kHz reference signal from ML10. Any difference in phase results in an output signal at the $\underline{Q}$ pin of ML9a which is used to drive the 2.8 MHz VCO and so eliminate the phase difference.

BFO Loop Filter

12. Operational amplifier ML7 is connected as a differential integrator. Potential divider R48, R49 sets the level at the non-inverting input to approximately +7V whilst the mark-to-space ratio of the $\overline{Q}$ output waveform from ML9a for the in-lock condition produces an average level of +7V at the inverting input of ML7.

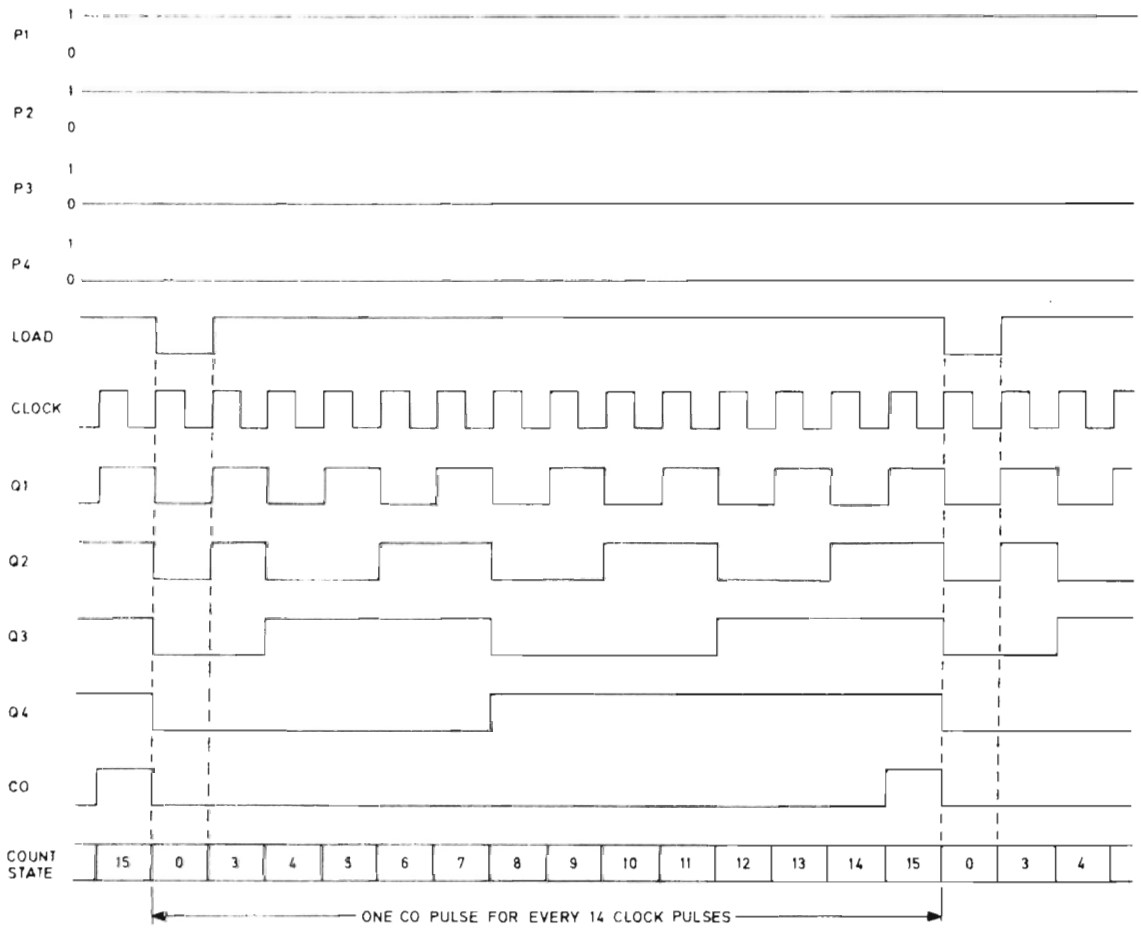


Fig.15(b) Timing Diagram: Divider ML15

2.8 MHz VCO

13. NOR gate G1 is connected as a voltage controlled oscillator. The input tuned circuit is formed by varactor diode D5, C59, L8 and C63, and the positive feedback path is via R67. G2 is connected as an operational amplifier (to ensure that the output waveform swings between OV and the supply rail), whilst G3 acts as a buffer. The potential divider formed by R57 and R58 provides a sample of the varactor drive voltage which is routed to the processor card for monitoring purposes.

Demodulator Selection (fig 15.2)

14. The 1.4 MHz IF signal at PL55 pin 53 is coupled by C11 to a wideband FM detector (ML1), by C12 to a medium/narrow band FM detector (ML4), and by C10 to an AM/SSB/CW detector ML5. The output signals from the three detector stages are coupled by capacitors C37, C38 and C39 to 1-of-8 analogue multiplexer ML3 which is controlled by the DIV9, DIV10 and DIV11 outputs from ML10; these outputs, in turn, are dependent on the selected mode and bandwidth (table 3).

Widband FM

15. For wideband FM, the DIV12 output from ML10 is at '0', and this removes the mute condition from the wideband FM detector stage ML1. At the same time, binary 4 is applied to the A, B and C select inputs of ML3 (DIV11 at '1'), and the audio output signal from ML1 is routed via C37, R35 and ML3 to amplifier stage ML2c.

16. ML1 consists of a 3-stage limiting IF amplifer, a quadrature detector and an AF pre-amplifier. It also provides an AFC output and has a muting capability.

Medium/Narrow Band FM

17. For the FM mode and a bandwidth of 30 kHz, 15 KHz or 8 KHz (nominal), binary 1, 2 or 3 is applied to the A, B and C select inputs of ML3 to select the audio output signal from ML4 (a similar device to ML1) via voltage-follower buffer stage ML2a, C38 and level compensating resistor R36, R37 or R38. The '0' at the DIV11 line is also applied to ML4 to remove the muting condition. A sample of the AFC output voltage from pin 7 of ML4 is taken from potential divider R23, R25 and is applied to the processor card where it is used for test purposes.

CW and SSB

18. For these two modes, the 1.4 MHz BFO signal from ML8b (fig 15.1) is applied to the carrier input of ML5, and the 1.4 MHz IF signal is applied to the signal input. Binary 6 is applied to the A, B and C select inputs of ML3, and the audio output from pin 6 of ML5 is routed via voltage-follower buffer stage ML2b, C39 and level compensating resistor R40.

AM

19. For the AM mode, the 1.4 MHz BFO signal is replaced with a limited 1.4 MHz carrier signal, taken from ML4 and applied to ML5 via emitter-follower stage TR4 and FET switch TR3. Binary 5 is applied to the A, B and C select inputs of ML3, and the audio output from ML5 is routed via ML2b, C39 and R39.

Audio Amplifier Stages

20. The audio output signal from pin 3 of ML3 is applied via amplifier stage ML2c and a 150 KHz low-pass active filter ML2d to a pair of audio amplifier stages, ML11a and ML11b. ML11a provides a 1 mW into 600 ohms balanced audio line output (output level preset by R51), whilst ML11b provides an audio output for an external 8 ohm loudspeaker (maximum 200 mW) and a 600 ohm unbalanced output (maximum 1 mW) for externally connected headphones. The audio level applied to ML11b is set by the front panel VOLUME control.

21. ML12 and TR5 form a wideband audio amplifier to provide a video output (0.35 volt r.m.s. into 75 ohms). ML16 and D6 form an audio peak detector for audio metering purposes.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		DEMODULATOR CARD (ST 80499)			
	Resistors				
R1	100	Metal Oxide		2	910388
R2	1 k	Metal Oxide		2	913489
R3	1 k5	Metal Oxide		2	911166
R4	1 k5	Metal Oxide		2	911166
R5	1 k	Metal Oxide		2	913489
R6	1 k	Metal Oxide		2	913489
R7	100	Metal Oxide		2	910388
R8	220	Metal Oxide	0.5W	2	909549
R9	1 k	Metal Oxide		2	913489
R10	15 k	Metal Oxide		2	920645
R11	6 k8	Metal Oxide		2	910112
R12	68	Metal Oxide		2	916476
R13	390	Metal Oxide		2	916331
R14	3 k3	Metal Oxide		2	910111
R15	10	Metal Oxide		2	920736
R16	390	Metal Oxide		2	916331
R17	1 k	Metal Oxide		2	913489
R18	390	Metal Oxide		2	916331
R19	3 k2	Metal Oxide		2	910111
R20	3 k3	Metal Oxide		2	910111
R21	3 k9	Metal Oxide		2	915074
R22	68	Metal Oxide		2	916476
R23	15 k	Metal Oxide		2	920645
R24	1k	Metal Oxide		2	913489
R25	47 k	Metal Oxide		2	913496
R26	4 k7	Metal Oxide		2	913490
R27	2 k2	Metal Oxide		2	916546
R28	3 k3	Metal Oxide		2	910111
R29	8 k2	Metal Oxide		2	918202
R30	68 k	Metal Oxide		2	916478
R31	8 k2	Metal Oxide		2	918202
R32	68 k	Metal Oxide		2	916478
R33	4 k7	Metal Oxide		2	913490
R34	4 k7	Metal Oxide		2	913490
R35	24 k	Metal Film	0.25	2	920769

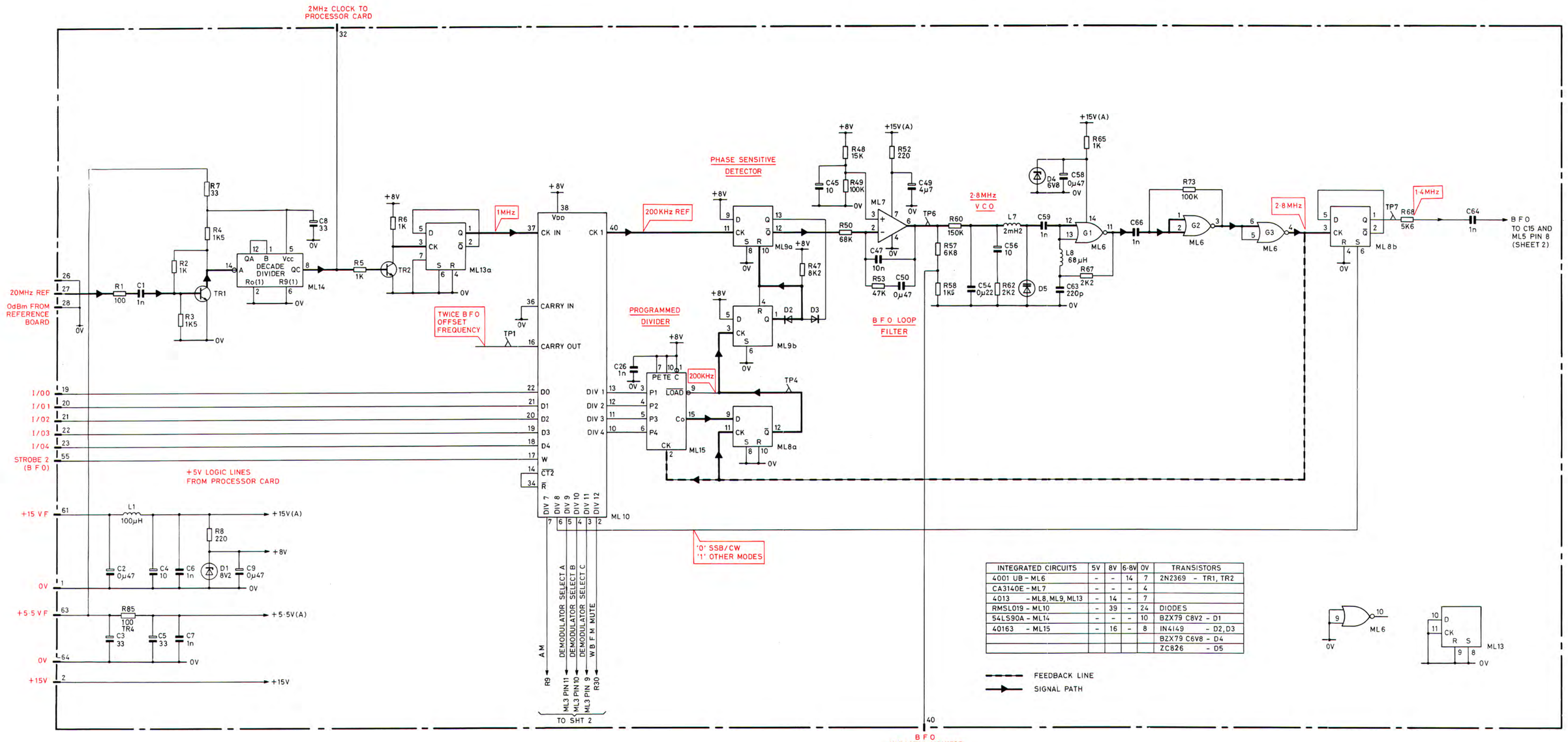
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R36	24 k	Metal Film	0.25	2	920769
R37	5 k6	Metal Oxide		2	918128
R38	100	Metal Film	0.25	2	910388
R39	220	Metal Oxide		2	910390
R40	15 k	Metal Oxide		2	920645
R41	4 k7	Metal Oxide		2	913490
R42	10 k	Metal Oxide		2	914042
R43	22 k	Metal Oxide		2	913493
R44	10 k	Metal Oxide		2	914042
R45	1 k	Metal Oxide		2	913489
R46	1 k	Metal Oxide		2	913489
R47	8 k2	Metal Oxide		2	918202
R48	15 k	Metal Oxide		2	920645
R49	100 k	Metal Oxide		2	915190
R50	68 k	Metal Oxide		2	916478
R51	10 k	Metal Oxide		2	928362
R52	220	Metal Oxide		2	910390
R53	47 k	Metal Oxide		2	913496
R54	6 k8	Metal Oxide		2	910112
R55	2 k2	Metal Oxide		2	916546
R56	2 k2	Metal Oxide		2	916546
R57	6 k8	Metal Oxide		2	910112
R58	1 k2	Metal Oxide		2	911179
R59	100 k	Metal Oxide		2	915190
R60	150 k	Metal Oxide		2	917954
R61	4 k7	Metal Oxide		2	913490
R62	2 k3	Metal Oxide		2	916546
R63	39	Metal Oxide		2	917062
R64	100 k	Metal Oxide		2	915190
R65	1 k	Metal Oxide		2	913489
R66	10	Metal Oxide		2	920736
R67	2 k2	Metal Oxide		2	916546
R68	5 k6	Metal Oxide		2	918128
R69	33	Metal Oxide		2	917060
R70	39 k	Metal Oxide		2	900993
R71	18 k	Metal Oxide		2	900994
R72	33 k	Metal Oxide		2	913495
R73	100 k	Metal Oxide		2	915190
R74	220 k	Metal Oxide		2	921771
R75	330	Metal Oxide		2	910200

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R76	560	Metal Oxide		2	917061
R77	82	Metal Oxide		2	917057
R78	100 k	Metal Oxide		2	915190
R79	10 k	Metal Oxide		2	914042
R80	100 k	Metal Oxide		2	915190
R81	6 k8	Metal Oxide		2	910112
	Capacitors		V		
C1	1 n	Ceramic Disc	50	20	915243
C2	0 µ47	Tantalum Bead	35	20	939267
C3	0 µ47	Tantalum Bead	35	20	939267
C4	10	Tantalum Bead	35	20	921256
C5	0 µ47	Tantalum Bead	35	20	939267
C6	1 n	Ceramic Disc	500	20	915243
C7	1 n	Ceramic Disc	500	20	915243
C8	0 µ47	Tantalum Bead	35	20	939267
C10	22 n	Ceramic Disc	25	+50 -25	926921
C11	22 n	Ceramic Disc	25	+50 -25	926921
C12	22 n	Ceramic Disc	25	+50 -25	926921
C13	10 n	Ceramic Disc	250	+40 -20	916187
C14	22 n	Ceramic Disc	25	+50 -25	926921
C15	22 n	Ceramic Disc	25	+50 -25	926921
C16	0 µ22	Ceramic Disc	100	20	931161
C17	10 n	Ceramic Disc	250	+40 -20	916187
C18	0 µ47	Tantalum Bead	35	20	939267
C19	22 n	Ceramic Disc	25	+50 -25	926921
C20	22 n	Ceramic Disc	25	+50 -25	926921
C21	10	Tantalum Bead	35	20	921256
C22	10 n	Ceramic Disc	250	+40 -20	916187
C23	10	Tantalum Bead	35	20	921256
C24	10 n	Ceramic Disc	250	+40 -20	916187
C25	0 µ22	Polyester	100	20	931161
C26	1n	Ceramic Disc	500	20	915243
C27	150 p	Silver Mica	100	2	931604
C28	1 n	Silver Mica	100	2	934054
C29	0 µ47	Tantalum Bead	35	20	939267
C30	220 p	Ceramic Disc	500	10	931148

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C31	10	Tantalum Bead	35	20	921256
C32	10	Tantalum Bead	35	20	921256
C33	10	Tantalum Bead	35	20	921256
C34	10	Tantalum Bead	35	20	921256
C35	220 p	Silver Mica	100	2	938998
C36	10 n	Ceramic Disc	250	+40 -20	916187
C37	0 µ22	Polyester	100	20	931161
C38	0 µ22	Polyester	100	20	931161
C39	2 µ2	Tantalum Bead	35	20	923572
C40	1 µ0	Tantalum Bead	35	20	923571
C41	0 µ47	Tantalum Bead	35	20	939267
C42	270 p	Silver Mica	100	2	938998
C43	270 p	Silver Mica	100	2	938998
C44	0 µ47	Tantalum Bead	35	20	939267
C45	10	Tantalum Bead	35	20	921256
C46	10	Tantalum Bead	35	20	921256
C47	10 n	Ceramic Disc	250	+40 -20	916187
C48	2 µ2	Tantalum Bead	35	20	923572
C49	4 µ7	Tantalum Bead	35	20	914026
C50	0 µ47	Tantalum Bead	35	20	939267
C51	10	Tantalum Bead	35	20	921256
C52	10	Tantalum Bead	35	20	921256
C53	100	Electrolytic	25	+50 -10	921546
C54	0 µ22	Polyester	100	20	931161
C55	2 µ2	Tantalum Bead	35	20	923572
C56	10	Tantalum Bead	35	20	921256
C57	100	Electrolytic	25	+50 -10	921546
C58	0 µ47	Tantalum Bead	35	20	939267
C59	1 n	Monolithic Ceramic	50	10	940312
C60	10 n	Ceramic Disc	250	+40 -20	916187
C61	470	Electrolytic	40	+50 -10	941812
C62	220	Electrolytic	16	+50 -10	926273
C63	220 p	Silver Mica	100	2	940016
C64	1 n	Ceramic Disc	500	20	915243
C65	0 µ22	Polyester	100	20	931161
C66	1 n	Ceramic Disc	500	20	915243
C67	100	Electrolytic	25	+50 -10	921546
C68	1 µ0	Tantalum Bead	35	20	923571
C69	1 n	Ceramic Disc	500	20	915243
C70	220	Electrolytic	16	+50 -10	926273
C71	1 µ	Tantalum Bead	35	20	923571
C72	33 µ	Tantalum Bead	10	20	923567

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Inductors					
L1	100 µH	Choke		10	939161
L2	100 µH	Choke		10	939161
L3	330 µH	Choke		10	939163
L4	150 µH	Choke		10	939162
L5		Coil Assembly			AT81875
L6		Coil Assembly			AT81875
L7	2m2H	Choke		10	926284
L8	68 µH	Choke		10	940015
Transformers					
T1		Transformer Assembly			AT81877
Diodes					
D1		Zener, 8.2 V , 400 mW BZX79C8V2			923962
D2		Silicon 1N4149			923222
D3		Silicon 1N4149			923222
D4		Zener, 6.8 V, 400 mW BZX79C6V8			921750
D5		Varactor ZC826			924932
D6		Silicon 1N4149			923222
Transistors					
TR1		NPN Silicon 2N2369			939306
TR2		NPN Silicon 2N2369			939306
TR3		N - Channel FET 2N4392			914907
TR4		NPN Silicon BC109			923234
TR5		PNP Silicon BFX48			915231

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Integrated Circuits					
ML1		FM IF Stage CA 3189E			938977
ML2		Quad Operational Amplifier LM248N			938969
ML3		Single 8-channel Multiplexer 4051			930035
ML4		FM IF Stage CA3189E			938977
ML5		Balanced Mixer MC1596L			939261
ML6		Quad 2-input NOR gate 4001UB			939165
ML7		Operational Amplifier CA3140E			932204
ML8		Dual D-type flip-flop 4013			926860
ML9		Dual D-type flip-flop 4013			926860
ML10		LSI Control Device RMSL019/B			AD80763/B
ML11		Dual Audio Amplifier LM377			928536
ML12		Operational Amplifier CA3140E			932204
ML13		Dual D-type Flip-flop 4013			926860
ML14		Decade counter 54LS90J			938878
ML15		Binary Counter 40163			931059
ML16		Operational Amplifier CA3140E			932204
Miscellaneous					
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		40-pin DIL IC socket			933814
		Board stiffener			BD79561
		Captive Screw M3 x 10 mm			AD81976



INTEGRATED CIRCUITS	5V	8V	6·8V	0V	TRANSISTORS
4001 UB - ML6	-	-	14	7	2N2369 - TR1, TR2
CA3140E - ML7	-	-	-	4	
4013 - ML8, ML9, ML13	-	14	-	7	
RMSL019 - ML10	-	39	-	24	DIODES
54LS90A - ML14	-	-	-	10	BZX79 C8V2 - D1
40163 - ML15	-	16	-	8	IN4149 - D2, D3
					BZX79 C6V8 - D4
					ZC826 - D5

RACAL

TH2449	DC80499	15.1	TH2449	DC80499	15.1
1	7	1/2	1		2/2

Circuit: Demodulator Card (Sheet 1) Fig.15.1

INTEGRATED CIRCUITS	5V	8V	15V	OV	TRANSISTORS
CA3189E — ML1, ML4	—	—	—	14	2N 4392 — TR3
LM248N — ML2	—	—	4	11	BC 109 — TR4
4051 — ML3	—	16	—	8	BFX 48 — TR5
MC1596L — ML5	—	—	—	14	
LM377 — ML11					DIODES
CA3140E — ML12, ML16	—	—	—	4	IN4149 — D6

±10% AC SIGNAL LEVELS MEASURED WITH RF mV METER OR OSCILLOSCOPE

±10% DC LEVELS MEASURED WITH D V M

SIGNAL PATH (SHOWN FOR 8KHz FM DETECTOR SELECTED)

ML1 WIDEBAND F M DETECTOR

ML4 MEDIUM/NARROW BAND FM DETECTOR

ML5 A.M SYNCHRONOUS DETECTOR SSB/CW PRODUCT DETECTOR

ML3 DEMODULATOR SELECTOR SWITCH

150 KHz FILTER

AUDIO OUTPUT AMPLIFIER

WIDEBAND OUTPUT AMPLIFIER

AUDIO DETECTOR

FROM ML10 DIV 12 W B F M MUTE (SHT. 1)

LIMITED CARRIER

1·4 MHz I F FROM I F FILTER CARD

100 mV r.m.s.

FROM ML10 DIV 7 A M (SHT. 1)

'1' A M '0' OTHER MODES

B F O FROM C64 (SHT. 1)

B F O SIGNAL (INHIBITED FOR A M/F M)

'0' MEDIUM/NARROW BAND F M '1' OTHER MODES

110 mV r.m.s.

R51 SET LINE O/P LEVEL

BALANCED 600Ω

LINE O/P BAL.

LINE O/P BAL.

HEADPHONES

HEADPHONES (OV)

LOUDSPEAKER

LOUDSPEAKER (OV)

VIDEO O/P

AUDIO LEVEL

FROM ML10 DIV 9 / DIV 10 / DIV 11 FROM SHT.1

TUNE LINE

VOLUME (OV)

VOLUME POT

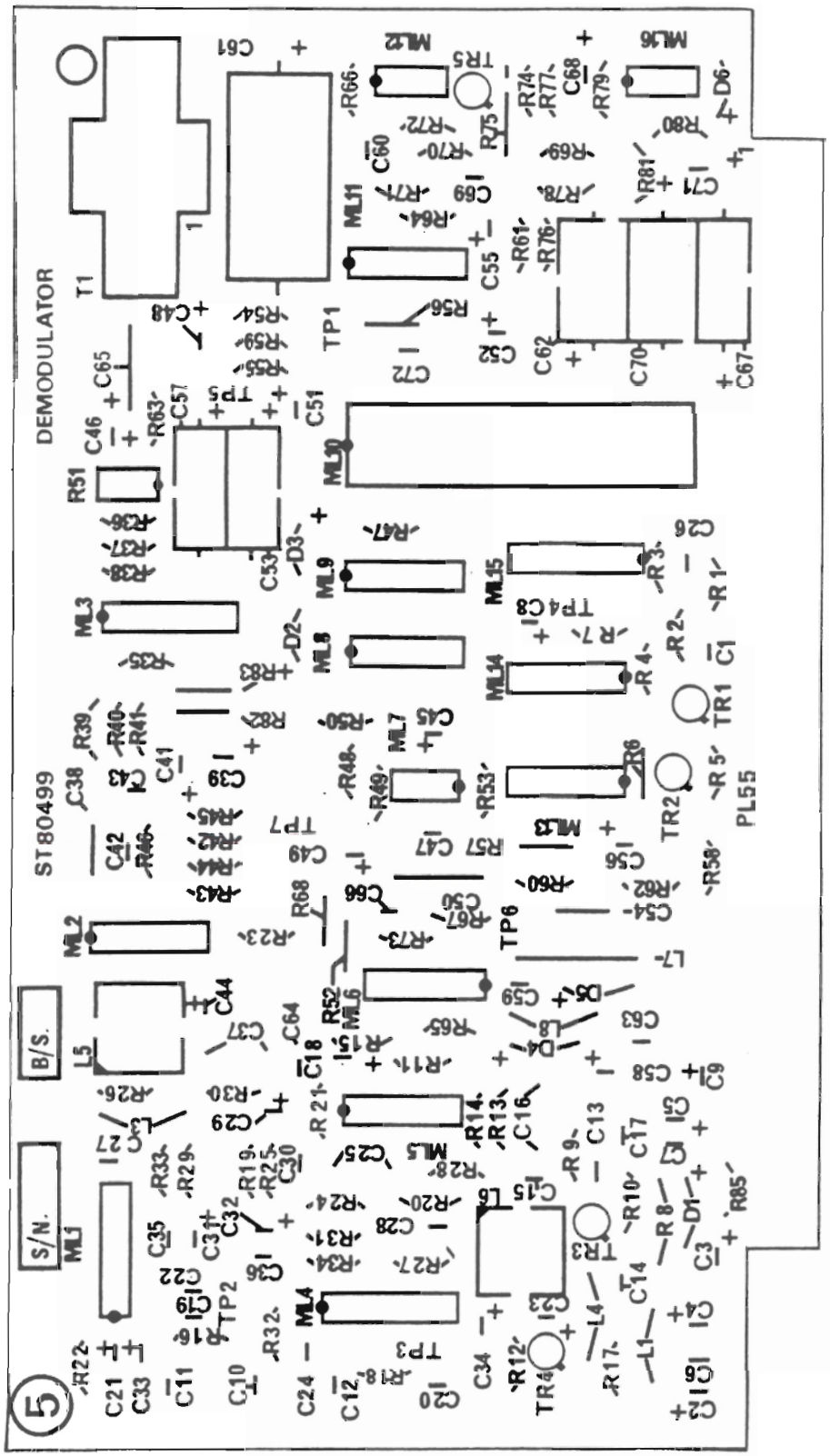
VOLUME WIPER

FRONT PANEL

RACAL

TH 2449	DC80499	15.2	H 2449	DC80499	15.2
1 2 3 4 5 6 7 8 9 1/2					2/2
10 11					

Circuit : Demodulator Card Fig.15.2 (Sheet 2)



DA80498/4

Layout: Demodulator Card Fig. 15.3

CHAPTER 16

SCORE INTERFACE CARD

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Tables

Illustrations

CHAPTER 16

SCORE INTERFACE CARD

Introduction

1. The SCORE (Serial Control Of Racal Equipment) interface is an optional internally mounted card which provides for extended or remote control of the receiver, using a control unit such as the Racal MA 1113, or another receiver. The SCORE control system is described in the following paragraphs.

SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc.) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with CCITT V10 and, over short distances, are compatible with RS232/CCITT V28.

4. The SCORE format for the words used by the RA 1794A (word numbers 0, 1, 2 and 4) is given in Table 1. Although word 0 may be sent as part of a control data sequence, it does not contain any control information and is used only for revertive data.

ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the forward control data does not contain change-of-function information, 'routine data' frames are sent in numerical sequence, and at a rate determined by the SCORE clock frequency. When a change-of-function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change-of-function is executed at the controlled receiver, the next frame to be sent will contain the data word carrying the change-of-function information. Thus the frames are sent out of numerical sequence and priority is given to those frames containing new data. This is achieved under software control where a flag is set each time a control setting is changed to indicate that the appropriate word requires transmission. The flag is reset when the data word is transmitted.

FRAME COMPARISON

6. Error detection is accomplished by the use of the frame comparison technique, which means that two identical frames must be received at the receiver before a change-of-function can occur.

Table 1: SCORE Data Format

	BIT NO.	BIT FUNCTION OR FORCED STATE	MONITOR (0)	FREQUENCY (1)	ANALOGUE (2)	VHF MODE (4)
PREAMBLE	0	0				
	1	1				
	2	1 SYNC				
	3	1 CODE				
	4	1				
	5	1				
	6	TRANSMIT				
	7	RECEIVE				
	8	CONTROL INHIBIT				
	9	RETURN MONITOR				
	10	ADDRESS	0	0	0	0
	11	EQUIPMENT	0	0	0	0
	12	1 DATA	0	1	0	0
	13	2 WORD	0	0	1	0
	14	4 IDENT	0	0	0	1
	15	8	0	0	0	0
DATA WORD	16	A	1	1	0	
	17	B USER	2	2 10 Hz	2 BFO	0 NOT
	18	C FUNCTION	4	4	4 x 10 Hz	0 USED
	19	D	8	8	8	0
	20	0	1	1	1	1 METERED
	21	COR	2	2 100 Hz	2 BFO	0 FUNCTION
	22	1 RECEIVER	4	4	4 x 100 Hz	0
	23	0 IDENT	8	8	8	0
	24	0	1	1	1 BFO	0
	25	0	2	2 1 kHz	2 x kHz	0 NOT
	26	0	4	4	4	0 USED
	27	0 NOT USED	8	8	BFO SIGN	SYMMETRICAL
	28	0	1	1	0	1 MODE
	29	0	2	2 10 kHz	1	2
	30	0	4	4	2	4
	31	0	8	8	4	0
	32	MUTE	1	1	8	1 COR
	33	FAULT	2	2 100 kHz	0 COR	2 CONTROL
	34	FC ERROR	4	4	16	0
	35	0	8	8	32	0
	36	RF METER	1	1	64	AGC DUMP
	37	0	2	2	128	1
	38	0 NOT	4	4 1 MHz	0	2 AGC
	39	0 USED	8	8	1	4
	40	1	1	1	2	1
	41	2	2	2 10 MHz	4 IF	2 BANDWIDTH
	42	4	4	4	8 GAIN	4
	43	0 METER READING	8	8	0	0
	44	8	1	1	16	W
	45	16	2	2 100 MHz	32	X USER
	46	32	4	4	64	Y FUNCTION
	47	64	8	8	128	Z

PREAMBLE

7. A 16-bit preamble is added to each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit-receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code, and a 4-bit data word identification code; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1's. The maximum number of consecutive '1's that occur in serial BCD data is four, e.g. BCD seven followed by BCD eight. This then makes five '1's a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of consecutive '1's. This is done to 'terminate' the sync. code and to prevent the generation of a false sync. code following a line break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state mutes the receiver and may also set an associated transmitter to the transmit condition. As mentioned in para. 8, these two bits must not consist of consecutive '1's. The coding of these bits is as follows:

Bit 7	Bit 6	Function
0	1	TRANSMIT
1	0	RECEIVE
1	1	NOT ALLOWED (fault)

Control Inhibit Bit

10. This bit of the preamble (bit 8) is normally used, as the name implies, to inhibit control of the receiver via the serial control data. Thus for as long as this bit is set in the control data frames sent to the receiver, further control information is ignored and the actual receiver settings are returned via the revertive data. Note however, that this bit cannot be set in control data frames generated by a receiver.

Return Monitor Bit

11. The return monitor bit is normally at '0' and is set to a '1' in control data frames sent to the receiver to cause continuous word 0 monitor frames to be returned via the revertive data. Note however, that this bit cannot be set in control data frames generated by a receiver.

Address Security Code

12. Bits 10 and 11 of the preamble are used in words 8 and 9 of the SCORE control system (equipment and operator addressing words respectively) to provide added security against incorrect addressing. These two bits are set to a '0' in all frames used by the RA 1794A.

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used for the data word identification code, in binary format, i.e. 0 to 15 (decimal) or 0 to F (hexadecimal).

DATA WORDS

14. As stated in para. 4, words 0, 1, 2 and 4 are used by the RA 1794A. These words are described in the following paragraphs which should be read in conjunction with Table 1. Certain words contain a number of 'forced zeros' to prevent the possible occurrence of five consecutive '1's which would otherwise be mistaken for a sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only. Although it may be transmitted as part of a forward control data sequence, it does not contain any control data. The word 0 data is thus produced by the receiver for transmission via the revertive data highway to the receiver control unit. Note that when one receiver is used to control another, the revertive word 0 data from the controlled receiver is not used or displayed by the control receiver.

User Functions

16. The first four bits of word 0 provide for the revertive user functions where up to four earth (0V) signals applied to the receiver are reproduced (via the revertive data) at the control unit. The four bits are labelled A, B, C and D, and correspond with the A, B, C and D connections at both the controlled receiver and the control unit.

Revertive Indications

17. Data bits 21, 22, 23, 32, 33 and 34 may all be used to convey status information from the receiver to a control unit, or to some other SCORE-compatible unit in a multi-equipment installation. This data may be used to control the illumination of various signal lamps, to sound an alarm, or, in the case of the receiver identification bits, for signal switching purposes.

Carrier Operated Relay (COR)

18. Bit 21 is used for the COR function and can be used to illuminate a CARRIER ON indicator.

Receiver Identification

19. Data bits 22 and 23 of the word 0 data are used to identify the type of receiver in use; for the RA 1794A, bit 22 is set to a '1' and bit 23 is set to '0'. The information conveyed via these data bits could be used, for example, for signal switching purposes in a multiple-receiver direction finding system.

Mute

20. Bit 32 is set to a '1' when a mute signal is applied to the receiver, and this may be conveyed to a control unit via the revertive data to illuminate a MUTE indicator.

Fault Bit

21. Data bit 33 is set to a '1' following the detection of a fault condition within the receiver; this may be used to illuminate a FAULT indicator at a control unit.

Frame Comparison Error Bit

22. Data bit 34 is the frame comparison error bit and is normally at '0'; it goes to a '1' when three consecutive frame comparison errors are detected at the receiver (para. 38), and this also may be used to illuminate a FAULT indicator at a control unit.

RF Metering

23. Data bit 36 is set to a '1' to select RF metering, and the RF meter reading data is conveyed, in 7-bit digital format, via data bits 40 to 42 and 44 to 47 (bit 43 is a forced zero).

WORD 1 - FREQUENCY

24. All 32 bits of this word are used to convey frequency setting information, in BCD format, as indicated in Table 1.

WORD 2 - ANALOGUE

25. Word 2 contains the analogue functions, BFO, COR threshold and IF gain. The maximum BFO offset frequency is restricted to the range plus and minus 7.79 kHz i.e. three data bits (24, 25 and 26) are used for the kHz digit (giving a maximum figure of 7), and to prevent the generation of a spurious sync. code, data bit 23 must not be set to a '1' (thus giving a maximum figure of 7 for the 100 Hz digit). Data bit 27 is the BFO sign bit and is set to a '1' for negative BFO offset frequencies, to a '0' for positive BFO offset frequencies.

26. The COR (carrier operated relay) threshold data is conveyed between control unit and receiver via data bits 29 to 32 and 34 to 37, whilst the IF gain control data is conveyed via data bits 39 to 42 and 44 to 47. Data bits 28, 33, 38 and 43 are forced zeros (para. 14).

WORD 4 - VHF MODE

27. This word is used for metered function, mode, COR control, AGC and bandwidth selection, and for the forward user functions.

Metered Function

28. Data bit 20 is set to a '1' to select receive signal level metering.

Mode

29. Bits 27 to 30 are concerned with mode selection. The state of bit 27 determines whether a symmetrical mode or a sideband mode is selected, as shown in the following table.

BCD Coding of Bits 28 to 30	Bit 27 State	Mode Selected	
0	0	USB	SIDEBAND
1	0	LSB	
2	1	CW	SYMMETRICAL
1	1	AM	
5	1	FM	

COR Control

30. The coding of the COR control bits (32 and 33) is as follows:

Bit 33	Bit 32	Function
0	0	COR OFF
0	1	COR ON
1	0	COR ON with Delay

AGC

31. Bit 36 is used for AGC dump; when set to a '1' it causes a rapid decay of the AGC voltage level so that the level may be re-established for the signal being received. The coding of bits 37, 38 and 39 is given below.

BCD Code	Function
0	Short with Manual threshold
1	Medium with Manual threshold
2	Long with Manual threshold
3	Manual Only
4	Short
5	Medium
6	Long
7	Not Allowed

Bandwidth

32. The coding of bits 40 to 42 is given below. The actual filters fitted are dependent upon the particular receiver options. The filter numbers given correspond with those on the IF filter card.

BCD Code	Filter No.
0	1 (Narrowest Bandwidth)
1	2
2	3
3	4
4	5
5	6
6	7
7	Not Used

User Function

33. The last four bits of word 4 provide for the forward user function where up to four earth (0V) signals applied to the receiver control unit are reproduced at the receiver. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the control unit and receiver respectively.

REVERTIVE DATA

34. The format of the revertive data is the same as for the control data. Frame comparison however, does not take place, and the revertive data is generally sent in single frames.

35. Provided that the control inhibit and return monitor bits of the forward data preamble are not set to a '1', and that no errors occur in the control data, then the form of the revertive data is given by the following example.

Forward Data	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 1 FREQ	WORD 2 BFO	WORD 2 BFO	WORD 4 MODE
Resulting Revertive Data		WORD 0 MON	WORD 0 MON	WORD 0 MON	WORD 1 FREQ	WORD 0 MON	WORD 2 BFO

36. In this example, the forward data consists of two word 0 frames, two word 1 frames, two word 2 frames and the first of two word 4 frames. Since two frames have to be sent and compared before any action can take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit frames (ignore for the moment the first revertive data word 0). The two forward data word 0 frames are compared; since no bit errors are present, the two frames are identical and a word 0 frame is returned. The next frame comparison however, is between a word 0 and a word 1. The comparison is therefore unsuccessful, and, although an error does not exist, it is arranged to send back a word 0 monitor frame. Two word 1 frames are now compared, and result in a revertive word 1 frame. The next comparison is between a word 1 frame and a word 2 frame, which results in a revertive word 0 frame, two word 2 frames result in a revertive word 2 frame, and so on. The content of the first (blank) revertive data frame is dependent on the previously sent data, whilst the next frame (the first word 0 frame in this example) must be a word 0 frame due to a comparison between two dissimilar frames.

Frame Comparison Error

37. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example:

Forward Data	WORD 1 FREQ	WORD 1 FREQ	WORD 2 BFO	WORD 2 BFO	WORD 4 MODE	WORD 4 MODE	WORD 0 MON
	ERROR						
Revertive Data			WORD 1 FREQ	WORD 0 MON	WORD 0 MON	WORD 0 MON	WORD 4 MODE
	MONITOR FRAME RESULTING FROM ERROR						BIT 34 SET

38. In this example the forward data consists of two word 1 frames, two word 2 frames, two word 4 frames and the first of a pair of word 0 frames. The two frequency word frames result in a revertive frequency word frame and the next two frames (frequency and BFO) result in a monitor word 0 frame. The two BFO word frames are compared, and this time, due to an error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (BFO and mode) being dissimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons; a frame comparison error signal is generated and this is conveyed by bit 34 of the revertive word 0 frame.

Control Inhibit

39. If the control inhibit bit (bit 8 of the preamble) in a forward control data frame is set to a '1', and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1', then the revertive data frames are sent in pairs and in numerical sequence and convey the actual receiver setting data.

Return Monitor

40. If the return monitor bit (bit 9 of the preamble) in a series of forward control data frames is set to a '1', then the revertive data consists of a series of continuous monitor frames.

CLOCK CIRCUITS

41. These provide the timing signals required by the various parts of the system. The basic data rate clock signal may be generated either by an external unit, such as a modem, or may be provided by an internal clock generator (7.8 kHz derived from the CPU clock).

SIGNAL-TO-LINE REQUIREMENTS

42. The signal-to-line requirements for the serial data and clock signals comply with CCITT Recommendation V10 (compatible with EIA RS 423). This specifies the electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications. It is intended for use at the lower signalling rates only and its use should be avoided in the following cases:

(1) Where the interconnecting cable is too long for proper unbalanced circuit operation.

(2) Where extraneous noise sources make unbalanced circuit operation impossible.

(3) Where it is necessary to minimise interference with other signals.

43. The main V10 characteristics (as far as the RA 1794A is concerned) are summarised below:

(1) Binary 0 for data circuits, or ON for control and timing circuits, is defined as a voltage more positive than +0.3 V.

(2) Binary 1 for data circuits, or OFF for control and timing circuits, is defined as a voltage more negative than -0.3 V.

(3) Maximum Data Rate: 9.6 Kbit/s

(4) Maximum Line Length: 1000 m at data rates up to 10 Kbit/s

(5) Open circuit Driver Voltage: from ± 4 V to ± 6 V

(6) Loaded Driver Voltage: equal to or greater than 0.9 times the open circuit driver voltage.

(7) Driver Output Load - Power Off: 100 microamperes (+0.25 V to -0.25 V)

(8) Driver Short-Circuit Current: ±150 mA

(9) Driver Slew Rate: Resistor controlled

(10) Receiver Input Resistance: Equal to or greater than 4 Kilohms

(11) Receiver Threshold: -0.2 V to +0.2 V

(12) Maximum Receiver Input Voltage: ±12 V.

SCORE INTERFACE CARD

44. The SCORE interface card handles the transmission and reception of SCORE data either between a pair of RA 1794A receivers, or between a receiver and an associated control unit. For a receiver set to LOCAL control i.e. REMOTE not selected, control is via the front panel controls only, and SCORE data (words 0, 1, 2 and 4), containing the front panel setting information, together with the SCORE clock signal, are available at the front panel CONTROL connector. For a receiver set to REMOTE control, i.e. REMOTE selected at the front panel, the remaining front panel controls are disabled and the receiver is under the control of either an external control unit or another receiver (set to local).

CIRCUIT DESCRIPTION (fig. 16.1)

SCORE INTERRUPT

45. The software SCORE handling routine is initiated following the receipt by the processor card of an interrupt signal from NAND gate G1 (TP8). This interrupt signal is derived from one of two sources dependent on whether the receiver is set to local or remote control. For local control, a '0' is latched at the Q6 output of ML11; this forces a '1' at the output of G2 (to enable G1), and is inverted by G4 to enable G3 for a logic '0' interrupt signal from the parallel-to-serial converter stage ML7 (para. 55).

46. For remote control, a '1' is latched at the Q6 output of ML11; this is inverted by G4 to force a '1' at the output of G3 (to enable G1), and also enables G2 for a logic '0' output from SCORE interrupt latch ML6a (para. 53).

CLOCK DETECTOR

47. The clock detector circuit comprises open-collector NAND gate G5, Schmitt trigger NAND gates G6 to G9 and two inverting buffers ML10b, ML10e. Its purpose is to detect the presence or absence of an externally applied clock signal (higher than approximately 300 Hz) and to allow the use of an internal SCORE clock signal only when the external clock signal is not present.

48. An externally applied SCORE clock signal (at edge connector pin 35) is routed via V10 line receiver ML16b to one input of G5 via inverter ML10b, and to the remaining input of G5 via delay components R5, C1. The resulting negative-going pulses at the output of G5 keep C2 discharged below the switching threshold of G6, producing a '1' at the output, which is applied to:

(1) G7, to enable the external SCORE clock signal from ML16b.

(2) Inverter ML10e, to force a '1' at the output of G8 and so enable G9 for the external SCORE clock signal from G7.

49. If the external SCORE clock is removed (or falls below approximately 300 Hz), capacitor C2 is allowed to charge via R6, to the point where G6 changes state. The resulting '0' output is inverted by ML10e to enable G8 for the internal SCORE clock signal at edge connector pin 44; it also forces a '1' at the output of G7 to enable G9 for the output signal from G8.

SYNC CODE DETECTOR

50. For a receiver set to remote control, the SCORE control data, at edge connector pin 36, is applied via line receiver ML16a to a serial-to-parallel converter stage ML17 (para. 54) and via inverting buffer ML10a to the DA input of a dual 4-stage shift register ML4. The Q3A output from one section of the register is applied to the reset (RB) of the other section, where the data input (DB) is connected to +5 V (logic '1'). Data is shifted into these registers on the positive-going transition of the SCORE clock signal from G9.

51. When an inverted sync. code is received, i.e. 1-0-0-0-0-0-X-X, it takes three clock pulses for the first '1' to reach the Q3A output; this holds the B section of the register in the reset state for the duration of the next clock pulse, and a further four clock pulses are required before the Q4B output changes to a '1' (Table 2). Thus the Q4B output of ML4 can only change to a '1' following the occurrence of five consecutive zeros at the DA input. This circuit does not detect the state of the last two bits of the received sync. code but this is subsequently checked by the system software. The '1' at the Q4B output of ML4 is applied to the clock input of the strobe pulse generator ML6b via glitch suppression components R7, C3.

STROBE PULSE GENERATOR

52. The strobe pulse generator comprises D-type flip flop ML6b. When clocked by the output from the sync. code detector, the '1' at the D input is transferred to the Q output, the '0' at the $\overline{Q}$ output is applied to G10, and ML6b is thus reset on the next negative-going transition of the SCORE clock waveform from G9. The positive-going strobe pulse is applied to:

(1) One input of G12, which forms part of the output counter synchronisation circuit (para. 62).

(2) The strobe input of 8-bit shift and store register ML17 to load the internal storage latches with the first eight bits (the sync. code) of the received frame (para. 54).

Table 2 Sync. Code Detector

SHIFT REGISTER STATES	1	2	3	4	5	6	7	8
Q1A	1	0	0	0	0	0	X	X
Q2A	X	1	0	0	0	0	0	X
Q3A	X	X	1	0	0	0	0	0
Q4A	X	X	0	1	0	0	0	0
Q1B	X	X	0	0	1	1	1	1
Q2B	X	X	0	0	0	1	1	1
Q3B	X	X	0	0	0	0	1	1
Q4B	X	X	0	0	0	0	0	1

X = 0 or 1

(3) The reset input of an 8-bit BCD up-counter ML5a. This counter produces a positive-going pulse at the Q4 output for every eight SCORE clock cycles following reset, and these pulses are applied to the set input of ML6b to produce the strobe pulses for the remaining five bytes of the received data frame.

53. At the negative-going edge of each strobe pulse, the $\overline{Q}$ output of ML6b returns to a '1', and this clocks the SCORE interrupt latch ML6a. Provided remote interrupts are enabled ('1' at the Q6 output of ML11), the resulting '0' at the $\overline{Q}$ output of ML6a is routed via G2 and G1 to the processor card as an interrupt signal. The processor subsequently pulses the strobe 9 line (TP1) to reset the interrupt latch and to output-enable the shift-and-store register ML17 (para. 54).

SERIAL-TO-PARALLEL CONVERTER

54. ML17 is an 8-stage serial shift register which has a storage latch associated with each stage. The data in each shift register stage is transferred to the storage register when a '1' is applied to the strobe (STB) input, and the stored data appears at the Q1 to Q8 parallel outputs when a '1' is applied to the enable (EN) input. When a '0' is present at the enable input, the Q1 to Q8 outputs are in the high-impedance 3-state condition.

PARALLEL-TO-SERIAL CONVERTER

55. The parallel-to-serial data converter comprises a pair of first in-first out (FIFO) registers ML7, ML12, and an 8-bit parallel or serial input/serial output shift register ML8. Each FIFO register is a 4-bits-wide by 16-bits-long storage device, and two such devices are used to produce an 8-bits-wide by 16-bits-long register. The 4 x 16 data register in each device is under constant control of a logic network. Each word

position in the array is clocked by a control flip-flop, which stores a marker bit; a '1' signifies an occupied position, whilst a '0' denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding control flip-flop. When a control flip-flop is in the '0' state and detects a '1' in the preceding flip-flop, it generates a clock pulse which transfers data from the preceding four data latches into its own data latches, and resets the preceding control flip-flop to '0'. The first and last control flip-flops have buffered outputs, designated DIR (data in ready) and DOR (data out ready) respectively. Since all empty locations 'bubble' automatically to the input end, and all valid data ripples through to the output end, the status of the first control flip-flop (DIR) indicates if the FIFO is full, and the status of the last control flip-flop (DOR) indicates if the FIFO contains data. Since the earliest data (first in) is removed from the bottom of the stack (the output end), all subsequently entered data propagates (ripples) towards the output. Data is shifted into the FIFO on a positive-going transition at the shift-in (SI) pin provided the DIR output is at a '1' (the DIR output momentarily goes to a '0' when the data is shifted in, and remains at '0' should all 16-word locations be filled with valid data).

56. As soon as the first word entered has rippled to the output, the DOR output goes to a '1', and output data is latched at the Q outputs. The next word is latched at the output by a negative-going transition at the SO (shift out) input, and when this occurs, the DOR output momentarily goes to a '0'; R20 and C14 are included to prevent these momentary 0V pulses affecting the operation of G15 and also to prevent the generation of spurious local interrupts (via G3). When the FIFO is empty, the DOR output remains at a '0' and generates (local control only) an interrupt. This allerts the processor which then loads the FIFO with 12 successive bytes (two frames) of SCORE data. In remote control, data is loaded into the FIFO under software control (para. 61).

57. ML8 is an 8-stage parallel or serial input/serial output shift register. When the parallel/serial control input is at logic '1', data at the parallel input pins (from the FIFO registers) is loaded into the register synchronously with the positive transition of the clock signal. When the parallel/serial control input is at logic '0', data is serially shifted into and out of the register synchronously with the positive transition of the clock signal. Note that the falling edge of the parallel/serial pulse shifts out the next byte of data from the FIFO registers, and this data is loaded into ML8 by the next parallel/serial control pulse.

58. The parallel/serial control pulse from inverting NOR gate G16 is produced by ML1b, and occurs once every eight SCORE clock periods due to the action of the output counter ML5b. The operation of the circuit is largely the same for both local and remote control, as follows (the differences for the remote control situation are described in para. 61).

PARALLEL/SERIAL CONTROL SIGNAL

59. ML5b is a BCD up-counter which is clocked by the SCORE clock signal from G9. When a count of eight is reached, the Q4 output changes to a '1', the output from NOR gate G13 changes to a '0', and the resulting '1' output from G14 sets ML1b. The Q output of ML1b is thus set to a '1', and this is routed to:

(1) NAND gate G15; provided the FIFO is not empty (DOR is at '1'), then a '0' is applied to G16 and a positive transition occurs at the output.

(2) The clock input of ML1a; with a '0' at the D input, the $\overline{Q}$ output goes to a '1', G11 is enabled, and the '0' at the $\overline{Q}$ output of ML1b resets ML5b. The Q output of ML1a goes to a '0', and this maintains the '1' at the output of G12.

60. One-half SCORE clock period later, ML1b is clocked by the output from SCORE clock inverter ML10f, and the '0' at the D input causes the Q output to return to a '0'. Thus a positive-going output pulse is applied to the parallel/serial input of ML8 once every eight SCORE clock periods.

61. When the receiver is operating in the remote condition, the loading of data into the FIFO register is under software control, and at the appropriate moment, the output counter ML5b is synchronised to the input counter ML5a by a start-in-sync. (SIS) signal from the processor (card edge connector pin 7). The action of the circuit is as follows.

62. Bytes of received SCORE control data from serial-to-parallel converter ML17 are routed to the processor card via the I/O bus and are temporarily stored in RAM. When a correct sync. code is recognised, a software counter is initialised and then counts successive bytes of the SCORE control data frame. When the last but one byte of the frame has been received, strobe 13 (edge connector pin 7) is applied to the set input of the start-in sync. (SIS) latch, and also to the reset input of ML1b, with the following results:

(1) The '0' at the $\overline{Q}$ output of ML1a forces a '1' at the output of NAND gate G11, and the output counter ML5b is held reset.

(2) The '1' at the $\overline{Q}$ output of ML1a enables NAND gate G12 for the next positive-going strobe pulse from ML6b.

(3) The '1' at $\overline{Q}$ output of ML1b is of no consequence at this point in the sequence.

(4) The '0' at the Q output of ML1b forces a '1' at the output of NAND gate G15, and the parallel/serial control input at ML8 pin 9 is held at a '0'.

63. A master reset signal (strobe 14) is then applied to the FIFO register, and a sync. code is loaded in by the processor. When the last byte of the control data frame has been received, the data is processed, and the remaining bytes of the revertive data frame to be returned are loaded into the FIFO register. The strobe pulse from ML6b which loaded the last byte of the received frame into ML17 is also applied to the reset input of the input counter ML5a, and to NAND gate G12; since the remaining input of G12 is also at a '1', a '0' occurs at the output, and this forces a '1' at the output of G14. ML1b is thus set, and is clocked one-half SCORE clock period later by the output from ML10f. The resulting positive-going pulse at the Q output of ML1b results in a positive-going pulse at the output of G16, and the previously loaded sync. code (which has rippled through to the output of the FIFO register) is parallel-loaded into the output shift register ML8.

64. At the same time, the positive-going pulse at the Q output of ML1b clocks ML1a, the '0' at the D input results in a '1' at the $\overline{Q}$ output, and this removes the reset from ML5b (via G11). The '0' at the Q output of ML1a forces a '1' at the output of G12, and this enables G14 for subsequent '1' outputs from G13. The input and output counters, ML5a and ML5b respectively, are now synchronised, and this ensures synchronism between input and output SCORE data frames.

USER FUNCTIONS

65. When the receiver is under remote control, the forward control data user functions (conveyed by SCORE word 4) are routed by the processor and the I/O bus to hex. D-type latch ML11; this latch is then clocked by the strobe 11 signal, and the user function data is routed via open-collector inverter transistors TR1 to TR4 to the appropriate pins of the front panel mounted CONTROL connector. The revertive data user functions (conveyed by SCORE word 0) are applied to the appropriate pins of the CONTROL connector and are then routed to the processor via the I/O bus by the application of strobe 12 which enables NAND gates G18 to G21.

SCORE INTERFACE CARD (ST 79796)

Resistors

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R1	2k7	Metal oxide		2	916548
R2	2k7	Metal oxide		2	916548
R3	330	Metal oxide		2	915690
R4	330	Metal oxide		2	915690
R5	10 k	Metal oxide		2	914042
R6	68 k	Metal oxide		2	916478
R7	68 k	Metal oxide		2	916478
R8	22 k	5-Resistor SIL Network		2	939649
R9	270 k	Metal oxide		2	923598
R10	22 k	Metal oxide		2	913493
R11	10 k	Metal oxide		2	914042
R12	10 k	Metal oxide		2	914042
R13	10 k	Metal oxide		2	914042
R14	10 k	Metal oxide		2	914042
R15	22 k	Metal oxide		2	913493
R16	22 k	Metal oxide		2	913493
R17	22 k	Metal oxide		2	913493
R18	22 k	Metal oxide		2	913493
R19	4k7	5-Resistor SIL Network		2	939649
R20	68 k	Metal oxide		2	916478

Capacitors

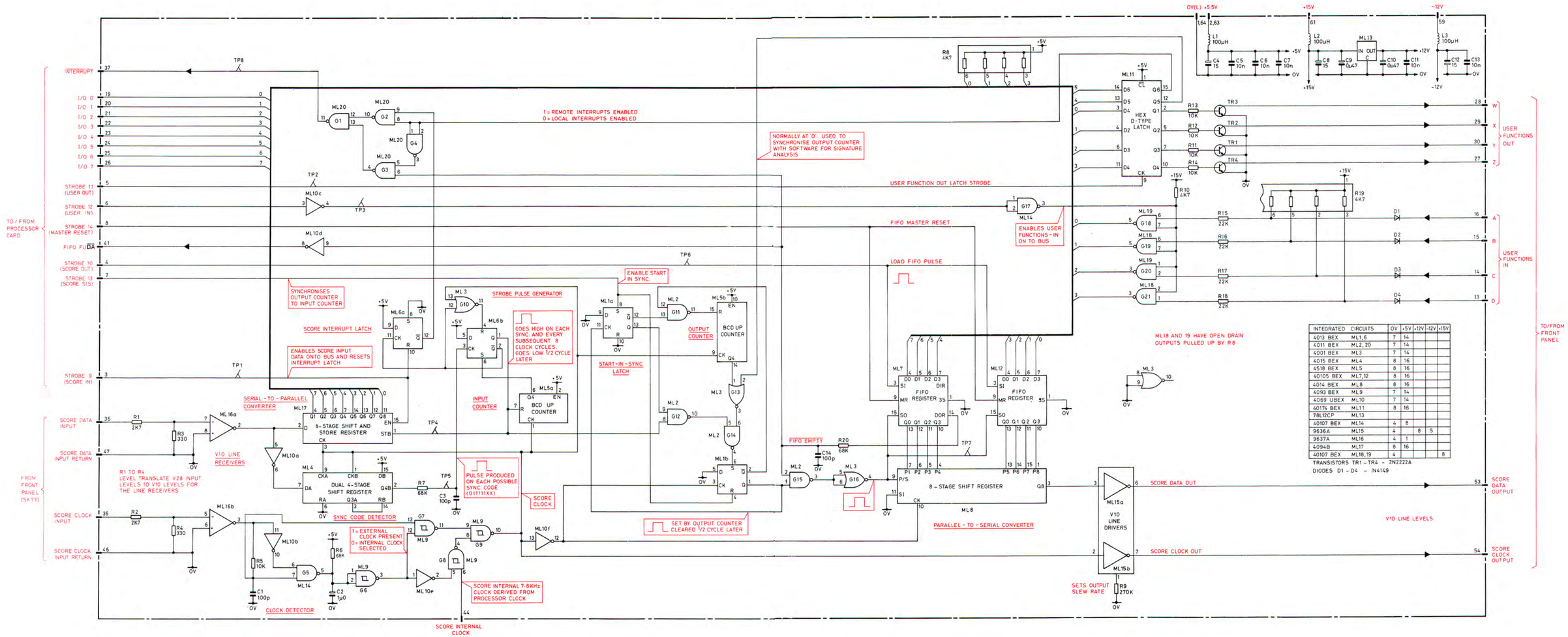
			Volts		
C1	100 p	Ceramic Disc	500	10	917417
C2	1µ0	Tantalum Bead	35	20	923571
C3	100 p	Ceramic Disc	500	10	917417
C4	15	Tantalum Tubular	20	20	935601
C5	10 n	Ceramic Disc	250	+40 -20	900067
C6	10 n	Ceramic Disc	250	+40 -20	900067
C7	10 n	Ceramic Disc	250	+40 -20	900067
C8	15	Tantalum Tubular	20	20	935601
C9	0µ47	Tantalum Bead	35	20	939267
C10	0µ47	Tantalum Bead	35	20	939267
C11	10n	Ceramic Disc	250	+40-20	900067
C12	15	Tantalum Tubular	20	20	935601
C13	10n	Ceramic Disc	250	+40-20	900067
C14	100 p	Ceramic Disc	500	10	917417

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Inductors					
L1	100 µH	Choke		10	939161
L2	100 µH	Choke		10	939161
L3	100 µH	Choke		10	939161
Diodes					
D1		Silicon 1N4149			914898
D2		Silicon 1N4149			914898
D3		Silicon 1N4149			914898
D4		Silicon 1N4149			914898
Transistors					
TR1		NPN Silicon 2N2222A			923217
TR2		NPN Silicon 2N2222A			923217
TR3		NPN Silicon 2N2222A			923217
TR4		NPN Silicon 2N2222A			923217
Integrated Circuits					
ML1		Dual D-type flip flop 4013BE			926860
ML2		Quad 2-input NAND gate 4011BE			930028
ML3		Quad 2-input NOR gate 4001BE			930027
ML4		Dual 4-bit shift register 4015BE			930973
ML5		Dual BCD up-counter 4518BE			928002
ML6		Dual D-type flip flop 4013BE			926860
ML7		FIFO Register 40105BE			931050
ML8		8-stage Shift Register 4014BE			930972
ML9		Quad 2-input NAND Schmitt 4093BE			930854
ML10		Hex Inverter 4069UBE			930999
ML11		Hex D-type flip flop 40174BE			931060
ML12		FIFO Register 40150BE			931050
ML13		+12 V Regulator 78L12CP			938880
ML14		Dual 2-input NAND Buffer 40107BE			931052
ML15		Dual line driver 9636A			937946

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
ML16		Dual line receiver 9637A			937945
ML17		8-bit shift register 4094BE			929324
ML18		Dual 2-input NAND buffer 40107BE			931052
ML19		Dual 2-input NAND buffer 40107BE			931052
ML20		Quad 2-input NAND gate 4011BE			930028

Miscellaneous

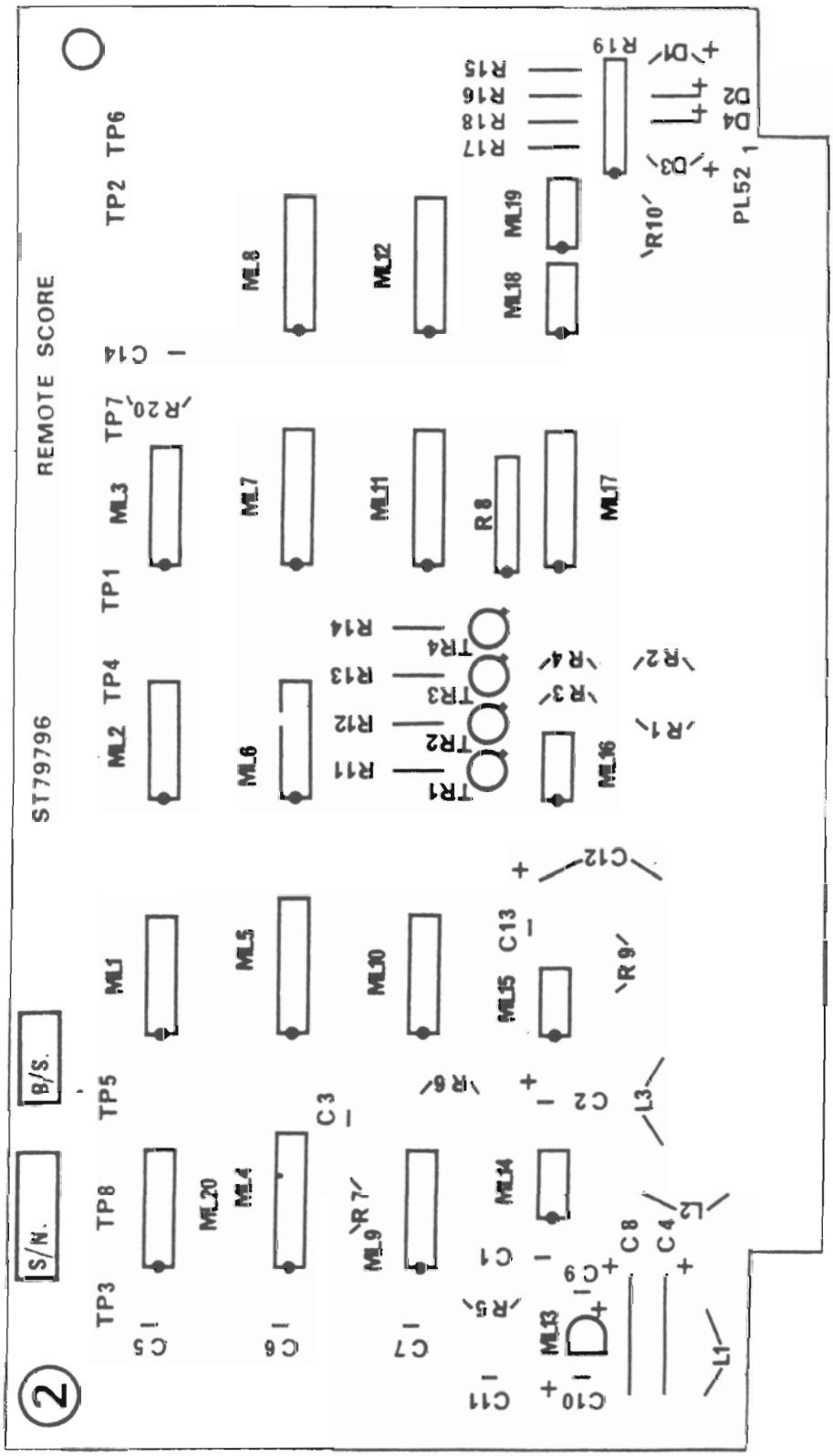
		8-pin DIL IC socket			940901
		14-pin DIL IC socket			940902
		16-pin DIL IC socket			940903
		Board Stiffener			BD79561
		Captive Screw M3 x 10 mm			AD81976
		Test point			936148



RACAL

TH2449	DC79796	16.1	TH2449	DC79796	16.1
1	2 3 4 5	1/2	1		2/2

Circuit : SCORE Interface Card Fig.16.1



Layout: SCORE Interface Card Fig. 16.2

CHAPTER 17

POWER SUPPLIES

CONTENTS

ILLUSTRATIONS,

CHAPTER 17

POWER SUPPLIES

INTRODUCTION

1. The power supply module uses a mixture of switching regulator and linear regulator circuits to produce, from the 10V to 32V DC supply, regulated outputs at +5.5V, +15V, +24V, -12V and -30V. The module contains two circuit boards, namely the switching regulator board (located inside the module) and the linear regulator board (mounted on the module lid).

FUNCTIONAL DESCRIPTION

2. In the functional diagram of the power supply module given in fig. 17.1 (at the end of the chapter), the main flow (for the +5.5V and +15V outputs) is shown using heavy lines.

Protection

3. This comprises a high-current rectifier diode (D3) to protect against supply input reversal, and a silicon controlled rectifier (SCR1) which conducts to blow the 6.3A supply fuse on the front panel should the 6.7V DC supply rise above 8.5V (output from the excess voltage detector TR6).

Linear Regulator

4. This stage (TR1, TR2) provides a +9V to +12V supply (marked V on fig. 17.1) for the two switching regulator stages (ML1, ML3), and for the supply level monitor (ML2a, ML2b).

6.7V Supply

5. The 6.7V supply is applied to the push-pull driver stage (TR7 to TR12) for the plus and minus 16V and 35V outputs, and is also applied to the +5.5V linear regulator stage on the linear regulator board. It is derived using a series chopper-regulator (TR3, TR4, TR5) which is controlled by the single-ended output from the switching regulator stage ML1. If the current flowing through the excess current selector exceeds approximately 4A, then a close-down signal is applied to ML1 and current foldback comes into operation.

Reference Buffer

6. A high stability +5V reference supply is taken from switching regulator ML1, is reduced by a potential divider to a level of +2.5V, and is then buffered before application to the control amplifier stages in both of the switching regulator stages ML1 and ML3.

16V and 35V Supplies

7. Plus and minus 16V and 35V supplies are derived using switching regulator stage ML3, push-pull driver stage TR7 to TR12 and transformer T1. If the

level of the supply voltage (at PL63) exceeds approximately 40V, the excess supply voltage detector circuit applies a close-down signal to switching regulator ML3. Conversely, if the supply voltage level falls below approximately 9V, close-down of ML3 is again achieved, this time by the SUPPLY FAILED output from the supply level monitor (ML2a, ML2b).

Linear Regulators

8. Linear regulator stages are used to produce the +5.5V, +15V, +24V, -12V and -30V outputs. Note that the reference supply for the +5.5V and +15V regulators is derived from the +24V output. Note also that production of the -12V supply is inhibited should the +5.5V supply fail or should the supply voltage level at PL63 fall below approximately 9V. The -30V supply is inhibited on failure of the -12V supply or should the supply voltage level at P63 fall below approximately 9.5V. The +5.5V, -12V and -30V supplies are interlocked in this way so that they are produced in the correct order at switch-on, and are removed in the correct order at switch-off, to suit the EAROM devices on the processor card.

Synchronisation

9. To reduce the effect of switching transients, a 62.5kHz squarewave signal from the processor card (derived from the CPU clock signal generator) is used to lock the switching regulators to the receiver internal reference signal. A monostable circuit (TR1, TR2), which is powered from the high stability +5V reference output from switching regulator ML3, produces positive-going one microsecond duration pulses which are applied to the oscillator input pins of the two switching regulator devices ML1 and ML3.

CIRCUIT DESCRIPTION
SWITCHING REGULATOR BOARD (Fig. 17.2)

Switching Regulator Stages

10. Although the two switching regulator devices ML1 and ML3 are identical, the first is used in the single-ended configuration, whilst the second is used in the dual-ended or push-pull configuration. A functional diagram of the device is given in fig. 17(a).

11. The oscillator section uses an external resistor (RT) to establish a constant charging current into an external capacitor (CT). In order to synchronise both regulator devices to the same external reference signal (from the monostable on the linear regulator board), the CT terminals are commoned and connected to a single timing capacitor (C10), timing resistors (R23, R24) are connected only to the RT terminal of ML1, and the external synchronisation signal is applied in parallel to the oscillator output pin on each device.

12. The error amplifier compares a sample of the output voltage applied to the inverting input (potential divider R38, R39 for the 6.7V supply, R57 and R58 for the +16V supply) with the reference 2.5V at the non inverting input (from voltage follower buffer stage ML2d). Any difference between the two voltage levels results in an increase or a decrease, as appropriate, in the width of the pulses at the EA and EB output pins, and hence a corresponding increase or decrease in the output voltage level.

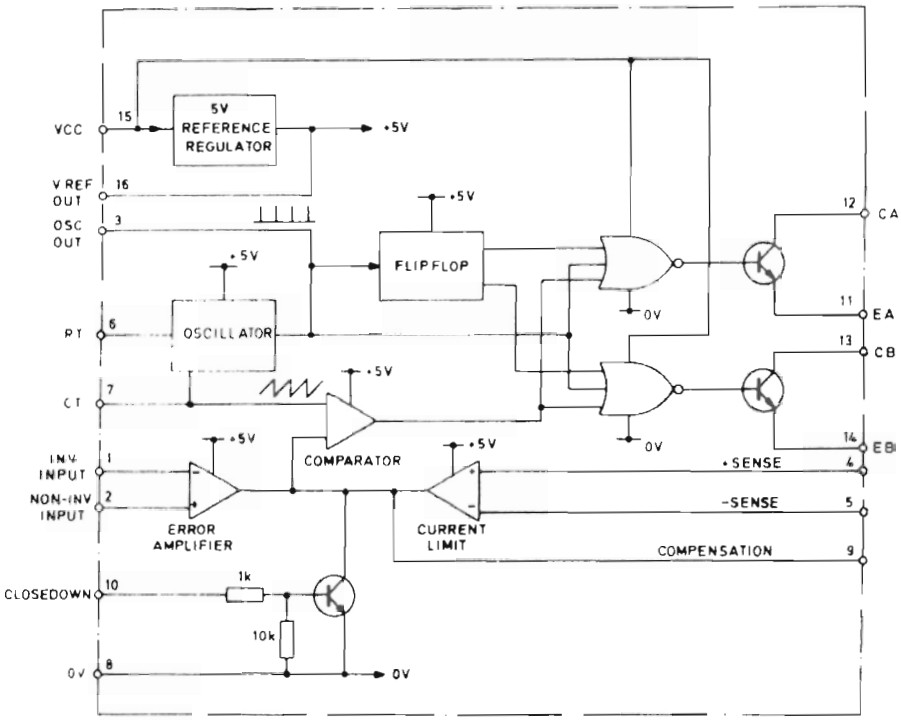


Fig 17(a) Functional Diagram: Switching Regulator

13. The current limit facility provided by ML1 is not used, and pins 4 and 5 are thus connected to 0V. For ML3 however, the primary curent drawn by transformer T1 is monitored by parallel-connected resistors R48, R49 and R50, such that should excessive current be drawn, the resulting voltage developed across the three resistors causes the regulator device to shut down.

Protection

14. Reverse polarity of the supply input is protected against by the inclusion of rectifier diode D3, which can pass sufficient current to cause the 6.3A supply fuse to blow. The Thyristor SCR1 connected across D3 will also cause the 6.3A supply fuse to blow if the level of the 6.7V supply rises above approximately 8.5V (excess voltage monitor stage TR6). Further protection is provided by potential divider R4, 36V zener diode D12 and R42 in that should the level of the supply input exceed approximately 40V, D12 conducts and causes the close-down of switching regulator device ML3.

6.7V Supply

15. The 6.7V supply is derived using a series chopping regulator stage TR3, TR4, TR5. The switching regulator stage ML1 varies the on-off time of TR4 to produce an average output voltage, after filtering, of 6.7V. The excess current monitor stage ML2c is connected as a wheatstone bridge where the slightly lower value of R33 compared with the value of R25 causes the voltage at the inverting input of ML2c to be slightly higher than that at the non-inverting input, and hence a '0' at the output. If

however, the current through resistors R27 and R28 exceeds aproximately 4A, the resultant voltage drop across these two resistors causes ML2c to change state, and a positive close-down voltage is applied to switching regulator stage ML1.

16V and 35V Supplies

16. The anti-phase EA and EB pulse width modulated outputs from ML3 are applied via emitter followers TR7, TR8 and TR11, TR12, to push-pull driver transistors TR9 and TR10. A sample of the +16V DC output from potential divider R57, R58 is fed back to the error amplifier of ML3 where it is compared with the 2.5V reference from ML2d. Any difference in the levels of these two voltages is then used to vary the conduction times of TR9 and TR10 to produce an average output after filtering of 16V.

Supply Level Monitor

17. The supply level monitor circuit comprises voltage comparators ML2a and ML2b; it monitors the level of the supply input at PL63 and provides a 0V SUPPLY FAILING signal if the supply input falls to less than 9.5V, and a 0V SUPPLY FAILED signal if the input voltage falls to less than 8.9V. Under normal operation, the voltage levels at the non-inverting inputs of ML2a and ML2b are more positive than the +3.3V reference levels at the inverting inputs, and thus both output signals are at the positive supply level. If the supply input level falls to approximately 9.5V, the voltage level at the non-inverting input falls below the 3.3V reference, ML2b changes state, and the 0V SUPPLY FAILING signal is produced. If the supply level falls below approximately 8.9V, then ML2a also changes state and the 0V SUPPLY FAILED signal is also produced.

LINEAR REGULATOR BOARD (Fig. 17.4)
+5.5V and +15V Regulators

18. The linear regulator stage for the +5.5V supply, comprising V-MOS power FET TR5, error amplifier ML2b, and current limit stage ML2a, is similar in design to the +15V regulator, comprising TR8, ML2d and ML2c. The reference voltage for both error amplifier stages (ML2b and ML2d) is set by R23, and is derived from the +24V regulator stage ML1. The operating supply for the quad comparator stage ML2 is taken from the +35V input line and is limited to a maximum of 30V by zener diode D6.

3-Terminal Regulators

19. The +24V, -30V and -12V supplies are all derived using 3-terminal regulator devices ML1, ML3 and ML4 respectively. These devices contain a current limiting circuit to limit the peak output current to a safe value. If the internal power dissipation becomes too high for the heat sinking provided, a thermal shut-down circuit takes over to prevent the device overheating.

20. The -30V supply circuit uses a -24V regulator device where the potential at the common terminal is set by the output from potential divider R6, R9 and preset potentiometer R13. Note that the supply to the -12V regulator stage ML4 is switched on by TR4 only when the +5.5V supply is present and the SUPPLY FAILED input is not present. Switching transistor TR7 is included to ensure that the -12V supply is available before the -30V

supply, and to remove the -30V supply should the 0V SUPPLY FAILING signal occur.

Sync Pulse Monostable

21. Transistors TR1 and TR2 are connected as a monostable to produce one microsecond-duration positive-going output pulses from the 62.5kHz squarewave signal at TP13. This pulsed signal is used to synchronise the switching regulator devices on the switching regulator board to the receiver internal reference signal, and so limit the effects of switching transients.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SWITCHING REGULATOR BOARD (ST 81938)			
Resistors			Watts		
R1	68k	Metal Oxide	0.25	2	916478
R2	3k9	Metal Oxide	0.25	2	915074
R3	39k	Metal Oxide	0.25	2	900993
R4	4k7	Metal Oxide	0.25	2	913490
R5	100	Metal Oxide	0.25	2	910388
R6	1k5	Metal Oxide	0.25	2	911166
R7	OR1	Wirewound	2.5	10	921359
R8	390	Metal Oxide	0.25	2	916331
R9	1M	Carbon Film	0.25	10	943027
R10	4M7	Carbon Film	0.25	10	925536
R11	10k	Metal Oxide	0.25	2	914042
R12	4k7	Metal Oxide	0.25	2	913490
R13	1k	Metal Oxide	0.25	2	913489
R14	1k3	Metal Oxide	0.25	2	920760
R15	680	Metal Oxide	0.25	2	910113
R16	4k7	Metal Oxide	0.25	2	913490
R17	680	Metal Oxide	0.25	2	910113
R18	4k7	Metal Oxide	0.25	2	913490
R19	1k	Metal Oxide	0.25	2	913489
R20	220	Wirewound	2.5	5	913604
R21	33	Wirewound	2.5	5	913584
R22	4k7	Metal Oxide	0.25	2	913490
R23	1k8	Metal Oxide	0.25	2	911148
R24	1k	Variable, preset			939863
R25	1k2	Metal Oxide	0.25	2	911179
R26	2k	Metal Oxide	0.25	2	917652
R27	OR1	Wirewound	2.5	10	921359
R28	OR1	Wirewound	2.5	10	921359
R29	15k	Metal Oxide	0.25	2	920646
R30	5k	Variable, preset			939865
R31	15k	Metal Oxide	0.25	2	920645
R32	330k	Carbon Film	0.25	10	940250
R33	1k	Metal Oxide	0.25	2	913489
R34	2k	Metal Oxide	0.25	2	917652
R35	2k2	Metal Oxide	0.25	2	916546

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R41	2k7	Metal Oxide	0.25	2	916548
R42	1k	Metal Oxide	0.25	2	913489
R43	2R2	Wirewound	2.5	5	917141
R44	100	Metal Oxide	0.5	2	913973
R45	82	Metal Oxide	0.5	2	909550
R46	82	Metal Oxide	0.5	2	909550
R47	15	Wirewound	2.5	5	913576
R48	OR1	Wirewound	2.5	10	921359
R49	OR1	Wirewound	2.5	10	921359
R50	OR1	Wirewound	2.5	10	921359
R51	15	Wirewound	2.5	5	913576
R52	4k7	Metal Oxide	0.25	2	913490
R53	100	Metal Oxide	0.5	2	913973
R54	2R2	Wirewound	2.5	5	917141
R55	4k7	Metal Oxide	0.25	2	913490
R56	330	Metal Oxide	0.5	2	910200
R57	18k	Metal Oxide	0.25	2	900994
R58	3k3	Metal Oxide	0.25	2	910111
Capacitors			Volts		
C1	10	Tantalum tubular	63	20	939262
C2	470p	Silver mica	100	2	939326
C3	47	Tantalum solid	63	10	940849
C4	10	Tantalum tubular	63	20	939262
C5	1u0	Tantalum tubular	35	20	906699
C6	220n	Polyester Rectangular	100	20	909882
C7	22n	Polyester	400	20	931166
C8	1n	Ceramic Plate	50	10	940312
C9	150	Tantalum tubular	16	20	939849
C10	10n	Polycarbonate	400	20	931136
C11	150	Tantalum tubular	16	20	939849
C12	68	Tantalum tubular	16	20	939850
C13	15	Tantalum tubular	20	20	935601
C14	33	Tantalum tubular	25	20	931175
C15	10n	Polycarbonate	400	10	931136
C16	3u3	Tantalum tubular	63	20	939852
C17	10n	Polycarbonate	400	10	931136
C18	220	Polyester Rectangular	100	20	909882
C19	33	Tantalum tubular	25	20	931175
C20	6u8	Tantalum tubular	35	20	939851
C21	47	Tantalum tubular	35	20	938987
C22	6u8	Tantalum tubular	35	20	939851

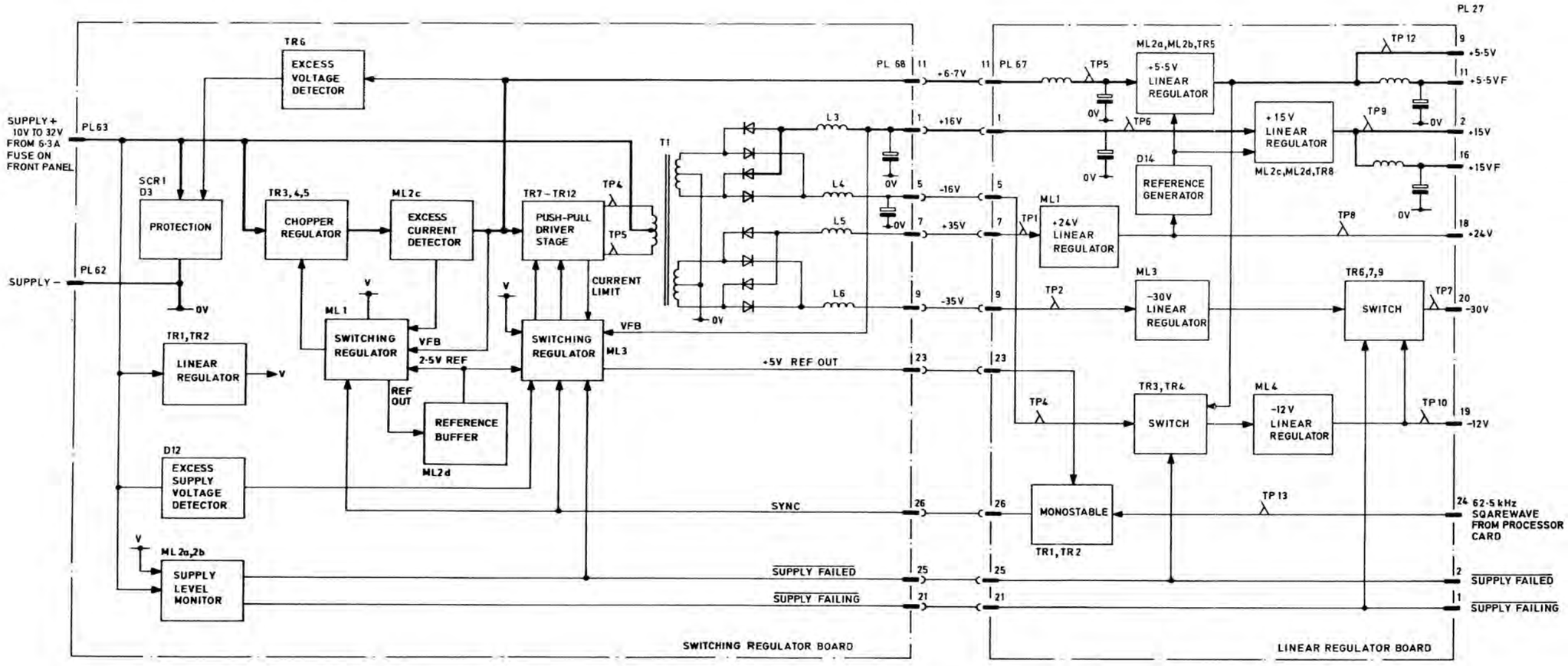
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Induction					
L1	20uH	Choke Assembly			AT82302
L2	200uH	Choke Assembly			AT82300
L3	470uH	Choke Assembly			AT82301
L4	4m7H	Choke Assembly			AT82295
L5	36mH	Choke Assembly			AT82296
L6	75mH	Choke Assembly			AT82297
Transformers					
T1		Transformer Assembly			AT82303
Connectors					
PL62) PL63)		Blade, 0.25 in, PCB mounting			939264
PL68		Plug, 26-way			938858
Diodes					
D1		Silicon 1N4149			914898
D2		Zener, 3.3V, 400mW BZX79C3V3			941517
D3		Silicon Rectifier MR752			941942
D4		Zener, 4.7V, 400mW BZX79C4V7			926429
D5		Silicon 1N4149			914898
D6		Silicon 1N4149			914898
D7		6A Silicon Rectifier VES1303			939862
D8		Silicon 1N4149			914898
D9		7A Silicon Rectifier BYW29-100			937939
D10		Silicon 1N4149			914898
D11		Zener 7.5V, 400mW BZX79C7V5			941639
D12		Zener, 36V, 3.25 W BZT 03-C36			943490
D13		Fast Recovery BYV95C			940652
D14		Fast Recovery BYV95C			940652
D15		6A Silicon Rectifier VES1303			939862
D16		Fast Recovery BYV95C			940652
D17		6A Silicon Rectifier VES1303			939862
D18		6A Silicon Rectifier VES1303			939862
D19		Fast Recovery BYV95C			940652
D20		Fast Recovery BYV95C			940652
D21		6A Silicon Rectifier VES1303			939862
D22		Fast Recovery BYV95C			940652
D23		Fast Recovery BYV95C			940652
D24		Fast Recovery BYV95C			940652
D25		Fast Recovery BYV95C			940652

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D26		Silicon 1N4149			914898
D27		Fast Recovery BYV95C			940652
D28		Silicon 1N4149			914898
D29		Silicon 1N4149			914898
SCR1		Silicon Controlled Rectifier 52600B			939151
Transistors					
TR1		NPN Silicon BC107			911929
TR2		PNP Silicon			941548
TR3		PNP Silicon BCY71			911928
TR4		PNP Silicon D45H11			939149
TR5		NPN Silicon			941547
TR6		PNP Silicon BCY71			911928
TR7		NPN Silicon BFY51			908753
TR8		PNP Silicon 2N4037			922991
TR9		NPN Silicon BU407			939859
TR10		NPN Silicon BU407			939859
TR11		NPN Silicon BFY51			908753
TR12		PNP Silicon 2N4037			922991
Integrated Circuits					
ML1		Switching Regulator SG1524			937496
ML2		Quad Comparator LM224J			938978
ML3		Switching Regulator SG1524			937496
Miscellaneous					
		Test Point			936148
		Heat Sink (TR7, 8, 11, 12)			939473
		14-pin IC Socket			930605
		16-pin IC Socket			930606
		Insulating Bead			917849
		LINEAR REGULATOR BOARD (ST81940)			
Resistors			**Watts**		
R1	10k	Metal Oxide	0.25	2	914042
R2	2k2	Metal Oxide	0.25	2	916546
R3	2k2	Metal Oxide	0.25	2	916546
R4	2k2	Metal Oxide	0.25	2	916546
R5	820	Metal Oxide	0.25	2	917065

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R6	390	Metal Oxide	0.5	2	909771
R7	4k7	Metal Oxide	0.25	2	913490
R8	1M	Carbon Film	0.25	10	943027
R9	470	Metal Oxide	0.5	2	918030
R10	0R1	Wirewound	2.5	10	921359
R11	0R1	Wirewound	2.5	10	921359
R12	390k	Carbon Film	0.25	10	941960
R13	20k	Variable, preset			940857
R14	4k7	Metal Oxide	0.25	2	913490
R15	820k	Carbon Film	0.25	10	943028
R16	2k2	Metal Oxide	0.25	2	916546
R17	10k	Metal Oxide	0.25	2	914042
R18	10k	Metal Oxide	0.25	2	914042
R19	10k	Metal Oxide	0.25	2	914042
R20	470	Metal Oxide	0.25	2	920758
R21	4k7	Metal Oxide	0.25	2	913490
R22	470	Metal Oxide	0.25	2	920758
R23	2k	Variable, preset			940854
R24	8k2	Metal Oxide	0.25	2	918202
R25	2k2	Metal Oxide	0.25	2	916546
R26	4k7	Metal Oxide	0.25	2	913490
R27	2k2	Metal Oxide	0.25	2	916546
R28	1M	Carbon Film	0.25	10	943027
R29	0R1	Wirewound	2.5	10	921359
R30	0R1	Wirewound	2.5	10	921359
R31	270k	Carbon Film	0.25	10	923598
R32	4k7	Metal Oxide	0.25	2	913490
R33	4k7	Metal Oxide	0.25	2	913490
R34	5k6	Metal Oxide	0.25	2	918128
R35	5k6	Metal Oxide	0.25	2	918128
R36	10k	Metal Oxide	0.25	2	914042
R37	560k	Carbon Film	0.25	10	925902
R38	10k	Metal Oxide	0.25	2	914042
R39	4k7	Metal Oxide	0.25	2	913490
R40	4k7	Metal Oxide	0.25	2	913490
R41	2k7	Metal Oxide	0.25	2	916548
R42	10k	Metal Oxide	0.25	2	914042
R43	22k	Metal Oxide	0.25	2	913493
R44	5k6	Metal Oxide	0.25	2	918128
R45	5k6	Metal Oxide	0.25	2	918128
R46	1M	Metal Oxide	0.25	10	943027

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors			Volts		
C1	6u8	Tantalum tubular	35	20	939851
C2	1u0	Polyester	100	10	931163
C3	1u0	Polyester	63	10	921639
C4	1u0	Tantalum tubular	35	20	908462
C5	100p	Ceramic Disc	500	10	917417
C6	1u0	Polyester	100	10	931163
C7	100n	Polyester	100	10	931130
C8	1u0	Tantalum tubular	35	20	908462
C9	100n	Polyester	100	10	931130
C10	68	Tantalum tubular	16	20	939850
C11	15	Tantalum tubular	20	20	935601
C12	4u7	Tantalum tubular	50	20	939853
C13	100 p	Ceramic Disc	500	20	917417
C14	470n	Polyester	100	20	931132
C15	100n	Polyester	100	10	931130
C16	15	Tantalum tubular	20	20	935601
C17	100 p	Ceramic Disc	500	20	917417
C18	100	Tantalum tubular	10	20	931172
C19	47	Tantalum tubular	35	20	938987
C20	47	Tantalum tubular	35	20	938987
C21	220	Tantalum tubular	10	20	938988
C22	1u0	Tantalum tubular	35	20	908462
C23	1n0	Ceramic Plate	50	10	940312
Induction					
L1	1mH	Choke			938956
L2		Coil Assembly			AT82298
L3		Coil Assembly			AT82299
L4		Coil Assembly			AT82298
Connectors					
PL27		Plug, 26-way			938858
PL67		Plug, 26-way			938858
Diodes					
D1		Silicon 1N4149			914898
D2		Zener, 39V, 3.25 W BZT 03-C39			922213
D3		Zener, 39V, 3.25 W BZT 03-C39			922213
D4		Zener, 24V, 2.5W BZX70C24			926830
D5		Silicon Rectifier 1N4002			923564

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
D6		Zener, 30V, 3.25W BZT03C30			927452
D7		Silicon Rectifier 1N4002			923564
D8		Silicon 1N4149			914898
D9		Silicon 1N4149			914898
D10		Zener, 4.3V, 400mW BZX79C4V3			941638
D11		Zener, 22V, 400mW BZX79C22			941643
D12		Silicon 1N4149			914898
D13		Silicon 1N4149			914898
D14		Zener, 6.2V, 400mW 1N823A			917244
D15		Zener, 9.1V, 400mW, BZX79C9V1			921751
D16		Zener, 22V, 400mW BZX79C22			941643
D17		Silicon 1N4149			914898
D18		Silicon 1N4149			914898
D19		Zener, 10V, 400mW BZX79C10			930320
D20		Silicon Rectifier 1N4002			923564
Transistors					
TR1		PNP Silicon BCY71			911928
TR2		NPN silicon BC107			911929
TR3		PNP Silicon BCY71			911928
TR4		NPN Silicon BFY51			908753
TR5		V-MOS Power FET IVN5201CNE			939860
TR6		PNP Silicon BCY71			911928
TR7		NPN Silicon BFY51			908753
TR8		V-MOS Power FET IVN5201CNE			939860
TR9		NPN Silicon BC107			911929
Integrated Circuits					
ML1		+24V Regulator MC7824CT			939854
ML2		Quad Comparator LM224J			938978
ml3		-24V Regulator MC7924CT			939856
ML4		-12V Regulator MC7912CT			939855
Miscellaneous					
		Test Point			936148
		14-pin IC Socket			940902
		Insulating Bead			909151



RACAL
TH 2449

Functional Diagram: Power Supply Module

Fig. 17.1

INTEGRATED CIRCUITS		DIODES	
ML1,3	SG1524	D1,5,6,8,10,26,28,29	IN4149
ML2	LM224J	D2	BZX79 C3V3
		D3	6051
		D4	BZX 79 C4V7
	TRANSISTORS	D7,15,17,18,21	UES1303
TR1	BC107	D9	BYW 29-100
TR2	BD140	D11	BZX79 C7V5
TR3,6	BCY71	D12	BZX 61 C36V
TR4	D45H11	D13,14,16,19,20,22-25,27	BYV 95C
TR5	BD139		
TR7,11	BFY51		
TR8,12	2N4037		
TR9,10	BU407		

NOTES

±10% DC VOLTAGES MEASURED WITH 10MΩ D.V.M

MAIN CURRENT PATH

FEEDBACK OR CONTROL PATH

WAVEFORMS

ON FULL LOAD WITH 24V SUPPLY AND SYNC PULSES PRESENT AT PL68-26

SYNC PULSES PL68-26: 4V, 0V; 1µs; 16µs

TP2: +23V, −1V

TP4: +48V, +24V, 0V

TP5: +48V, +24V, 0V

SUPPLY +VE
10 TO 35V D.C FROM 6.3A FUSE ON FRONT PANEL

SUPPLY -VE

SUPPLY FILTER

LINEAR REGULATOR SUPPLYING CONTROL CIRCUITS

SERIES CHOPPER REGULATOR (6·7V)

EXCESS CURRENT MONITOR (6·7V)

EXCESS VOLTAGE MONITOR (6·7V)

PUSH PULL FORWARD CONVERTER
MAIN OUTPUT IS +16V, THE −16 +35 AND −35V LOW CURRENT SUPPLIES TRACK THE +16V PROVIDED THE CURRENTS DRAWN ARE APPROXIMATELY CORRECT

CROWBAR THYRISTOR BLOWS SUPPLY FUSE IF +6·7V LINE RISES ABOVE 8·5V

REVERSE POLARITY PROTECTION DIODE (D3)

ZERO FOR NORMAL OPERATION

CONTROL CIRCUIT (6·7V)
VARIES ON-OFF TIME OF TR4 TO PRODUCE AVERAGE VOLTAGE OF 6·7V AFTER FILTERING

CONTROL CIRCUIT (+16V)
VARIES CONDUCTION TIMES OF TR9 AND TR10 TO PRODUCE AN AVERAGE OUTPUT OF +16V AFTER FILTERING

SUPPLY MONITORING CIRCUIT
SUPPLY FAILING GOES LOW IF INPUT VOLTAGE IS LESS THAN 9·5V SUPPLY FAILED GOES LOW IF INPUT VOLTAGE IS LESS THAN 8·6 TO 8·9V.

R24 SET TO GIVE FREE RUNNING FREQUENCY OF ABOUT 50KHz, THIS THEN BECOMES 62·5KHz WHEN SYNC PULSES ARE PRESENT

BUFFER FOR REFERENCE VOLTAGE
HIGH STABILITY REFERENCE COMES FROM ML1 AND BECOMES 2·5V FOR CONTROL AMPLIFIERS IN BOTH REGULATORS.

IF SUPPLY EXCEEDS 40V D12 CONDUCTS TAKING ML3 PIN 10 TO +1·5V TO CLOSE DOWN THE REGULATOR DEVICE

SOFT START CIRCUIT
ALSO INHIBITS PUSH PULL REGULATOR WHEN SUPPLY FAILED IS LOW

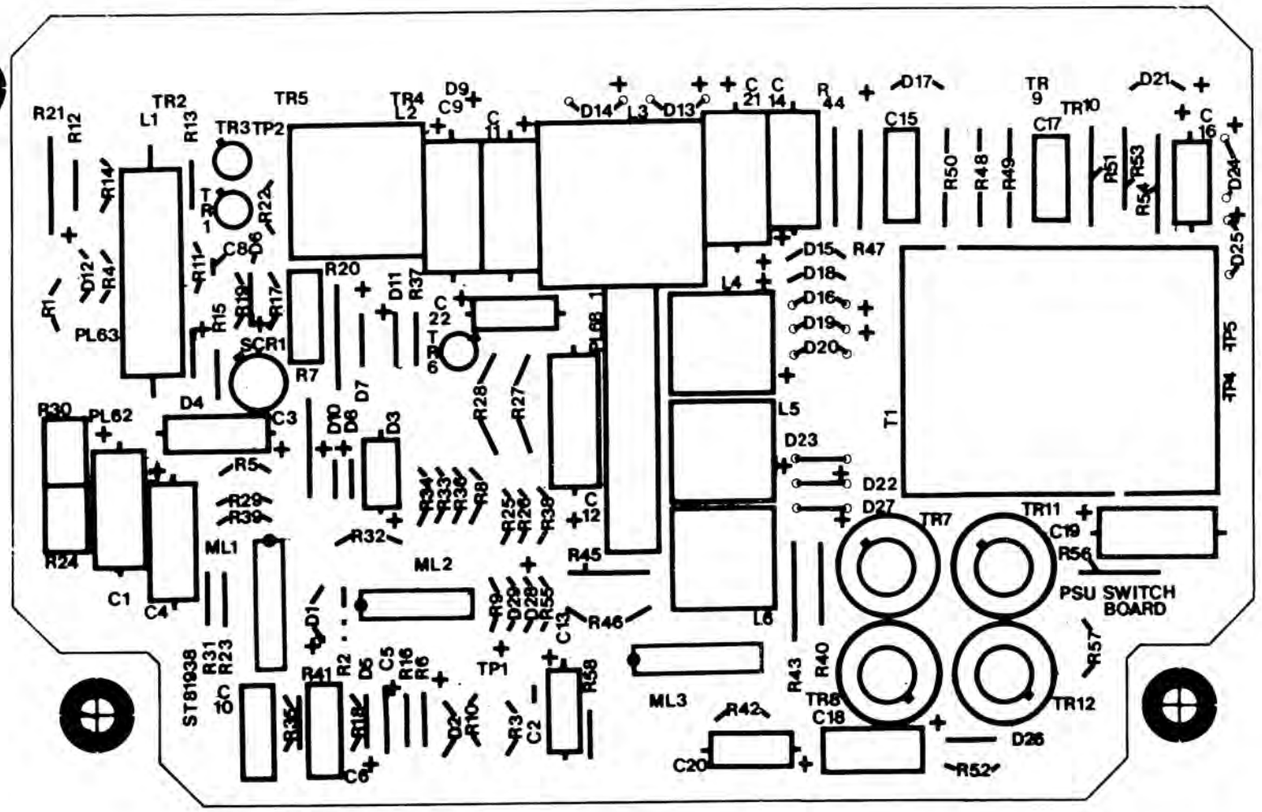
SUPPLY FAILED

SUPPLY FAILING

RACAL
TH2449
L 81937

Circuit:
Switching Regulator Board

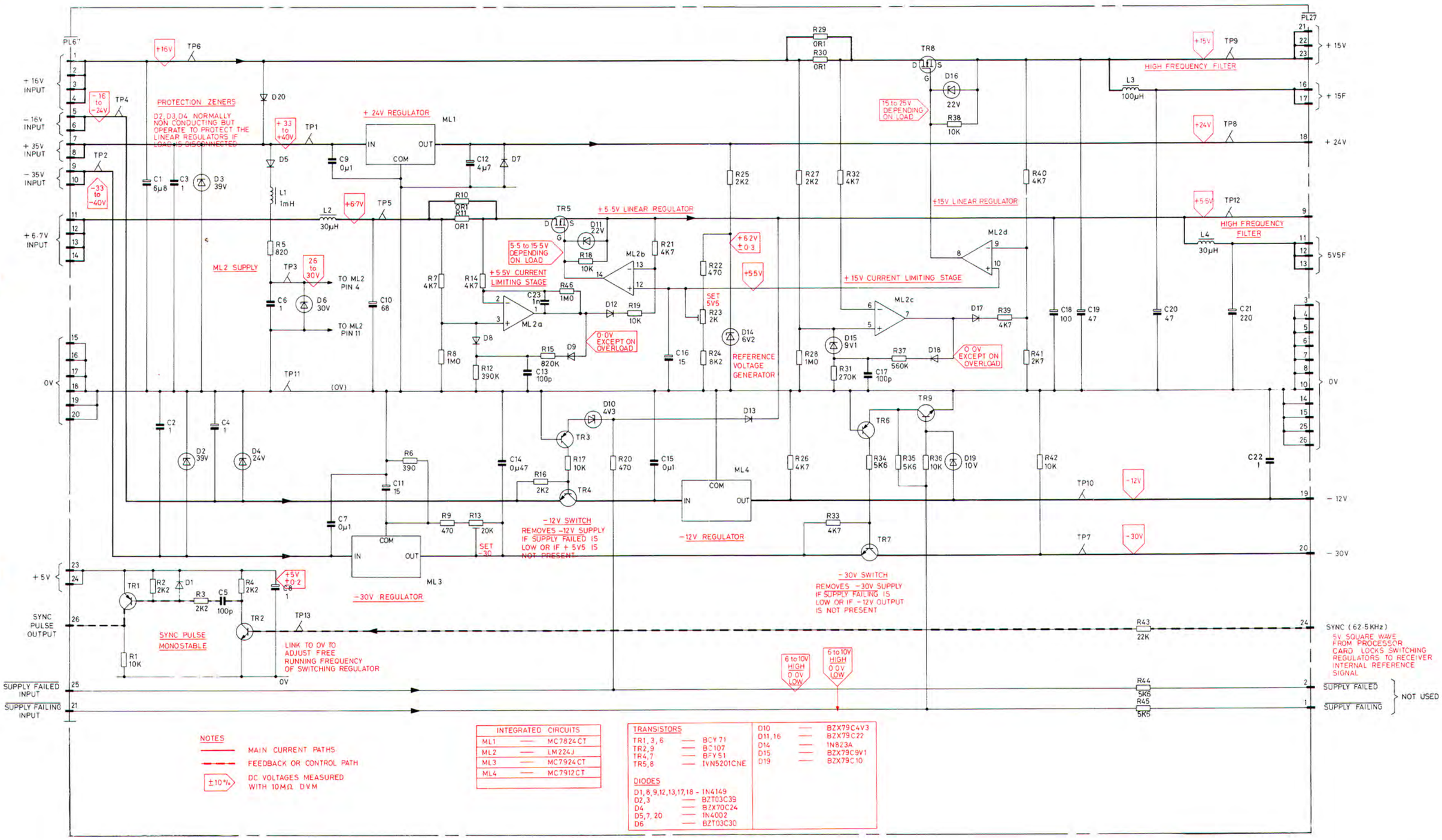
Fig.17.2



RACAL

TH 2449	DE 81938
1 2 3 4 5 6 7 8	

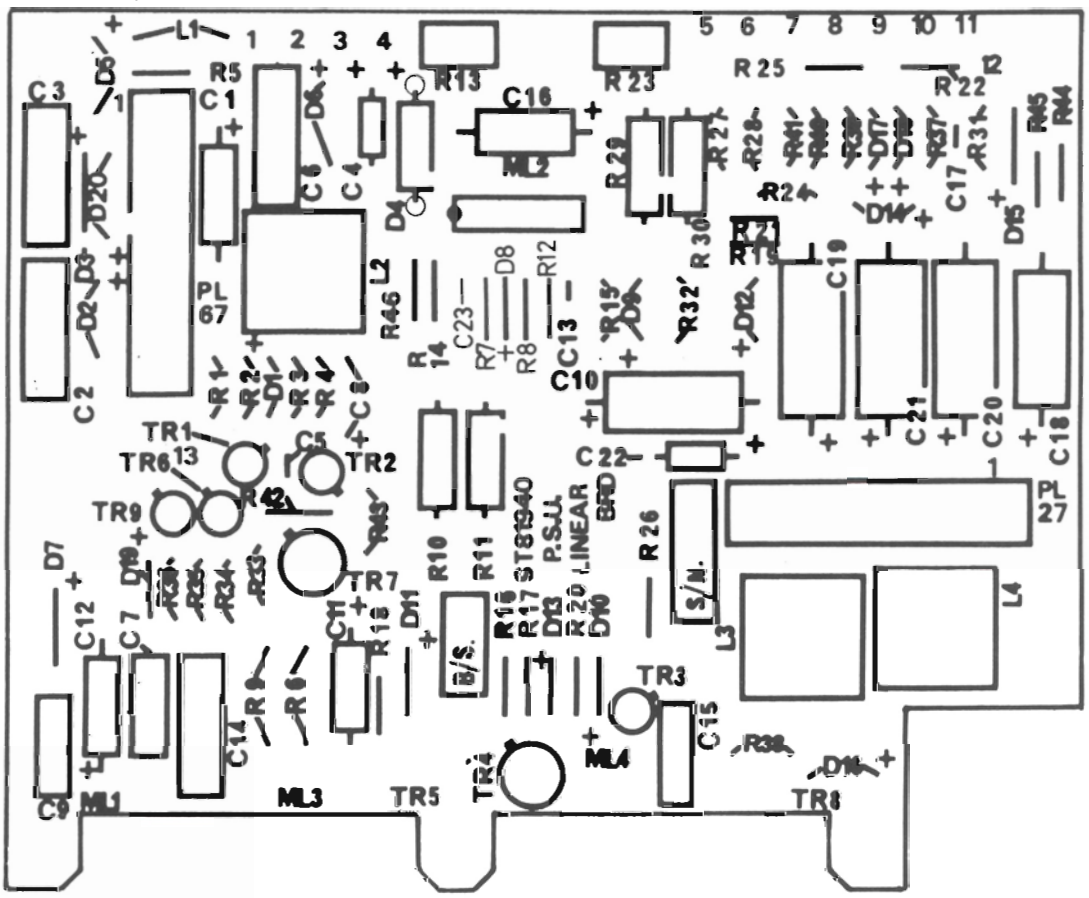
Layout: Switching Regulator Fig.17.3



RACAL
TH2449 DC81940 1 2 3 4 5 6 7 8
TH2449 DC81940 -1 -2

Circuit:
Linear Regulator Board

Fig.17.4



CHAPTER 18

MOTHER BOARD AND INTERCONNECTIONS

CONTENTS

Illustrations

CHAPTER 18

MOTHER BOARD AND INTERCONNECTIONS

INTRODUCTION

1. This chapter brings together the circuit diagrams and other details of the mother board, the interconnection diagram and the extender card. For external connection details, refer to chap. 2.

MOTHER BOARD

2. The mother board (figs. 18.1 and 18.2) houses the printed circuit cards (seven including the extender card and the optional SCORE interface card). Component details are given at the end of the chapter.

INTERCONNECTION DIAGRAM

3. The overall interconnection diagram for the receiver is given in fig. 18.3. Note that chassis-mounted component details are given in chap. 22.

EXTENDER CARD

4. The extender card (fig. 18.4) normally resides in mother board edge connector number 4 (SK54), and in this position it may be used as a convenient monitoring point for a number of signals (fig. 18.1). It may be inserted into any other mother board edge connector to extend the appropriate card for testing or fault location purposes.

SUPPRESSION BOARDS

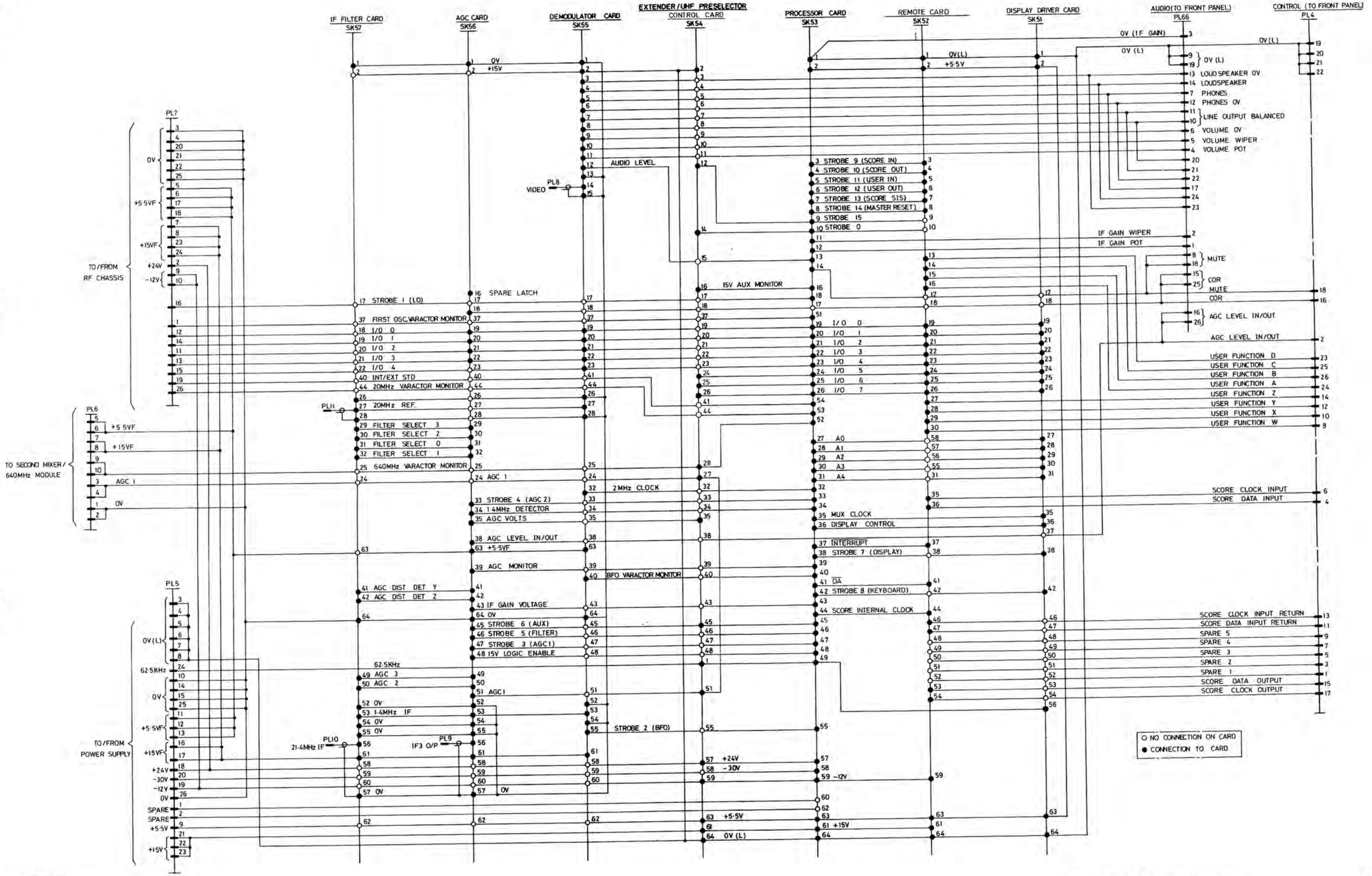
5. Three suppression boards are used to ensure that externally connected signals are free from interference. The positions of these boards within the receiver, are shown in Fig. 18.3. The switch on suppression board B must be in the NORMAL position except when the receiver is used in DF systems in which processed audio is connected to the RA1794 speaker amplifier via the AUDIO 1 connector.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		MOTHER BOARD (ST 83775)			
Connectors					
PL4		Plug, 26-way			938858
PL5		Plug, 26-way			938858
PL6		Plug, 10-way			938859
PL7		Plug, 26-way			938858
PL8		Plug, Coaxial, 50 ohms			938989
PL9		Plug, Coaxial, 50 ohms			938989
PL10		Plug, Coaxial, 50 ohms			938989
PL11		Plug, Coaxial, 50 ohms			938989
PL66		Plug, 26-way			938858
SK51 to SK57		Socket, 64 x 2 way			932937
Sockets					
SK51-SK57		Edge connector, 64-way + 64-way			932937
Miscellaneous					
		Captive fastener			930396
		EXTENDER CARD (ST 79810)			
Connectors					
		Edge Connector, 64-way + 64-way			940274
Miscellaneous					
		Connector Bracket			AD82043
		Test Point			936148

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		SUPPRESSION BOARDS A, B and C			
Resistors					
R1	470 R			2	920758
R2	470 R			2	920758
R3	470 R			2	920758
R4	470 R			2	920758
R5	470 R			2	920758
R6	470 R			2	920758
R7	470 R			2	920758
R8	470 R			2	920758
R9	470 R			2	920758
R10	470 R			2	920758
R11	1KO			2	913489
Capacitors			**Volts**		
C1	10n		50		940356
C2	10n		50		940356
C3	10n		50		940356
C4	10n		50		940356
C5	10n		50		940356
C6	10n		50		940356
C7	10n		50		940356
C8	10n		50		940356
C9	10n		50		940356
C10	10n		50		940356
C11	10n		50		940356
C12	10n		50		940356
C13	10n		50		940356
C14	10n		50		940356
C15	10n		50		940356
C16	10n		50		940356
C17	10n		50		940356
C18	10n		50		940356
C19	10n		50		940356
C20	10n		50		940356
C21	10n		50		940356
C22	10n		50		940356
C23	10n		50		940356
C24	10n		50		940356
C25	10n		50		940356

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C26	10n		50		940356
C27	10n		50		940356
C28	10n		50		940356
C29	10n		50		940356
C30	10n		50		940356
C31	10n		50		940356
C32	10n		50		940356
C33	10n		50		940356
C34	10n		50		940356
C35	470n		50		945600
C36	470n		50		945600
C37	470n		50		945600
C38	470n		50		945600
C39	10n	250	250	+40-20	900067
C40	10n	250	250	+40-20	900067
C41	10n	250	250	+40-20	900067
C42	10n	250	250	+40-20	900067
C43	10n	250	250	+40-20	900067
C44	10n	250	250	+40-20	900067
C45	10n	250	250	+40-20	900067
C46	10n	250	250	+40-20	900067
C47	10n	250	250	+40-20	900067
C48	10n	250	250	+40-20	900067
C49	10n	250	250	+40-20	900067
C50	10n	250	250	+40-20	900067
C51	10n	250	250	+40-20	900067
C52	10n	250	250	+40-20	900067
C53	10n	250	250	+40-20	900067
C54	10n	250	250	+40-20	900067
C55	10n	250	250	+40-20	900067
C56	10n	250	250	+40-20	900067
C57	10n	250	250	+40-20	900067
C58	10n	250	250	+40-20	900067
C59	10n	250	250	+40-20	900067
C60	10n	250	250	+40-20	900067
C61	10n	250	250	+40-20	900067
Inductors					
L1	100µ			10	939161
L2	100µ			10	939161
L3	100µ			10	939161
L4	100µ			10	939161

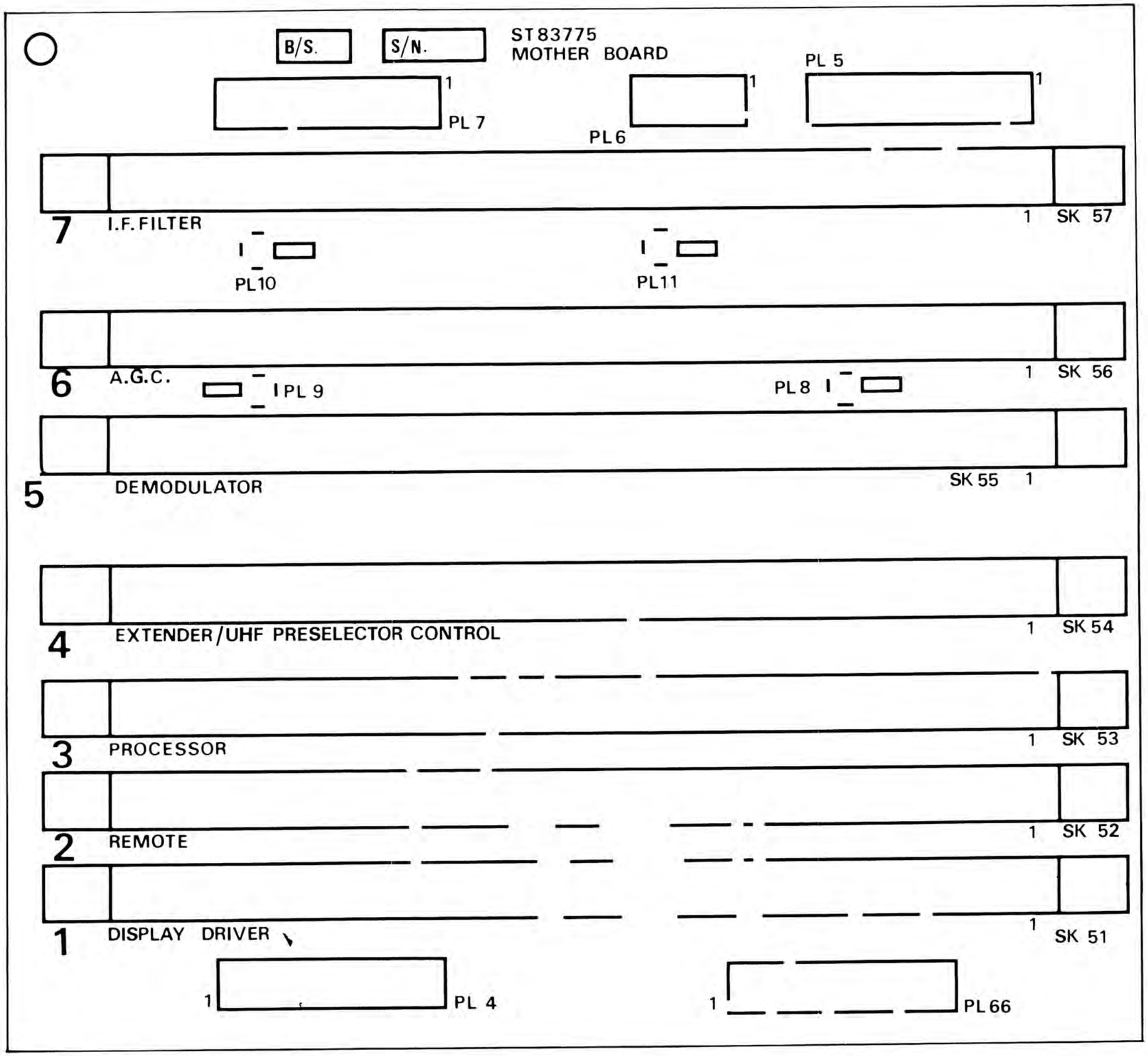
Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Ferrite Beads					
FX1		Mullard FX4003			940358
FX2		Mullard FX4003			940358
FX3		Mullard FX4003			940358
FX4		Mullard FX4003			940358
FX5		Mullard FX4003			940358
FX6		Mullard FX4003			940358
FX7		Mullard FX4003			940358
FX8		Mullard FX4003			940358
FX9		Mullard FX4003			940358
FX10		Mullard FX4003			940358
FX11		Mullard FX4003			940358
FX12		Mullard FX4003			940358
FX13		Mullard FX4003			940358
FX14		Mullard FX4003			940358
FX15		Mullard FX4003			940358
FX16		Mullard FX4003			940358
FX17		Mullard FX4003			940358
FX18		Mullard FX4003			940358
FX19		Mullard FX4003			940358
FX20		Mullard FX4003			940358
FX21		Mullard FX4003			940358
FX22		Mullard FX4003			940358
FX23		Ferrite Core			945809
FX24		Ferrite Core			945809
Miscellaneous					
SW1		Switch 2 pole 2 way			941853
PL1		Plug 4-way			940354
PL78		Plug 26-way			938858
PL79		Plug 26-way			938858
PL80		Plug 16-way			938860
PL81		Plug 20-way			938861
SK42		Socket 10-way			936894
SK43		Socket 10-way			936894
SK73		Socket 26-way			940355
SK80		Cable Assembly			BA83122
SK81		Cable Assembly			BA83123



RACAL
TH2449 OC83775
1 2 3

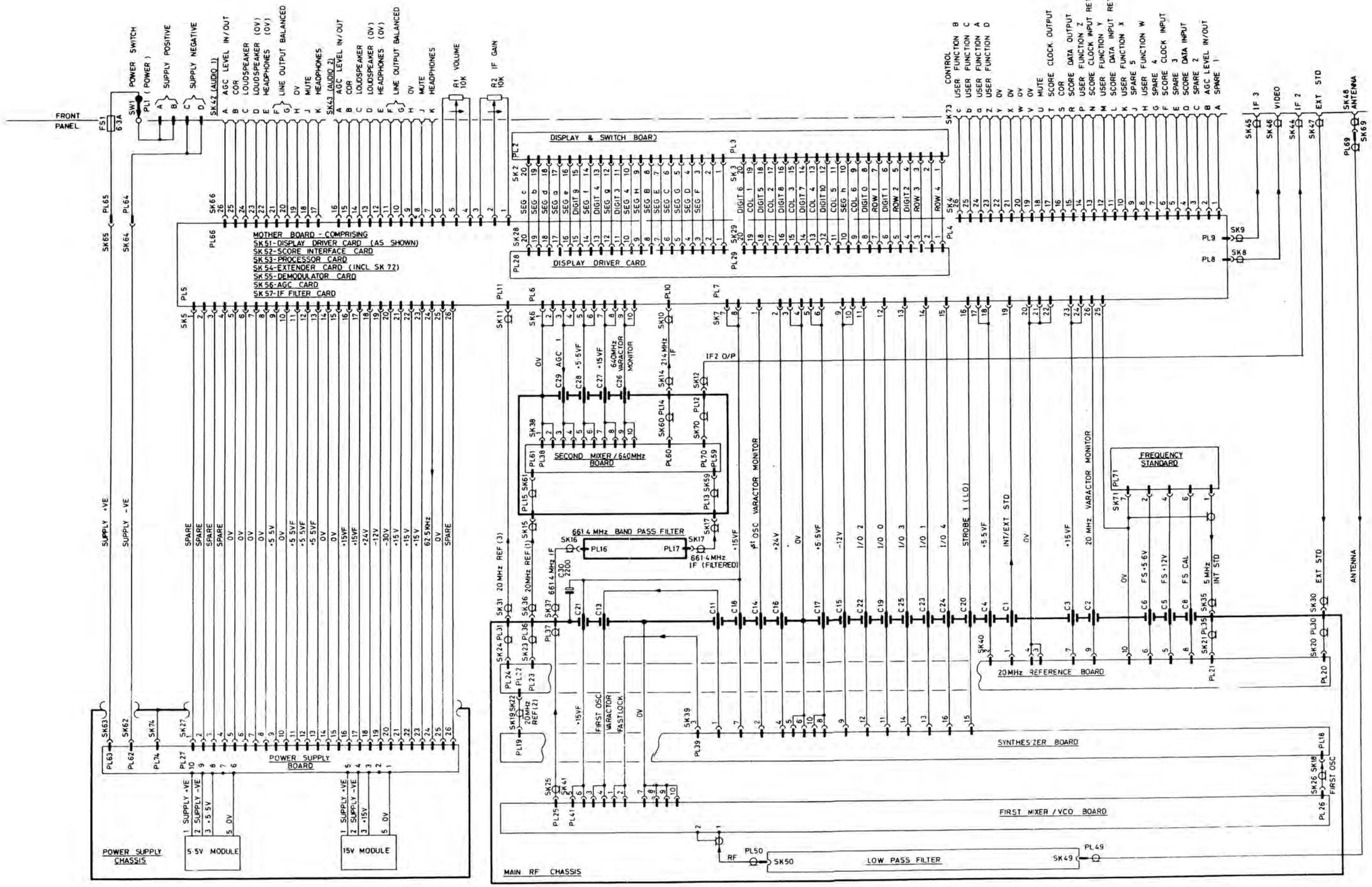
Circuit: Mother Board

Fig. 18.1



Layout: Motherboard

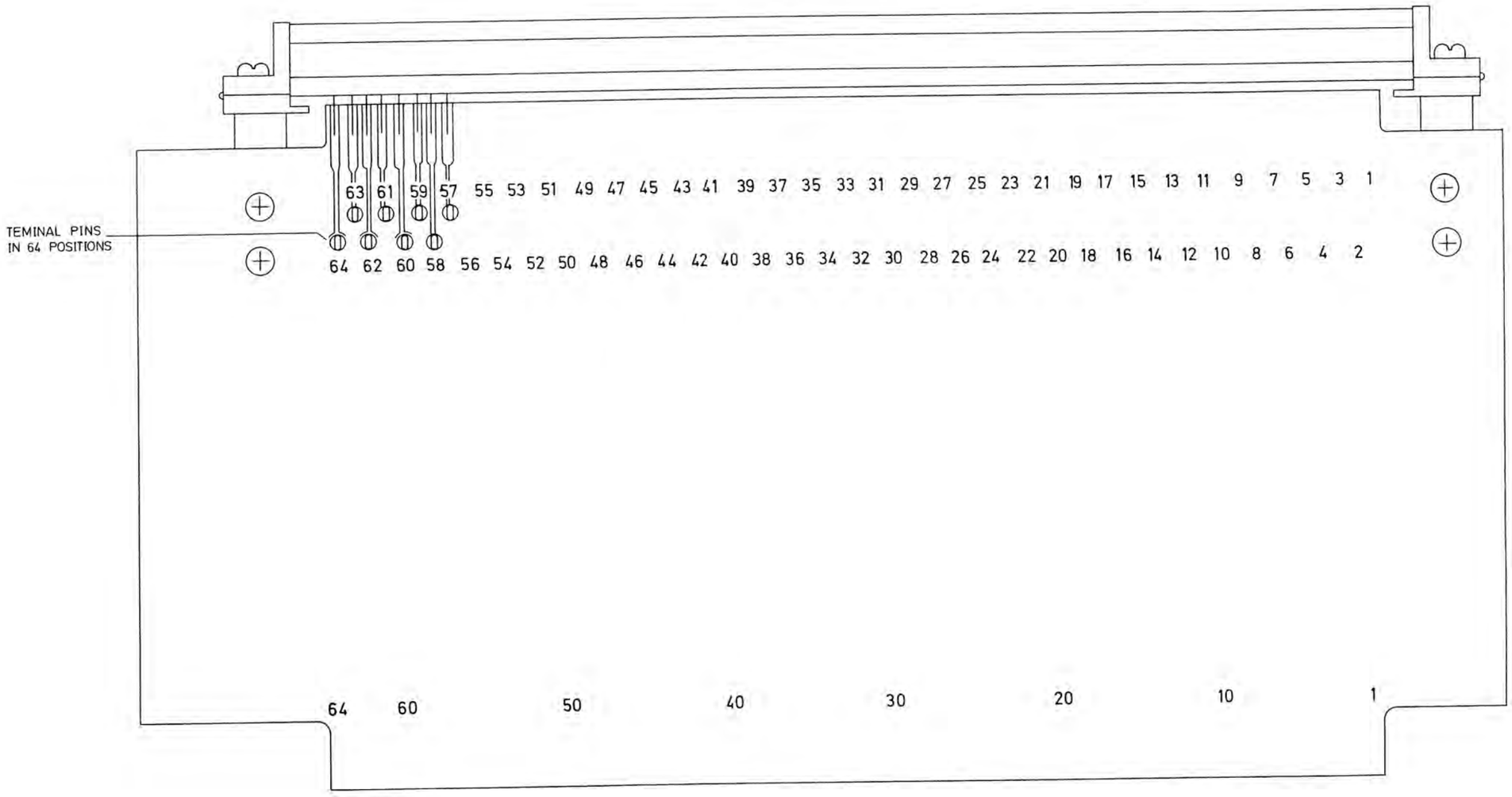
Fig.18.2



RACAL
TH2449 | DC 79540
1

Interconnection Diagram

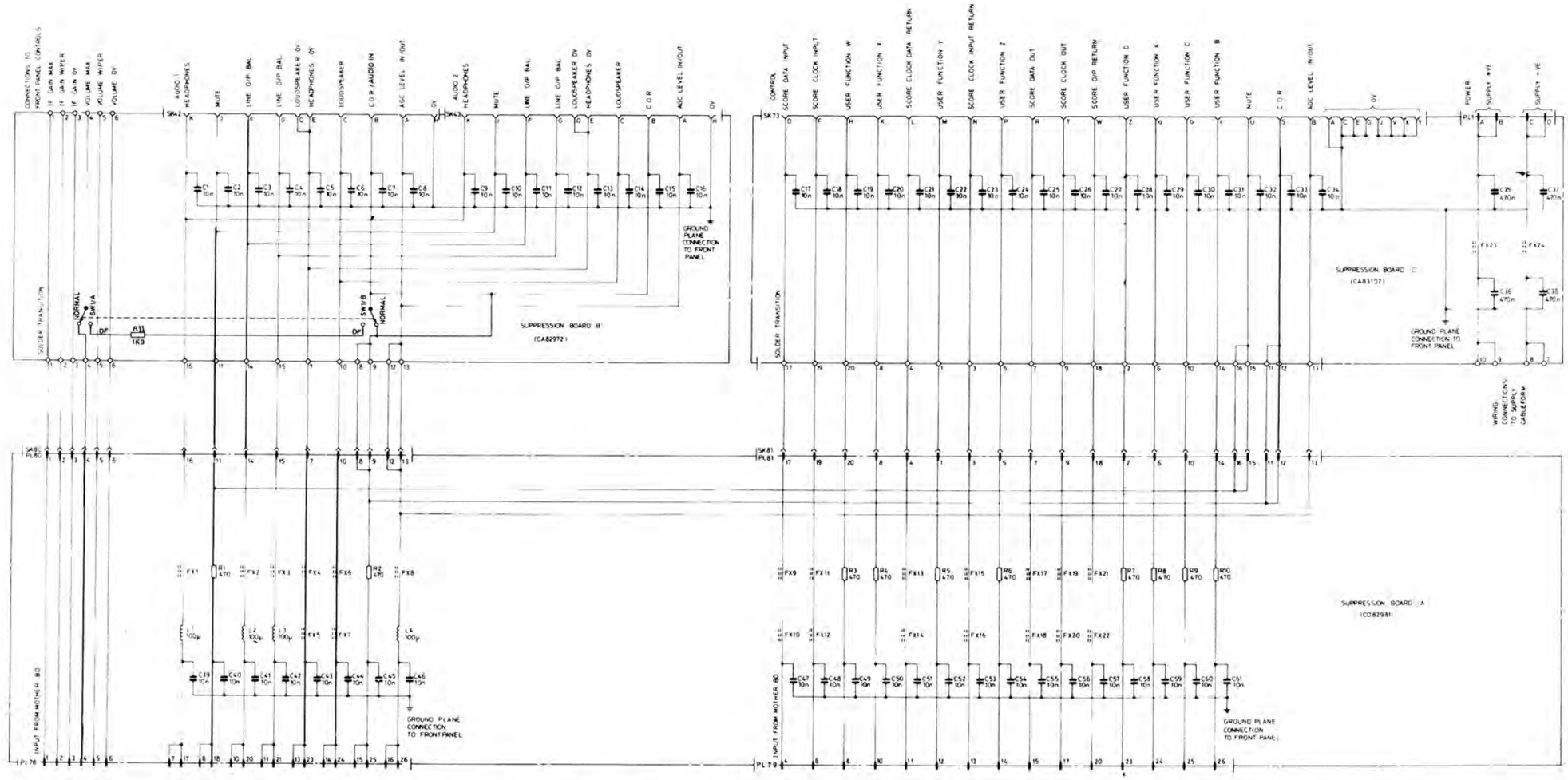
Fig.18.3



RACAL
TH2449 | DE79810
2

Layout : Extender Card

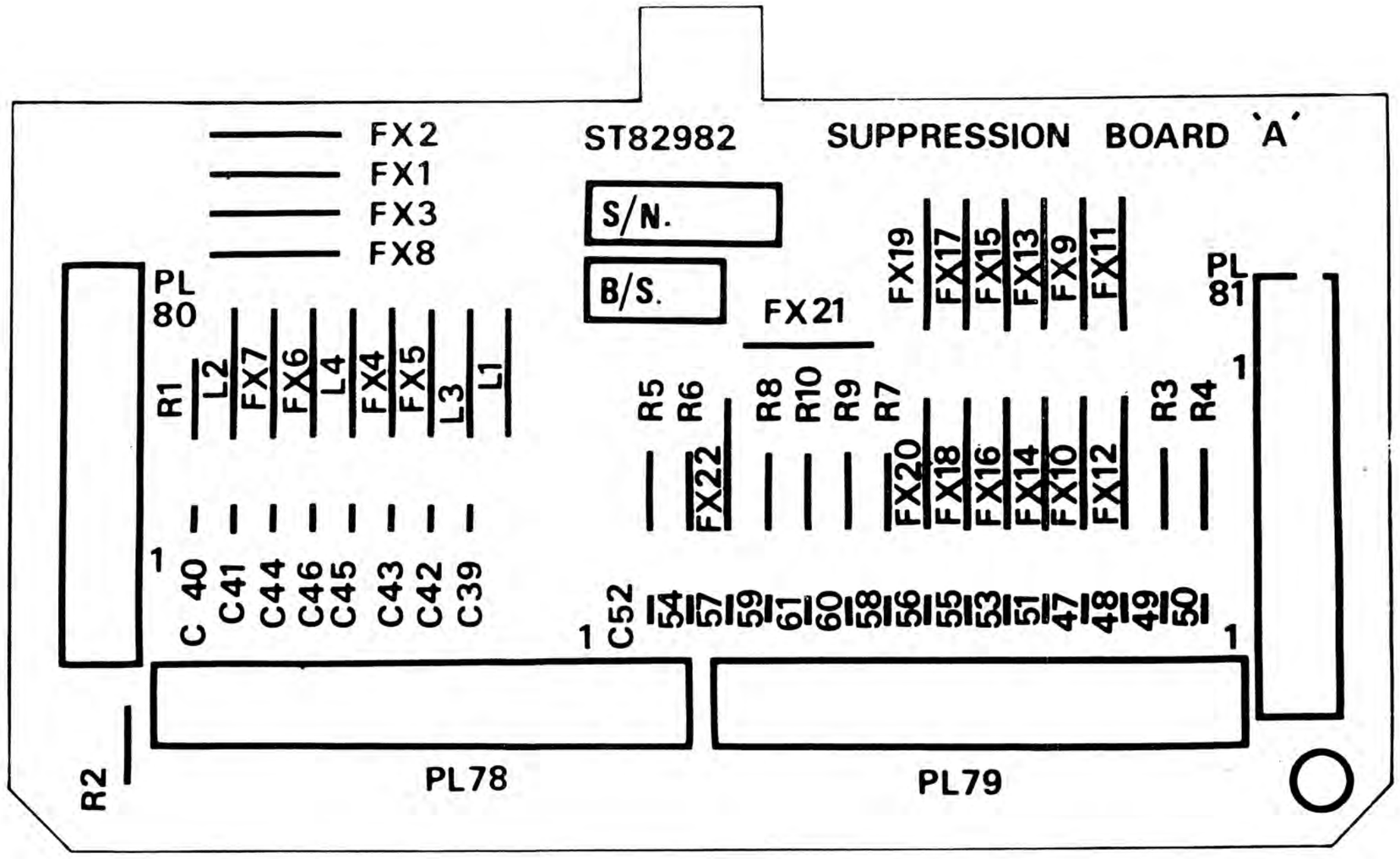
Fig. 18.4



RACAL
TH 2449 DC82982

Circuit:
Combined Suppression Boards

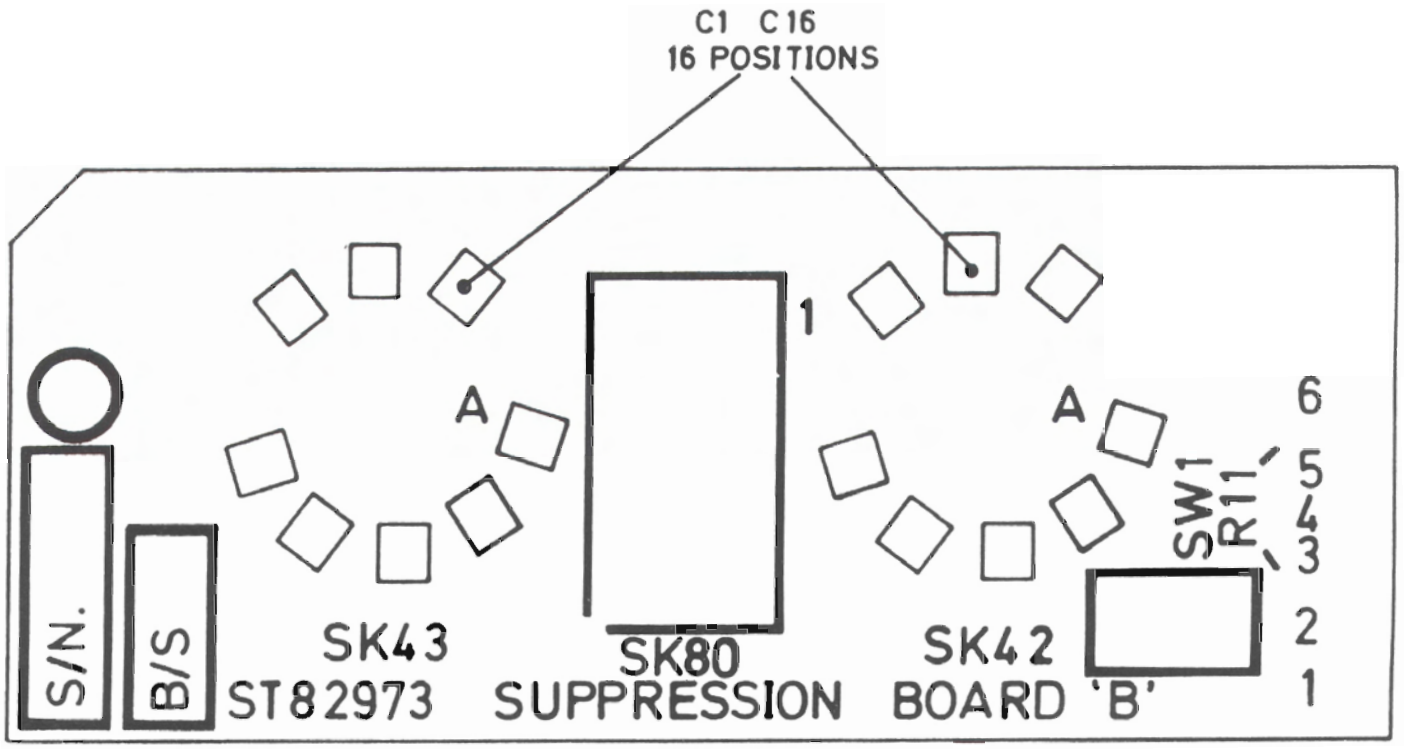
Fig.18.5



RACAL
TH2449 CA82981

Layout:
Suppression Board A

Fig.18.6

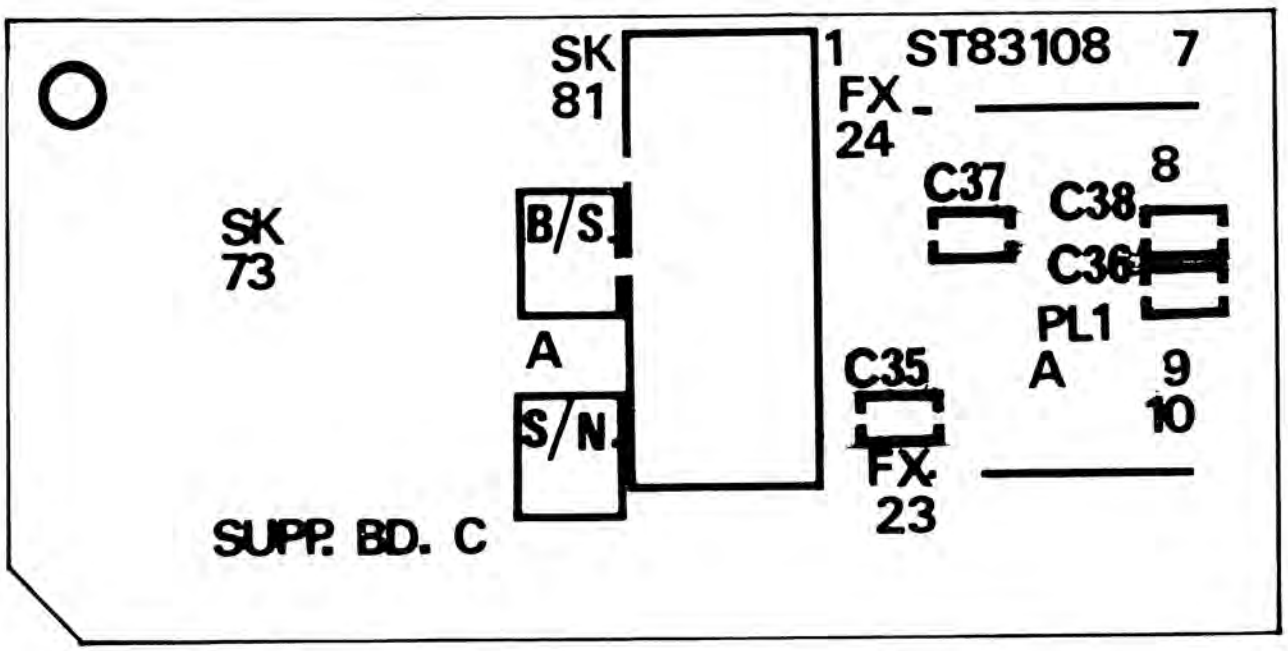


RACAL

TH2449 CA82972
3

Layout : Suppression Board B.

Fig.18.7



TH2449	CA83107
5	

Layout : Suppression Board C Fig.18.8

CHAPTER 19

SELF-TEST ROUTINES

CONTENTS

CHAPTER 19

SELF-TEST ROUTINES

INTRODUCTION

1. The RA 1794 contains a number of built-in test routines (stored in ROM) which may be used as part of a functional test procedure (as detailed in Chapter 20) and also to assist in the location of a fault (Chapter 21). This chapter describes the test routine, provides an interpretation of the test results when a failure is detected, and refers the reader to the associated manual tests given in Chapter 21 to localise a faulty assembly or component. The routines, commonly referred to as BITE (built-in test equipment), are described firstly in the form of a tabulated flow chart, and then each routine is described in detail.

2. To enter the self-test mode, press and hold the MODE key, press the TEST key, and then release both keys together. The front panel display will wipe out then fill up segment by segment.

3. To proceed with the test routine, the CHAN key is pressed and released. Test number 00 should flash in the channel display, and the first and last bars of the meter display should flash to denote that the receiver is in the self-test mode. Now press and release the ENTER key, and routines 00 to 28 are sequenced through automatically (assuming no fault is detected) in approximately forty seconds, finishing with a flashing 28 in the channel display. If a fault is detected, the failed test number is displayed, FAULT is illuminated, and an error code is also displayed.

4. Test 31 is used to test the front-panel keyboard switches, which have to be pressed and released in a specified order.

NOTES: 1. If, during the self-test routine, a fault is detected, the routine is halted at the failed test number. To repeat the failed test, press and release the ENTER key. To proceed with the remaining self-test routines, press and release the UP key followed by the ENTER key.

2. To enter a specific test, press and release the CHAN key followed by the desired test routine number keys, and then press and release the ENTER key.

3. To exit from the self-test routine, press and hold the MODE key, press the TEST key and then release both keys together. If the exit is not achieved, set the front panel POWER switch to OFF and then back to ON.

FLOWCHART

5. The following flowchart refers the reader (when a fault is detected) to the appropriate manual tests contained in Chapter 21. The number of the manual test, preceded by the letter M, is the same as the failed self-test routine number, for further details see para: 6 to 19.

SELF-TEST ROUTINE FLOWCHART

STEP 1	Press and hold the MODE key, press the TEST key, and release both keys together. Is the front panel display test running correctly, i.e. all displays extinguished and then each segment illuminated and extinguished in sequence?
Action:	YES: Step 2 NO: Test M00/a
STEP 2	Press and release the CHAN key. Is a flashing test number 00 displayed together with flashing first and last bars of meter display?
Action:	YES: Step 3 NO: Test M00/a
STEP 3	Press and release the ENTER key. Wait approximately forty seconds. Is a flashing test number 28 displayed?
Action:	YES: Step 4 NO: Step 6
STEP 4	Press and release the CHAN key followed by keys '3', '1' and 'ENTER'. Is 00 indicated in the least significant frequency display?
Action:	YES: Step 5 NO: Test M29
STEP 5	Press and release, in turn, the front panel keys, in the order left-to-right and top-to-bottom. Does the displayed number increment by one after each key press (when the last (CHAN) key is pressed, the displayed number 23 is blanked, and test number 31 again flashes to denote that the procedure may be repeated)?
Action:	YES: Seccessful completion of test routine NO: Test M13

STEP 6	Is test number 00 displayed together with FAULT and a fault code (10Hz frequency display)?	
Action:	YES:	Test M00 - ROM check sum incorrect
	NO:	Step 7
STEP 7	Is test number 01 displayed together with FAULT and a fault code?	
Action:	YES:	Test M01 - RAM failure
	NO:	Step 8
STEP 8	Is test number 02 displayed together with FAULT and a fault code?	
Action:	YES:	Test M02 - +5V supply failure
	NO:	Step 9
STEP 9	Is test number 03 displayed together with FAULT and a fault code?	
Action:	YES:	Test M03 - -12V supply failure
	NO:	Step 10
STEP 10	Is test number 04 displayed together with FAULT and a fault code?	
Action:	YES:	Test M04 - -30V supply failure
	NO:	Step 11
STEP 11	Is test number 05 displayed together with FAULT and a fault code?	
Action:	YES:	Test M05 - +15V supply failure
	NO:	Step 12
STEP 12	Is test number 06 displayed together with FAULT and a fault code?	
Action:	YES:	Test M06 - +24V supply failure
	NO:	Step 13
STEP 13	Is test number 07 displayed together with FAULT and a fault code?	
Action:	YES:	Test M07 - EAROM fault
	NO:	Step 14

STEP 14	Is test number 08 displayed together with FAULT and a fault code?	
Action:	YES:	Test M08 - Channel contents fault
	NO:	Step 15
STEP 15	Is test number 10 displayed together with FAULT and a fault code?	
Action:	YES:	Test M10 - 20 MHz oscillator fault
	NO:	Step 16
STEP 16	Is test number 11 displayed together with FAULT and a fault code?	
Action:	YES:	Test M11 - 640 MHz oscillator fault
	NO:	Step 17
STEP 17	Is test number 12 displayed together with FAULT and a fault code?	
Action:	YES:	Test M12 - 1st Local oscillator fault
	NO:	Step 18
STEP 18	Is test number 13 displayed together with FAULT and a fault code?	
Action:	YES:	Test M13 - BFO oscillator fault
	NO:	Step 19
STEP 19	Is test number 14 displayed together with FAULT and a fault code?	
Action:	YES:	Test M14 - 1st Local Oscillator sweep test fault.
	NO:	Step 20
STEP 20	Is test number 15 displayed together with FAULT and a fault code?	
Action:	YES:	Test M15 - 1.4 MHz AGC Detector fault.
	NO:	Step 21
STEP 21	Is test number 16 displayed together with FAULT and a fault code?	
Action:	YES:	Test M16 - AGC Monitor Fault
	NO:	Step 22

STEP 22	Is test number 17 displayed together with FAULT and a fault code?
Action:	YES: Test M17 - Audio Detector Fault NO: Step 23

STEP 23	Is test number 18 displayed together with FAULT and a fault code?
Action:	YES: Test M18 - BFO/Local Oscillator fault

SELF-TEST ROUTINE DESCRIPTION

Routine 00 - ROM Check Sum

6. This routine performs a check sum calculation for each of the two read only memory (ROM) devices fitted to the processor card (PD1 and PD2). Each byte stored in ROM is transferred, in turn, to a CPU register where its numeric value is added to that of the next byte, to arrive at a total figure for that particular ROM. This figure is then compared with the correct figure (stored in ROM), and if a difference is detected, FAULT is displayed together with the PD number (1 or 2) of the faulty ROM device. The interpretation of the fault code is as follows:

1 = PD1 failed
2 = PD2 failed

Routine 01 - RAM Test

7. This routine clears the RAM on the processor card (256 x 4-bit devices ML4 and ML5), writes FF, in turn, to each byte, checking that the remaining locations remain cleared, then 'walks' a '1' through each location followed by a '0' through each location. If the test fails, FAULT is illuminated, and a code of 1 or 2 is indicated in the 10Hz frequency display. The interpretation of the fault code is as follows:

1 = ML4 failed

2 = ML5 failed

Routine 02 to 06 - Supply Voltage Levels

8. These routines monitor the levels of the +5V, -12V, -30V, +15V and +24V regulated supplies (in that order), to check that they are within approximately plus or minus 10% of nominal. If a supply voltage is found to be out-of-range, the respective routine number is displayed together with FAULT and either H or L to signify too high or too low respectively.

Routine 7 - EAROM Test

9. Test routine 7 fully tests one otherwise unused byte in the upper EAROM device ML3. If the test fails, test number 7 is displayed together with FAULT and numeral 1 in the 10 Hz frequency display.

Routine 8 - Channel Contents

10. Test routine 8 indicates number of first channel with incorrect data. It assumes that there is something stored in all 100 channels.

11. Routine 9 - Blank.

Routine 10 - 20MHz Varactor Line

12. Test routine 10 checks that the 20MHz reference oscillator varactor line voltage is within the prescribed limits. If the varactor voltage level is out-of-range, test number 10 is displayed together with FAULT and either H (level too high) or L (level too low).

Routine 11 - 640MHz Varactor Line

13. This routine checks the level of the 640 MHz oscillator varactor line voltage. If the voltage level is out-of-range, test number 11 is displayed together with FAULT and either H (level too high) or L (level too low).

Routine 12 - Local Oscillator Varactor Line

14. Routine 12 checks that the level of the first local oscillator varactor voltage is within the prescribed limits. If the level is out-of-range, test number 12 is displayed together with FAULT and either H (level too high) or L (level too low). (Measured with existing RX Settings).

Routine 13 - BFO Varactor Line

15. This routine checks the level of the BFO varactor line voltage. If the voltage level is out-of-range, test number 13 is displayed together with FAULT and either H (level too high) or L (level too low). (Measured with existing RX Settings).

Routine 14 - Local Oscillator Sweep Test

16. This routine checks the level of varactor volts when the 1st local oscillator is swept. If the voltage is out of range test number 14 is displayed together with FAULT and numerals 01-05 in the 10 Hz frequency display. These codes denote the following:

01 = out of lock low varactor volts.
02 = out of lock high varactor volts.
03 = Non monotonic
04 = Step in varactor volts too large
05 = varactor volts did not change.

Routine 15 - 1.4 MHz AGC Detector

17. Routine 15 checks the output level of the detector at 1.4 MHz when the local oscillator is tuned to the first IF. If the test fails, test number 15 is displayed together with FAULT and either H (level too high) or L (level too low).

Routine 16 AGC Monitor

18. This routine checks the AGC voltage when the local oscillator is tuned to the first IF. If the test fails, test number 16 is displayed with FAULT and either H (level too high) or L (level too low).

Routine 17 - Audio Detector

19. This routine checks the Audio Detector output when the local oscillator is tuned to the first IF and a BFO signal tuned to 1 kHz. If the level is out of range test number 17 is displayed together with FAULT and either H (level too high) or L (level too low).

Routine 18 - BFO Beat against First Local Oscillator

20. This routine starts with the receiver and BFO both tuned to zero and checks for the absence of an audio signal. The BFO frequency is stepped and an audio signal is detected, followed by an equal step in LO frequency and the absence of an audio signal. If the test fails test number 18 is displayed together with FAULT. The LO and BFO frequencies are displayed in their respective displays.

21. Routines 19 to 28 Blank

Routine 29 Audio Test

22. This routine sets a 1 kHz, audio tone equivalent to normal CW output when the local oscillator is tuned to the first IF. This test is used for setting the line output level. (Press ENTER to enable).

Routine 30 Program Identify

23. Routine 30 displays the program number and issue (As printed on PD1 and PD2). (Press ENTER to enable).

Routine 31 Keyboard Test

24. This routine requires the operator to press the keys one at a time in order from left to right and top to bottom i.e. starting with 'DOWN' and finishing with 'CHAN'. The displayed number should increment by 1 for each button, going from 00 to 23 (Press ENTER to enable).

25. Routines 32 to 98 Blank

Routine 99 Manual

26. Routine 99 enables manual gain and manual AGC TC selection after exit from BITE.

ADDITIONAL TEST ROUTINES

27. Three further test programs are provided and are selectable by the setting of switches SA to SF located on the processor card, as follows:

SF	SE	SD	SC	SB	SA	ROUTINE
O	O	O	O	O	O	Normal Operating Program
O	O	O	O	O	C	Processor Card Test
O	O	O	O	C	O	Hardware Signature Analysis
O	O	O	C	O	C	Software Signature Analysis

O denotes Open, C denotes Closed

Processor Card Test Routine

28. This test routine is confined to the processor card; it tests the CPU, ROM and RAM devices and then illuminates the LED on the processor card on the successful completion of the routine. The test takes approximately five seconds to complete and is started by setting the POWER switch to OFF, closing switch SA and then returning the POWER switch to ON. The routine may be re-run simply by setting the POWER switch to OFF and then back to ON.

Hardware Signature Analysis

29. The closure of switch SB on the processor card initiates a DMA-OUT sequence where data is read out of ROM at the address contained in CPU internal register R(0). R(0) is then incremented and the process continues for as long as switch SB remains closed. Thus a repetitive data pattern is presented and this is used for signature analysis testing of the processor card.

Software Signature Analysis

30. The closure of switches SA and SC (prior to the closure of the POWER switch) causes the operation of a comprehensive signature analysis routine for the testing of various circuits within the receiver. Details of these tests are given in Chapter 21.

CHAPTER 20

FUNCTIONAL TEST & ALIGNMENT

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Tables

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CHAPTER 20

FUNCTIONAL TEST & ALIGNMENT

INTRODUCTION

1. This chapter contains a detailed test procedure to check the performance of the receiver. The tests may be carried out as part of a routine maintenance schedule or as an aid to fault location. The remainder of the chapter contains the receiver alignment procedure.

NOTE: It is assumed that the receiver is fitted with an internal frequency standard. If this is not the case, then a suitable external frequency standard must be connected to the EXT STD socket.

TEST EQUIPMENT

2. The items of test equipment listed below are required for the following procedures.

(1) Synthesized Signal Generator.

Frequency Range: 1 to 512 MHz
Modulation: AM and FM

Example: Adret 7100B

(2) Audio millivoltmeter
Example: Racal-Dana Instruments 9300

(3) UHF Frequency Counter

Example: Racal-Dana Instruments 9921

(4) Digital Multimeter

Example: Racal-Dana Instruments 4002

(5) CA617 Serial Data Test Set - SCORE versions only

(Racal Communications Ltd)

(6) Audio Signal Generator - SCORE versions only

Example: Racal-Dana Instruments 9083

(7) Oscilloscope, Dual Trace

Example: Tektronix 465 or Hewlett Packard 1740A

(8) RF Millivoltmeter

Example: Racal-Dana Instruments 9301A

(9) Spectrum Analyser/Tracking Generator, 100KHz - 110MHz

Example: Hewlett packard HP141T/8443A/8553B/8552B

(10) High Impedance probe

Example: Hewlett Packard HP1121A

(11) Test lead 1 (fig. 20 (a)) comprising:

Plug, 10-way, Amphenol 62GB-16J-12-10P (Racal 926474)
Terminal block, 10-way
Connecting cable

(12) Test lead 2 (fig. 20 (b)) comprising:

Plug, 26-way, Amphenol 62GB-16J-16-26P (Racal 9XXXXX)
Plug, 25-way, Cannon DB25P (Racal 928311)
Junction, shell, Cannon DB 51212-1 (Racal 918108)
Retainer, Cannon, DB51221-1 (Racal 914245)
Plug, coaxial, BNC (Racal 900038)
Terminal block, 12-way
Connecting cables

TEST LEADS

3. Make up test leads 1 and 2, as shown in figs. 20 (a) and 20 (b). These test leads provide convenient points for monitoring purposes and for the connection of test equipment. Note that the 25-way connector, the BNC connector and the user function connections to TB2 may be omitted from test lead 2 where the optional SCORE interface card is not fitted.

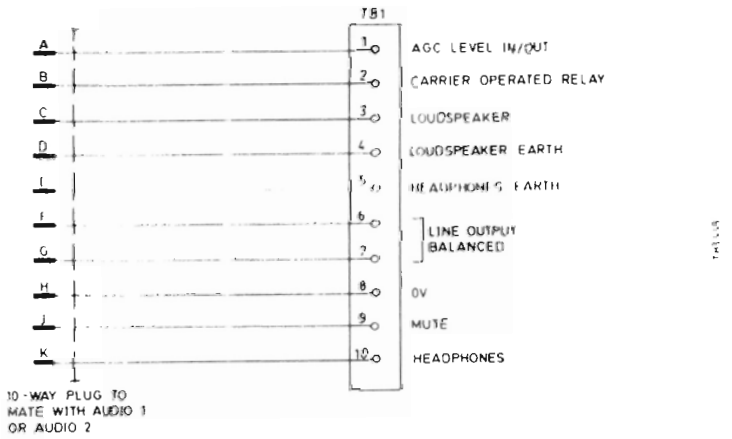

Fig. 20(a) Test Lead 1

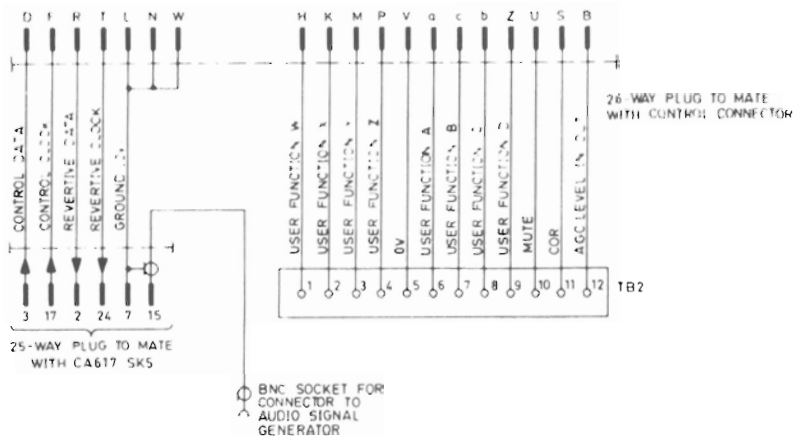

Fig. 20(b) Test Lead 2

PRELIMINARY

4. (1) Place the receiver on a flat, clean working surface.

(2) Connect the receiver POWER plug to a suitable source of DC power (18 V to 36 V).

(3) Connect test lead 1 to one of the AUDIO sockets on the receiver front panel.

(4) Set the POWER switch to ON.

(5) Set the receiver as follows:

Frequency:	111.11111 MHz
Mode	AM
Bandwidth	8 KHz

(6) Wait for 90 seconds

(7) Within a period of 45 seconds, set the receiver as follows:

Frequency	222.22222 MHz
Mode	CW
Bandwidth	1.2 KHz
BFO	2.22 KHz
POWER switch	OFF

(8) Wait for 60 seconds and then set the POWER switch to ON. Check that the receiver settings are as follows:

Frequency	222.22222 MHz
Mode	CW
Bandwidth	1.2 KHz
BFO	2.22 KHz

FRONT PANEL CONTROLS

(1) Press and release the REM Key. Check that REM is displayed on the front panel.

(2) Press and release the REM Key again and check that the REM indicator is extinguished.

(3) Press and release the FREQ Key. Check that a flashing channel display = = occurs, that the frequency display is set to zero, and that a - prompt signal appears at the 100 MHz digit position.

(4) Press, in turn, keys 1, 2, 3, 4, 5, 6, 7 and 8. Check that after each key is pressed, the - prompt signal moves progressively to the right and the digit is displayed (when the 8 key is pressed, the prompt should disappear).

(5) Press and release the ENTER key. Check that the flashing = = channel display is extinguished.

(6) Press and release the TUNE key. Press and hold the UP key and check that the displayed frequency increases. Release the UP key.

(7) Press and hold the DOWN key and check that the displayed frequency decreases. Release the DOWN key.

(8) Press and release the STEP key. Press and release the numeral 1 key.

(9) Press and hold the UP key and check that the displayed frequency increases in 9 KHz increments. Release the UP key.

(10) Press and hold the DOWN key and check that the displayed frequency decreases in 9 KHz increments.

(11) Repeat steps (8), (9) and (10) for the step sizes tabulated below by pressing STEP followed by the appropriate numeric key.

Numeric Key	Step Size
1	9 KHz
2	6.25 KHz
3	12.5 KHz
4	25 KHZ
5	50 KHz

(12) Press and release the MODE key. Press and release the CW key and check that CW and BFO are displayed.

(13) Press and release, in turn, the AM, FM, USB and LSB keys. Check that the appropriate mode is displayed and that the BFO indicator is extinguished.

(14) Press and release the SQLCH key and check that SQLCH is displayed. Press and release the SQLCH key again and check that the SQLCH indicator is extinguished.

(15) Press and hold the MODE key, press the TEST key, and then release both keys together. Check that the receiver enters the self test mode (the display is first blanked, each segment, in turn, is then displayed until all are displayed, and then each segment, in turn is extinguished). To exit from the self-test mode, press and hold the MODE key, press the TEST key, and then release both keys together.

(16) Press and release the MODE button, followed by the AM button. Check that AM is displayed.

(17) Press and release the BW+ key a number of times to select and display the available bandwidth filters. Press and release the BW- key a number of times and check that all the available bandwidths are displayed. The standard filter bandwidths are as follows:

0.3 KHz
1.2 KHz
3.0 KHz
8.0 KHz
15 KHz
30 KHz
300 KHz

(18) Select the CW mode. Press and release the BFO key. Press and hold in turn, the UP key and the DOWN key. Check that the BFO frequency increments and decrements respectively. Ensure that the BFO frequency does not exceed plus or minus 7.79 KHz.

(19) Press and release the CHAN key. Check that the channel display-only mode is entered, denoted by a flashing channel number display.

(20) Press twice the numberal 8 key and check that channel number 88 is displayed.

(21) Press and hold the UP key and check that the displayed channel number increases. Release the UP key.

(22) Press and hold the DOWN key and check that the displayed channel number decreases. Release the DOWN key.

(23) Press and release the FREQ key. Press and release, in turn, keys 1, 2, 3, 4, 5, 6, 7 and 8, and then the ENTER key. Check that a frequency of 123.45678 MHz is displayed.

(24) Press and release the FREQ key. Press and release, in turn, keys 2, 3, 4, 5, 6, 7, 8 and 9. DO NOT press the ENTER key. Check that a frequency of 234.56789 MHz is displayed.

(25) Press and release the RCL key and check that a frequency of 123.45678 MHz is displayed.

(26) Press and hold the MODE key, press the TEST key, and then release both keys together to set the receiver to the self-test mode.

(27) Press and release the CHAN key and then select channel number 99 (press the numeral 9 key twice).

(28) Press and hold the MODE key, press the TEST key, and then release both keys together (to exit from the self-test mode with manual selection of AGC time constant enabled).

(29) Press and release the MODE key.

(30) Press, in turn, numeral keys 7, 8 and 9 and check that the appropriate AGC time constant indication is displayed, as below.

KEY	AGC	DISPLAY
7	SHORT	5
8	MEDIUM	n
9	LONG	L

(31) Press and release the SQLCH key and check that SQLCH is displayed, together with a . adjacent to the displayed AGC time constant character (denoting manual gain control with AGC).

(32) Load channels 00 to 09 with the following receiver settings (to load a channel, set the receiver to display the required settings, press and hold the STORE key, press the requied channel number digits i.e. 00, 01 etc, and then release the STORE key).

CHANNEL	FREQUENCY (MHz)	MODE	BW	BFO	AGC
00	000.00000	LSB	3 KHz	-	L
01	111.11111	USB	3 KHz	-	L
02	222.22222	AM	0.3 KHz	-	S
03	333.33333	CW	1.2 KHz	+3.33	L
04	444.44444	FM	8 KHz	-	S + SQLCH
05	055.55555	FM	15 KHz	-	S + SQLCH
06	066.66666	CW	30 KHz	+6.66	L
07	077.77777	CW	300 KHz	+1.23	L
08	088.88888	CW	3 KHz	-7.23	L
09	099.99999	CW	3 KHz	+7.79	L

(33) Press and release the CHAN key.

(34) Enter channel number 00 and then press and release the ENTER key. Check that the correct receiver settings are displayed.

(35) Press the UP key and check that the correct receiver settings are displayed for channels 01 to 09.

SELF-TEST ROUTINE

6. (1) Press and hold the MODE key, press the TEST key, and then release both keys together to enter the self-test mode.

(2) The front panel displays are all extinguished and then each segment is illuminated and extinguished, in sequence. One complete cycle takes approximately 15 seconds.

(3) Press and release the CHAN key. Test number 00 should flash in the channel display, and the first and last bars of the meter display should flash to denote that the receiver is in the self-test mode.

(4) Press and release the ENTER key. Self-test routines 00 to 29 are automatically sequenced through (assuming no fault is detected) test routines 29, 30 and 31 require the ENTER key to be depressed enabling the tests to continue, in approximately 40 seconds, finishing with a flashing 99 in the channel display. If a fault is detected, the failed test number is displayed, FAULT is illuminated, and an error code is also displayed. For a full description of the self-test routines, and the interpretation of the error codes, refer to Chapter 19.

(5) Repeat sub para. (3). Press and release the ENTER key. Test routine number 29 flashes to denote that operator intervention is required. Press and release the ENTER key twice and check that 00 is indicated in the least sifnificant frequency display. Then press and release, in turn, the front panel keys, in the order left to right and top to bottom, and check that the displayed number increments by one after each key press. When the last (ENTER) key is pressed, the displayed number 23 is blanked, and test routine number 29 again flashes to denote that the procedure may be repeated.

NOTES: 1. If, during the self-test routine, a fault is detected, the routine is halted at the failed test number. To repeat the failed test, press and release the ENTER key. To proceed with the remaining self-test routine, press and release the UP key followed by the ENTER key.

2. To enter a specific test, press and release the CHAN key followed by the desired test routine number keys, and then press and release the ENTER key.

3. To exit from the self-test routine, press and hold the MODE key, press the TEST key, and then release both keys together. If the exit is not achieved, set the front panel POWER switch to OFF and then back to ON.

(6) Press and release the CHAN key and select channel 99. Press and hold the MODE key, press the TEST key, and then release both keys together (to exit from the self-test routine with manual selection to AGC time constant enabled).

BFO CHECK

7. (1) Connect the digital frequency meter to the VIDEO socket on the receiver front panel.

(2) Select the CW mode, a 300 kHz bandwidth, and short AGC.

(3) Set the receiver and BFO frequencies as below and check that the correct receiver output frequency is obtained (plus or minus 1 Hz).

FREQUENCY		
RECEIVER (MHz)	BFO (kHz)	OUTPUT (kHz)
000.00000	+1.23	1.230
000.00000	+7.79	7.790
000.00000	-7.79	7.790
000.00100	+0.01	1.010

SENSITIVITY CHECK

8. (1) Connect the CW output of the signal generator, set to a frequency of 48.15 MHz and an output level of 0dBμV e.m.f., to the receiver antenna socket.

(2) Connect the audio millivoltmeter between to TB1 of test lead 1, pins 6 and 7 (balanced audio line output).

(3) Set the receiver to a frequency of 48.15 MHz, CW mode, 0.8 kHz BFO frequency, 0.3 kHz bandwidth and manual IF gain only (SQLCH selected, long, medium or short not selected). Set the IF GAIN control fully clockwise.

(4) Tune the signal generator to the receiver (where necessary) for a maximum indication on the audio millivoltmeter.

(5) Check that the audio millivoltmeter indicates -13dBm plus or minus 6dB. Record the level.

(6) Select, in turn, each bandwidth filter fitted and check that for all bandwidths except 300 kHz the audio line output level is within plus or minus 2dB of the level recorded at step (5). With the 300 kHz filter selected, check that the level is within plus and minus 6dB of the recorded level.

(7) Set the receiver bandwidth to 3 kHz and record the audio line output level.

(8) Increase the signal generator frequency by 1 MHz and check that the audio line output level reduces by at least 13dB.

(9) Repeat steps (7) and (8) for the following receiver and signal generator settings.

FREQUENCY (MHz)		
RECEIVER	SIGNAL GENERATOR	MODE
2.15	2.15	CW
511.999	511.999	CW
48.15	48.1485	LSB
48.15	48.1515	USB

(10) Set the signal generator to a frequency of 48.15 MHz, with 1 kHz 70% amplitude modulation, output level +10dBμV e.m.f.

(11) Set the receiver frequency to 48.15 MHz, AM mode, 8 kHz bandwidth and short AGC.

(12) Note the audio line output level as indicated on the audio millivoltmeter.

(13) Set the signal generator to CW and check that the audio line output level reduces by not less than 13dB.

(14) Set the signal generator for FM modulation at 1 kHz, 4 kHz deviation.

(15) Set the receiver to the FM mode, bandwidth to 15 kHz, and note the audio line output level.

(16) Set the signal generator to CW and check that the audio line output level reduces by not less than 13dB.

(17) Set the signal generator for FM modulation at 1 kHz, 11 kHz deviation.

(18) Set the receiver bandwidth to 30 kHz and note the audio line output level.

(19) Set the signal generator to CW and check that the audio line output level reduces by not less than 13dB.

(20) Set the signal generator for FM modulation at 1 kHz, 30 kHz deviation. Increase the signal generator output level to +20dBµV e.m.f.

(21) Set the receiver bandwidth to 300 kHz and note the audio line output level.

(22) Set the signal generator to CW and check that the audio line output level reduces by not less than 10dB.

(23) Set the signal generator output level to 0dBµV, CW.

(24) Set the receiver to the CW mode, 1.2 kHz bandwidth, manual IF gain only, BFO frequency 0.3 kHz and IF GAIN to maximum. Note the audio line output level.

(25) Increase the signal generator frequency by 1 MHz and check that the audio line output level reduces by not less than 16dB. Reset the signal generator frequency to 48.15 MHz.

(26) Set the receiver bandwidth the 0.3 kHz and note the audio line output level.

(27) Increase the signal generator frequency by 1 MHz and check that the audio line output level reduces by not less than 18dB.

SIGNAL-PLUS-NOISE TO NOISE RATIO

9. (1) Connect the signal generator, set to the frequency of 48.15000 MHz and a CW output level of 0dBμV e.m.f., to the receiver antenna socket.

(2) Connect the audio millivoltmeter to TB1 of test lead 1, pins 6 and 7 (balanced audio line output).

(3) Set the receiver to a frequency of 48.15000 MHz, CW mode, 1.70 kHz BFO frequency, 3 kHz bandwidth, manual only IF gain, and IF GAIN control fully clockwise.

(4) Check that the audio millivoltmeter indicates -13dB plus or minus 6dB. Record the level obtained.

(5) Increase the signal generator frequency by 1 MHz and record the level indicated on the audio millivoltmeter. Check that the difference between this level and that recorded at step (4) is within the range 13 to 23dB.

(6) Repeat steps (3), (4) and (5) with the signal generator and receiver set to the frequencies given in the following table. Check that the signal plus-noise to noise ratio figures obtained are as given.

FREQUENCY (MHz)	S+N: N RATIO (dB)	
	MIN	MAX
48.15000	13	23
100.15000	13	23
200.15000	13	23
350.15000	13	23
511.99990	13	23
10.15000	13	23
5.15000	13	23
3.15000	13	23
2.15000	11	23
1.15000	9	23

MANUAL GAIN AND AGC

10. (1) Connect the audio millivoltmeter to TB1 of test lead 1, pins 6 and 7 (balanced audio line output).

(2) Connect the digital voltmeter to TB1 of test lead 1, pins 1 (AGC IN/OUT) and 8 (0V).

(3) Connect the signal generator, set to a frequency of 48.15000 MHz and a CW output level of 0dBμV e.m.f., to the receiver antenna socket.

(4) Set the receiver frequency to 48.15000 MHz, CW mode, 0.80 kHz BFO frequency 3 kHz bandwidth, manual only gain control, and set the IF GAIN control fully clockwise.

(5) Note the level indicated on the audio millivoltmeter, which should be -13dBm plus or minus 6dB.

(6) Check that the digital voltmeter indication is between 9.7V and 10.7V DC.

(7) Increase the signal generator output level in 10dB steps up to a level of +110dBµV e.m.f. Check that at each step the digital voltmeter reading is within the range tabulated below, and that the increase in the audio line output level does not exceed 2dB.

ANTENNA INPUT LEVEL (dBµV emf)	AGC LEVEL (VOLTS) MIN	MAX
0	9.7	10.8
+ 10	9.3	10.5
+ 20	8.3	9.8
+ 30	7.0	8.5
+ 40	6.0	7.5
+ 50	5.3	6.8
+ 60	5.0	6.5
+ 70	4.5	6.0
+ 80	4.0	5.5
+ 90	3.5	5.0
+100	3.0	4.5
+110	1.5	3.5

(8) At the receiver select the AM mode, 8 kHz bandwidth and SHORT AGC.

(9) Set the signal generator, tuned to a frequency of 48.15000 MHz, for 30% amplitude modulation at 1 kHz. Set the output level to +2dBµV e.m.f.

(10) Check that the audio line output level is -13dBm plus or minus 2dB, and that the AGC voltage is between 9.7V and 10.7V DC.

(11) Increase the signal generator output level to +112dBµV e.m.f. and check that the increase in the audio output level is not greater than 2dB.

(12) Reduce the signal generator output level to +80dBµV e.m.f. Disconnect and then reconnect the signal generator. Check that the AGC response time is just perceptible for both attack and decay time.

(13) At the receiver, select MEDIUM AGC. Disconnect and then reconnect the signal generator. Check that the AGC decay time is perceptible with no hang time and that the attack time is instantaneous.

(14) At the receiver, select LONG AGC. Disconnect and then reconnect the signal generator. Check that the AGC decay time is approximately five seconds with no hang time, and that the attack time is instantaneous.

(15) Set the signal generator for a CW output, and set the receiver to the CW mode, SHORT AGC.

(16) Disconnect and then reconnect the signal generator. Check that after a short hang time the AGC decay is instantaneous and that the attack time is also instantaneous.

(17) At the receiver, select MEDIUM AGC. Disconnect and then reconnect the signal generator. Check that the AGC decay time is perceptible after a two second hang time and that the attack time is instantaneous.

(18) At the receiver, select LONG AGC. Disconnect and then reconnect the signal generator. Check that the decay time is approximately six seconds after a two second hang time, and that the attack time is instantaneous.

(19) Disconnect the signal generator. Set the IF GAIN control fully counter-clockwise. Select LONG AGC with MANUAL (SQLCH) and check that the meter indicates full-scale deflection.

(20) Reselect manual IF gain (press SQLCH) and check that the meter indication instantly falls to minimum. Reconnect the signal generator.

(21) Set the signal generator output level to 0dBμV e.m.f.

(22) At the receiver, select manual only IF gain control and set the IF GAIN control fully clockwise.

(23) Ensure that the audio line output level is -13dBm plus or minus 2dB.

(24) Slowly rotate the IF GAIN control counter-clockwise to minimum whilst increasing the signal generator output level to maintain the audio line output level. Check that the IF GAIN control operates smoothly throughout the range.

(25) Check that, with the IF GAIN control fully counter-clockwise, the signal generator output level required to obtain an audio line output level of -13dBm plus or minus 2dB is not less than +110dBμV e.m.f.

SCORE INTERFACE TESTS

11. (1) Connect the 26-way plug of test lead 2 to the CONTROL connector on the receiver front panel, and the 25-way plug to SK5 on the CA617. Connect the BNC socket to the audio signal generator, set to a frequency of approximately 4800Hz and an output level of approximately 5V peak-to-peak.

NOTE: The CA617 internally generated clock signal runs at 19.2 kHz. Since this is too high for satisfactory operation of the RA 1794A, an externally produced master clock signal must be provided for application to the CA617. This external clock signal (i.e. the 4800Hz output from the audio signal generator) automatically overrides the internally generated clock signal.

(2) Ensure that the receiver is not set to remote control (REM indicator not illuminated). If it is, press and release the REM key.

(3) Set the receiver as follows:

Frequency	0.00000 MHz
Mode:	AM and SQLCH
Bandwidth:	8kHz
AGC	Short (key 7)
IF GAIN	Fully clockwise
POWER	ON

(4) Set the CA617 controls as follows:

SINGLE FRAMES	UP (Off)
ADDRESS WORD SEND	UP (Off)
Remaining ADDRESS WORD switches not applicable	
RETURN MONITOR	UP (Off)
CONTROL INHIBIT	UP (Off)
TRANSMIT	UP (Off)
Forward Data Send X	UP (Off)
Forward Data Send Y	UP (Off)
Forward Data Send Z	UP (Off)
SUPPLY	ON

(5) At the CA617, set the REVERTIVE DATA WORD switch, in turn, to all sixteen positions (0 to F) and check that the RECENT DATA lamp illuminates only for word numbers 0, 1, 2 and 4. Ensure that the TX lamp is off and that the RX lamp is on.

(6) At the CA617, set the REVERTIVE DATA WORD switch to 0 and ensure that the revertive data display is as follows:

X	X	1	0	0	0	6	0	0
8	7	6	5	4	3	2	1	0

X denotes any number

(7) Whilst observing digit 1 of the revertive data display on the CA617, momentarily connect pin 5 (OV) of TB2 (connected to test lead 2), in turn, to pins 6, 7, 8 and 9 of TB2 (user functions A, B, C and D). Check that the CA617 indicates 1, 2, 4 and 8 respectively.

(8) Set the CA617 REVERTIVE DATA WORD switch to 1 and ensure that the revertive data display is as follows:

0	0	0	0	0	0	0	0	0
8	7	6	5	4	3	2	1	0

(9) At the receiver set the frequency to 123.45678 MHz and ensure that the CA617 revertive data display is as follows:

1	2	3	4	5	6	7	8	0
8	7	6	5	4	3	2	1	0

(10) Set the receiver to a frequency of 234.56789 MHz and ensure that the CA617 revertive data display is as follows:

2	3	4	5	6	7	8	9	0
8	7	6	5	4	3	2	1	0

(11) Set the CA617 REVERTIVE DATA WORD switch to 2 and ensure that the revertive data display is as follows:

X	X	X	X	X	0	0	0	0
8	7	6	5	4	3	2	1	0

X denotes any number

(12) Rotate the receiver IF GAIN control and check that digits 4 to 8 of the revertive data displayed on the CA617 change.

(13) Set the CA617 REVERTIVE DATA WORD switch to 4 and ensure that the revertive data display is as follows:

X	3	0	2	1	8	1	0	0
8	7	6	5	4	3	2	1	0

(14) Whilst observing digit 6 of the revertive data display, press and release the ENTER key. Ensure that the display changes to 1 and then reverts to 0.

(15) At the receiver, select the USB mode, long AGC time constant (9 key), and no squelch. Ensure that the CA617 revertive data display is as follows:

X	0	C	2	0	0	1	0	0
8	7	6	5	4	3	2	1	0

(15) At the CA617 set the X, Y and Z FORWARD DATA switches as follows:

	8	7	6	5	4	3	2	1	WORD
X	3	4	5	6	7	8	9	0	1
Y	0	0	0	0	0	0	0	0	2
Z	0	0	8	1	2	8	1	0	4

(16) At the receiver, press and release the REM key and ensure that REM is illuminated.

(17) At the CA617, set the X SEND switch to on (down) and ensure that the receiver frequency display changes to 345.67890 MHz.

(18) Set the CA617 REVERTIVE DATA WORD switch to 1 and ensure that the revertive data display is as follows:

3	4	5	6	7	8	9	0	0
8	7	6	5	4	3	2	1	0

(19) Set the CA617 SINGLE FRAMES switch to on (down) and set the X FORWARD DATA switches as follows:

8	7	6	5	4	3	2	1	WORD
4	5	6	7	8	9	0	1	1

(20) Whilst observing the receiver frequency display, press and release the CA617 SEND FRAME pushbutton and ensure that the receiver frequency display does not change.

(21) Press and release the CA617 SEND FRAME pushbutton again and ensure that the receiver frequency display changes to 456.78901 MHz.

(22) Set the CA617 X, Y and Z SEND switches to ON, and the SINGLE FRAMES switch to off.

(23) Ensure that the receiver is set to a frequency of 456.78901 MHz, with CW mode, 0.3 kHz bandwidth, short AGC and 0.00 kHz BFO frequency.

(24) Set the CA617 FORWARD DATA switches as follows:

8	7	6	5	4	3	2	1	WORD
0	0	0	0	0	1	2	3	2

(25) Ensure that the receiver BFO frequency is set to 1.23 kHz.

(26) At the CA617, set digit 7 of the Z word forward data, in turn, to 0, 1, 2, 3, 4, 5 and 6. Ensure that the receiver bandwidth (BW) display indicates 0.3, 1.2, 3.0, 8.0, 15.0, 30 and 300 kHz respectively.

(27) Switch off and disconnect all test equipment.

ALIGNMENT PROCEDURES

12. Under normal operating conditions the receiver will maintain the factory alignment over a long period of time. Re-alignment should therefore only be carried out following the replacement of an assembly or components which affect the alignment, or where a known mis-alignment exists.

13. Should it be necessary to re-align the complete receiver, the following procedures should be carried out in the order given. Before attempting to re-align an individual assembly, it must be ascertained, where applicable, that the preceding assemblies are functioning correctly. If the specified performance cannot be attained by re-alignment, then a fault must be suspected and reference should be made to Chapter 21.

14. A limited amount of dismantling is necessary to gain access to certain areas of the receiver. Details for dismantling and reassembly are given in Chapter 4. After alignment ensure that all dismantled assemblies are correctly reassembled and that all screening covers are replaced using all the screws provided.

15. The required trimming tools are provided with each receiver; these are included in a linen bag which is attached to the receiver at the factory prior to despatch.

POWER SUPPLY MODULE

16. The power supply module contains two printed circuit boards, the linear board and the switching regulator board. Supplies to the receiver can be monitored on pins TP1 to TP12 using the digital multimeter (DMM) the voltages are with respect to TP11 (0 V).

TP1	+33 V to 40 V
TP2	-33 V to -40V
TP3	26 V to 31 V
TP4	-15 V to -24 V
TP5	+6.7 V nominal
TP6	+16.0 V nominal
TP7	-30 V ±0.2 V (set by R13 on the linear board)
TP8	+24 V (±1.2 V)
TP9	+15 V (±0.25 V)
TP10	-12 V (±0.6 V)
TP12	+5.5 V ±0.05 V (set by R23 on the linear board)

17. To adjust R13 and R23 take the following action.

(1) Unscrew the four captive screws securing the power supply module to the rear of the receiver.

(2) Carefully withdraw the power supply module, taking care to maintain the connections to PL27 and to the supply lug connectors.

(3) Connect the DMM to TP7 (-) and TP11 (0 V) adjust R13 for a reading of -30 V ±0.2 V.

(4) Transfer the DMM to TP12 (+) and TP11 (0 V) adjust R23 for a reading of +5.5 V ±0.05 V.

(5) Disconnect the DMM and assemble the power supply module to the receiver.

20 MHz REFERENCE BOARD

18. Apart from preset resistor R51, which is the fine-tune control for the type 9420 frequency standard module (if fitted - see para. 30), there are no adjustable components on the 20 MHz reference board. The correct functioning of the 20 MHz reference board should however, be ascertained, as follows, before proceeding with the alignment procedures.

19. (1) Position the unit underside up and remove the cover from the 20 MHz reference board compartment (fig. 4.2).

(2) If the receiver is not fitted with an internal frequency standard, ensure that a suitable external reference source is connected to the EXT STD socket on the front panel.

(3) Remove the coaxial socket connected to PL22 on the 20 MHz reference board and connect PL22 to the RF milivoltmeter. Ensure that the RF millivoltmeter indicates between 0 and -3dBm.

(4) Disconnect the RF millivoltmeter and connect in its place the frequency counter. Check that the frequency counter indicates 20 000 000 Hz plus or minus 1 Hz.

(5) Disconnect the frequency counter and replace the coaxial socket removed from PL22.

(6) Repeat steps (3) to (5) for the 20 MHz output signals from connectors PL23 and PL24 on the 20 MHz reference board.

(7) Replace the screening cover to the board compartment.

PROCESSOR CARD

20. (1) Set the receiver POWER switch to OFF.

(2) Remove the extender card from mother board slot 4, and the processor card from mother board slot 3. Insert the extender card into mother board slot 3, mount the processor card onto the extender card and carry out the following adjustments.

(3) Ensure that the processor card self test switches are all in the OFF position.

(4) Connect the oscilloscope probe to TP6 on the processor card. Rotate R14 on the processor card until the level on TP6 goes 'low', then back off slightly until the level on TP6 <u>just</u> goes 'high'. Disconnect oscilloscope probe.

(5) Set the receiver to AGC 'SQUELCH OFF'. Press MODE and TEST keys and measure TP7 with a DMM set to the 10 V range. Adjust R8 for a reading of 2.70 volts ±0.02 volts.

(6) Set the receiver POWER switch to OFF, remove the extender card, return the processor card to mother board slot 3, and return the POWER switch to ON.

DISPLAY DRIVER CARD

21. The display driver card contains a single preset control to set the brillance level of the front panel LED displays. For optimum display brillance, this control (R6) should be set to near-maximum i.e. fully clockwise.

SYNTHESIZER BOARD

22. (1) With the receiver positioned underside up, remove the covers from the synthesizer board and first mixer/VCO board compartments (fig. 4.2.).

(2) Connect the oscilloscope probe to TP6 on the synthesizer board and ensure that a trace having an amplitude of 1.5 volts plus or minus 0.2 volts peak-to-peak and a pulse repetition rate of 1 MHz is displayed.

(3) Transfer the oscilloscope probe to TP7 on the synthesizer board and ensure that a trace having an amplitude of 1.5 volts plus or minus 0.2 volt peak-to-peak and a pulse repetition rate of 1 MHz is displayed.

(4) Transfer the oscilloscope probe to TP10 on the synthesizer board. Adjust R51 for a ramp amplitude of 0.35V plus or minus 0.05 V peak-to-peak.

(5) Adjust R36 for minimum displayed AC component. Disconnect the oscilloscope probe from TP10.

FIRST MIXER/VCO BOARD

23. (1) Disconnect coaxial socket SK17 from PL17 on the 661.4 MHz bandpass filter (attached to the second mixer/640 MHz module - fig. 4.3.).

(2) Connect the RF millivoltmeter to PL17 on the 661.4 MHz bandpass filter.

(3) Connect the signal generator, set to a frequency of 500 MHz and a CW output level of 10 mV p.d., to the receiver ANTENNA socket.

(4) Set the receiver to a frequency of 500.00000 MHz, and tune the signal generator for a maximum indication on the RF millivoltmeter.

(5) Adjust C19 on the first mixer/VCO board for a maximum indication on the RF millivoltmeter. Ensure that the RF millivoltmeter indication is not less than -3dB relative to 10mV.

(6) Disconnect the signal generator and the RF millivoltmeter.

(7) Reconnect the coaxial socket to PL17 removed at step (1).

SECOND MIXER/640 MHz MODULE

24. The second mixer/640 MHz board and the 661.4 MHz bandpass filter are dealt with as a complete assembly.

IMPORTANT NOTE

THE 661.4 MHz FILTER IS SUPPLIED AS A FULLY PRE-ALIGNED UNIT. DO NOT, UNDER ANY CIRCUMSTANCES, ADJUST THE SCREWS ON THE TOP OF THIS BANDPASS FILTER.

Adjustment of C35

25. (1) Connect the digital multimeter, set to the 20V d.c. range, between TP4 and OV on the second mixer/640 MHz board, and adjust, if necessary, C35 for a reading of 5.5V.

(2) Disconnect the digital multimeter.

661.4 MHz IF Amplifier Adjustment

26. (1) Connect the signal generator, set to a frequency of 15 MHz and a CW output level of 10 mV p.d., to the receiver ANTENNA socket.

(2) Connect the RF millivoltmeter to the IF2 socket on the receiver front panel.

(3) Set the receiver to a frequency of 15.00000 MHz. Disable the AGC to the 661.4 MHz amplifiler by temporarily removing ML6 (CA 3406) on the AGC card.

(4) Adjust capacitors C9, C17 and C20 on the second mixer/640 MHz board repeatedly for a maximum indication on the RF millivoltmeter.

(5) Ensure that the RF millivoltmeter indicates 10 mV plus or minus 3dB.

(6) Disconnect the signal generator and the RF millivoltmeter.

(7) Replace ML6 on the AGC card.

IF FILTER CARD

27. (1) Set the receiver POWER switch to OFF.

(2) Remove the extender card and the IF filter card from mother board slots 4 and 7 respectively (fig. 4.1.).

(3) Insert the extender card into mother board slot 7 and mount the IF filter card onto the extender card.

(4) Remove ML6 (CA 3046) from the AGC card.

(5) Set the receiver POWER switch to ON.

(6) Remove coaxial socket SK14 from PL14 on the second mixer (640 MHz module (fig. 4.3.)).

(7) Connect the tracking generator output to the removed coaxial socket SK14.

(8) At the receiver front panel, select AM or CW, 15 kHz bandwidth, set the IF GAIN fully clockwise and select manual only gain control (see para. 26(3)(a) to 26(3)(f) for details).

(a) Press and hold the MODE key, press the TEST key and then release both keys together to enter the self-test mode.

(b) Press and release the CHAN key and then select channel 99.

(c) Press and hold the MODE key, press the TEST key, and then release both keys together to exit from the self-test mode.

(d) Press and release the MODE key.

(e) Cancel SHORT (5), MEDIUM (n) or LONG (L), if selected, by pressing and releasing numeral key 7, 8 or 9 respectively.

(f) If manual gain (.) is not selected, press and release the SQLCH key.

(9) Set the tracking generator to a frequency to 21.4 MHz and an output level of -83dBm

(10) Set the spectrum analyser controls as follows:

Centre frequency:	21.4 MHz
Sweep width:	10 kHz per division
Scale:	10 dB per division

(11) Using the high impedance probe connect the spectrum analyser to TP1 on the IF filter card.

(12) Adjust L7 and L10 on the IF filter card for a peak output at 21.4 MHz.

(13) Set the spectrum analyser controls as follows:

Scale:	2 dB per division
Bandwidth:	1 kHz

(14) Re-adjust L7 and L10 for a peak output at 21.4 MHz.

(15) Select 300 kHz bandwidth, adjust L2 and L4 for max. O/P at 21.4 MHz.

(16) Measure the passband and ripple and ensure that the figures given in table 1 for the 300 kHz bandwidth are obtained.

(17) Set the spectrum analyser scale to 10 dB per division. Increase the tracking generator output level (overloading the analyser only in the passband) and ensure that the filter stop band complies with the figure given in table 1 (for the 300 kHz bandwidth).

(18) Reduce the tracking generator output level to -83 dBm. Measure and record the level indicated by the spectrum analyser. Ensure that the level is 45 dBm plus or minus 3 dB.

(19) At the receiver front panel, select a bandwidth of 30 kHz.

(20) Set the spectrum analyser controls as follows:

Centre frequency:	21.4 MHz
Sweep speed:	5 kHz per division
Scale:	2 dB per division

(21) Measure the bandwidth and the passband ripple; ensure that they comply with the figures given in table 1 (for the 30 kHz bandwidth).

(22) Set the spectrum analyser controls as follows:

Sweep width:	10 kHz per division
Scale:	10 dB per division

(23) Increase the tracking generator output level (overloading the analyser only in the passband) and ensure that the filter stopband complies with the figure given in table 1.

(24) Reduce the tracking generator output level to -83 dBm. Measure and record the level indicated by the spectrum analyser and ensure that it is within plus or minus 2 dB of the level noted at step (16).

(25) Repeat steps (20) to (24) with the 15 kHz bandwidth selected.

(26) Disconnect the tracking generator and spectrum analyser.

(27) Connect the signal generator, set to a frequency of 21.4 MHz and a CW output level of -57dBm, to coaxial socket SK14 (removed from PL14 on the second mixer/640 MHz module).

(28) Connect the probe of the RF millivoltmeter to PL77 on the IF filter card.

(29) Make only slight adjustments to L8, L9 and L11 for a maximum indication on the RF millivoltmeter, coincident with a flat response (the -4 dB bandwidth should be 21.4 MHz plus or minus 150 kHz to plus or minus 175 kHz).

(30) Note the level indicated on the RF millivoltmeter and check that it is -32 dBm plus or minus 6 dB.

(31) Disconnect the signal generator and the RF millivoltmeter.

(32) Set the receiver POWER switch to OFF. Carefully remove ML5 from the IF filter card and store in a safe place. Set the POWER switch back to ON.

(33) Connect the output of the tracking generator to PL77 on the IF filter card. Set the tracking generator to a frequency of 1.4 MHz and an output level of -32 dBm.

(34) Connect the spectrum analyser, using the high impedance probe, to the test pin on the extender card connected to edge connector pin 53 (1.4 MHz output from the IF filter card).

(35) Ensure that the receiver is set to manual only gain control, and that the IF GAIN control is turned fully clockwise.

(36) Set R57 on the IF filter card fully anti-clockwise.

NOTE: Variable resistors R57 and R60 on the IF filter card are multi-turn devices. An audible click is made when either end-stop is reached.

(37) Set the spectrum analyser controls as follows:

Centre frequency:	1.4 MHz
Sweep width:	50 kHz per division
Scale:	2 dB per division

(38) Adjust R60 on the IF filter card for an output level of -30 dBm, as indicated on the spectrum analyser. Reduce the output level of the tracking generator to -73 dBm. Adjust R57 to restore the output level to -30 dBm.

(39) Adjust L12, L13 and L14 on the IF filter card for a peak output at 1.4 MHz and best flat response. Ensure that the -4dB bandwidth is 1.4 MHz plus or minus 150 kHz to plus or minus 175 kHz. ensure that the passband ripple between +120 kHz and -120 kHz does not exceed plus or minus 3 dB.

(40) At the receiver front panel select a bandwidth of 15 kHz (filter FL5). Measure and record the output level displayed on the spectrum analyser.

(41) Select, in turn, bandwidths of 8 kHz, 3 kHz, 1.2 kHz and 300 Hz (filters FL4, FL3, FL2 and FL1). Measure the bandwidth, passband ripple and stopband for each filter and ensure that the figures obtained are as given in table 1. Ensure that the passband levels are all within plus or minus 2 dB of the level measure at step (45).

(42) Set the receiver POWER switch to OFF, disconnect all test equipment, and replace ML5 to the IF filter card and ML6 on the AGC Card.

(43) Remove the extender card and return the IF filter card to mother board slot 7.

(44) Replace coaxial socket SK14 to PL14 on the second mixer (640 MHz module).

Table 1: IF Filter Response Data

FILTER No.	DRAWING No.	NOMINAL BANDWIDTH	PASSBAND	MAXIMUM PASSBAND RIPPLE	MINIMUM STOPBAND ATTENUATION
1	BD81071	300 Hz	(-4dB) ±150 Hz to ±400 Hz	3dB between ±125 Hz	55dB at ±1.2 kHz
2	BD81072	1.2 kHz	(-4dB) ±600 Hz to ±900 Hz	3dB between ±500 Hz	55dB at ±1.8 kHz
3	BD81073	3 kHz	(-4dB) ±1.5 kHz to ±1.8 kHz	3dB between ±1.2 kHz	55dB at ±3 kHz
4	BD81074	8 kHz	(-6dB) ±4 kHz to ±7 kHz	3dB between ±3 kHz	55dB at ±10 kHz
5	BD81075	15 kHz	(-4dB) ±7.5 kHz to ±14 kHz	3dB between ±6 kHz	80dB at ±25 kHz
6	BD 81076	30 kHz	(-4dB) ±15 kHz to ±25 kHz	3dB between ±12 kHz	80dB at ± 50 kHz
7	Fig. I3.1	300 kHz	(-4dB) ±150 kHz to ± 175 kHz	3dB between ±120 kHz	80dB at ±500 kHz

DEMODULATOR CARD

28. (1) Set the receiver POWER switch to OFF.

(2) Remove the demodulator card from mother board slot 5. Insert the extender card into mother board slot 5 and mount the demodulator card onto the extender card.

(3) At the receiver front panel set the POWER switch to ON, set the frequency to 0.00000 MHz and select medium AGC (press and release the MODE key followed by the numeral 8 key). Ensure that manual gain is not also selected (press and release the SQLCH key if necessary).

NOTE: With the receiver set to a frequency of 0.00000 MHz, the synthesized local oscillator signal is set to a frequency of 661.4 MHz and provides an input signal to the receiver IF stages; this is used as a convenient test signal.

(4) Connect the digital multimeter to TP2 on the demodulator card and adjust L5 for a reading of 6.7 volts plus or minus 0.05V.

(5) Transfer the digital multimeter to TP3 and adjust L6 for a reading of 6.7 volts plus or minus 0.05V.

(6) The line output level potentiometer R51 can be set for a line output level between -20dBm and +10dBm into 600 ohms. The setting up procedure is given in para. 29.

(7) Disconnect the digital multimeter.

(8) Set the receiver POWER switch to OFF, remove the extender card, and return the demodulator card to mother board slot 5. Return the POWER switch to ON.

FINAL ADJUSTMENTS

29. (1) Connect test lead 1 to the AUDIO 1 socket on the receiver front panel.

(2) Connect the audio millivoltmeter to TB1 of test lead 1, pins 6 and 7.

(3) Connect the signal generator set to a frequency of 48.15 MHz and an output level of +40 dBμV e.m.f, to the receiver antenna socket.

(4) Set the receiver frequency to 48.15 MHz, CW mode, 3 kHz bandwidth, 0.80 kHz BFO frequency, and short AGC (press and release the MODE key followed by the numeral 7 key). Ensure that 'S' for AGC short is displayed, and that manual gain is not also selected (if necessary press and release the SQLCH key).

(5) Adjust R51 on the demodulator card for an indication on the audio millivoltmeter of -13 dBm plus or minus 2 dB. Note the level.

(6) Cancel short AGC and select manual only gain control. Set the IF GAIN control fully clockwise.

(7) On the IF filter card, set R57 fully anti-clockwise (30 turns).

(8) Adjust R60 on the IF filter card for an indication on the audio millivoltmeter equal to that noted at step (5).

(9) Reduce the signal generator output level to 0dBµV e.m.f.

(10) On the IF filter card, adjust R57 clockwise for an inidcation on the audio millivoltmeter equal to that noted at step (5).

(11) Increase the signal generator output level to 25dBµV e.m.f.

(12) Select short AGC (MODE followed by 7) and cancel maunal gain (SQLCH). Ensure that 'S' is displayed.

(13) Connect the RF millivoltmeter to PL77 on the IF filter card.

(14) On the AGC card, set R65 fully anti-clockwise and then adjust clockwise until the level at PL77 falls by between 0.5 and 1.0 dB.

(15) Disconnect the RF millivoltmeter.

(16) If an audio line level of other than -13dBm is required, repeat steps (3) and (4) and (5), adjusting R51 on the demodulator card for the required audio level, as indicated on the audio millivoltmeter.

(17) Disconnect all test equipment.

INTERNAL FREQUENCY STANDARD ADJUSTMENT

NOTE 1: Before carrying out the following procedure ensure that no connection is made to the EXT STD socket on the receiver front panel, and that the receiver has been operating continuously for at least one hour.

NOTE 2: The following procedure requires the use of an external frequency standard which has a higher degree of accuracy and stability than the 9442 or the 9420, as appropriate.

30. (1) Ensure that an external standard is not connected to the EXT STD socket on the front panel.

(2) Ensure that the receiver has been running continuously for at least one hour.

(3) Disconnect coaxial socket SK15 from PL15 on the second mixer/640 MHz module (fig. 4.3.). Connect the removed coaxial socket SK15 to the oscilloscope Channel A input.

(4) Connect the external frequency standard (1 MHz, 5 MHz, 10 MHz) to the oscilloscope Channel B input.

(5) Set the oscilloscope to display Channel A on the vertical axis and Channel B on the horizontal axis.

(6) For the 9420 standard only, set R51 on the 20 MHz reference board to mid-position (11 turns from either end stop). R51 is accessible through a hole in the compartment screening cover.

(7) Adjust the oscilloscope controls to display an elliptical Lissajou figure.

(8) Remove the rubber plug from the receiver frequency standard and using the trimming tool provided, adjust the internal trimmer for a stable Lissajou figure, moving less than one cycle in 5 seconds.

(9) Replace the rubber plug.

(10) For the 9420 standard only (ensure that the rubber plug has been replaced), adjust R51 on the 20 MHz reference board for a stable display.

(11) Switch off and disconnect all test equipment.

CHAPTER 21

FAULT DIAGNOSIS

(ST83771 PROCESSOR CARD)

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CHAPTER 21

FAULT DIAGNOSIS

(ST83771 PROCESSOR CARD)

INTRODUCTION

1. This chapter provides information to assist in the location of a faulty component or sub-assembly. A series of checks and suggestions are given with references to the self-test routines contained in Chapter 19 and to functional test routines contained in chapter 20. Signature analysis tests are included towards the end of the chapter.

TEST EQUIPMENT

2. The items of test equipment required are as given in chapter 20 with the following additional items:

Signature Analyser - Hewlett Packard HP5004A
Plug, 26-way, Amphenol 62GB-16J-16-26P
Resistor, 10K, 0.25W (Racal 914042)
Resistor, 22K, 0.25W (Racal 913493)

PRELIMINARY

3. Set the front panel POWER switch to OFF, disconnect all external connectors, and if necessary, transfer the unit to a flat, clean working suface.

4. If the nature of the fault is unknown, carry out the functional test procedures given in Chapter 20. These make use of some of the built-in self-test routines detailed in Chapter 19. If a fault is indicated whilst carrying out these routines, or if the routines do not run, refer to the manual tests (with the same respective test numbers) given in this chapter (paras. 7 to 19).

5. If the fault is associated with the optional SCORE interface card, then carry out the SCORE interface tests given in chapter 20.

6. If the self-test routines do not reveal a fault condition, further checks of the logic circuitry can be made by carrying out the signature analysis routines given in paras. 25 to 47. Once the digital circuitry has been checked, a signal generator can be connected to the receiver antenna socket and the signal paths can be checked using the information provided on the appropriate circuit diagrams.

MANUAL TESTS

7. The following paragraphs detail the manual tests to be carried out when a fault is indicated whilst carrying out the self-test routines (described in Chapter 19 and called in Chapter 20). For ease of reference, each manual test is given the same number as that of the associated self-test routine.

Test M00/a - Self Test Does Not Run

8. (1) Check whether the RUN/FAULT indicator D1 on the processor card is flashing (dimly) on and off. If not, check that switches SA to SF on the processor card are all set to the open position, and check the power supplies on the processor card (using the extender card), as follows:

SUPPLY	MONITORING POINT
+5.5V	Edge connector pin 63
+5VA	ML6 pin 40
+5VB	ML12 pin 14

(2) If the +5.5V supply is present and either the +5VA or the +5VB supply is incorrect, replace the processor card or check the supply circuitry, TR1, TR2, TR3, ML1.

(3) If the +5.5V supply is not present at edge connector pin 63 on the processor card, trace back to the power supply module. If necessary, unplug each card, in turn, to check for a short circuit.

(4) Run the processor card test routine, as follows:

(a) Set the front panel POWER switch to OFF.

(b) Set switch SA on the processor card to the closed position, and ensure that the remaining switches SB to SF are all set to the open position.

(c) Set the front panel POWER switch to ON and check that after approximately five seconds the RUN/FAULT indicator D1 on the processor card illuminates.

(5) If the processor card test routine fails to illuminate the RUN/FAULT indicator, replace the processor card or carry out the hardware signature analysis checks given in paras. 33 to 38 to localise the fault.

(6) If the processor card test routine is completed successfully, suspect a faulty display driver card, a faulty display and switch board, or a wiring fault. Check the front panel display using the procedure given in para. 42, and, if necessary, carry out the display driver card signature analysis routine (also para. 42).

Test M00 - ROM Check Sum Fault

9. (1) Replace the processor card or the ROM devices PD1 and PD2.

(2) If the fault persists following ROM replacement, replace the processor card or carry out the following:

(a) Check the supplies to each individual integrated circuit on the processor card.

(b) Carry out the processor card test routine, as described in para. 8(4).

(c) Carry out the processor card signature analysis routines given in paras. 33 to 38.

Test M01 - RAM Failure

10. Replace the processor card with a known serviceable spare, or carry out the following:

(1) Check the RAM devices on the processor card (ML4 and ML5) by replacement.

(2) Carry out the signature analysis routines given in paras. 28 to 33.

Test M02 to M06 - Power Supply Failure

11. Self-test routines 02 to 06 check the +5V, -12V, -30V, +15V and +24V supplies, in that order, on the processor card. Each voltage level is firstly scaled down using a potential divider, and is then applied, in turn, to a D to A converter via a multiplexer stage. The level of each supply is checked to ensure that it lies between preset upper and lower limits; if a supply level is found to be out of range by more than approximately plus or minus 10%, the test number is displayed, together with FAULT and either H (high) or L (low). If the +5V supply is out of range (test number 02 displayed), check whether any further supplies are out of range by pressing and releasing the UP key followed by the ENTER key. If all of the supplies are out of range, suspect the analogue monitoring circuitry on the processor card (ML1, ML8, ML9, ML17).

12. The levels of the +24V and -30V supplies are set by potentiometers R24 and R27 respectively on the power supply module; the remaining supplies are non-adjustable. If a supply is faulty, trace back to the power supply module. If necessary, unplug boards or remove cards to check for a short circuit.

Test M7 - EAROM Fault

13. Replace the processor board or carry out the following:

(1) Check for the correct supplies (+5V, -12V, -30V, 0V) at each of the two EAROM devices, ML2 and ML3, on the processor card.

(2) Carry out the signature analysis routine given in para. 30 to check the EAROM address and data bus lines.

(3) If no faults are found, suspect a faulty EAROM device.

Test M8 - Channel Checksum Fault

14. Self-test number 8 provides a confidence check to ensure that channel frequency and mode data stored in EAROM has not altered since it was initially entered. If this test fails, then attempt to re-enter the channel frequency and mode data. If this cannot be achieved, an EAROM fault must be suspected and the procedures given in para. 13 should be followed.

Test M010 - 20 MHz Reference Fault

15. (1) Ensure that either:

(a) The unit is fitted with an internal frequency standard module.

or (b) that a suitable external frequency standard is connected to the EXT STD socket on the front panel.

(2) Replace the 20 MHz reference board, or use the oscilloscope to check the internal/external reference interface circuits, and the 20 MHz phase-locked loop circuit, with reference to the circuit diagram of the 20 MHz reference board (fig 9.1).

Test M011 - 640 MHz Oscillator Fault

16. (1) Use the oscilloscope to check that 10 MHz squarewave signals, at TTL levels, are present at TP1 and TP2 on the second mixer/640 MHz board.

(2) Replace the second mixer/640 MHz board, or carry out the following:

(a) Carry out the alignment procedure for the second mixer/640 MHz board given in Chapter 20, para. 25.

(b) If the varactor line voltage at TP4 cannot be adjusted to +5.5V, replace the board or use the oscilloscope to check the phase comparator circuitry and use the spectrum analyser to check the 640 MHz oscillator and buffer amplifier circuitry.

Test M012 - Local Oscillator Fault

17. (1) Ensure that the 20 MHz reference signal is present at PL19 on the synthesizer board.

(2) Replace the synthesizer board and/or the first mixer/VCO board, or carry out the following:

(a) Carry out the alignment procedures for the synthesizer board given in Chapter 20, para. 22. If the specified performance cannot be achieved, carry out the signature analysis routines given in para. 38.

(b) Carry out the alignment procedures for the first mixer/VCO board given in Chapter 20, para. 23. If the specified performance cannot be achieved, replace the board or use the RF millivoltmeter and signal generator to check the first mixer/VCO board, with reference to the circuit diagram given in Chapter 11.

Test M13 - BFO Fault

18. (1) Ensure that the 20 MHz reference signal is present at edge connector pin 27 (resistor R1) on the demodulator card.

(2) Replace the demodulator card, or carry out the following:

(a) Carry out the signature analysis routine for the demodulator card given in para. 45.

(b) Use the oscilloscope to check the BFO circuitry on the demodulator card, as shown on sheet 1 of the circuit diagram, fig. 15.1.

Test M14 First Local Oscillator Sweep Test Failure

19. (1) Ensure that the 20 MHz reference signal is present at PL19 on the synthesizer board.

(2) Replace the synthesizer board and/or the first mixer /VCO board, or carry out the following:

(a) Run self-test routine 14 to determine the fault code. Refer to Chapter 19, para. 16 for an interpretation of the fault code and then carry out measurement checks on the synthesizer board, with refernce to the circuit diagram (Chapter 10, Fig. 10.1).

(b) If the varactor voltage is out of range, carry out the alignment procedures for the synthesizer board given in Chapter 20, para. 22 and the first mixer /VCO board given in Chapter 20, para.23.

(c) If the specified performance cannot be achieved, replace the first mixer /VCO board or use the RF millivoltmeter and signal generator to check the first mixer /VCO board, with reference to the circuit diagram given in Chapter 11, Fig. 11.1

(d) If the synthesizer is not functioning correctly, check the power supplies to each integrated circuit.

(e) Carry out the signature analysis routine given in Chapter 21, Para. 43.

(f) If the fault code indicates the varactor volts were 'Non-monotonic' or 'Step too large' (codes 03 and 04) use the oscilloscope to check the fast lock circuitry.

(g) Use the oscilloscope and frequency counter to check the synthesizer board, with reference to Chapter 10.

Test M15 - 1.4 MHz Detector Fault

20. (1) Ensure that the 1.4 MHz signal level at the AGC card edge connector pin 53 is approximately 100 mV rms. If so then the fault is on the AGC card, AGC Detector circuitry or the interconnection from the AGC card edge connector pin 34 (1.4 MHz Detector Output) to the processor card.

Replace the AGC card or, using the oscilloscope, check the AGC Detector circuitry with reference to the circuit diagram Fig. 14.1.

(2) If the 1.4 MHz signal is not present at pin 53:-

(a) Check the IF Filter card by removing SK14 from the second mixer module and connecting SK14 to the signal generator set to 21.4 MHz at +60 dB µV. If this does not result in a 1.4 MHz signal

at pin 53 then the fault is on the IF filter card. Ensure that the 20 MHz reference signal at the IF filter card edge connector pin 27 is at a level of 0 dBm ± 3 dB. Replace the IF filter card or use the oscilloscope to check the signal path with reference to the circuit diagram Fig. 13.1.

(b) If the procedure in (a) produces a 1.4 MHz signal at the AGC card edge connector pin 53 then the fault is on the signal path on either the First mixer/VCO board or the second mixer module or their interconnections.

(c) Reconnect SK14 onto the second mixer module. Disconnect SK13 from the second mixer module. Connect the signal generator, set to 661.4 MHz at +60 dBμV to PL13 on the second mixer module. If this does not produce a 1.4 MHz signal at the AGC card pin 53 then the fault is on the second mixer module.

Ensure that the 20 MHz reference is present at SK15 at a level of 0 dBm ± 3 dB.

Replace the second mixer module or using the millivoltmeter and oscilloscope check the circuitry with reference to the circuit diagram Fig. 12.1

(d) If the procedure in (c) produces a 1.4 MHz signal at the AGC card then the fault is in the Band Pass Filter or the 1st Mixer/VCO board.

Using the signal generator and millivoltmeter ensure that the insertion loss through the Band Pass filter at 661.4 MHz does not exceed 4.5 dB.

Replace the 1st Mixer/VCO board or check its circuitry with reference to the circuit diagram Fig. 11.1.

Test M16 - AGC Monitor Test Failure

21. (1) Replace the AGC card, or carry out the following:

(2) Run self-test routine 16 to determine the fault code. Refer to Chapter 19, para. 18 for an interpretation of the fault code. Carry out measurement checks on the AGC card with reference to the circuit diagram Fig. 14.1

(3) Check operation of outputs AGC1, 2, and 3 by varying the IF Gain Control on the Front Panel whilst in manual only control. Refer to Chapter 3 para. 27 to select AGC time constants and Manual only control.

Test M17 - Audio Detector Test Failure

22. (1) Replace the Demodulator card or carry out the following:

(2) Ensure that the 20 MHz reference signal is present at the Demodulator Card edge connector pin 27 at a level of 0 dBm ± 3 dB.

(3) Run self-test Routine 17 to determine the fault code. Refer to Chapter 19, Para. 18 for an interpretation of the fault code. Carry out measurement checks on the Demodulator Card Audio circuitry with reference to the circuit diagram Fig. 15.1

Test M18 - BFO Beat against first local oscillator

23. (1) Ensure no antenna input is connected.

(2) Replace the Demodulator card and/or the Synthesizer board or carry out the following:

(a) Carry out the signature analysis routines for the Demodulator card given in Chapter 21, para. 45.

(b) Use the Oscilloscope and frequency counter to check the BFO circuitry and audio detect on the demodulator card, with reference to the circuit diagrams given in Chapter 15, Figs. 15.1 and 15.2

(c) Carry out the signature analysis routines for the Synthesizer board given in Chapter 21, para. 43.

(d) Use the oscilloscope and frequency counter to check the synthesizer board, with reference to Chapter 10.

Test M31 - Keyboard Fault

24. Replace the display and switch board with a known serviceable spare, or carry out the following:

(1) Set the receiver POWER switch to OFF and mount the display driver card onto the extender card (inserted into the display driver card connector -slot 1).

(2) With reference to the circuit diagrams of the display and switch board (fig 5.1) and the display driver card (fig 6.1), use the multimeter to check that no short-circuts are present between switch matrix column inputs and row outputs (PL/SK3 and PL/SK29).

(3) Use the multimeter to check for continuity between the appropriate column input and row output for each front-panel key (when depressed).

SIGNATURE ANALYSIS

25. When the receiver is operating correctly, the non-sequential program instructions cause continuously changing data patterns to be present within the logic circuitry. Because these data patterns are continuously changing, data analysis or data checking using conventional test equipment (oscilloscope, logic probes, etc.) becomes almost impossible. The signature analysis technique requires the processor to continuously execute a single instruction (or continuously run a short test program) and so produce repetitive data patterns at selected data nodes throughout the logic circuitry. If the signature analyser START, STOP, CLOCK and GROUND leads are connected to the appropriate test points on a known serviceable unit, and the signature analyser probe is connected, in turn, to a number of circuit nodes, then a series of unique 4-digit alpha-numeric 'signatures' will be obtained. If these signatures are recorded, they may be used at a later date as a reference when the same tests are made during the test or fault location procedures. If an incorrect signature is found at a particular node, the operator simply traces back through gates, memory devices, etc. until an element with a correct signature at the input and a faulty signature at the output is isolated.

26. Use is made of the signature analyser to interpret the result of the processor card test (SA only closed) should the RUN/FAULT LED fail to illuminate after approximately five seconds from switch-on. The procedure is given in para. 27.

27. The RA 1794A contains two signature analysis routines for testing various parts of the unit. The first to be described is a hardware signature analysis routine (para. 33) for the procesor card. The closure of switch SB on the processor card initiates a DMA-OUT sequence where data is read out of ROM at the address contained in CPU internal register R(0). R(0) is then incremented and the process continues for as long as switch SB remains closed. The closure of switches SA and SC (prior to the closure of the POWER switch) causes the operation of a comprehensive software signature analysis routine, for the testing of various parts of the receiver (para. 39 onwards).

Use of Signature Analyser

28. The type of signature analyser required to carry out the procedures given in this chapter has an integral logic probe which may be used as a test instrument independently of the signature measuring capability. The logic probe incorporates a lamp, and this may be used to indicate one of the following four conditions:

(1) Probe lamp OFF (L) - Logic '0' (GND)

(2) Probe lamp ON (H) - Logic '1'

(3) Probe lamp half-on - High impedance/poor logic level

(4) Probe lamp flashing (F) - Data stream.

(5) In the remainder of this chapter, the signatures given all have a flashing probe tip, except where indicated /H or /L to show logic levels as in (1) and (2).

29. The signature analyser has START, STOP and CLOCK inputs for connection to the circuit under test, and a logic probe for connection to a circuit node to obtain a signature. The logic levels at the START, STOP and logic probe inputs are strobed into the signature analyser on either the rising or falling edge of the CLOCK input (as selected by the CLOCK pushbutton. Either rising or falling edges of the START and STOP inputs may be selected to initiate and terminate a time period (window or gate) during which measurement takes place.

30. When the START, STOP, CLOCK and GROUND connections are made correctly and the signature analysis routine is being executed, the GATE indicator should flash. The correct configuration for a particular test can be verified by checking the logic '1' signature, obtained by connecting the probe tip to the positive supply.

31. If the HOLD pushbutton is depressed, the instrument will hold a single one-time signature. The probe can then be removed from the test node whilst the signature comparison is made. The displayed signature is reset by pressing and releasing the RESET button on the probe.

PROCESSOR CARD TEST FAILURE INTERPRETATION (ST 83771)

32. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SA on the processor card is set to the closed position, and that the remaining switches SB to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor board as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the receiver POWER switch to ON.

(6) Wait at least ten seconds and then connect the signature analyser probe to any convenient +5V connection e.g. ML6 pin 40.

(7) Check the signature obtained with those given below to determine the faulty ROM or RAM device. If the signature obtained does not agree with any of the following, carry out the hardware signature analysis routine for the processor card given in para. 33. If the pass signature is obtained (and the receiver is faulty) the processor card is probably functioning correctly and the remainder of the unit should be checked using the procedures given in paras. 39 onwards.

+5V SIGNATURE/TIP STATE	FAILED DEVICE
9CP9/H	PASS
7U39/H	ROM PD1
U399/H	ROM PD2
399F/H	ROM PD3
99FA/H	RAM ML4
9FA8/H	RAM ML5

HARDWARE SIGNATURE ANALYSIS (PROCESSOR CARD)

Clock Divider

33. (1) Set the front panel POWER switch to OFF and mount the processor card onto the extender card (inserted into slot 3).

(2) Set switch SB on the processor card to the closed (on) position, the remaining switches (SA and SC to SF) to the open (off) position.

(3) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	OUT (positive edge)
CLOCK pusbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP2
STOP	TP2
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the processor card given below and check that correct signatures are obtained.

+5V - ML6 pin 40 - 826P/H
0V - Negative end of C8 - 0000/L

(7) Connect the signature analyser probe, in turn, to the points given in table 1 and check that correct signatures are obtained.

Table 1: Clock Divider Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT			
		ML15	ML6	TP	EC
0V	0000/L	8	20	-	-
5V	826P/H	16	16,40	-	-
RESET	0000/L	11	-	-	-
CK	826P	10	33	TP1	-
Q2	2A1F	7	-	-	49
Q5	8P3U	3	-	-	35,44
Q12	U81P	1	23	TP2	-

EC denotes Edge Connector

ROM Devices & Test Switch Buffer

34. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(3) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(4) Set the front panel POWER switch to ON.

(5) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- C690/H
0V	-	Negative end of C40	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(6) Connect the signature analyser probe, in turn, to the points given in table 2 and check that correct signatures are obtained.

RAM and EAROM Devices

35. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

Table 2: ROM Device and Test Switch Buffer Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC pin No.)					
		ML6	ML10	ML11	PD1	PD2/3	ML14
A0	9270	25	1	-	8	8	-
A1	71H0	26	2	-	7	7	-
A2	1AF5	27	-	1	6	6	-
A3	HF6A	28	-	2	5	5	-
A4	825P	29	3	3	4	4	-
A5	U801	30	4	4	3	3	-
A6	C9HC	31	15	16	2	2	-
A7	1511	32	-	-	1	1	-
TPA	0000(F)	34	17	17	-	-	-
$\overline{MRD}$	0000(F)	7	5,6	-	-	-	-
$\overline{MWR}$	C690/H	35	-	6	-	-	-
$\overline{AV}$	0000(F)	-	-	5	-	-	-
0V	0000/L	20	9,14	9,14	12	12	8
+5V	C690/H	16,40	16,18	18	21,24	21,24	16
A8	178U	-	7	-	23	23	-
A9	U9U7	-	8	-	22	22	-
A10	0548	-	-	7	19	19	-
A11	HAA7	-	-	8	18	18	-
$\overline{CS0}$	P254	-	13	-	20	-	-
$\overline{CS1}$	H6AA	-	12	-	-	20(PD2)	-
$\overline{CS2}$	34UP	-	11	-	-	20(PD3)	-
$\overline{CS3}$	C690(F)	-	10	-	-	-	1
D0	U08P	15	-	-	-	-	-
*D1	33H6	14	-	-	-	-	-
*D2	4H7H	13	-	-	-	-	-
*D3	210A	12	-	-	-	-	-
*D4	SU5P	11	-	-	-	-	-
*D5	H7H2	10	-	-	-	-	-
*D6	599P	9	-	-	-	-	-
*D7	H313	8	-	-	-	-	-

* These signatures are dependant upon the software fitted in the equipment. If these signatures are required, they can be provided from analysis of a known working receiver having the same program number and software issue. The signatures relate to P82892 Issue 02.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- 755U/H
OV	-	Negative end of C8	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 3 and check that correct signatures are obtained.

Table 3: RAM and LAROM Device Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC PIN No.)								
		ML6	ML10	ML11	ML4	ML5	ML12	ML14	ML2	ML3
0V	0000/L	20	9,14	9,14	8	8	7	8	9	9
5V	755U/H	16,40	16,18	18	-	-	14	16	22	22
A0	H335	25	1	-	4	4	-	-	16	16
A1	C113	26	2	-	3	3	-	-	17	17
A2	7050	27	-	1	2	2	-	-	18	18
A3	0772	28	-	2	1	1	-	-	19	19
A4	C4C3	29	3	3	21	21	-	-	20	20
A5	AA08	30	4	4	5	5	-	-	21	21
A6	/211	31	15	16	6	6	-	-	3	3
A7	A3C1	32	-	-	7	7	-	-	4	4
TPA	0000(F)	34	17	17	-	-	-	-	-	-
$\overline{MRD}$	0000(F)	7	5,6	-	18	18	-	-	-	-
$\overline{MWR}$	755U/H	35	-	6	20	20	-	-	-	-
$\overline{AV}$	0000(F)	-	-	5 -	-	-	-	-	-	
A8	7707	-	7	-	-	-	-	-	5	5
A9	577A	-	8	-	-	-	-	-	6	6
A10	HH86	-	-	7	-	-	-	-	7	7
A11	89F1	-	-	8	-	-	-	-	8	8
$\overline{CS0}$	A207	-	-	13	-	-	-	14	-	-
$\overline{CS1}$	H6A3	-	-	12	-	-	-	12	-	-
$\overline{CS2}$	755U/H	-	-	11	-	-	-	-	-	-
$\overline{CS3}$	H24U	-	-	10	19	19	-	-	-	-
$\overline{CLEAR}$	755U/H	3	-	-	17	17	-	-	-	-
$\overline{DMAOUT}$	0000	37	-	-	-	-	6	-	-	-
D1S	755U/H	-	-	-	-	-	8	15	-	-
OUT5	755U/H	-	-	-	-	-	-	13	14,15	-
OUT6	755U/H	-	-	-	-	-	-	11	-	14,15
+5VB	755U/H	-	-	-	22	22	-	-	-	-

Self-Test Switches

36. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- 826P/H
0V	-	Negative end of C8	- 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 4 and check that correct signatures are obtained.

Table 4: Self-Test Switch Signatures

SIGNAL	SIGNATURE/ TIP STATE	SWITCH SETTINGS						TEST POINT	
		F	E	D	C	B	A	ML6	ML14
0V	0000/L	0	0	0	0	C	0	20	8
+5V	826P/H	0	0	0	0	C	0	16,40	16
DIS	0000	0	0	0	0	C	0	-	1
IN1	826P/H	0	0	0	0	C	0	-	10
IN1	0000/L	0	0	0	C	C	0	-	10
OUT1	826P	0	0	0	0	C	0	15	9
OUT1	0000	0	0	0	C	C	0	15	9
IN2	826P/H	0	0	0	0	C	0	-	6
IN2	0000/L	0	0	C	0	C	0	-	6
OUT2	826P	0	0	0	0	C	0	14	7
OUT2	0000	0	0	C	0	C	0	14	7
IN3	826P/H	0	0	0	0	C	0	-	4
IN3	0000/L	0	C	0	0	C	0	-	4
OUT3	826P	0	0	0	0	C	0	13	5
OUT3	0000	0	C	0	0	C	0	13	5
IN4	826P/H	0	0	0	0	C	0	-	2
IN4	0000/L	C	0	0	0	C	0	-	2
OUT4	826P	0	0	0	0	C	0	12	3
OUT4	0000	C	0	0	0	C	0	12	3
$\overline{EF1}$	826P/H	0	0	0	0	C	0	24	-
$\overline{EF1}$	0000/L	0	0	0	0	C	C	24	-

0 = ON

C = OFF

Address Valid Circuit

37. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST PUSHBUTTON	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor board and check that correct signatures are obtained.

+5V	-	ML6 pin 40	-C690/H
OV	-	Negative end of C8	-0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 5 and check that correct signatures are obtained.

Table 5: Address Valid Circuit Signatures

SIGNAL	SIGNATURE/ TIP STATUS	TEST POINT (IC Pin No.)				
		ML6	ML7	ML20	ML19	ML12
+5V	C690/H	-	14	16,15	5,14	14
OV	0000/L	-	7	8,6	6,7	7
CK	C690(F)	1	3	-	-	-
$\overline{CK}$	0000(F)	-	4	9	-	-
$\overline{MRD}$	0000(F)	7	-	7	-	13
MRDD	0000(F)	-	-	10	3	-
$\overline{AV}$	0000(F)	-	-	14	2	-
$\overline{MWR}$	C690/H	35	-	-	-	2
$\overline{MRD}.\overline{MWR}$	0000(F)	-	-	1	-	1
AR	0000(F)	-	-	13	4	-

CPU, Address Bus & Address Decoder

38. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)

CLOCK pushbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	ML6 pin 32
STOP	ML6 pin 32
CLOCK	ML6 pin 34
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained:

+5V	- ML6 pin 40	-0001/H
OV	- Negative end of C8	- 0000/L

(7) Connect the signature analyser probe, in turn, to the points given in table 6 and check that correct signatures are obtained.

Table 6: CPU, Address Bus & Address Decoder Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT		
		ML6	ML10	TP
OV	0000/L	20	9,14	
+5V	0001/H	16,40	16,18	
CK	0000(F)	1	-	
$\overline{\text{WAIT}}$	0001/H	2	-	
$\overline{\text{CLEAR}}$	0001/H	3	-	
$\overline{\text{DMA IN}}$	0001/H	38	-	
$\overline{\text{DMA OUT}}$	0000/L	37	-	
TPA	0001(F)	34	17	
MA0	HC89	25	1	
MA1	2H70	26	2	
MA2	HPP0	27	-	
MA3	1293	28	-	
MA4	HAP7	29	3	
MA5	3C96	30	4	
MA6	3827	31	15	
MA7	755U	32	-	
$\overline{\text{MRC}}$	0000(F)	7	5	
$\overline{\text{CSO}}$	822A	-	13	TP4
$\overline{\text{CS1}}$	A169	-	12	
$\overline{\text{CS2}}$	CFU3	-	11	
$\overline{\text{CS3}}$	AP96	-	10	TP5

SOFTWARE SIGNATURE ANALYSIS

The signatures in this section relate to P 82892 Issue 02 software.

Processor Card PIO Device

39. (1) Set the front panel POWER switch to OFF.

(2) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(3) Mount the processor card onto the extender card (inserted into slot 3).

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads to the processor card as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	-P254/H
0V	-	Negative end of C8	-0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card clock divider test routine given in para. 33.

(8) Connect the signature analyser probe, in turn, to the points given in tables 7, 8 and 9 and check that correct signatures are obtained.

Table 7: PIO Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)					
		ML6	ML13	ML7	ML19	EC	ML18
0V	0000/L	20	20	7	7	1,64	12
+5V	P254/H	16,40	40	14	14	2,63	24
TPA	0000(F)	34	1	-	11	-	-
TPB	0000(F)	33	37,38	-	10	-	-
$\overline{MRD}$	C14C	7	39	-	-	-	-
$\overline{CLEAR}$	P254/H	3	13	-	-	-	-
N0	46HH	19	3	-	-	-	-
N1	4637	18	4	-	-	-	-
N2	0000/L	17	-	5	-	-	-
$\overline{N2}$	P254/H	-	2	6	-	-	-
B0	F59F	15	5	-	-	-	-
B1	5PAH	14	6	-	-	-	-
B2	0F92	13	7	-	-	-	-
B3	2888	12	8	-	-	-	-
B4	0C42	11	9	-	-	-	-
B5	3H01	10	10	-	-	-	-
B6	3743	9	11	-	-	-	-
B7	U426	8	12	-	-	-	-
'A'RDY	0000(F)	-	36	-	9	-	-
'A'ST	8075	-	35	-	13	-	-
INH	6221	-	-	-	12	-	23

EC denotes Edge Connector

F denotes flashing probe

Table 8: PIO Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
		ML13	ML18	ML17	ML12	EC
PA0	2P0A	34	-	-	-	19
PA1	4F62	33	-	-	-	20
PA2	PP2C	32	-	-	-	21
PA3	P246	31	-	-	-	22
PA4	HAPP	30	-	-	-	23
PA5	PC4F	29	-	-	-	24
PA6	02A7	28	-	-	-	25
PA7	H710	27	-	-	-	26
'B'ST	0000/L	17	-	-	-	-
PB0	7875	18	2	10	-	-
PB1	UHF1	19	3	11	-	-
PB2	F6CA	21	21	14	-	-
PB3	5947	22	22	13	-	-
PB4	P254/H	23	-	-	9	-
PB5	CHFF	24	-	15	12	-
PB6	AC4H	25	-	-	-	36
PB7	5U82	26	-	-	-	48
STB	0000(F)	1	-	-	-	-

EC denotes Edge Connector

Table 9: PIO Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		ML18	EC
0	0000/L	11	10
1	366U	9	18
2	U5H5	10	55
3	525U	8	47
4	89F8	7	33
5	71C0	6	46
6	9A72	5	45
7	7654	4	38
8	0000/L	18	42
9	0000/L	17	3
10	1FA0	20	4
11	196P	19	5
12	0000/L	14	6
13	0000/L	13	7
14	0000/L	16	8
15	0000/L	15	9

EC denotes Edge Connector

Processor Card DAC

40. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switches SA and SC on the processor card are set to the closed position, and that switches SB, SD, SE and SF are set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained:

+5V - ML6 pin 40 -P254/H
0V - Negative end of C8 -0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor and clock divider test routine given in para. 33.

(7) Connect the signature analyser probe, in turn, to the points given in table 10 and check that correct signatures are obtained.

Table 10: DAC Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		ML6	ML9
0V	0000/L	20	8,9
+5V	P254/H	16,40	10
B0	F59F	15	2
B1	5PAH	14	1
B2	0F92	13	16
B3	2888	12	15
B4	0C42	11	14
B5	3H01	10	13
B6	3743	9	12
B7	U426	8	11
$\overline{EN}$	00F1	-	4

(8) Use the oscilloscope to monitor TP7 on the processor card and check that the displayed waveform is as given in fig. 21(a).

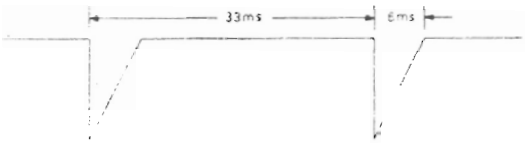

Fig. 21(a) TP7 Waveform

Processor Card Latched I/O

41. With the processor card switch settings, signature analyser controls and signature analyser lead connections as detailed in para. 40, connect the signature analyser probe, in turn, to the points given in table 11 and check that correct signatures are obtained. Remove the extender card and return the processor card to slot 3.

Table 11: Latched I/O Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT		
		ML6	ML16	EC
0V	0000/L	20	8	1,64
+5V	P254/H	16,40	16	63
TPB	0000(F)	33	9	-
N1	4637	18	-	-
A0	2766	25	14	-
A1	9H44	26	13	-
A2	4PU5	27	11	-
A3	IP26	28	4	-
A4	6C0P	29	6	-
$\overline{\text{CLEAR}}$	P254/H	-	1	-
LA0	3C0C	-	15	27
LA1	CAC2	-	12	28
LA2	CC6P	-	10	29
LA3	C68C	-	5	30
LA4	5722	-	7	31

EC denotes Edge Connector
F denotes Flashing Probe.

Display Driver Card (ST 79784)

42. (1) Set the front panel POWER switch to OFF.

(2) Set switch SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(3) Set the front panel POWER switch to ON.

(4) Compare the front panel display with that given in fig. 21(b). If the display is incorrect proceed with the following signature analysis checks of the display driver card.

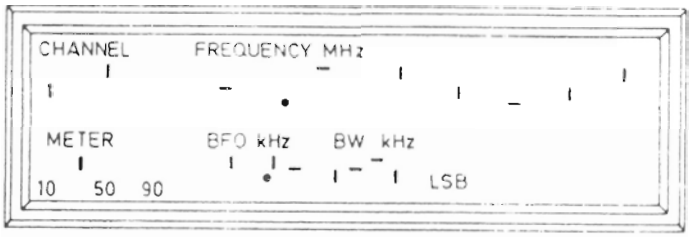

Fig. 21(b) Front Panel Test Display

(5) Set the front panel POWER switch to OFF.

(6) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(7) Mount the display driver card onto the extender card (inserted into slot 1).

(8) Connect the signature analyser leads as follows:

START	TP5)
STOP	TP5) Processor card
CLOCK	TP1)
GROUND	Negative end of C1 on the display driver card.

(9) Set the front panel POWER switch to ON.

(10) Connect the signature analyser probe, in turn, to the following points on the display driver card and check that correct signatures are obtained.

+5V - Positive end of C1 - P254/H
0V - Negative end of C1 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks detailed in paras. 33 to 38.

(11) Connect the signature analyser probe, in turn, to the points given in tables 12, 13, and 14, and check that correct signatures are obtained.

(12) Set the front panel POWER switch to OFF.

(13) Remove the extender card and return the display driver card to slot 1.

Table 12: Display Driver Card Signatures 1

SIGNAL	SIGNATURE TIP STATE	TEST POINT (PIN NO.)									
		EC	ML2	ML1	ML11	ML17	ML9	ML6	ML8	ML7	ML10
0V	0000/L	1,64	8	7	8,15	8,5	8	8	8	8	8
+5V	P254/H	2,63	16	14	16	10,16	16	16	16	16	16
A0	3C0C	27	14	-	2	-	-	-	-	-	-
A1	CAC2	28	-	-	3	4	-	-	-	-	-
A2	CC6P	29	-	-	-	12	-	-	-	-	-
A3	C68C	30	-	-	-	13	-	-	-	-	-
A4	5722	31	-	-	-	3	-	-	-	-	-
I00	2P0A	19	-	-	-	-	-	4	-	4	3
I01	4F62	20	-	-	-	-	-	6	-	6	5
I02	PP2C	21	-	-	-	-	-	10	-	10	7
I03	P246	22	-	-	-	-	-	12	-	12	9
I04	HAPP	23	-	-	-	-	4	-	4	-	11
I05	PC4F	24	-	-	-	-	6	-	6	-	13
I06	02A7	25	-	-	-	-	10	-	10	-	-
I07	H710	26	-	-	-	-	12	-	-	-	
MUX-CK	P955	35	3	-	-	-	-	-	-	-	-
DC	AC4H	36	-	-	-	-	-	-	-	-	-
CKD.DC	51PA	-	1,13	2	-	1	-	-	-	-	-
STB7	7654	38	-	-	13	-	-	-	-	-	-
STB8	0000/L	42	-	-	14	-	-	-	-	-	-
CK.P	PH12	-	6	1	-	15	-	-	-	-	-
$\overline{\text{STB.D}}$	9400	-	15	-	10	-	-	-	-	-	-
$\overline{\text{STB.KB}}$	P254/H	-	-	-	11,1	-	-	-	-	-	1,15
DISP BLANK	5PAF			3,5,8	-	-	-	-	-	-	-

EC denotes Edge Connector

Table 13: Display Driver Card Signatures 2

SIGNAL	SIGNATURE TIP STATUS	TEST POINT (PIN NO)						
		ML2	ML1	ML17	ML9	ML6	ML8	ML7
EN1	P7C3	10	9	-	-	-	-	-
EN2	91P7	9	6	-	-	-	-	-
$\overline{ME1}$	5C4C	-	10	-	2	2	-	-
$\overline{ME2}$	2H1U	-	4	-	-	-	2	2
A	7PUF	-	-	6	1	1	1	1
B	36CH	-	-	11	15	15	15	15
C	A171	-	-	14	14	14	14	14
D	C8CH	-	-	2	13	13	13	13
R	0000(F)	-	-	9	-	-	-	-

F denotes flashing probe tip

Table 14: Display Driver Card Signatures 3

SIGNAL	SIGNATURE/ TIP STATUS	TEST POINT (PIN NO.)									
		ML3	ML1	ML17	ML14	ML15	ML16	ML12	ML13	ML4	ML5
0V	0000/L	4	-	5,8	12	4	4	4	4	4	4
+5V	P254/H	7	-	10,16	1,24	8	8	8	8	8	8
A	7PUF	-	-	6	-	-	-	-	-	-	-
B	36CH	-	-	11	3	-	-	-	-	-	-
C	A171	-	-	14	21	-	-	-	-	-	-
D	C8CH	-	-	2	22	-	-	-	-	-	-
R	0000(F)	-	-	9	19	-	-	-	-	-	-
Q0	2HA8	-	-	-	11	1	-	-	-	-	-
Q1	6A1C	-	-	-	9	6	-	-	-	-	-
Q2	H892	-	-	-	10	-	1	-	-	-	-
Q3	64C9	-	-	-	8	-	6	-	-	-	-
Q4	AFU5	-	-	-	7	-	-	1	-	-	-
Q5	95P3	-	-	-	6	-	-	6	-	-	-
Q6	843U	-	-	-	5	-	-	-	1	-	-
Q7	1F58	-	-	-	4	-	-	-	6	-	-
Q8	53A9	-	-	-	18	-	-	-	-	1	-
Q9	U9P5	-	-	-	17	-	-	-	-	6	-
Q10	12U1	-	-	-	20	-	-	-	-	-	1

Synthesizer Board (ST 79782)

43. (1) Set the front panel POWER switch to OFF.

(2) Position the unit on its side and remove the cover from the synthesizer board compartment.

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5)	
STOP	TP5)	Processor card
CLOCK	TP1)	
GROUND	Any convenient OV point (chassis).	

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained.

+5V - ML16 pin 39 - P254/H
OV - ML16 pin 24 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 15 and check that correct signatures are obtained.

Table 15: Synthesizer Board Signatures 1

SIGNAL	SIGNATURE/ TIP STAT	TEST POINT	
		PL39	ML16
OV	0000/L	5,6	24
+5V	P254/H	8,10	39
* +15V	P254/H	7	38
+9V	P254/H	-	38
STB1	366U	15	17
IO0	2P0A	11	22
IO1	4F62	13	21
IO2	PP2C	12	20
IO3	P246	14	19
IO4	HAPP	16	18
CTL1	F378	-	15,34

(*+15V - use potential divider.
See Figure 21c on page 21-32)

(9) Set the front panel POWER switch to OFF.

(10) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Connect the signature analyser leads to the following points on the synthesizer board.

START	ML16 pin 2
STOP	ML16 pin 2
CLOCK	ML16 pin 17
GROUND	ML16 pin 24

(12) Set the front panel POWER switch to ON.

(13) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained:

+5V - ML16 pin 39 - 494P/H
0V - ML16 pin 24 - 0000/L

(14) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 16 and check that correct signatures are obtained.

(15) Set the front panel POWER switch to OFF. Disconnect the signature analyser leads. Replace the cover of the synthesizer compartment. Position the unit upright.

Table 16: Synthesizer Board Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
		ML16	ML12	ML13	ML17	ML15
0V	0000/L	24	8,7	8,7,10	8,7,5	7,8
+5V	494P/H	39	1,16	1,16	1,16	14
+9V	494P/H	38	-	-	-	-
CK IN	494P(F)	37	-	-	-	-
$\overline{CK2}$	494P(F)	1	-	-	-	-
CO	0000/L	16	-	-	-	-
CTL1	3413	15,34	-	-	-	-
DIV3	P7C7	11	6	-	-	-
DIV4	CFU6	10	5	-	-	-
DIV5	PAU3	9	-	12	-	-
DIV6	CH5P	8	-	11	-	-
DIV7	37AC	7	-	6	-	-
DIV8	86U5	6	-	5	-	-
DIV9	OP1C	5	-	-	12	-
DIV10	01F3	4	-	-	11	-
DIV11	0038	3	-	-	6	-
DIV12	0007	2	-	-	-	10
D0	59PF	22	-	-	-	-
D1	U4H1	21	-	-	-	-
D2	F3P5	20	-	-	-	-
D3	U159	19	-	-	-	-
D4	F535	18	-	-	-	-
$\overline{W}$	494P(F)	17	-	-	-	-

IF Filter Card (ST 80453)

44. (1) Using the 10K and 22K resistors, make up a potential divider, as shown in fig. 21(c), to reduce the +15V logic levels encountered at some points on the IF filter card to the +5V logic levels required by the signature analyser.

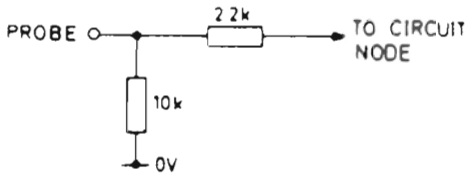

Fig. 21(c) 15V Logic Potential Divider

(2) Set the front panel POWER switch to OFF.

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Mount the IF filter card onto the extender card (inserted into slot 7).

(6) Connect the signature analyser leads as follows:

START	TP5)
STOP	TP5) Processor Card
CLOCK	TP1)
GROUND	Any convenient 0V point (chassis)

(7) Set the front panel POWER switch to ON.

(8) Connect the signature analyser probe, in turn, to the following points on the IF filter card and check that correct signatures are obtained:

+15V - ML4 pin 16 - P254/H
0V - ML4 pin 8 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(9) Using the potential divider where necessary, connect the signature analyser probe, in turn, to the points on the IF filter card given in table 17 and check that correct signatures are obtained.

(10) Set the front panel POWER switch to OFF.

(11) Remove the extender card and replace the IF filter card (slot 7).

Table 17: IF Filter Card Signatures

		SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
				EC	ML4
		0V	0000/L	1,64	8
	*	+15V	P254/H	61	16
	*	F0	97U3	31	2,14
	*	F1	9UA5	32	3,13
#	*	F2	4727	30	1
#	*	F3	9C91	29	15
#	*	FL1	7193	-	12
#	*	FL2	97U3	-	11
#	*	FL3	9UA5	-	10
#	*	FL4	0000/L	-	9
#	*	FL6	97U3	-	5
#	*	FL7	9UA5	-	6

These signatures are dependant upon software fitted in this equipment. If these signatures are required they can be provided from analysis of known working receiver having the same program number and software issue.

These examples relate to program P82892 Iss. 2.

* +15V logic - use potential divider.

EC denotes Edge Connector

Demodulator Card (ST 80499)

45. (1) Set the front panel POWER switch to OFF.

(2) Mount the demodulator card onto the extender card (inserted into slot 5).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5	
STOP	TP5	Processor Card
CLOCK	TP1	
GROUND	Any convenient OV point (chassis)	

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the demodulator card and check that correct signatures are obtained.

+8V - ML10 pin 39 - P254/H
OV - ML10 pin 24 - 0000/L

Note: If the correct +8V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature probe, in turn, to the points on the demodulator card given in table 18 and check that correct signatures are obtained.

Table 18: Demodulator Card Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		EC	ML10
OV	0000/L	1,64	24
+5V	P254/H	61	-
+8V	P254/H	-	38,39
I00	2P0A	19	22
I01	4F62	20	21
I02	PP2C	21	20
I03	P246	22	19
I04	HAPP	23	18
STB2	U5H5	55	17

EC denotes Edge Connector

(9) Set the front panel POWER switch to OFF.

(10) Transfer the signature analyser leads to the following points on the demodulator card:

START	ML10 pin 13
STOP	ML10 pin 13
CLOCK	ML10 pin 17
GROUND	ML10 pin 24

(11) Set the front panel POWER switch to ON.

(12) Connect the signature analyser probe, in turn, to the following points on the demodulator card and check that correct signatures are obtained:

+8V	- ML10 pin 39	-	494P/H
0V	- ML10 pin 24	-	0000/L

(13) Connect the signature analyser probe, in turn, to the points on the demodulator card given in table 19 and check that correct signatures are obtained.

(14) Set the front panel POWER switch to OFF.

(15) Disconnect the signature analyser leads.

(16) Remove the extender card and replace the demodulator card into slot 5.

Table 19: Demodulator Card Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)			
		ML10	ML15	ML3	ML8
0V	0000/L	24	8	8	7,4
+8V	494P/H	38,39	1,7,10,16	16	14
CI	0000/L	36	-	-	-
CK.IN	494P(F)	37	-	-	-
CK1	(F)	40	-	-	-
D0	6PC4	22	-	-	-
D1	04UP	21	-	-	-
D2	3017	20	-	-	-
D3	3UUC	19	-	-	-
D4	H416	18	-	-	-
$\overline{W}$	0000/L	17	-	-	-
C0	0000/L	16	-	-	-
CTL2	4946	34,14	-	-	-
DIV1	6929	13	3	-	-
DIV2	846C	12	4	-	-
DIV3	9481	11	5	-	-
DIV4	7290	10	6	-	-
DIV5	PHFA	9	-	-	-
DIV6	3HC9	8	-	-	-
DIV7	P7C7	7	-	-	-
DIV8	CFU6	6	-	-	6
DIV9	PAU3	5	-	11	-
DIV10	CH5P	4	-	10	-
DIV11	37AC	3	-	9	-
DIV12	86U5	2	-	-	-

(F) denotes flashing probe tip.

AGC Card (ST 85491)

46. (1) Set the front panel POWER switch to OFF.

(2) Mount the AGC card onto the extender card (inserted into slot 6).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5	
STOP	TP5	Processor card
CLOCK	TP1	
GROUND	Any convenient OV point (chassis)	

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the AGC card and check that correct signatures are obtained.

+5V - ML14 pin 1 - P254/H
OV - ML14 pin 8 - 0000/L

Note: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 28 to 33.

(8) Using the potential divider shown in fig. 21(c) where necessary for 15V logic signals, connect the signature analyser probe, in turn, to the points on the AGC card given in tables 20, 21 and 22, and check that correct signatures are obtained.

(9) Set the front panel POWER switch to OFF.

(10) Remove the extender card and return the AGC card to slot 6.

Table 20: AGC Card Signatures 1

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
			EC	ML16	ML14	ML15	ML17
	OV	0000/L	1,64	8	8	8	8
	+5V	P254/H	63	1	1	-	-
*	+15V	P254/H	61	16	16	16	16
	I00	2P0A	19	10	-	-	-
	I01	4F62	20	6	-	-	-
	I02	PP2C	21	14	-	-	-
	I03	P246	22	3	-	-	-
	EN	5U82	48	2,7,9	2,7,9	-	-
	STB3	525U	47	-	14	-	-
	STB4	89F8	33	-	10	-	-
	STB5	71C0	46	-	3	-	-
	STB6	9A72	45	-	6	-	-
*	I00	P117	-	11	-	4	7
*	I01	A6U8	-	5	-	14	13
*	I02	FC29	-	13	-	13	4
*	I03	AHC2	-	4	-	7	14

EC denotes Edge Connector
* +15V Logic - use potential divider

Table 21: AGC Card Signatures 2

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)			
			EC	ML14	ML15	ML17
*	STB3	525U	-	13	-	-
*	STB4	89F8	-	11	-	-
*	STB5	71C0	-	4	5	-
*	STB6	9A72	-	5	-	5
*	POL	P254/H	-	-	6	6
*	F0	97U3	31	-	2	-
*	F1	9UA5	32	-	1	-
*	F2	4727	30	-	11	-
*	F3	9C91	29	-	10	-
*	L0	4518	-	-	-	10
*	L1	3H11	-	-	-	11
*	L2	F58U	-	-	-	2
*	L3	72C1	16	-	-	1

EC denotes Edge Connector
* +15V logic - use potential divider

Table 22: AGC Card Signatures 3

SIGNAL	SIGNATURE	TEST POINT (PIN NO)							
		ML16	ML14	ML9	ML1	ML2	ML10	ML3	ML11
0V	0000/L	8	8	8	4	4	7	7	7
+5V	P254/H	1	1	-	-	-	-	-	-
* +15V	P254/H	16	16	16	8	8	14	14	14
* IO0	P117	11	-	14	-	-	5	-	-
* IO1	A6U8	5	-	4	-	-	-	-	-
* IO2	FC29	13	-	13	-	-	-	-	5
* IO3	AHC2	4	-	7	-	-	9	-	-
* STB3	525U	-	13	5	-	-	-	-	-
* STB4	89F8	-	11	-	-	-	3,11	-	3
* STB5	71C0	-	4	-	-	-	-	-	-
* STB6	9A72	-	5	-	-	-	-	-	-
* POL	P254/H	-	-	6	-	-	-	-	-
* HANG 0	U01A	-	-	1	-	-	-	-	-
* HANG 1	377F	-	-	2	-	-	-	-	-
* DECAY 0	2A8H	-	-	11	6	-	-	-	-
* DECAY 1	2UFA	-	-	10	-	6	-	-	-
Ø*DUMP	F3P6	-	-	-	-	1,2	1	5	-
Ø DR	0000/L	-	-	-	-	-	4	-	-
R/S	0000/L	-	-	-	-	-	6,8,10	-	4,6
* PEAK	6C58	-	-	-	-	-	13	13	-
* $\overline{\text{PEAK}}$	890F	-	-	-	-	-	12	6	-
* MAN	8158	-	-	-	-	-	-	12	2
* SAMPLE	3330	-	-	-	-	-	-	-	-

Ø Remove IF Filter Card to obtain signature

* 15V Logic - use potential divider

SCORE Interface Card (ST 79796)

47. (1) Set the front panel POWER switch to OFF.

(2) Mount the SCORE interface card onto the extender card (inserted into slot 2).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature leads as follows:

START	TP5
STOP	TP5 Processor card
CLOCK	TP1
GROUND	Any convenient OV point (chassis)

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the SCORE interface card and check that correct signatures are obtained.

+5V - Positive end of C4 - P254/H
OV - Negative end of C4 - 0000/L

Note: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature analyser probe, in turn, to the points on the SCORE interface card given in tables 23, 24, 25 and 26 and check that correct signatures are obtained.

(9) Set the front panel POWER switch to OFF.

(10) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Transfer the signature analyser leads to the following points on the SCORE interface card:

START	ML7 pin 14
STOP	ML7 pin 14
CLOCK	ML9 pin 10
GROUND	ML9 pin 7

Table 23: SCORE Interface Card Signatures 1

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
			EC	ML12	ML7	ML11	ML17
	0V	0000/L	1,64	1,8	1,8	8	8
	+5V	P254/H	2,63	16	16	16,1	16
*	+15V	P254/H	61	-	-	-	-
	-12V	0000/L	59	-	-	-	-
	IO0	2P0A	19	7	-	6	11
	IO1	4F62	20	6	-	4	12
	IO2	PP2C	21	5	-	3	13
	IO3	P246	22	4	-	11	14
	IO4	HAPP	23	-	7	13	7
	IO5	PC4F	24	-	6	14	6
	IO6	02A7	25	-	5	-	5
	IO7	H710	26	-	4	-	4
	STB11	196P	5	-	-	9	-
	STB12	0000/L	6	-	-	-	-
	STB14	0000/L	8	9	9	-	-
#	FIFO	0000	41	-	-	-	-
	STB10	1FA0	4	3	3	-	-
	STB13	0000/L	7	-	-	-	-
	STB9	0000/L	3	-	-	-	-
	CK.INT	P955	44	-	-	-	-

EC denotes Edge Connector

* 15V logic - use potential divider

\# This signature changes to 0000(F) on earlier boards.

Table 24: SCORE Interface Card Signatures 2

SIGNAL	SIGNATURE	TEST POINT		
		EC	ML11	TR COLLECTOR
Q3	56A6	-	7	
Q2	7H55	-	5	
Q1	7H9U	-	2	
Q4	435U	-	10	
SAS	8U1O	-	12	
R/L	7463	-	15	

EC denotes Edge Connector

Table 25: SCORE Interface Card Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)								
		EC	ML16	ML10	ML14	ML9	ML5	ML3	ML1	ML2
0V	0000/L	1,64	4	7	4	7	8	7	5,7,9	7
+5V	P254/H	2,63	1	14	8	14	10,16	14	14	14
INT.CK	P955	44	-	-	-	6	-	-	-	-
CK.IN	0000/L	35	5	-	-	-	-	-	-	-
CK.RTN	0000/L	46	6	-	-	-	-	-	-	-
$\overline{\text{CK.IN}}$	0000/L	-	3	11	-	13	-	-	-	-
CK.IN	P254/H	-	-	10	6	-	-	-	-	-
CK.D	0000/L	-	-	-	7	-	-	-	-	-
CK.E	P254/H	-	-	-	5	1,2	-	-	-	-
EXT.P	0000/L	-	-	1	-	3,12	-	-	-	-
$\overline{\text{EXT.P}}$	P254/H	-	-	2	-	5	-	-	-	-
EXT.SEL	P254/H	-	-	-	-	9,11	-	-	-	-
INT.SEL	0C01	-	-	-	-	8,4	-	-	-	-
SCORE.CK	P955	-	-	13	-	10	9	-	-	-
$\overline{\text{SCORE.CK}}$	0C01	-	-	12	-	-	-	-	3	-
Q4	0000(F)	-	-	-	-		14	1	-	-
SAS	8U10	-	-	-	-	-	-	2	-	-
$\overline{\text{Q4}}$	6H44	-	-	-	-	-	-	3	-	-
STB13	0000/L	7	-	-	-	-	-	-	4,8	-
SIS	0000/L	-	-	-	-	-	-	-	13	9
$\overline{\text{SIS}}$	P254/H	-	-	-	-	-	-	-	12	13
$\overline{\text{SYNC}}$	P254/H	-	-	-	-	-	-	-	-	10,5
SET	8U10	-	-	-	-	-	-	-	6	4
LOAD	9HH1	-	-	-	-	-	-	-	11,1	-
$\overline{\text{LOAD}}$	7U85	-	-	-	-	-	-	-	2	12
RESET	9HH1	-	-	-	-	-	15	-	-	11

Table 26: SCORE Interface Card Signatures 4

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)						
		ML12	ML7	ML10	ML2	ML3	ML8	ML15
$\overline{\text{FIFO}}$	U5PA	-	2	9 *	-	-	-	-
DOR	300C	-	14	-	-	-	-	-
LOAD	9HHI	-	-	-	1	-	-	-
$\overline{\text{SO}}$	3AIC	-	-	-	3	5,6	-	-
SO	H84U	15	15	-	-	4	9	-
P1	F64H	-	13	-	-	-	7	-
P2	P4H5	-	12	-	-	-	6	-
P3	C6FA	-	11	-	-	-	5	-
P4	4301	-	10	-	-	-	4	-
P5	943A	13	-	-	-	-	13	-
P6	9132	12	-	-	-	-	14	-
P7	UFC6	11	-	-	-	-	15	-
P8	2396	10	-	-	-	-	1	-
CK	0C01	-	-	-	-	-	10	-
Q8	F0U1	-	-	-	-	-	3	3

* ML10 Pin 9 is P254 on earlier Boards.

(12) Link the pins of a 26-way plug (para. 2) as listed below and connect to the CONTROL socket on the receiver front panel

Pin D to pin R
Pin H to pin a
Pin K to pin c
Pin M to pin b
Pin P to pin Z

(13) Set the front panel POWER switch to ON.

(14) Connect the signature analyser probe, in turn, to the following points on the SCORE interface and check that correct signatures are obtained.

+5V - Positive end of C4 - CC34/H
0V - Negative end of C4 - 0000/L

(15) Connect the signature analyser probe, in turn, to the points on the SCORE interface card given in table 27 and check that correct signatures are obtained.

(16) Set the front panel POWER switch to OFF.

(17) Disconnect the signature analyser leads.

(18) Remove the extender card and return the SCORE interface card to slot 2.

Table 27: SCORE Interface Card Signatures 5

SIGNAL	SIGNA-TURE	TEST POINT (PIN NO.)										
		ML8	ML15	EC	ML16	ML17	ML10	ML4	ML6	ML5	ML3	ML20
0V	0000/L	8,11	4	-	4	8	7	8,6	7,8	8	7	7
-12V	0000/L	-	5	-	-	-	-	-	-	-	-	-
+5V	CC34/H	16	-	-	1	16	14	16	14	16	14	14
+12V	CC34/H	-	8	-	-	-	-	-	-	-	-	-
$\overline{CK}$	CC34(F)	10	-	-	-	-	-	-	-	-	-	-
SO	0000(F)	9	-	-	-	-	-	-	-	-	-	-
P8	A486	3	3	-	-	-	-	-	-	-	-	-
DO	1UC2	-	6	53	-	-	-	-	-	-	-	-
CK	0000(F)	-	2	-	-	3	-	1,9	-	1	13	-
CO	CC34(F)	-	7	54	-	-	-	-	-	-	-	-
DI	1UC2	-	-	36	-	-	-	-	-	-	-	-
SI	A486	-	-	-	2	2	5	-	-	-	-	-
$\overline{SI}$	IUC2	-	-	-	-	-	6	7	-	-	-	-
Q3A	4UA4	-	-	-	-	-	-	3,14	-	-	-	-
Q4B	PP9U	-	-	-	-	-	-	2	-	-	-	-
TP5	PP9U	-	-	-	-	-	-	-	3	-	-	-
SYNC	0000(F)	-	-	-	-	-	-	-	1	7	-	-
SYNC	CC34(F)	-	-	-	-	-	-	-	2,11	-	12	-
PS	0000(F)	-	-	-	-	-	-	-	6	6	-	-
PR	0000(F)	-	-	-	-	-	-	-	4	-	11	-
$\overline{LINT}$	0000/L	-	-	-	-	-	-	-	12	-	-	9
$\overline{L/R}$	0000(F)	-	-	-	-	-	-	-	-	-	-	1,2,8
LS	CC34/H	-	-	-	-	-	-	-	-	-	-	10
$\overline{L/R}$	CC34(F)	-	-	-	-	-	-	-	-	-	-	3,5
$\overline{RINT}$	659A	-	-	-	-	-	-	-	-	-	-	6
RS	HPAP	-	-	-	-	-	-	-	-	-	-	4
$\overline{INT}$	659A	-	-	37	-	-	-	-	-	-	-	11

CHAPTER 22

PARTS LIST

CONTENTS

NOTE

This chapter gives parts list information for assemblies and chassis-mounted components only. Detailed components lists for the printed circuit boards and cards are given at the end of the respective chapters.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

BASIC ASSEMBLY (ST 79545)

Sub-Assemblies

	Main Chassis Assembly	ST79541
	Front Panel Assembly	ST79542
	Power Supply Module	ST79546
	Second Mixer/640 MHz Module	ST79544
	Display Driver Card	ST79784
	Processor Card	ST79794
	Extender Card	ST79810
	IF Filter Card	ST80453
	AGC Card	ST80495
	Demodulator Card	ST80499

Connectors

PL49/PL69	Cable Assembly	BA81839
	Comprising:	
	Plug, coaxial, straight (PL49)	938893
	Plug, coaxial, right-angle (PL69)	938894
	Cable, coaxial, semi-rigid	938895
SK2/SK28	Cable Assembly	BA82056/1
	Comprising:	
	Socket, 20-way (2-off)	934819
	Cable, flat, 20-way	939396
SK3/SK29	Cable Assembly	BA82050/2
	Comprising:	
	Socket, 20-way (2-off)	934819
	Cable, flat, 20-way	939396
SK5/SK27	Cable Assembly	BA82063/1
	Comprising:	
	Socket, 26-way (2-off)	934820
	Cable, flat, 26-way	939395
SK10/SK14	Cable Assembly	BA81224/1
	Comprising:	
	Socket, Coaxial, Straight (2 off)	939469
	Cable, Coaxial, VRM 110	925438
SK17/SK31	Cable Assembly	BA81117/1
	Comprising:	
	Socket, Coaxial, Straight (SK 11)	939469
	Socket, Coaxial, Right-angle (SK31)	939470
	Cable, Coaxial, VRM 1110	925438

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
SK15/SK36		Cable Assembly			BA81117/3
		Socket, Coaxial, Straight (SK 15)			939469
		Socket, Coaxial, Right-angle (SK 36)			939470
		Cable, Coaxial, VRM 110			925438
SK16/SK37		Cable Assembly			BA81117/4
		Comprising:			
		Socket, Coaxial, Straight (SK 16)			939469
		Socket, Coaxial, right-angle (SK37)			939470
		Cable, Coaxial, VRM 110			925438
SK62/63/64/65		Cable Assembly			
		Comprising:			
		Terminal, receptacle (4 off)			939265
		Insulating Boot (4 off)			939266
		Wire, Red, 32/0.2			CD77486/2
		Wire, Black, 32/0.2			CD77486/122
Miscellaneous					
		O ring seal (front panel to case)			BD80818/2
		O ring seal (rear panel to case)			BD80819/2
		O ring seal (lower supply to rear panel)			BD80819/1
		Rear Panel Casting			EA82221
		Case			EA80811
		Screw, Socket (front and rear panel fixing)			938757
		Screw, captive (power supply fixing)			AD79562
		Allen key, 4mm			908503
		Spare fuse, 6.3A			922454
		Trimming Tool			921603
		Trimming Tool			927294
		Desiccator Assembly			909909

NOTE: When the receiver is fitted with an internal frequency standard (type 9442 or type 9420) an additional trimming tool is supplied to facilitate adjustment.

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		MAIN CHASSIS ASSEMBLY (ST 79541)			
Capacitors			volts		
C1-C6	1n	Ceramic, Feed through	50	+80 -20	930250
C7	Not used				
C8	1n	Ceramic, Feed through	50	+80 -20	930250
C9,C10	Not used				
C11	1n	Ceramic, Feed through	50	+80 -20	930250
C12	Not used				
C13 -C19	1n	Ceramic, Feed through	50	+80 -20	930250
C20	330 p	Cermaic, Feed through	50	+80 -20	940991
C21 -C25	1 n	Ceramic, Feed through	50	+80 -20	930250
C26 -C29	See Second Mixer/640 MHz Module (Chapter 12)				
C30	2200	Electrolytic	40	+50 -10	941063
C31 -C35	100 n	Ceramic Plate	100 V	20	938857
Connectors					
PL30/SK20		Cable Assembly			BA81119/6
		Comprising:			
		Plug, coaxial, straight (PL30)			945475
		Socket, coaxial, right-angle (SK20)			939470
		Cable, coaxial VRM 110			925438
PL31/SK24		Cable assembly			BA891119/4
		Comprising:			
		Plug, coaxial, straight (PL31)			945475
		Socket, coaxial, right angle (SK24)			939470
		Cable, coaxial VRM110			925438
PL35/SK21		Cable assembly			BA81119/9
		Comprising:			
		Plug, coaxial, straight (PL35)			945475
		Socket, coaxial, right angle (SK21)			939470
		Cable, coaxial, VRM 110			925438
PL36/SK23		Cable assembly			BA81119/5
		Comprising:			
		Plug, coaxial straight (PL36)			945475
		Socket, coaxial, right-angle (SK23)			939470
		Cable, coaxial, VRM 110			925438
PL37/SK25		Cable assembly			BA81119/7
		Comprising:			
		Plug, coaxial, straight (PL 37)			945475
		Socket, coaxial, right-angle (SK 25)			939470
		Cable, coaxial, VRM 110			925438
SK7		Cable Assembly			BA82062
		Comprising:			
		Socket, 26-way			931537
		Cable, flat, 26-way			939395

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
SK18/SK26		Cable Assembly			BA81118/2
		Comprising:			
		Socket, coaxial, right-angle (2 off)			939470
		Cable, coaxial, VRM 110			925438
SK19/SK22		Cable assembly			BA11118/1
		Comprising:			
		Socket, coaxial, right-angle (2 off)			939470
		Cable, coaxial, VRM 110			925438
SK35		Cable assembly			BA81225/1
		Comprising:			
		Socket, coaxial, right-angle			939470
		Cable, coaxial, VRM 110			925438
SK39		Cable assembly			BA82057
		Comprising:			
		Socket, 16-way			934518
		Cable, flat, 16-way			939923
SK40		Cable assembly			BA82059
		Comprising:			
		Socket, 10-way			931535
		Cable, flat, 10-way			939399
SK41		Cable assembly			BA92060
		Comprising:			
		Socket, 10-way			931535
		Cable, flat, 10-way			939399

Sub-Assemblies

Synthesizer Board		ST79782
Mother board		ST79792
20 MHz Reference Board		ST79798
First Mixer/VCO Board		ST79802
Lowpass filter		BD81227
Frequency Standard:	9442	933706
	9420	921601

Miscelleneous

Synthesizer compartment cover	BD81202
20 MHz compartment cover	BD81204
First Mixer compartment cover	BD81206
Synthesizer cover gasket	BD81832
20 MHz cover gasket	BD81833
First Mixer cover gasket	BD81834
Connector, frequency standard, B7G	907140

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
		FRONT PANEL ASSEMBLY (ST 79542)			
Resistors					
	10 k	Variable (IF GAIN)			BD81249
	10 k	Variable (VOLUME)			BD81249
Fuses					
FS1	6.3 A	Fuselink			922454
		Fuseholder			927656
Connectors					
SK4		Cable Assembly			BA82304
		Comprising:			
		Socket, 26-way (SK4)			934820
		Cable, flat, 26-way			939395
SK8/SK46		Cable Assembly			BA81229/1
		Comprising:			
		Socket, Coaxial, straight (SK8)			939469
		Socket, BNC (VIDEO)			916506
		Cable, coaxial VRM 110			925438
SK9/SK45		Cable Assembly			BA81229/2
		Comprising:			
		Socket, Coaxial, Straight (SK9)			939469
		Socket, BNC (IF3)			916506
		Cable, coaxial VRM 110			925438
SK12/SK44		Cable Assembly			BA81229/3
		Comprising:			
		Socket, coaxial, straight (SK12)			939469
		Socket, BNC (IF2)			916506
		Cable, coaxial VRM 110			925438
SK30/SK47		Cable Assembly			BA91228/1
		Comprising:			
		Socket, coaxial, right-angle (SK30)			939470
		Socket, BNC (EXT STD)			916506
		Cable, coaxial VRM 110			925438

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
SK44		Straight 50 ohms BNC co-ax			916506
SK45		Straight 50 ohms BNC co-ax			916506
SK46		Straight 50 ohms BNC co-ax			916506
SK47		Straight 50 ohms BNC co-ax			916506
SK48		Adaptor, Bulkhead (ANTENNA)			940563
SK66		Cable Assembly			BA82035
		Comprising:			
		Socket 26-way (SK66)			934820
		Cable, flat, 26-way			939395
SK75		Terminal receptacle			939265
SK76		Terminal receptacle			939265
SK78		Socket 26-way			934820
SK79		Socket 26-way			934820

Assemblies

		Display and Switch Board			ST79806

Miscellaneous

		Window, red			BD79552
		Window Seal			BD79573
		O Ring Seal, Front Bezel assy			BD80819/2
		Knob (IF GAIN, VOLUME)			BD81290
		Handle			CD80566
		Keypad Moulding			CD80564
		Cable Clamp			AD82442

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number

POWER SUPPLY MODULE (ST79546)

Power Supply Board	ST79808
Heatsink	DA79579
PSU Switching Board	ST81938
PSU Linear Board	ST81940
Captive screw, M3 x 12 mm	AD81988
Connecting Socket 26 way	934820
Connecting Socket 26 way	934820

POWER SUPPLY BOARD ASSEMBLY (ST79808) Part of ST79546

Resistors			W		
R1	47k	Metal Oxide	0.25	2	913496
R2	1k0	Metal Oxide	0.25	2	913489
R3	2k2	Metal Oxide	0.25	2	916546
R4	47k	Metal Oxide	0.25	2	913496
R5	10k	Metal Oxide	0.25	2	914042
R6	270k	Metal Oxide	0.25	2	923598
R7	2k2	Metal Oxide	0.25	2	916546
R8	270k	Metal Oxide	0.25	2	923598
R9	270k	Metal Oxide	0.25	2	923598
R10	100k	Metal Oxide	0.25	2	915190
R11	2k2	Metal Oxide	0.25	2	916546
R12	100k	Metal Oxide	0.25	2	915190
R13	4k7	Metal Oxide	0.25	2	913490
R14	10k	Metal Oxide	0.25	2	914042
R15	2k2	Metal Oxide	0.25	2	916546
R16	1k2	Metal Oxide	0.25	2	911179
R17	33k	Metal Oxide	0.25	2	913495
R18	470k	Metal Oxide	0.25	2	920758
R19	100k	Metal Oxide	0.25	2	915190
R20	1k0	Metal Oxide	0.25	2	913489
R21	1k0	Metal Oxide	0.25	2	913489
R22	1k8	Metal Oxide	0.25	2	911148
R23	820k	Metal Oxide	0.25	2	917065
R24	1k0	Ceramic			920315
R25	1k8	Metal Oxide	0.25	2	811148
R26	820k	Metal Oxide	0.25	2	917065
R27	2k2	Ceramic			920310

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors			V		
C1	1µ0	Tantalum Tabular	40		931177
C2	10µ	Tantalum Tabular	63		939262
C3	220µ	Tantalum Tabular	10		938988
C4	47µ	Tantalum Tabular	35		938987
C5	4µ7	Tantalum Tabular	35		938983
C6	22p	Ceramic Disc	500		940026
C7	10n	Ceramic Disc	250		900067
C8	220p	Ceramic Disc	500		931148
C9	47µ	Tantalum Tabular	35		938987
C10	15µ	Tantalum Tabular	20		935601
C11	1µ0	Tantalum Tabular	63		938981
C12	22µ	Tantalum Tabular	40		931179
C13	1µ0	Tantalum Tabular	63		938981
C14	1µ0	Tantalum Tabular	40		931177
C15	1µ0	Tantalum Tabular	40		931177
C16	1µ0	Tantalum Tabular	40		931177
C17	1µ0	Tantalum Tabular	40		931177
C18	1µ0	Tantalum Tabular	40		931177
Inductors			W		
L1		Inductor Assembly			AT81882
L2		Inductor Assembly			AT81881
L3	47µH	Inducator	0.2	10	939160
Transformer					
T1		Transformer Assembly			AT81883
Diodes					
D1		1N4448			938991
D2		1N4448			938991
D3		Zener Z58 33			920569
D4		1N4448			938991
D5		1N4448			938991
D6		1N4448			938991
D7		1N4448			938991
D8		1N4448			938991
D9		1N4448			938991
D10		1N4448			938991
D11		1N4448			938991
D12		1N4448			938991
D13		1N4448			938991
D14		1N4448			938991
D15		1N4448			938991

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Transistors					
TR1		BCY71			930992
TR2		VN88 AF			938868
Integrated Circuits					
ML1		4047 CMS			930992
ML2		78L12			938880
ML3		78L12			938880
ML4		78L12			938880
ML5		239			938962
Connectors					
PL27		Plug 26 way			938858
PL62		Terminal Spade			939264
PL63		Terminal Spade			939264
PL66		Terminal Spade			939264
TP1		Terminal Assembly			936148
TP2		Terminal Assembly			936148
TP3		Terminal Assembly			936148
TP4		Terminal Assembly			936148
TP5		Terminal Assembly			936148
TP6		Terminal Assembly			936148
TP7		Terminal Assembly			936148
TP8		Terminal Assembly			936148

SWITCHING REGULATOR BOARD (ST81938)
(Part of ST79546)

Resistors

	Ω				
R1	68 k	Metal Oxide	0.25	2	916478
R2	3.9 k	Metal Oxide	0.25	2	915074
R3	36 k	Metal Oxide	0.25	2	921437
R4	4.7 k	Metal Oxide	0.25	2	913490
R5	100	Metal Oxide	0.25	2	910388
R6	1.5 k	Metal Oxide	0.25	2	911166
R7	0.1	Wirewound	2.5	10	933956
R8	390	Metal Oxide	0.25	2	916331
R9	1 M	Metal Oxide	0.25	2	943027
R10	4.7 M	Carbon Film	0.25	10	925536
R11	10 k	Metal Oxide	0.25	2	914042
R12	4.7 k	Metal Oxide	0.25	2	913490
R13	1 k	Metal Oxide	0.25	2	913489
R14	1.3 k	Metal Oxide	0.25	2	920760
R15	680	Metal Oxide	0.25	2	910113

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R16	4.7 k	Metal Oxide	0.25	2	913490
R17	680	Metal Oxide	0.25	2	910113
R18	4.7 k	Metal Oxide	0.25	2	913490
R19	1 k	Metal Oxide	0.25	2	913489
R20	220	Wirewound	2.5	5	913604
R21	33	Wirewound	2.5	5	913584
R22	4.7 k	Metal Oxide	0.25	2	913490
R23	1.8 k	Metal Oxide	0.25	2	911148
R24	1 k	Variable, preset			939863
R25	1.2 k	Metal Oxide	0.25	2	911179
R26	2 k	Metal Oxide	0.25	2	917652
R27	0.1	Wirewound	2.5	10	933956
R28	0.1	Wirewound	2.5	10	933956
R29	15 k	Metal Oxide	0.25	2	920646
R30	5 k	Variable, preset			939865
R31	15 k	Metal Oxide	0.25	2	920645
R32	330 k	Metal Oxide	0.25	2	940250
R33	1 k	Metal Oxide	0.25	2	913489
R34	2 k	Metal Oxide	0.25	2	917652
R35	2.2 k	Metal Oxide	0.25	2	916546
R36	150	Metal Oxide	0.25	2	910389
R37	150	Metal Oxide	0.25	2	910389
R38	5.6 k	Metal Oxide	0.25	2	918128
R39	3.3 k	Metal Oxide	0.25	2	910111
R40	330	Metal Oxide	0.25	2	915690
R41	2.7 k	Metal Oxide	0.25	2	916548
R42	1 k	Metal Oxide	0.25	2	913489
R43	2.2	Wirewound	2.5	5	917141
R44	100	Metal Oxide	0.5	2	913973
R45	82	Metal Oxide	0.5	2	909550
R46	82	Metal Oxide	0.5	2	909550
R47	15	Wirewound	2.5	5	913576
R48	0.1	Wirewound	2.5	10	933956
R49	0.1	Wirewound	2.5	10	933956
R50	0.1	Wirewound	2.5	10	933956
R51	15	Wirewound	2.5	5	913576
R52	4.7 k	Metal Oxide	0.25	2	913490
R53	100	Metal Oxide	0.5	2	913973
R54	2.2	Wirewound	2.5	5	917141
R55	4.7 k	Metal Oxide	0.25	2	913490
R56	330	Metal Oxide	0.5	2	910200
R57	18 k	Metal Oxide	0.25	2	900994
R58	3.3 k	Metal Oxide	0.25	2	910111

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Capacitors			V		
	F				
C1	10 µ	Tantalum tubular	63	20	939262
C2	470 p	Silver mica	100	2	939326
C3	47 µ	Tantalum solid	63	10	940849
C4	10 µ	Tantalum tubular	63	20	939262
C5	1 µ	Tantalum tubular	35	20	939848
C6	220 n	Polyester	100	20	931161
C7	22 n	Polyester	400	20	931166
C8	1 n	Silver mica	100	2	934054
C9	150 µ	Tantalum tubular	16	20	939849
C10	10 n	Polycarbonate	400	10	931136
C11	150 µ	Tantalum tubular	16	20	939849
C12	68 µ	Tantalum tubular	16	20	939850
C13	15 µ	Tantalum tubular	20	20	938986
C14	33 µ	Tantalum tubular	25	20	931175
C15	10 n	Polycarbonate	400	10	931136
C16	3.3 µ	Tantalum tubular	63	20	939852
C17	10 n	Polycarbonate	400	10	931136
C18	220 n	Polyester	100	20	931161
C19	33 µ	Tantalum tubular	25	20	931175
C20	6.8 µ	Tantalum tubular	35	20	939851
C21	47 µ	Tantalum tubular	35	20	938987
C22	6.8 µ	Tantalum tubular	35	20	939851
Inductors					
	H				
L1	20 µ	Choke Assembly			AT82302
L2	200 µ	Choke Assembly			AT82300
L3	470 µ	Choke Assembly			AT82301
L4	4.7 m	Choke Assembly			AT82295
L5	35 m	Choke Assembly			AT82296
L6	75 m	Choke Assembly			AT82297
Transformers					
T1		Transformer Assembly			AT82303
Connectors					
PL62)					
PL63)		Blade, 0.25 in, PCB mounting			939264
PL68		Plug, 26-way			938858

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
Diodes					
D1		Silicon 1N4149			923222
D2		Zener, 3.3 V, 400mW BZX79C3V3			941517
D3		Silicon Rectifier 60S1			939152
D4		Zener, 4.7 V, 400 mW BZX79C4V7			926429
D5		Silicon 1N4149			923222
D6		Silicon 1N4149			923222
D7		6A Silicon Rectifier VES1303			939862
D8		Silicon 1N4149			923222
D9		7A Silicon Rectifier BYW29-100			937939
D10		Silicon 1N4149			923222
D11		Zener, 7.5 V, 400mW BZX79C7V5			941639
D12		Zener, 36 V, 1.3 W BZT03C36			943490
D13		Fast Recovery BYV95C			940652
D14		Fast Recovery BYV95C			940652
D15		6A Silicon Rectifier VES1303			939862
D16		Fast Recovery BYV95C			940652
D17		6A Silicon Rectifier VES1303			939862
D18		6A Silicon Rectifier VES1303			939862
D19		Fast Recovery BYV95C			940652
D20		Fast Recovery BYV95C			940652
D21		6A Silicon Rectifier VES1303			939862
D22		Fast Recovery BYV95C			940652
D23		Fast Recovery BYV95C			940652
D24		Fast Recovery BYV95C			940652
D25		Fast Recovery BYV95C			940652
D26		Silicon 1N4149			923222
D27		Fast Recovery BYV95C			940652
D28		Silicon 1N4149			923222
D29		Silicon 1N4149			923222
SCR1		Silicon Controlled Rectifier 52600B			939151
Transistors					
TR1		NPN Silicon BC107			911929
TR2		PNP Silicon BD140			941548
TR3		PNP Silicon BCY71			911928
TR4		PNP Silicon D45H11			939149
TR5		NPN Silicon BD139			941547
TR6		PNP Silicon BCY71			911928
TR7		NPN Silicon BFY51			908753
TR8		PNP Silicon 2N4037			922991
TR9		NPN Silicon BU 407			939859
TR10		NPN Silicon BU 407			939859

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
TR11		NPN Silicon BFY51			908753
TR12		PNP Silicon 2N4037			922991
Integrated Circuits					
ML1		Switching Regulator SG1524			937496
ML2		Quad Comparator LM224J			938978
ML3		Switching Regulator SG1524			937496
Miscellaneous					
		Test Point			936148
		Heat Sink (TR7, 8, 11, 12)			939473
		14-pin IC Socket			930605
		16-pin IC Socket			930606

LINEAR REGULATOR BOARD (ST81940) (Part of ST79546)

Resistor	Ω		Watts		
R1	10 k	Metal Oxide	0.25	2	914042
R2	2.2 k	Metal Oxide	0.25	2	916546
R3	2.2 k	Metal Oxide	0.25	2	916546
R4	2.2 k	Metal Oxide	0.25	2	916546
R5	820	Metal Oxide	0.25	2	917065
R6	390	Metal Oxide	0.5	2	909771
R7	4.7 k	Metal Oxide	0.25	2	913490
R8	1 M	Metal Oxide	0.25	2	943027
R9	470	Metal Oxide	0.5	2	918030
R10	0.1	Wirewound	2.5	10	933956
R11	0.1	Wirewound	2.5	10	933956
R12	390 k	Metal Oxide	0.25	10	941960
R13	20 k	Variable, preset			939866
R14	4.7 k	Metal Oxide	0.25	2	913490
R15	820 k	Metal Oxide	0.25	2	943028
R16	2.2 k	Metal Oxide	0.25	2	916546
R17	10 k	Metal Oxide	0.25	2	914042
R18	10 k	Metal Oxide	0.25	2	914042
R19	10 k	Metal Oxide	0.25	2	914042
R20	470	Metal Oxide	0.25	2	920758
R21	4.7 k	Metal Oxide	0.25	2	913490
R22	470	Metal Oxide	0.25	2	920758
R23	2 k	Variable, preset			939864
R24	8.2 k	Metal Oxide	0.25	2	918202
R25	2.2 k	Metal Oxide	0.25	2	916546

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
R26	4.7 k	Metal Oxide	0.25	2	913490
R27	2.2 k	Metal Oxide	0.25	2	916546
R28	1 M	Metal Oxide	0.25	2	943027
R29	0.1	Wirewound	2.5	10	933956
R30	0.1	Wirewound	2.5	10	933956
R31	270 k	Metal Oxide	0.25	2	923598
R32	4.7 k	Metal Oxide	0.25	2	913490
R33	4.7 k	Metal Oxide	0.25	2	913490
R34	47 k	Metal Oxide	0.25	2	913496
R35	5.6 k	Metal Oxide	0.25	2	918128
R36	10k	Metal Oxide	0.25	2	914042
R37	560 k	Metal Oxide	0.25	2	926902
R38	10 k	Metal Oxide	0.25	2	914042
R39	4.7 k	Metal Oxide	0.25	2	913490
R40	4.7 k	Metal Oxide	0.25	2	913490
R41	2.7 k	Metal Oxide	0.25	2	916548
R42	10 k	Metal Oxide	0.25	2	914042
R43	22 k	Metal Oxide	0.25	2	913493
R44	47 k	Metal Oxide	0.25	2	913496
R45	47 k	Metal Oxide	0.25	2	913496
Capacitors			V		
	F				
C1	6.8 µ	Tantalum tubular	35	20	939851
C2	1 µ	Polyester	100	10	940387
C3	1 µ	Polyester	63	10	921639
C4	1 µ	Tantalum tubular	35	20	939848
C5	100 p	Ceramic Disc	500	10	917417
C6	1 µ	Polyester	100	10	940387
C7	100 n	Polyester	100	10	931130
C8	1 µ	Tantalum tubular	35	20	939848
C9	100 n	Polyester	100	10	931130
C10	68 µ	Tantalum tubular	16	20	939850
C11	15 µ	Tantalum tubular	20	20	938986
C12	4.7 µ	Tantalum tubular	50	20	939853
C13	100 p	Ceramic Disc	500	10	917417
C14	470 n	Polyester	100	20	931132
C15	100 n	Polyester	100	10	931130
C16	15 u	Tantalum tubular	20	20	938986
C17	100 p	Ceramic Disc	500	10	917417
C18	100 µ	Tantalum tubular	10	20	931172
C19	47 µ	Tantalum tubular	35	20	938987
C20	47 µ	Tantalum tubular	35	20	938987

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
C21	220 µ	Tantalum tubular	10	20	938988
C22	1 µ	Tantalum tubular	35	20	939848
C23	1 n	Ceramic Plate	50	10	940312
Inductors					
L1	H / I m	Choke			938956
L2		Coil Assembly			AT82298
L3		Coil Assembly			AT82298
L4		Coil Assembly			AT82298
Connectors					
PL27		Plug, 26-way			938858
PL67		Plug, 26-way			938858
Diodes					
D1		Silicon 1N4149			923222
D2		Zener, 39 V, 3.25 W BZT03C39			922213
D3		Zener, 39 V, 3.25 W BZT03C39			922213
D4		Zener, 24 V, 2.5 W BZX70C24			926830
D5		Silicon Recitifer 1N4002			923564
D6		Zener, 30 V, 3.25 W BZT03C30			927452
D7		Silicon Recitifer 1N4002			923564
D8		Silicon 1N4149			923222
D9		Silicon 1N4149			923222
D10		Zener, 4.3 V, 400 mW BZX79C4V3			941638
D11		Zener, 22 V, 400 mW BZX79C22			941643
D12		Silicon 1N4149			923222
D13		Silicon 1N4149			923222
D14		Zener, 6.2 V, 400 mW 1N823A			917244
D15		Zener, 9.1 V, 400 mW BZX79C9V1			921751
D16		Zener, 22 V, 400 mW BZX79C22			941643
D17		Silicon 1N4149			923222
D18		Silicon 1N4149			923222
D19		Zener, 10 V, 400 mW BZX79C10			930320
D20		Silicon Recitifer 1N4002			923564
Transistors					
TR1		PNP Silicon BCY71			911928
TR2		NPN Silicon BC107			911929
TR3		PNP Silicon BCY71			911928
TR4		NPN Silicon BFY51			908753
TR5		V-MOS Power FET IVN5201CNE			939860

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
TR6		PNP Silicon BCY71			911928
TR7		NPN Silicon BFY51			908753
TR8		V-MOS Power FET IVN5201CNE			939860
TR9		NPN Silicon BC107			911929
Integrated Circuits					
ML1		+24 V Regulator MC7824CT			939854
ML2		Quad Comparator LM224J			938978
ML3		-24 V Regulator MC7924CT			939856
ML4		-12 V Regulator MC7912CT			939855
Miscellaneous					
		Test Point			936148
		14-pin IC Socket			930605
		SECOND MIXER/640 MHz MODULE (ST 79544)			
Sub-Assemblies					
		Second mixer/640 MHz board			ST79804
		Bandpass filter			BD91226
Capacitors					
C26	1n	Ceramic, feed through	50	+80 -20	930250
C27	1n	Ceramic, feed through	50	+80 -20	930250
C28	1n	Ceramic, feed through	50	+80 -20	930250
C29	1n	Ceramic, feed through	50	+80 -20	930250
Connectors					
PL12/SK70		Cable Assembly			BA81119/1
		Comprising:			
		Plug, coaxial, straight (PL12)			945475
		Socket, coaxial, right-angle (SK70)			939470
		Cable, coaxial, VRM 110			925438
PL13/SK59		Cable Assembly			BA81119/2
		Comprising:			
		Plug, coaxial, straight (PL13)			945475
		Socket, coaxial, right-angle (SK59)			939470
		Cable, coaxial VRM 110			925438
PL14/SK60		Cable Assembly			BA81119/3
		Comprising:			
		Plug, coaxial, straight (PL14)			945475
		Socket, coaxial, right-angle (SK61)			939470
		Cable, coaxial, VRM 110			925438

Cct. Ref.	Value	Description	Rat	Tol %	Racal Part Number
PL15/SK61		Cable Assembly			BA81119/8
		Comprising:			
		Plug, coaxial, straight (PL15)			945475
		Socket, coaxial, right-angle (SK61)			939470
		Cable, coaxial, VRM 110			925438
SK6		Cable Assembly			BA82061
		Comprising:			
		Socket, 10-way			931535
		Cable, flat, 10-way			939399
SK13/SK17		Cable Assembly			BA81117/2
		Comprising:			
		Socket, coaxial, straight (SK13)			939469
		Socket, coaxial, right-angle (SK17)			939470
		Cable, coaxial, VRM 110			925438
SK38		Cable Assembly			BA92058
		Comprising:			
		Socket, 10-way			931535
		Cable, flat, 10-way			939399
Miscellaneous					
		Module cover			BD81208
		Cover gasket			BD81831
		Captive screw (10 off)			AD81213
		Cable clamp			AD82036

APPENDIX 1

PROCESSOR CARD, (ST79794)

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Tables

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APPENDIX 1

PROCESSOR CARD, ST79794

INTRODUCTION

1. The RA 1794A receiver uses four devices from the 1800 microprocessor family, and all are located on the processor card. The CDP 1802 C-MOS Central Processing Unit (CPU) is an 8-bit register-orientated device which, in this application, uses a pair of CDP 1868 memory latch and decoder devices to interface with the memory devices (ROM, RAM, and EAROM) fitted to the processor card. The remaining device of the 1800 family is a CDP 1851 programmable input/output (PIO) interface device, which has two high-speed 8-bit I/O parts. One of these is used to produce a number of data strobe signals and to control a 16-line analogue multiplex circuit, whilst the other forms the main communications link between the CPU and the remainder of the receiver. The circuit diagram of the card is given in fig 7.1 (at the end of the chapter).

NOTE:
Fault diagnosis for this Processor Card is covered in Appendix 2.

CENTRAL PROCESSING UNIT

2. A simplified block diagram of the CDP 1802 CPU is given in fig 7 (a). This shows the register-orientated architecture of the device and also shows all external connections; these are described in the following paragraphs.

MA0-MA7 Memory Address Bus

3. The high order byte of a 16-bit memory address is placed on the memory address bus and is loaded into external address latches (in this application, a pair of CDP 1868 memory latch and decoder devices) by timing pulse TPA. The low-order byte of the 16-bit memory address then appears on the memory address bus after termination of the TPA pulse.

Q Output

4. A single bit output from the CPU which can be set or reset under program control. In this application, the Q output is used to continuously flash a light emitting diode (LED), mounted on the processor card, whilst the program is running.

$\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$ Inputs

5. These two control inputs allow the selection of one of four modes, as given in table 1. In this application, the $\overline{\text{WAIT}}$ input is not used (permanently connected to +5 V) and this limits the operational modes to RESET and RUN according to the state of the $\overline{\text{CLEAR}}$ input.

TABLE 1 CPU Control Modes

$\overline{\text{CLEAR}}$	$\overline{\text{WAIT}}$	MODE
0	0	LOAD
0	1	RESET
1	0	PAUSE
1	1	RUN

6. The logic level present at the $\overline{\text{CLEAR}}$ input is controlled by a power on/power fail detector circuit (para. 35). This circuit is so arranged that when the receiver is switched on, the RESET mode is automatically entered and is then quickly followed by the RUN mode. During the RESET mode, internal registers I, N, and Q are reset, the data bus is set to the all-zero state, and interrupts are enabled. Immediately following the transition from the RESET mode to the RUN mode, an initialisation cycle commences (which clears registers R(0), X and P) and this is followed either by a DMA (direct memory access) cycle or a fetch operation from memory location 0000, dependent on the state of the $\overline{\text{DMA IN}}$ and $\overline{\text{DMA OUT}}$ inputs (Para 9).

XTAL and CLOCK Connections

7. The CPU has an internal oscillator that requires an external crystal connected between the XTAL and CLOCK pins. In this application however, an externally derived 2 MHz clock signal is used and this is applied to the CLOCK pin.

$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ Flag Inputs

8. These four flag inputs may be used to convey status information to the CPU, provided the software includes the appropriate conditional branch instructions. In this application, $\overline{\text{EF1}}$ is used to convey the setting of a card-mounted TEST switch, $\overline{\text{EF2}}$ is fed from a 16 millisecond-period squarewave output signal from a clock divider, and is used to update various software timers, $\overline{\text{EF3}}$ is used to convey the output signal from a digital-to-analogue converter, and $\overline{\text{EF4}}$ is used to signal when a register on the optional SCORE interface card is full of SCORE data.

$\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$, and $\overline{\text{INT}}$ Inputs

9. These are all interrupt request signals, where $\overline{\text{DMA-IN}}$ has the highest priority, followed by $\overline{\text{DMA-OUT}}$ and then $\overline{\text{INT}}$. The three basic ways in which the CPU can communicate with input/output (I/O) devices are (1) programmed I/O, (2) interrupt I/O and (3) direct memory access (DMA). In the programmed I/O mode, all data transfer is controlled and timed by the program. In the interrupt I/O mode, the CPU responds to an I/O generated signal. In the DMA mode a direct high-speed data channel is established between memory and the I/O device.

10. The levels present at the $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$ and $\overline{\text{INT}}$ inputs are sampled by the CPU during the interval between the leading edges of two timing signals TPA and TPB (para 13). When either $\overline{\text{DMA-IN}}$ or $\overline{\text{DMA-OUT}}$ is detected, the CPU completes the execution of the current instruction. Data is then loaded into ($\overline{\text{DMA-IN}}$) or read out of ($\overline{\text{DMA-OUT}}$) memory at the address contained in register R(0). R(0) is then incremented and the process continues for as long as the $\overline{\text{DMA}}$ signal is present. In this application, $\overline{\text{DMA IN}}$ is unused (permanently connected to + 5V), whilst $\overline{\text{DMA OUT}}$ is used to execute a test routine when signature analysis is selected (see Chap 21).

11. The $\overline{\text{INT}}$ input is produced by the optional SCORE interface card (Chap 16); it occurs every eight SCORE clock periods and also when a correct synchronisation code is detected.

SC1 and SC0 Outputs

12. The levels present at these two outputs denote the current CPU state; they are available for external gating purposes, although are not used in this application. The CPU machine cycle during which an instruction byte is fetched from memory is called state S0 (SC1 and SC0 both at '0'), whilst the cycle during which the instruction is executed is called S1 (SC0 at '1'). During the execution of a program, the CPU state generally alterates between S0 and S1. When however, a DMA request is processed, or an interrupt request is acknowledged, then the CPU state is called S2 or S3 respectively. The four CPU states are shown in table 2.

TABLE 2 : CPU State Coding

STATE TYPE	STATE CODE LINES	
	SC1	SC0
S0 (FETCH)	0	0
S1 (EXECUTE)	0	1
S2 (DMA)	1	0
S3 (INTERRUPT)	1	1

TPA, TPB, $\overline{MWR}$ and $\overline{MWD}$ Timing Signals

13. Positive-going timing pulses occur at both TPA amd TPB once in each machine cycle (TPB follows TPA). The state of $\overline{MWR}$ and $\overline{MRD}$ determines whether a byte is to be read from the addressed location, written into it, or neither operation performed (table 3).

TABLE 3 : Memory Control Lines

CPU LINES	MEMORY READ	MEMORY WRITE	NON-MEMORY OPERATION
$\overline{MRD}$	0	1	1
$\overline{MRW}$	1	0	1

NO, N1 and N2 Input/Output Command Lines

14. These software-controlled outputs are used as command codes or I/O device selection codes. All three lines are at '0' except when an I/O instruction is being executed. During this time, the state of the three N bits is the same as that of the least significant three bits in the N register.

B0 to B7 Data Bus

15. This is an 8-bit bi-directional bus for the transfer of data between the CPU, memory and I/O devices.

Vcc, Vdd and Vss Supply Lines

16. The internal voltage supply Vdd is isolated from the input/output voltage supply Vcc so that the processor may operate at maximum speed whilst interfacing with external circuitry operating from a +5 V supply (Vcc must be less than or equal to Vdd, and all outputs swing from Vss (0V) to Vcc. In this application, the Vdd and Vcc lines are commoned and fed from a +5 V supply.

MEMORY INTERFACE DEVICE CDP 1868

17. Two of these devices are used to interface the CPU with the memory devices (ML10 and ML11 - fig 7.1). Each device consists of a 4-bit latch and a decoder; a functional diagram is given in fig. 7(b) and associated truth tables are given in tables 4 and 5.

TABLE 4 : CDP 1868 $\overline{CS}$ Outputs

	INPUTS								OUTPUTS			
	$\overline{MRD}$	$\overline{MWR}$	CE1	$\overline{CE2}$	$\overline{CE3}$	CK	MA3	MA2	$\overline{CS0}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
	0	0	1	0	0	1	0	0	0	1	1	1
	0	1	1	0	0	1	0	0	0	1	1	1
	1	0	1	0	0	1	0	0	0	1	1	1
	0	0	1	0	0	1	0	1	1	0	1	1
	0	1	1	0	0	1	0	1	1	0	1	1
	1	0	1	0	0	1	0	1	1	0	1	1
*	0	0	1	0	0	1	1	0	1	1	0	1
	0	1	1	0	0	1	1	0	1	1	1	1
*	1	0	1	0	0	1	1	0	1	1	0	1
	0	0	1	0	0	1	1	1	1	1	1	0
	0	1	1	0	0	1	1	1	1	1	1	0
	1	0	1	0	0	1	1	1	1	1	1	0
	1	1	X	X	X	X	X	X	1	1	1	1
	X	X	0	X	X	X	X	X	1	1	1	1
	X	X	X	1	X	X	X	X	1	1	1	1
	X	X	X	X	1	X	X	X	1	1	1	1

X denotes either 0 or 1

* For these two conditions $\overline{CS2}$ follows $\overline{MWR}$ regardless of the state of $\overline{MRD}$.

TABLE 5 : CDP 1868 A8 & A9 Outputs

INPUTS			OUTPUTS	
CK	MA1	MA0	A9	A8
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1
0	X	X	PREVIOUS STATE	

18. The high-order byte of a 16-bit memory address from the CPU is clocked into ML10 and ML11 by the TPA clock signal, and the decoded result is latched at the chip select ($\overline{CS0}$ to $\overline{CS3}$), A8 and A9 output pins, for application to the addressed device. The low order byte of the 16-bit memory address from the CPU is then applied direct to the addressed device.

READ ONLY MEMORY

19. Two 4 K by 8-bit read only memory (ROM) devices, desigated PD1 and PD2, are provided, which contain the operating program and a number of test routines. An examination of tables 3, 4 and 5 shows that with $\overline{MRD}$ at a '0' and $\overline{MWR}$ at a '1', a '0' is produced at the $\overline{CS}$ input of PD1 for CPU read addresses 0000 to 0FFF, whilst a '0' is produced at the $\overline{CS}$ input of PD2 for CPU read addresses 1000 to 1FFF.

20. The ROM devices usually fitted to the processor card are of the ultra-violet (UV) erasable type (these may be identified from all other types in that a transparent window is set into the top surface). Where UV erasable type devices are in use they must at all times be protected from direct light.

ROM REPLACEMENT INSTRUCTIONS

21. Ensure that both ROM devices fitted to the processor card have the same last suffix letter and the same program issue number. When ordering a replacement ROM device, quote the RA 1794A serial number, the B/S number (if present) of the processor card and the full information printed on the label attached to the faulty device. The label information takes the following form:

P82227/1/A
Iss 1

Where:

(1) P82227 is the system software reference number

(2) The first suffix number (1 in this example) is the programmed device (PD) number.

(3) The second suffix (A in this example) defines the type of ROM device.

(4) Iss denotes the program issue number (1 in this example)

RANDOM ACCESS MEMORY

22. The RAM comprises two 256 by 4-bit static C-MOS devices, ML4, ML5, connected as a single 256 by 8-bit memory. The separate data input (DI) and data output (DO) connections are joined and connected to the CPU data bus. Two chip select signals, $\overline{CS1}$ and CS2, are provided. The $\overline{CS1}$ signal, which is produced by ML11 ($\overline{CS0}$ output), goes to a '0' for addresses in the range 4000 to 4 off (tables 3,4 and 5), whilst the CS2 signal is fed from the $\overline{CLEAR}$ line. This line is normally at '1' and goes to '0' should the level of the +5 VA supply fall below +4.75 V (para.35). The RAM devices are powered from the + 5 VB supply, which is maintained by the inclusion of a high-value capacitor (C8) during supply interruptions lasting up to one minute (see para. 35 for details).

ELECTRICALLY ALTERABLE ROM

23. ML2 and ML3 are 1K by 4-bit, non-volatile electrically alterable read only memory (EAROM) devices. They are used for the storage of pre-programmed channel information (channels 00 to 99), as well as the storage of the latest front panel setting information so that the receiver returns to these same settings when switched on again after a period of non-usage (the stored front panel control setting data is updated at one-minute intervals).

24. Each EAROM device has an active-low chip-enable ($\overline{CE}$) input, an active-low write enable ($\overline{WE}$) input, and two mode control inputs, C0 and C1. The code set on the two mode control lines (table 6) is latched into the device on the negative-going edge of the $\overline{CE}$ signal.

TABLE 6 : EAROM Mode Control

C1	C0	Mode
0	0	READ
0	1	WRITE
1	0	BLOCK ERASE (not used)
1	1	WORD ERASE

25. In order to write to EAROM, the $\overline{WE}$ input must be taken low when the address and data bus lines are in a valid and static state. To achieve this, the '1' at the $\overline{MRD}$ output of the CPU is delayed by four clock cycles by shift register stage ML20a and is then inverted by ML19a to enable address decoder ML11. This allows time for the address and data bus lines to become static before either ML2 or ML3 is enabled by a '0' at the $\overline{CS2}$ or $\overline{CS3}$ output respectively of ML11. Tri-state buffer ML14a allows

protection of EAROM under software control (via ML13 pin 23), and also when signature analysis is selected by the closure of switch SB. ML19a is subsequently reset by ML20b, when $\overline{MWR}$ and $\overline{MRD}$ both return to the '1' normal (non-memory-operation) state.

EAROM ADDRESSING

26. The EAROM devices require that each write or erase cycle is followed by a dummy read cycle. When in the read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is latched in the write or erase mode. Since the C0 and C1 mode control pins are connected to the A10 and A11 address lines (which come from the A8 and A9 outputs respectively of ML11), the required sequence of modes is attained under software control by the application of the appropriate addrssses. The read, write and erase addresses for both ML2 and ML3 (which may be obtained by examination of tables 3, 4, 5 and 6) are given in table 7.

TABLE 7 : EAROM Addresses

ADDRESS									MODE	DEVICE
HEX	15	14	13	12	11	10	9	8		
6000	0	1	1	0	0	0	0	0	READ	ML2
63FF	0	1	1	0	0	0	1	1		
6400	0	1	1	0	0	1	0	0	WRITE	
67FF	0	1	1	0	0	1	1	1		
6C00	0	1	1	0	1	1	0	0	WORD ERASE	
6FFF	0	1	1	0	1	1	1	1		
7000	0	1	1	1	0	0	0	0	READ	ML3
73FF	0	1	1	1	0	0	1	1		
7400	0	1	1	1	0	1	0	0	WRITE	
77FF	0	1	1	1	0	1	1	1		
7C00	0	1	1	1	1	1	0	0	WORD ERASE	
7FFF	0	1	1	1	1	1	1	1		

SELF-TEST SWITCHES

27. Six in-line single-pole switches, labelled SA to SF, are provided to facilitate testing of the processor card. For normal receiver operation, all switches are set to the open position. To test the card, SA is set to the closed position, whilst SB is closed for signature analysis. The remaining four switches, SC to SF, are for the selection of a particular test program (stored in ROM). The state of these switches is periodically checked by the CPU by the application of any address in the range 3000 to 3FFF. This results in a negative - going pulse at the $\overline{CS3}$ output of ML10, the disable condition is momentarily removed from tri-state buffer ML14b, and the state of the switches is conveyed to the CPU via data bus lines D0 to D3.

DIGITAL-TO-ANALOGUE CONVERTER

28. The remaining chip select output from ML10 not so far mentioned is the $\overline{CS2}$ output; this is produced for any address in the range 2000 to 2FFF, and is used to enable an 8-bit digital-to-analogue converter (DAC) ML9. This stage is used by the CPU for the measurement of analogue signals, in conjunction with a software successive approximation routine. The analogue signals to be measured are applied to a 16-way multiplexer device ML17 and the software selected one-of-sixteen analogue output signal at the COMMON pin is applied to a comparator stage ML1a. A successive approximation routine then increments or decrements the binary input applied to the digital-to-analogue converter (ML9 1 to 8 inputs) until the analogue output from ML8 is equal to that from ML17 i.e. until the output signal from comparator ML1a changes state. The binary level at the D-to-A converter input then represents, in digital format, the measured analogue signal.

29. Of the sixteen analogue signals applied to ML17, two only, namely IF GAIN WIPER and AGC MONITOR, are measured by the receiver operating program; the remainder are measured during the receiver self-test routines. The level at the AGC MON line is monitored, at 8 ms intervals, for squelch control purposes, and is remeasured, at 32 ms intervals, for metering purposes. The IF GAIN WIPER level is measured, at 32 ms intervals (local control only), and the resulting level at TP7 is then transferred to the sample-and-hold capacitor C4. The voltage stored in C4 thus represents the manual IF gain level, and is applied to the AGC card via edge connector pin 43 (it is also applied to ML17, for test purposes only).

30. For most of the time, i.e. except when the AGC MON level is being monitored and measured, and when the IF GAIN WIPER level is being measured, the 16-way multiplexer stage ML17 is inhibited, and analogue switch ML12b is enabled, by a '1' at the port B line 5 output from ML13. At the same time, the digital level established during the last IF GAIN WIPER measurement is applied to the D-to-A converter to maintain the correct charge in capacitor C4.

CDP 1851 PIO DEVICE

31. ML12 (fig 7 (c)) is a programmable two-port input/output device, with four programmable modes, input, output, bidirectional and bit-programmable. Port A is programmable for all modes, whilst Port B is programmable for the input, output and bit-programmable modes. In this application, Port A is normally programmed for the output mode and is periodically briefly set to the input mode when data input is required, whilst Port B is set to the bit programmable mode with all lines programmed to be outputs.

32. The P10 device is cleared by a high-to-low transition at the $\overline{\text{CLEAR}}$ input when the unit is switched on. This resets a number of internal registers and also sets both A and B ports to the input mode. The required mode is then programmed by the application of the appropriate levels to the control inputs CS (chip select), RA0 and RA1 (registerer selection). WR/$\overline{\text{RE}}$ (WRITE/$\overline{\text{READ ENABLE}}$) and RD/$\overline{\text{WE}}$ (READ/$\overline{\text{WRITE ENABLE}}$), to select the control register (table 8), together with the appropriate levels at the data bus lines 0 to 7 (table 9).

TABLE 8 : P10 Control Inputs

CS	RA1	RA0	RD/$\overline{\text{WE}}$	WR/$\overline{\text{RE}}$	ACTION
0	X	X	X	X	
X	0	0	X	X	NO OPERATION BUS IN
X	X	X	0	0	HIGH IMPEDANCE STATE
X	X	X	1	1	
1	0	1	1	0	* READ STATUS REGISTER
1	0	1	0	1	LOAD CONTROL REGISTER
1	1	0	1	0	* READ PORT A
1	1	0	0	1	LOAD PORT A
1	1	1	1	0	* READ PORT B
1	1	1	0	1	LOAD PORT B

X denotes 0 or 1

* READ : RD/$\overline{\text{WE}}$ at '1' and WR/$\overline{\text{RE}}$ at '0' at trailing edge of CLOCK (TPA).

TABLE 9 : Control Register Selection

DATA BUS								
7	6	5	4	3	2	1	0	ACTION
0	0	X	B	A	X	1	1	Set Port Input Mode
0	1	X	B	A	X	1	1	Set Port Output Mode
1	0	X	0	1	X	1	1	Set A Port Bidirectional Mode
1	1	X	B	A	X	1	1	Set Port Bit-Programmable Mode

A and B: 1 to Set

X : Either 0 or 1

33. Port A is used for the two-way transfer of data between the CPU and other parts of the receiver on the application of the appropriate strobe from ML18, which is controlled by the Port B output. When Port A is set to the input mode, a dummy read cycle is executed to produce a '1' at the A RDY output; this is applied to the D input of strobe pulse generator stage ML19b such that at the next positive-going transition of the TPA clock signal, the following action ensues:

(1) A '0' is produced at the $\overline{Q}$ output of ML9b; this removes the inhibit condition and a positive-going strobe pulse is produced at one of the sixteen output pins, as selected by the levels at the 0 to 3 Port B output lines.

(2) A '1' is produced at the Q output of ML9b; this is applied to the A STROBE input of ML13, and the data at the Port A input lines (resulting from the strobe pulse produced by ML18) is loaded into ML13 for transfer to the CPU via the data bus.

(3) ML19b is then reset by the next TPB clock pulse, the '0' at the Q output terminates the A STROBE pulse, and the '1' at the $\overline{Q}$ output reapplies the inhibit condition to ML18.

34. The action of the circuit when Port A is set to the output mode is similar, except that the output data is latched at the Port A output pins before a '1' occurs at the A RDY output to produce the strobe pulse.

POWER FAIL DETECTOR

35. The purpose of the power fail detector is to produce the power-on $\overline{CLEAR}$ signal required by the CPU (ML6) and the PIO (ML13), and subsequently to reapply the $\overline{CLEAR}$ signal should the +5 VA supply fall below +4.75 V (the lower supply threshold of the ROM devices).

36. Both the +5 VA and +5 VB supplies are derived from the +5.5 V supply at card edge connector pin 63. The +5 V supply from series - pass transistor TR2 is used to power the two static RAM devices ML4, ML5, and also the analogue switch device ML12. In the event of a supply interruption, TR1 ceases conduction, and turns off TR2; this isolates resevoir capacitor C8 which then maintains the +5 VB supply for a period of not less than one minute. At the same time, ML12c is disabled by the $\overline{CLEAR}$ signal from ML1d (para 38), and the +5 VB supply is applied to the $\overline{CS1}$ inputs of both ML4 and ML5 to prevent chip selection (ML12 is powered from the +5 VB supply to ensure that pin 4 of ML12c is in the high impedance condition during supply interruptions).

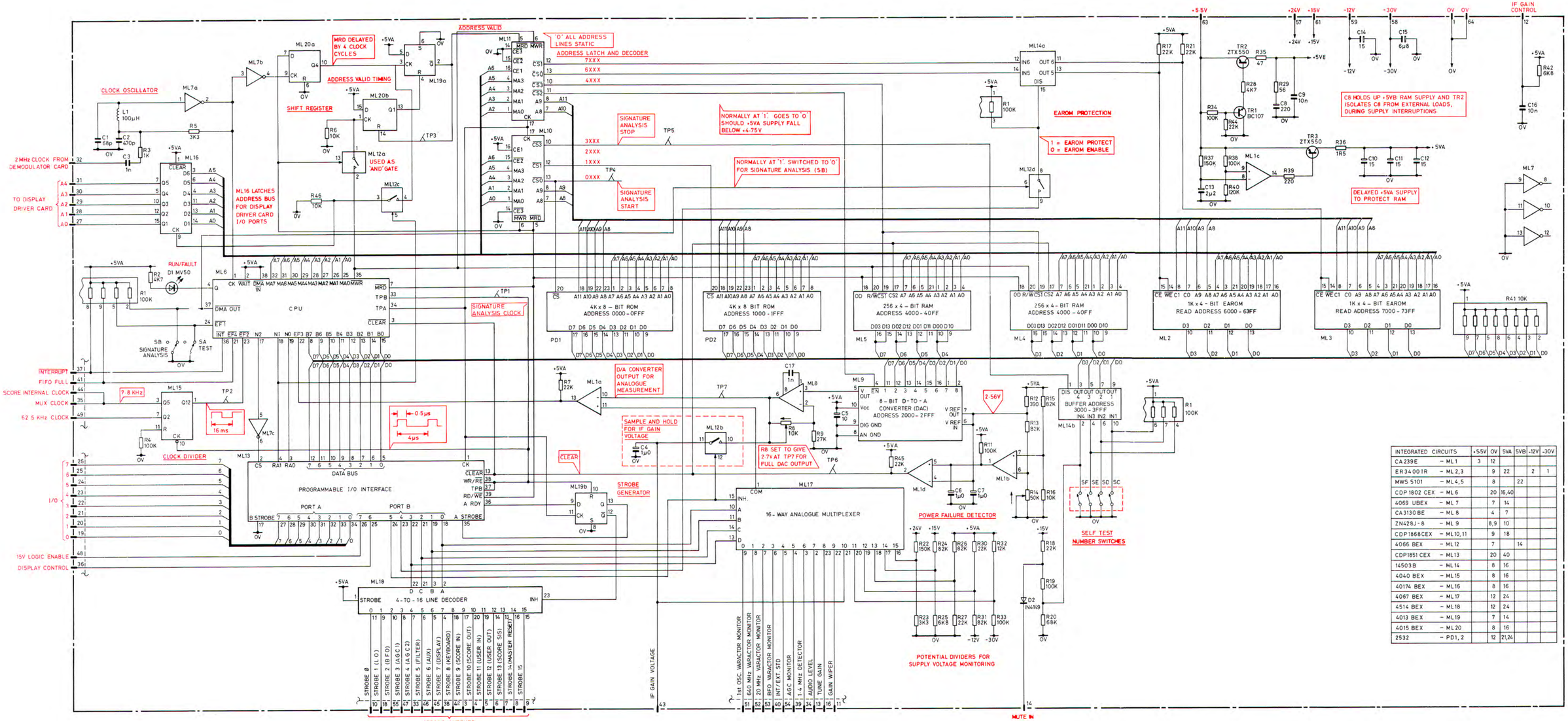
37. ML1c and series-pass transistor TR3 are included to delay the application of the +5 VA supply until the +5 VB supply has been established; this is a requirement of the static RAM devices, ML4 and ML5.

38. The $\overline{CLEAR}$ signal is produced by comparator stages ML1b and ML1d. Potential divider R15, R16, sets the level at the non-inverting input of ML1b to approximately +0.5 V, whilst potential divider R13, R14, applies a sample of the +2.56 V reference output from digital-to-analogue converter stage ML9 to the inverting input of ML1b. The level at the inverting input of ML1b is normally lower than that at the non-inverting input (resulting in a nominal +5 V output) and R14 is adjusted so that the

output of ML1b changes state (goes to '0') when the level of the +5 VA supply falls below +4.75 V. Thus at switch on, the $\overline{\text{CLEAR}}$ line is at '0' and goes to a '1' when the level at the non-inverting input of ML1d rises above the +2.56 V reference level (the time constant R1, C6 ensures that the $\overline{\text{CLEAR}}$ line is held low for the duration of several CPU clock cycles to initialise the CPU, and the inclusion of ML1d is to impart a fast rise time at the end of the $\overline{\text{CLEAR}}$ signal). Should the level of the +5 VA supply subsequently fall below + 4.75 V, then the output of ML1b changes state and the resulting $\overline{\text{CLEAR}}$ signal is maintained until the +5 VA supply returns to normal.

CLOCK DIVIDER

39. The TPB clock signal from the CPU (ML6 pin 33) is applied to the clock input of a 12-stage binary counter ML15. This produces a nominal 16 millisecond period squarewave signal at the Q12 output (used by the CPU for timing various events), a 7.8 kHz signal at the Q5 output (SCORE interval clock and display multiplexer), and a 62.5 kHz signal at the Q2 output (used by the power supply generation circuit).

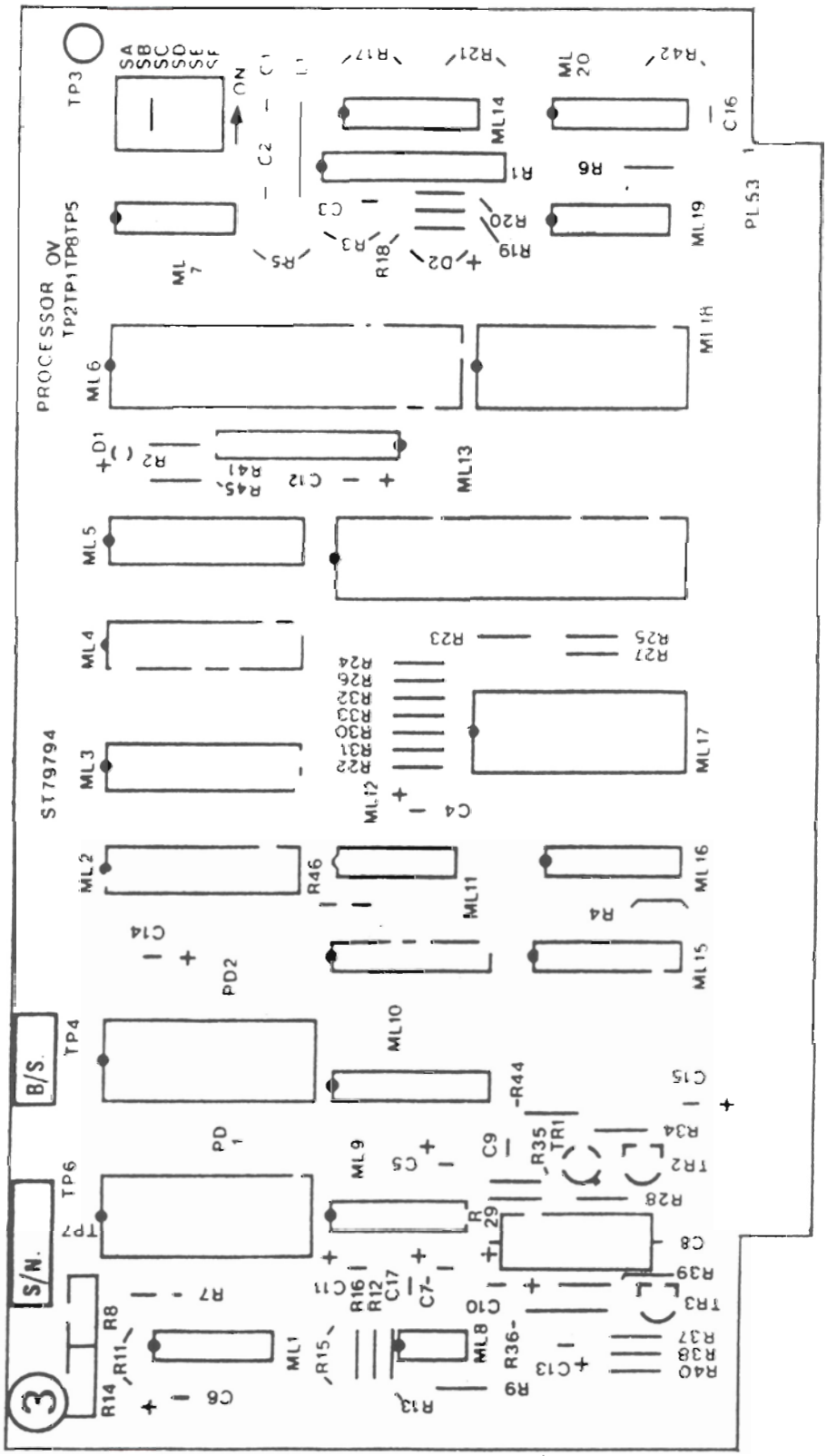


INTEGRATED CIRCUITS		+5.5V	0V	5VA	5VB	-12V	-30V
CA 239E	– ML 1	3	12				
ER 3400 1R	– ML 2,3		9	22		2	1
MWS 5101	– ML 4,5		8		22		
CDP 1802 CEX	– ML 6		20	16,40			
4069 UBEX	– ML 7		7	14			
CA 3130 BE	– ML 8		4	7			
ZN 428J - 8	– ML 9		8,9	10			
CDP 1868 CEX	– ML 10,11		9	18			
4066 BEX	– ML 12		7		14		
CDP 1851 CEX	– ML 13		20	40			
14503 B	– ML 14		8	16			
4040 BEX	– ML 15		8	16			
40174 BEX	– ML 16		8	16			
4067 BEX	– ML 17		12	24			
4514 BEX	– ML 18		12	24			
4013 BEX	– ML 19		7	14			
4015 BEX	– ML 20		8	16			
2532	– PD 1, 2		12	21,24			

RACAL TH2449 DC79794 1/6 1/2 TH2449 DC79794 1/6 2/2

Circuit: Processor Card

Fig. App. 1.1



DA79793/4

RACAL

TH 2449/3 ST79794

APP 1

Layout:
Processor Card

Fig. App.1.2

APPENDIX 2

FAULT DIAGNOSIS

(ST79794 PROCESSOR CARD)

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APPENDIX 2

FAULT DIAGNOSIS

(ST79794 PROCESSOR CARD)

INTRODUCTION

1. This appendix provides information to assist in the location of a faulty component or sub-assembly in equipments fitted with the ST79794 Processor Card. A series of checks and suggestions are given with references to the self-test routines contained in Chapter 19 and to functional test routines contained in chapter 20. Signature analysis tests are included towards the end of the chapter.

TEST EQUIPMENT

2. The items of test equipment required are as given in chapter 20 with the following additional items:

Signature Analyser - Hewlett Packard HP5004A
Plug, 26-way, Amphenol 62GB-16J-16-26P
Resistor, 10K, 0.25W (Racal 914042)
Resistor, 22K, 0.25W (Racal 913493)

PRELIMINARY

3. Set the front panel POWER switch to OFF, disconnect all external connectors, and if necessary, transfer the unit to a flat, clean working suface.

4. If the nature of the fault is unknown, carry out the functional test procedures given in Chapter 20. These make use of some of the built-in self-test routines detailed in Chapter 19. If a fault is indicated whilst carrying out these routines, or if the routines do not run, refer to the manual tests (with the same respective test numbers) given in this chapter (paras. 7 to 19).

5. If the fault is associated with the optional SCORE interface card, then carry out the SCORE interface tests given in chapter 20.

6. If the self-test routines do not reveal a fault condition, further checks of the logic circuitry can be made by carrying out the signature analysis routines given in paras. 25 to 47. Once the digital circuitry has been checked, a signal generator can be connected to the receiver antenna socket and the signal paths can be checked using the information provided on the appropriate circuit diagrams.

MANUAL TESTS

7. The following paragraphs detail the manual tests to be carried out when a fault is indicated whilst carrying out the self-test routines (described in Chapter 19 and called in Chapter 20). For ease of reference, each manual test is given the same number as that of the associated self-test routine.

Test M00/a - Self Test Does Not Run

8. (1) Check whether the RUN/FAULT indicator D1 on the processor card is flashing (dimly) on and off. If not, check that switches SA to SF on the processor card are all set to the open position, and check the power supplies on the processor card (using the extender card), as follows:

SUPPLY	MONITORING POINT
+5.5V	Edge connector pin 63
+5VA	ML6 pin 40
+5VB	ML12 pin 14

(2) If the +5.5V supply is present and either the +5VA or the +5VB supply is incorrect, replace the processor card or check the supply circuitry, TR1, TR2, TR3, ML1.

(3) If the +5.5V supply is not present at edge connector pin 63 on the processor card, trace back to the power supply module. If necessary, unplug each card, in turn, to check for a short circuit.

(4) Run the processor card test routine, as follows:

(a) Set the front panel POWER switch to OFF.

(b) Set switch SA on the processor card to the closed position, and ensure that the remaining switches SB to SF are all set to the open position.

(c) Set the front panel POWER switch to ON and check that after approximately five seconds the RUN/FAULT indicator D1 on the processor card illuminates.

(5) If the processor card test routine fails to illuminate the RUN/FAULT indicator, replace the processor card or carry out the hardware signature analysis checks given in paras. 33 to 38 to localise the fault.

(6) If the processor card test routine is completed successfully, suspect a faulty display driver card, a faulty display and switch board, or a wiring fault. Check the front panel display using the procedure given in para. 42, and, if necessary, carry out the display driver card signature analysis routine (also para. 42).

Test M00 - ROM Check Sum Fault

9. (1) Replace the processor card or the ROM devices PD1 and PD2.

(2) If the fault persists following ROM replacement, replace the processor card or carry out the following:

(a) Check the supplies to each individual integrated circuit on the processor card.

(b) Carry out the processor card test routine, as described in para. 8(4).

(c) Carry out the processor card signature analysis routines given in paras. 33 to 38.

Test M01 - RAM Failure

10. Replace the processor card with a known serviceable spare, or carry out the following:

(1) Check the RAM devices on the processor card (ML4 and ML5) by replacement.

(2) Carry out the signature analysis routines given in paras. 28 to 33.

Test M02 to M06 - Power Supply Failure

11. Self-test routines 02 to 06 check the +5V, -12V, -30V, +15V and +24V supplies, in that order, on the processor card. Each voltage level is firstly scaled down using a potential divider, and is then applied, in turn, to a D to A converter via a multiplexer stage. The level of each supply is checked to ensure that it lies between preset upper and lower limits; if a supply level is found to be out of range by more than approximately plus or minus 10%, the test number is displayed, together with FAULT and either H (high) or L (low). If the +5V supply is out of range (test number 02 displayed), check whether any further supplies are out of range by pressing and releasing the UP key followed by the ENTER key. If all of the supplies are out of range, suspect the analogue monitoring circuitry on the processor card (ML1, ML8, ML9, ML17).

12. The levels of the +24V and -30V supplies are set by potentiometers R24 and R27 respectively on the power supply module; the remaining supplies are non-adjustable. If a supply is faulty, trace back to the power supply module. If necessary, unplug boards or remove cards to check for a short circuit.

Test M7 - EAROM Fault

13. Replace the processor board or carry out the following:

(1) Check for the correct supplies (+5V, -12V, -30V, 0V) at each of the two EAROM devices, ML2 and ML3, on the processor card.

(2) Carry out the signature analysis routine given in para. 30 to check the EAROM address and data bus lines.

(3) If no faults are found, suspect a faulty EAROM device.

Test M8 - Channel Checksum Fault

14. Self-test number 8 provides a confidence check to ensure that channel frequency and mode data stored in EAROM has not altered since it was initially entered. If this test fails, then attempt to re-enter the channel frequency and mode data. If this cannot be achieved, an EAROM fault must be suspected and the procedures given in para. 13 should be followed.

Test M010 - 20 MHz Reference Fault

15. (1) Ensure that either:

(a) The unit is fitted with an internal frequency standard module.

or (b) that a suitable external frequency standard is connected to the EXT STD socket on the front panel.

(2) Replace the 20 MHz reference board, or use the oscilloscope to check the internal/external reference interface circuits, and the 20 MHz phase-locked loop circuit, with reference to the circuit diagram of the 20 MHz reference board (fig 9.1).

Test M011 - 640 MHz Oscillator Fault

16. (1) Use the oscilloscope to check that 10 MHz squarewave signals, at TTL levels, are present at TP1 and TP2 on the second mixer/640 MHz board.

(2) Replace the second mixer/640 MHz board, or carry out the following:

(a) Carry out the alignment procedure for the second mixer/640 MHz board given in Chapter 20, para. 25.

(b) If the varactor line voltage at TP4 cannot be adjusted to +5.5V, replace the board or use the oscilloscope to check the phase comparator circuitry and use the spectrum analyser to check the 640 MHz oscillator and buffer amplifier circuitry.

Test M012 - Local Oscillator Fault

17. (1) Ensure that the 20 MHz reference signal is present at PL19 on the synthesizer board.

(2) Replace the synthesizer board and/or the first mixer/VCO board, or carry out the following:

(a) Carry out the alignment procedures for the synthesizer board given in Chapter 20, para. 22. If the specified performance cannot be achieved, carry out the signature analysis routines given in para. 38.

(b) Carry out the alignment procedures for the first mixer/VCO board given in Chapter 20, para. 23. If the specified performance cannot be achieved, replace the board or use the RF millivoltmeter and signal generator to check the first mixer/VCO board, with reference to the circuit diagram given in Chapter 11.

Test M13 - BFO Fault

18. (1) Ensure that the 20 MHz reference signal is present at edge connector pin 27 (resistor R1) on the demodulator card.

(2) Replace the demodulator card, or carry out the following:

(a) Carry out the signature analysis routine for the demodulator card given in para. 45.

(b) Use the oscilloscope to check the BFO circuitry on the demodulator card, as shown on sheet 1 of the circuit diagram, fig. 15.1.

Test M14 First Local Oscillator Sweep Test Failure

19. (1) Ensure that the 20 MHz reference signal is present at PL19 on the synthesizer board.

(2) Replace the synthesizer board and/or the first mixer /VCO board, or carry out the following:

(a) Run self-test routine 14 to determine the fault code. Refer to Chapter 19, para. 16 for an interpretation of the fault code and then carry out measurement checks on the synthesizer board, with refernce to the circuit diagram (Chapter 10, Fig. 10.1).

(b) If the varactor voltage is out of range, carry out the alignment procedures for the synthesizer board given in Chapter 20, para. 22 and the first mixer /VCO board given in Chapter 20, para.23.

(c) If the specified performance cannot be achieved, replace the first mixer /VCO board or use the RF millivoltmeter and signal generator to check the first mixer /VCO board, with reference to the circuit diagram given in Chapter 11, Fig. 11.1

(d) If the synthesizer is not functioning correctly, check the power supplies to each integrated circuit.

(e) Carry out the signature analysis routine given in Appendix 2, Para. 43.

(f) If the fault code indicates the varactor volts were 'Non-monotonic' or 'Step too large' (codes 03 and 04) use the oscilloscope to check the fast lock circuitry.

(g) Use the oscilloscope and frequency counter to check the synthesizer board, with reference to Chapter 10.

Test M15 - 1.4 MHz Detector Fault

20. (1) Ensure that the 1.4 MHz signal level at the AGC card edge connector pin 53 is approximately 100 mV rms. If so then the fault is on the AGC card, AGC Detector circuitry or the interconnection from the AGC card edge connector pin 34 (1.4 MHz Detector Output) to the processor card.

Replace the AGC card or, using the oscilloscope, check the AGC Detector circuitry with reference to the circuit diagram Fig. 14.1.

(2) If the 1.4 MHz signal is not present at pin 53:-

(a) Check the IF Filter card by removing SK14 from the second mixer module and connecting SK14 to the signal generator set to 21.4 MHz at +60 dB µV. If this does not result in a 1.4 MHz signal

at pin 53 then the fault is on the IF filter card. Ensure that the 20 MHz reference signal at the IF filter card edge connector pin 27 is at a level of 0 dBm ± 3 dB. Replace the IF filter card or use the oscilloscope to check the signal path with reference to the circuit diagram Fig. 13.1.

(b) If the procedure in (a) produces a 1.4 MHz signal at the AGC card edge connector pin 53 then the fault is on the signal path on either the First mixer/VCO board or the second mixer module or their interconnections.

(c) Reconnect SK14 onto the second mixer module. Disconnect SK13 from the second mixer module. Connect the signal generator, set to 661.4 MHz at +60 dBμV to PL13 on the second mixer module. If this does not produce a 1.4 MHz signal at the AGC card pin 53 then the fault is on the second mixer module.

Ensure that the 20 MHz reference is present at SK15 at a level of 0 dBm ± 3 dB.

Replace the second mixer module or using the millivoltmeter and oscilloscope check the circuitry with reference to the circuit diagram Fig. 12.1

(d) If the procedure in (c) produces a 1.4 MHz signal at the AGC card then the fault is in the Band Pass Filter or the 1st Mixer/VCO board.

Using the signal generator and millivoltmeter ensure that the insertion loss through the Band Pass filter at 661.4 MHz does not exceed 4.5 dB.

Replace the 1st Mixer/VCO board or check its circuitry with reference to the circuit diagram Fig. 11.1.

Test M16 - AGC Monitor Test Failure

21. (1) Replace the AGC card, or carry out the following:

(2) Run self-test routine 16 to determine the fault code. Refer to Chapter 19, para. 18 for an interpretation of the fault code. Carry out measurement checks on the AGC card with reference to the circuit diagram Fig. 14.1

(3) Check operation of outputs AGC1, 2, and 3 by varying the IF Gain Control on the Front Panel whilst in manual only control. Refer to Chapter 3 para. 27 to select AGC time constants and Manual only control.

Test M17 - Audio Detector Test Failure

22. (1) Replace the Demodulator card or carry out the following:

(2) Ensure that the 20 MHz reference signal is present at the Demodulator Card edge connector pin 27 at a level of 0 dBm ± 3 dB.

(3) Run self-test Routine 17 to determine the fault code. Refer to Chapter 19, Para. 18 for an interpretation of the fault code. Carry out measurement checks on the Demodulator Card Audio circuitry with reference to the circuit diagram Fig. 15.1

Test M18 - BFO Beat against first local oscillator

23. (1) Ensure no antenna input is connected.

(2) Replace the Demodulator card and/or the Synthesizer board or carry out the following:

(a) Carry out the signature analysis routines for the Demodulator card given in Appendix 2, para. 45.

(b) Use the Oscilloscope and frequency counter to check the BFO circuitry and audio detect on the demodulator card, with reference to the circuit diagrams given in Chapter 15, Figs. 15.1 and 15.2

(c) Carry out the signature analysis routines for the Synthesizer board given in Appendix 2, para. 43.

(d) Use the oscilloscope and frequency counter to check the synthesizer board, with reference to Chapter 10.

Test M31 - Keyboard Fault

24. Replace the display and switch board with a known serviceable spare, or carry out the following:

(1) Set the receiver POWER switch to OFF and mount the display driver card onto the extender card (inserted into the display driver card connector -slot 1).

(2) With reference to the circuit diagrams of the display and switch board (fig 5.1) and the display driver card (fig 6.1), use the multimeter to check that no short-circuts are present between switch matrix column inputs and row outputs (PL/SK3 and PL/SK29).

(3) Use the multimeter to check for continuity between the appropriate column input and row output for each front-panel key (when depressed).

SIGNATURE ANALYSIS

25. When the receiver is operating correctly, the non-sequential program instructions cause continuously changing data patterns to be present within the logic circuitry. Because these data patterns are continuously changing, data analysis or data checking using conventional test equipment (oscilloscope, logic probes, etc.) becomes almost impossible. The signature analysis technique requires the processor to continuously execute a single instruction (or continuously run a short test program) and so produce repetitive data patterns at selected data nodes throughout the logic circuitry. If the signature analyser START, STOP, CLOCK and GROUND leads are connected to the appropriate test points on a known serviceable unit, and the signature analyser probe is connected, in turn, to a number of circuit nodes, then a series of unique 4-digit alpha-numeric 'signatures' will be obtained. If these signatures are recorded, they may be used at a later date as a reference when the same tests are made during the test or fault location procedures. If an incorrect signature is found at a particular node, the operator simply traces back through gates, memory devices, etc. until an element with a correct signature at the input and a faulty signature at the output is isolated.

26. Use is made of the signature analyser to interpret the result of the processor card test (SA only closed) should the RUN/FAULT LED fail to illuminate after approximately five seconds from switch-on. The procedure is given in para. 27.

27. The RA 1794A contains two signature analysis routines for testing various parts of the unit. The first to be described is a hardware signature analysis routine (para. 33) for the ST79794 procesor card. The closure of switch SB on the processor card initiates a DMA-OUT sequence where data is read out of ROM at the address contained in CPU internal register R(0). R(0) is then incremented and the process continues for as long as switch SB remains closed. The closure of switches SA and SC (prior to the closure of the POWER switch) causes the operation of a comprehensive software signature analysis routine, for the testing of various parts of the receiver (para. 39 onwards).

Use of Signature Analyser

28. The type of signature analyser required to carry out the procedures given in this chapter has an integral logic probe which may be used as a test instrument independently of the signature measuring capability. The logic probe incorporates a lamp, and this may be used to indicate one of the following four conditions:

(1) Probe lamp OFF (L) - Logic '0' (GND)

(2) Probe lamp ON (H) - Logic '1'

(3) Probe lamp half-on - High impedance/poor logic level

(4) Probe lamp flashing (F) - Data stream.

(5) In the remainder of this appendix, the signatures given all have a flashing probe tip, except where indicated /H or /L to show logic levels as in (1) and (2).

29. The signature analyser has START, STOP and CLOCK inputs for connection to the circuit under test, and a logic probe for connection to a circuit node to obtain a signature. The logic levels at the START, STOP and logic probe inputs are strobed into the signature analyser on either the rising or falling edge of the CLOCK input (as selected by the CLOCK pushbutton. Either rising or falling edges of the START and STOP inputs may be selected to initiate and terminate a time period (window or gate) during which measurement takes place.

30. When the START, STOP, CLOCK and GROUND connections are made correctly and the signature analysis routine is being executed, the GATE indicator should flash. The correct configuration for a particular test can be verified by checking the logic '1' signature, obtained by connecting the probe tip to the positive supply.

31. If the HOLD pushbutton is depressed, the instrument will hold a single one-time signature. The probe can then be removed from the test node whilst the signature comparison is made. The displayed signature is reset by pressing and releasing the RESET button on the probe.

PROCESSOR CARD TEST FAILURE INTERPRETATION

32. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SA on the processor card is set to the closed position, and that the remaining switches SB to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor board as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the receiver POWER switch to ON.

(6) Wait at least five seconds and then connect the signature analyser probe to any convenient +5V connection e.g. ML6 pin 40.

(7) Check the signature obtained with those given below to determine the faulty ROM or RAM device. If the signature obtained does not agree with any of the following, carry out the hardware signature analysis routine for the processor card given in para. 33. If the pass signature is obtained (and the receiver is faulty) the processor card is probably functioning correctly and the remainder of the unit should be checked using the procedures given in paras. 39 onwards.

+5V SIGNATURE/TIP STATE	FAILED DEVICE
P007/H	PASS
7U39/H	ROM PD1
U399/H	ROM PD2
399F/H	RAM ML4
99FA/H	RAM ML5

HARDWARE SIGNATURE ANALYSIS (PROCESSOR CARD)

Clock Divider

33. (1) Set the front panel POWER switch to OFF and mount the processor card onto the extender card (inserted into slot 3).

(2) Set switch SB on the processor card to the closed (on) position, the remaining switches (SA and SC to SF) to the open (off) position.

(3) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	OUT (positive edge)
CLOCK pusbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP2
STOP	TP2
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the points on the processor card given below and check that correct signatures are obtained.

+5V - ML6 pin 40 - 826P/H
0V - Negative end of C8 - 0000/L

(7) Connect the signature analyser probe, in turn, to the points given in table 1 and check that correct signatures are obtained.

Table 1: Clock Divider Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT			
		ML15	ML6	TP	EC
0V	0000/L	8	20	-	-
5V	826P/H	16	16,40	-	-
RESET	0000/L	11	-	-	-
CK	826P	10	33	TP1	-
Q2	2A1F	7	-	-	49
Q5	8P3U	3	-	-	35,44
Q12	U81P	1	23	TP2	-

EC denotes Edge Connector

ROM Devices & Test Switch Buffer

34. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- C690/H
0V	-	Negative end of C40	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 2 and check that correct signatures are obtained.

RAM and EAROM Devices

35. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

Table 2: ROM Device and Test Switch Buffer Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC pin No.)					
		ML6	ML10	ML11	PD1	PD2	ML14
A0	9270	25	1	-	8	8	-
A1	71H0	26	2	-	7	7	-
A2	1AF5	27	-	1	6	6	-
A3	HF6A	28	-	2	5	5	-
A4	825P	29	3	3	4	4	-
A5	U801	30	4	4	3	3	-
A6	C9HC	31	15	16	2	2	-
A7	1511	32	-	-	1	1	-
TPA	0000	34	17	17	-	-	-
$\overline{MRD}$	0000	7	5,6	-	-	-	-
$\overline{MWR}$	C690/H	35		6	-	-	-
$\overline{AV}$	0000	-	-	5,6	-	-	-
0V	0000/L	20	9,14	9,14	12	12	-
+5V	C690/H	16,40	16,18	18	21,24	21,24	8
A8	178U	-	7	-	23	23	16
A9	U9U7	-	8	-	22	22	-
A10	0548	-	-	7	19	19	-
A11	HAA7	-	-	8	18	18	-
$\overline{CS0}$	P254	-	13	-	20	-	-
$\overline{CS1}$	H6AA	-	12	-	-	20	-
$\overline{CS2}$	34UP	-	11	-	-	-	-
$\overline{CS3}$	C690	-	10	-	-	-	1
D0	160H	15	-	-	-	-	-
D1	P360	14	-	-	-	-	-
D2	U6A3	13	-	-	-	-	-
D3	441C	12	-	-	-	-	-
D4	PF1H	11	-	-	-	-	-
D5	315H	10	-	-	-	-	-
D6	PUAU	9	-	-	-	-	-
D7	P7UA	8	-	-	-	-	-

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	- 755U/H
0V	-	Negative end of C8	- 0000/L

Note: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 3 and check that correct signatures are obtained.

Table 3: RAM and EAROM Device Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC PIN No.)								
		ML6	ML10	ML11	ML4	ML5	ML12	ML14	ML2	ML3
0V	0000/L	20	9,14	9,14	8	8	7	8	9	9
5V	755U/H	16,40	16,18	18	-	-	14	16	22	22
A0	H335	25	1	-	4	4	-	-	16	16
A1	C113	26	2	-	3	3	-	-	17	17
A2	7050	27	-	1	2	2	-	-	18	18
A3	0772	28	-	2	1	1	-	-	19	19
A4	C4C3	29	3	3	21	21	-	-	20	20
A5	AA08	30	4	4	5	5	-	-	21	21
A6	7211	31	15	16	6	6	-	-	3	3
A7	A3C1	32	-	15	7	7	-	-	4	4
TPA	0000	34	17	17	-	-	-	-	-	-
$\overline{\text{MRD}}$	0000	7	5,6	-	18	18	-	-	-	-
$\overline{\text{MWR}}$	755U/H	35	-	6	20	20	-	-	-	-
$\overline{\text{AV}}$	0000	-	-	5 -	-	-	-	-	-	
A8	7707	-	7	-	-	-	-	-	5	5
A9	577A	-	8	-	-	-	-	-	6	6
A10	HH86	-	-	7	-	-	-	-	7	7
A11	89F1	-	-	8	-	-	-	-	8	8
$\overline{\text{CS0}}$	A207	-	-	13	-	-	-	14	-	-
$\overline{\text{CS1}}$	H6A3	-	-	12	-	-	-	12	-	-
$\overline{\text{CS2}}$	755U/H	-	-	11	-	-	-	-	-	-
$\overline{\text{CS3}}$	H24U	-	-	10	19	19	-	-	-	-
$\overline{\text{CLEAR}}$	755U/H	3	-	-	17	17	-	-	-	-
$\overline{\text{DMAOUT}}$	0000	37	-	-	-	-	6	15	-	-
D15	755U/H	-	-	-	-	-	8	-	-	-
OUT5	755U/H	-	-	-	-	-	-	13	14,15	-
OUT6	755U/H	-	-	-	-	-	-	11	-	14,15
+5VB	755U/H	-	-	-	22	22	-	-	-	-

Self-Test Switches

36. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V - ML6 pin 40 - 826P/H
0V - Negative end of C8 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 33.

(7) Connect the signature analyser probe, in turn, to the points given in table 4 and check that correct signatures are obtained.

Table 4: Self-Test Switch Signatures

SIGNAL	SIGNATURE/ TIP STATE	SWITCH SETTINGS						TEST POINT	
		F	E	D	C	B	A	ML6	ML14
0V	0000/L	0	0	0	0	C	0	20	8
+5V	826P/H	0	0	0	0	C	0	16,40	16
DIS	0000	0	0	0	0	C	0	-	1
IN1	826P/H	0	0	0	0	C	0	-	10
IN1	0000/L	0	0	0	C	C	0	-	10
OUT1	826P	0	0	0	0	C	0	15	9
OUT1	0000	0	0	0	C	C	0	15	9
IN2	826P/H	0	0	0	0	C	0	-	6
IN2	0000/L	0	0	C	0	C	0	-	6
OUT2	826P	0	0	0	0	C	0	14	7
OUT2	0000	0	0	C	0	C	0	14	7
IN3	826P/H	0	0	0	0	C	0	-	4
IN3	0000/L	0	C	0	0	C	0	-	4
OUT3	826P	0	0	0	0	C	0	13	5
OUT3	0000	0	C	0	0	C	0	13	5
IN4	826P/H	0	0	0	0	C	0	-	2
IN4	0000/L	C	0	0	0	C	0	-	2
OUT4	826P	0	0	0	0	C	0	12	3
OUT4	0000	C	0	0	0	C	0	12	3
$\overline{EF1}$	826P/H	0	0	0	0	C	0	24	-
$\overline{EF1}$	0000/L	0	0	0	0	C	C	24	-

0 = ON

C = OFF

Address Valid Circuit

37. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST PUSHBUTTON	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	TP4
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor board and check that correct signatures are obtained.

+5V	-	ML6 pin 40	-C690/H
OV	-	Negative end of C8	-0000/L

NOTE: If the correct +5V signature is not obtained, carry out the signature analysis routine for the CPU, address bus and address decoder given in para. 38.

(7) Connect the signature analyser probe, in turn, to the points given in table 5 and check that correct signatures are obtained.

Table 5: Address Valid Circuit Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (IC Pin No.)				
		ML6	ML7	ML20	ML19	ML12
+5V	C690/H	-	14	16,15	5,14	14
OV	0000/L	-	7	8,6	6,7	7
CK	C690	1	3	0	0	0
$\overline{CK}$	0000	-	4	9	-	-
$\overline{MRD}$	0000	7	-	7	-	13
MRDD	0000	-	-	10	3	-
$\overline{AV}$	0000	-	-	14	2	-
$\overline{MWR}$	C690/H	35	-	-	-	2
$\overline{MRD}.\overline{MWR}$	0000/L	-	-	1	-	1
AR	0000	-	-	13	4	-

CPU, Address Bus & Address Decoder

38. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switch SB on the processor card is set to the closed position, and that switches SA and SC to SF are all set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)

CLOCK pushbutton	IN (negative edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card, as follows:

START	ML6 pin 32
STOP	ML6 pin 32
CLOCK	ML6 pin 34
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained:

+5V	-	ML6 pin 40	-0001/H
OV	-	Negative end of C8	- 0000/L

(7) Connect the signature analyser probe, in turn, to the points given in table 6 and check that correct signatures are obtained.

Table 6: CPU, Address Bus & Address Decoder Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT		
		ML6	ML10	TP
OV	0000/L	20	9,14	
+5V	0001/H	16,40	16,18	
CK	F	1	-	
$\overline{\text{WAIT}}$	0001/H	2	-	
$\overline{\text{CLEAR}}$	0001/H	3	-	
$\overline{\text{DMA IN}}$	0001/H	38	-	
$\overline{\text{DMA OUT}}$	0000/L	37	-	
TPA	F	34	17	
MA0	HC89	25	1	
MA1	2H70	26	2	
MA2	HPP0	27	-	
MA3	1293	28	-	
MA4	HAP7	29	3	
MA5	3C96	30	4	
MA6	3827	31	15	
MA7	755U	32	-	
$\overline{\text{MRD}}$	0000	7	5	
$\overline{\text{CS0}}$	822A	-	13	TP4
$\overline{\text{CS1}}$	A169	-	12	
$\overline{\text{CS2}}$	CFU3	-	11	
$\overline{\text{CS3}}$	AP96	-	10	TP5

SOFTWARE SIGNATURE ANALYSIS

The signatures in this section relate to PD 82891 Issue 2 software, this is fitted into 'B' series processor cards, ST79794.

Processor Card PIO Device

39. (1) Set the front panel POWER switch to OFF.

(2) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(3) Mount the processor card onto the extender card (inserted into slot 3).

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads to the processor card as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained.

+5V	-	ML6 pin 40	-P254/H
0V	-	Negative end of C8	-0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card clock divider test routine given in para. 33.

(8) Connect the signature analyser probe, in turn, to the points given in tables 7, 8 and 9 and check that correct signatures are obtained.

Table 7: PIO Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)					
		ML6	ML13	ML7	ML19	EC	ML18
0V	0000/L	20	20	7	7	1,64	12
+5V	P254/H	16,40	40	14	14	2,63	24
TPA	F	34	1	-	11	-	-
TPB	F	33	37,38	-	10	-	-
$\overline{\text{MRD}}$	C14C	7	39	-	-	-	-
$\overline{\text{CLEAR}}$	P254/H	3	13	-	-	-	-
N0	46HH	19	3	-	-	-	-
N1	4637	18	4	-	-	-	-
N2	0000/L	17	-	5	-	-	-
$\overline{\text{N2}}$	P254/H	-	2	6	-	-	-
B0	7FU9	15	5	-	-	-	-
B1	P8H3	14	6	-	-	-	-
B2	U418	13	7	-	-	-	-
B3	7437	12	8	-	-	-	-
B4	59HU	11	9	-	-	-	-
B5	6U9F	10	10	-	-	-	-
B6	65HP	9	11	-	-	-	-
B7	U426	8	12	-	-	-	-
'A'RDY	0000	-	36	-	9	-	-
'A'ST	8075	-	35	-	13	-	-
INH	6221	-	-	-	12	-	23

EC denotes Edge Connector

F denotes flashing probe

Table 8: PIO Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
		ML13	ML18	ML17	ML12	EC
PA0	2P0A	34	-	-	-	19
PA1	4F62	33	-	-	-	20
PA2	PP2C	32	-	-	-	21
PA3	P246	31	-	-	-	22
PA4	HAPP	30	-	-	-	23
PA5	PC4F	29	-	-	-	24
PA6	02A7	28	-	-	-	25
PA7	H710	27	-	-	-	26
'B'ST	0000/L	17	-	-	-	-
PB0	7875	18	2	10	-	-
PB1	UHF1	19	3	11	-	-
PB2	F6CA	21	21	14	-	-
PB3	5947	22	22	13	-	-
PB4	P254/H	23	-	-	9	-
PB5	CHFF	24	-	15	12	-
PB6	AC4H	25	-	-	-	36
PB7	SU82	26	-	-	-	48
STB	0000	1	-	-	-	-

EC denotes Edge Connector

Table 9: PIO Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		ML18	EC
0	0000/L	11	10
1	366U	9	18
2	U5H5	10	55
3	525U	8	47
4	89F8	7	33
5	71C0	6	46
6	9A72	5	45
7	7654	4	38
8	0000/L	18	42
9	0000/L	17	3
10	1FA0	20	4
11	196P	19	5
12	0000/L	14	6
13	0000/L	13	7
14	0000/L	16	8
15	0000/L	15	9

EC denotes Edge Connector

Processor Card DAC

40. (1) Set the front panel POWER switch to OFF.

(2) Ensure that switches SA and SC on the processor card are set to the closed position, and that switches SB, SD, SE and SF are set to the open position.

(3) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(4) Connect the signature analyser leads to the processor card as follows:

START	TP5
STOP	TP5
CLOCK	TP1
GROUND	Negative end of C8

(5) Set the front panel POWER switch to ON.

(6) Connect the signature analyser probe, in turn, to the following points on the processor card and check that correct signatures are obtained:

+5V - ML6 pin 40 -P254
0V - Negative end of C8 -0000

NOTE: If the correct +5V signature is not obtained, carry out the processor and clock divider test routine given in para. 33.

(7) Connect the signature analyser probe, in turn, to the points given in table 10 and check that correct signatures are obtained.

Table 10: DAC Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		ML6	ML9
0V	0000/L	20	8,9
+5V	P254/H	16,40	10
B0	7FU9	15	2
B1	P8H5	14	1
B2	U418	13	16
B3	7437	12	15
B4	59HU	11	14
B5	6U9F	10	13
B6	65HP	9	12
B7	U426	8	11
$\overline{EN}$	00F1	-	4

(8) Use the oscilloscope to monitor TP7 on the processor card and check that the displayed waveform is as given in fig. app 2 (a).

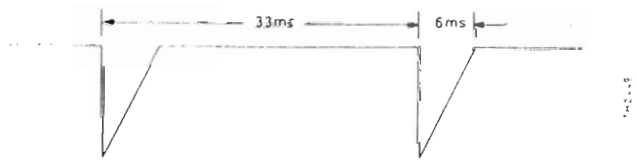

Fig App 2(a) TP7 Waveform

Processor Card Latched I/O

41. With the processor card switch settings, signature analyser controls and signature analyser lead connections as detailed in para. 40, connect the signature analyser probe, in turn, to the points given in table 11 and check that correct signatures are obtained. Remove the extender card and return the processor card to slot 3.

Table 11: Latched I/O Signatures

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT		
		ML6	ML16	EC
0V	0000/L	20	8	1,64
+5V	P254/H	16,40	16	63
TPB	F	33	9	-
N1	4637	18	-	-
A0	1AP6	25	14	-
A1	A7P9	26	13	-
A2	HASF	27	11	-
A3	AP44	28	4	-
A4	H05C	29	6	-
CLEAR	P254/H	-	1	-
LA0	4145	-	15	27
LA1	4037	-	12	28
LA2	7616	-	10	29
LA3	PA69	-	5	30
LA4	0U54	-	7	31

EC denotes Edge Connector

Display Driver Card

42. (1) Set the front panel POWER switch to OFF.

(2) Set switch SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(3) Set the front panel POWER switch to ON.

(4) Compare the front panel display with that given in fig. 21(b). If the display is incorrect proceed with the following signature analysis checks of the display driver card.

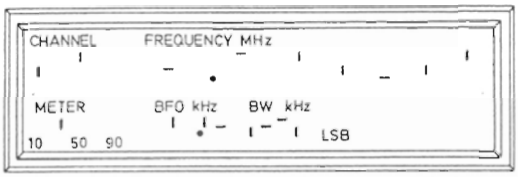

Fig App 2(b) Front Panel Test Display

(5) Set the front panel POWER switch to OFF.

(6) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(7) Mount the display driver card onto the extender card (inserted into slot 1).

(8) Connect the signature analyser leads as follows:

START	TP5)
STOP	TP5) Processor card
CLOCK	TP1)
GROUND	Negative end of C1 on the display driver card.

(9) Set the front panel POWER switch to ON.

(10) Connect the signature analyser probe, in turn, to the following points on the display driver card and check that correct signatures are obtained.

+5V - Positive end of C1 - P254/H
0V - Negative end of C1 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks detailed in paras. 33 to 38.

(11) Connect the signature analyser probe, in turn, to the points given in tables 12, 13, and 14, and check that correct signatures are obtained.

(12) Set the front panel POWER switch to OFF.

(13) Remove the extender card and return the display driver card to slot 1.

Table 12: Display Driver Card Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)									
		EC	ML2	ML1	ML11	ML17	ML9	ML6	ML8	ML7	ML10
0V	0000/L	1,64	8	7	8,15	8,5	8	8	8	8	8
+5V	P254/H	2,63	16	14	16	10,16	16	16	16	16	16
A0	4145	27	14	-	2	-	-	-	-	-	-
A1	4037	28	-	-	3	4	-	-	-	-	-
A2	7616	29	-	-	-	12	-	-	-	-	-
A3	PA69	30	-	-	-	13	-	-	-	-	-
A4	0U54	31	-	-	-	3	-	-	-	-	-
IO0	2P0A	19	-	-	-	-	-	4	-	4	3
IO1	4F62	20	-	-	-	-	-	6	-	6	5
IO2	PP2C	21	-	-	-	-	-	10	-	10	7
IO3	P246	22	-	-	-	-	-	12	-	12	9
IO4	HAPP	23	-	-	-	-	4	-	4	-	11
IO5	PC4F	24	-	-	-	-	6	-	6	-	13
IO6	02A7	25	-	-	-	-	10	-	10	-	-
IO7	H7I0	26	-	-	-	-	12	12	-	-	
MUX-CK	P955	35	3	-	-	-	-	-	-	-	-
DC	AC4H	36	1,13	2	-	1	-	-	-	-	-
STB7	7654	38	-	-	13	-	-	-	-	-	-
STB8	0000/L	42	-	-	14	-	-	-	-	-	-
CK.P	PH12	-	6	1	-	15	-	-	-	-	-
$\overline{\text{STB.D}}$	9400	-	15	-	10	-	-	-	-	-	-
$\overline{\text{STB.KB}}$	P254/H	-	-	-	11,1	-	-	-	-	-	1,15
DISP BLANK	A40C			3,5,8							

EC denotes Edge Connector

Table 13: Display Driver Card Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)						
		ML2	ML1	ML17	ML9	ML6	ML8	ML7
EN1	P7C3	10	9,12	-	-	-	-	-
EN2	91P7	9	6,13	-	-	-	-	-
$\overline{ME1}$	A1PF	-	10	-	2	2	-	-
$\overline{ME2}$	H7C8	-	4	-	-	-	2	2
A	845C	-	-	6	1	1	1	1
B	36CH	-	-	11	15	15	15	15
C	5CH6	-	-	14	14	14	14	14
D	C8CH	-	-	2	13	13	13	13
R	F	-	-	9	-	-	-	-

F denotes flashing probe tip

Table 14: Display Driver Card Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)									
		ML3	ML1	ML17	ML14	ML15	ML16	ML12	ML13	ML4	ML5
0V	0000/L	4	-	5,8	12	4	4	4	4	4	4
+5V	P254/H	7	-	10,16	1,24	8	8	8	8	8	8
A	845C	-	-	-	-	-	-	-	-	-	-
B	36CH	-	-	11	3	-	-	-	-	-	-
C	5CH6	-	-	14	21	-	-	-	-	-	-
D	C8CH	-	-	2	22	-	-	-	-	-	-
R	0000	-	-	9	19	-	-	-	-	-	-
Q0	H70U	-	-	-	11	1	-	-	-	-	-
Q1	6A1C	-	-	-	9	6	-	-	-	-	-
Q2	H892	-	-	-	10	-	1	-	-	-	-
Q3	64C9	-	-	-	8	-	6	-	-	-	-
Q4	AFU5	-	-	-	7	-	-	1	-	-	-
Q5	6U44	-	-	-	6	-	-	6	-	-	-
Q6	843U	-	-	-	5	-	-	-	1	-	-
Q7	1F58	-	-	-	4	-	-	-	6	-	-
Q8	53A9	-	-	-	18	-	-	-	-	1	-
Q9	U9P5	-	-	-	17	-	-	-	-	6	-
Q10	12U1	-	-	-	20	-	-	-	-	-	1

* R6 must be fully clockwise

Synthesizer Board

43. (1) Set the front panel POWER switch to OFF.

(2) Position the unit on its side and remove the cover from the synthesizer board compartment.

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5)	
STOP	TP5)	Processor card
CLOCK	TP1)	
GROUND	Any convenient OV point (chassis).	

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained.

+5V - ML16 pin 39 - P254/H
OV - ML16 pin 24 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 15 and check that correct signatures are obtained.

Table 15: Synthesizer Board Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		PL39	ML16
OV	0000/L	5,6	24
+5V	P254/H	8,10	39
* +15V	P254/H	7	38
+9V	P254/H	-	3
STB1	366U	15	17
IO0	2P0A	11	22
IO1	4F62	13	21
IO2	PP2C	12	20
IO3	P246	14	19
IO4	HAPP	16	18
CTL1	F378	-	15,34

* 15V - use potential divider

(9) Set the front panel POWER switch to OFF.

(10) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Connect the signature analyser leads to the following points on the synthesizer board.

START	ML16 pin 2
STOP	ML16 pin 2
CLOCK	ML16 pin 17
GROUND	ML16 pin 24

(12) Set the front panel POWER switch to ON.

(13) Connect the signature analyser probe, in turn, to the following points on the synthesizer board and check that correct signatures are obtained:

+5V - ML16 pin 39 - 494P/H
0V - ML16 pin 24 - 0000/L

(14) Connect the signature analyser probe, in turn, to the points on the synthesizer board given in table 16 and check that correct signatures are obtained.

(15) Disconnect the signature analyser leads.

Table 16: Synthesizer Board Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
		ML16	ML12	ML13	ML17	ML15
0V	0000/L	24	8,7	8,7,10	8,7,5	7,8
+5V	494P/H	39	1,16	1,16	1,16	14
+9V	494P/H	38	-	-	-	-
CK IN	494P	37	-	-	-	-
$\overline{CK2}$	494P	1	-	-	-	-
C0	0000	16	-	-	-	-
CTL1	3413	15,34	-	-	-	-
DIV3	P7C7	11	6	-	-	-
DIV4	CFU6	10	5	-	-	-
DIV5	PAU3	9	-	12	-	-
DIV6	CH5P	8	-	11	-	-
DIV7	37AC	7	-	6	-	-
DIV8	86U5	6	-	5	-	-
DIV9	OP1C	5	-	-	12	-
DIV10	01F3	4	-	-	11	-
DIV11	0038	3	-	-	6	-
DIV12	0007	2	-	-	-	10
D0	59PF	22	-	-	-	-
D1	U4H1	21	-	-	-	-
D2	F3P5	20	-	-	-	-
D3	U159	19	-	-	-	-
D4	F535	18	-	-	-	-
$\overline{W}$	494P(F)	17	-	-	-	-

IF Filter Card

44. (1) Using the 10K and 22K resistors, make up a potential divider, as shown in fig. 21(c), to reduce the +15V logic levels encountered at some points on the IF filter card to the +5V logic levels required by the signature analyser.

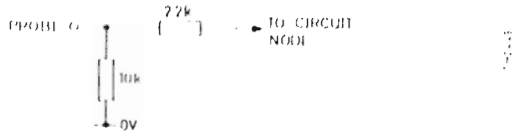

Fig App2(c) 15V Logic Potential Divider

(2) Set the front panel POWER switch to OFF.

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Mount the IF filter card onto the extender card (inserted into slot 7).

(6) Connect the signature analyser leads as follows:

START	TP5)
STOP	TP5) Processor Card
CLOCK	TP1)
GROUND	Any convenient OV point (chassis)

(7) Set the front panel POWER switch to ON.

(8) Connect the signature analyser probe, in turn, to the following points on the IF filter card and check that correct signatures are obtained:

+15V - ML4 pin 16 - P254/H
OV - ML4 pin 8 - 0000/L

NOTE: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(9) Using the potential divider where necessary, connect the signature analyser probe, in turn, to the points on the IF filter card given in table 17 and check that correct signatures are obtained.

(10) Set the front panel POWER switch to OFF.

(11) Remove the extender card and replace the IF filter card (slot 7).

Table 17: IF Filter Card Signatures

		SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
				EC	ML4
		0V	0000/L	1,64	8
	*	+15V	P254/H	61	16
	*	F0	97U3	31	2,14
	*	F1	9UAS	32	3,13
#	*	F2	635C	30	1
#	*	F3	670U	29	15
#	*	FL1	P25H	-	12
#	*	FL2	C190	-	11
#	*	FL3	4970	-	10
#	*	FL4	0000/L	-	9
#	*	FL6	IC67	-	5
#	*	FL7	F346	-	6

These signatures are dependant upon software fitted in this equipment. If these signatures are required they can be provided from analysis of known working receiver.

* +15V logic - use potential divider.

EC denotes Edge Connector

Demodulator Card

45. (1) Set the front panel POWER switch to OFF.

(2) Mount the demodulator card onto the extender card (inserted into slot 5).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5
STOP	TP5 Processor Card
CLOCK	TP1
GROUND	Any convenient OV point (chassis)

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the demodulator card and check that correct signatures are obtained.

+8V - ML10 pin 39 - P254/H
OV - ML10 pin 24 - 0000/L

Note: If the correct +8V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature probe, in turn, to the points on the demodulator card given in table 18 and check that correct signatures are obtained.

Table 18: Demodulator Card Signatures 1

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT	
		EC	ML10
OV	0000/L	1,64	24
+5V	P254/H	61	-
+8V	P254/H	-	38,39
I00	2P0A	19	22
I01	4F62	20	21
I02	PP2C	21	20
I03	P246	22	19
I04	HAPP	23	18
STB2	U5H5	55	17

EC denotes Edge Connector

(9) Set the front panel POWER switch to OFF.

(10) Transfer the signature analyser leads to the following points on the demodulator card:

START	ML10 pin 13
STOP	ML10 pin 13
CLOCK	ML10 pin 17
GROUND	ML10 pin 24

(11) Set the front panel POWER switch to ON.

(12) Connect the signature analyser probe, in turn, to the following points on the demodulator card and check that correct signatures are obtained:

+8V	- ML10 pin 39	-	494P/H
0V	- ML10 pin 24	-	0000/L

(13) Connect the signature analyser probe, in turn, to the points on the demodulator card given in table 19 and check that correct signatures are obtained.

(14) Set the front panel POWER switch to OFF.

(15) Disconnect the signature analyser leads.

(16) Remove the extender card and replace the demodulator card into slot 5.

Table 19: Demodulator Card Signatures 2

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)			
		ML10	ML15	ML3	ML8
0V	0000/L	24	8	8	7,4
+8V	494P/H	38,39	1,7,10,16	16	14
CI	0000/L	36	-	-	-
CK.IN	0000	37	-	-	-
CK1	(F)	40	-	-	-
D0	6PC4	22	-	-	-
D1	04UP	21	-	-	-
D2	3017	20	-	-	-
D3	3UUC	19	-	-	-
D4	H416	18	-	-	-
$\overline{W}$	0000	17	-	-	-
CO	0000/L	16	-	-	-
CTL2	4946	34,14	-	-	-
DIV1	6929	13	-	-	-
DIV2	846C	12	3	-	-
DIV3	9481	11	4	-	-
DIV4	7290	10	5	-	-
DIV5	PHFA	9	6	-	-
DIV6	3HC9	8	-	-	-
DIV7	P7C7	7	-	-	-
DIV8	CFU6	6	-	-	6
DIV9	PAU3	5	-	11	-
DIV10	CH5P	4	-	10	-
DIV11	37AC	3	-	9	-
DIV12	86U5	2	-	-	-

(F) denotes flashing probe tip

AGC Card

46. (1) Set the front panel POWER switch to OFF.

(2) Mount the AGC card onto the extender card (inserted into slot 6).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature analyser leads as follows:

START	TP5
STOP	TP5 Processor card
CLOCK	TP1
GROUND	Any convenient OV point (chassis)

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the AGC card and check that correct signatures are obtained.

+5V - positive end of C20 - P254/H
OV - negative end of C20 - 0000/L

Note: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 28 to 33.

(8) Using the potential divider shown in fig. 21(c) where necessary for 15V logic signals, connect the signature analyser probe, in turn, to the points on the AGC card given in tables 20, 21 and 22, and check that correct signatures are obtained.

(9) Set the front panel POWER switch to OFF.

(10) Remove the extender card and return the AGC card to slot 6.

Table 20: AGC Card Signatures 1

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
			EC	ML14	ML12	ML13	ML15
	OV	0000/L	1,64	8	8	8	8
	+5V	P254/H	63	1	1	-	-
*	+15V	P254/H	61	16	16	16	16
	IO0	2P0A	19	10	-	-	-
	IO1	4F62	20	6	-	-	-
	IO2	PP2C	21	14	-	-	-
	IO3	P246	22	3	-	-	-
	EN	5U82	48	2,7,9	2,7,9	-	-
	STB3	525U	47	-	14	-	-
	STB4	89F8	33	-	10	-	-
	STB5	71C0	46	-	3	-	-
	STB6	9A72	45	-	6	-	-
*	IO0	P117	-	11	-	4	7
*	IO1	A6U8	-	5	-	14	13
*	IO2	FC29	-	13	-	13	4
*	IO3	AHC2	-	4	-	7	14

EC denotes Edge Connector
* +15V Logic - use potential divider

Table 21: AGC Card Signatures 2

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)			
			EC	ML12	ML13	ML15
*	STB3	525U	-	13	-	-
*	STB4	89F8	-	11	-	-
*	STB5	71C0	-	4	5	-
*	STB6	9A72	-	5	-	5
*	POL	P254/H	-	-	6	6
*	F0	97U3	31	-	2	-
*	F1	9UA5	32	-	1	-
*	F2	4727	30	-	11	-
*	F3	9C91	29	-	10	-
*	L0	4518	-	-	-	10
*	L1	3H11	14	-	-	11
*	L2	F58U	15	-	-	2
*	L3	72C1	16	-	-	1

EC denotes Edge Connector
*+15V logic - use potential divider

Table 22: AGC Card Signatures 3

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO)							
			ML14	ML12	ML9	ML1	ML2	ML10	ML3	ML11
	0V	0000/L	8	8	8	4	4	7	7	7
	+5V	P254/H	1	1	-	-	-	-	-	-
*	+15V	P254/H	16	16	16	8	8	14	14	14
*	I00	P117	11	-	14	-	-	5	-	-
*	I01	A6U8	5	-	4	-	-	-	-	9
*	I02	FC29	13	-	13	-	-	-	-	5
*	I03	AHC2	4	-	7	-	-	9	-	-
*	STB3	525U	-	13	5	-	-	-	-	-
*	STB4	89F8	-	11	-	-	-	3,11	-	3,11
*	STB5	71C0	-	4	-	-	-	-	-	-
*	STB6	9A72	-	5	-	-	-	-	-	-
*	POL	P254/H	-	-	6	-	-	-	-	-
*	HANG 0	U01A	-	-	1	-	-	-	-	-
*	HANG 1	377F	-	-	2	-	-	-	-	-
*	DECAY 0	2A8H	-	-	11	6	-	-	-	-
*	DECAY 1	2UFA	-	-	10	-	6	-	-	-
Ø*	DUMP	F3P6	-	-	-	-	1,2	1	5	-
Ø	DR	0000/L	-	-	-	-	-	4	-	-
	R/S	0000/L	-	-	-	-	-	6,8,10	-	6,8,10
*	PEAK	6C58	-	-	-	-	-	13	12	-
*	$\overline{\text{PEAK}}$	890F	-	-	-	-	-	12	6	-
*	MAN	8158	-	-	-	-	-	-	-	2
*	SAMPLE	3330	-	-	-	-	-	-	13	13

Ø Remove IF Filter Card to obtain signature

* 15V Logic - use potential divider

SCORE Interface Card

47. (1) Set the front panel POWER switch to OFF.

(2) Mount the SCORE interface card onto the extender card (inserted into slot 2).

(3) Set switches SA and SC on the processor card to the closed position, switches SB, SD, SE and SF to the open position.

(4) Set the signature analyser controls as follows:

START pushbutton	IN (negative edge)
STOP pushbutton	IN (negative edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(5) Connect the signature leads as follows:

START	TP5
STOP	TP5 Processor card
CLOCK	TP1
GROUND	Any convenient OV point (chassis)

(6) Set the front panel POWER switch to ON.

(7) Connect the signature analyser probe, in turn, to the following points on the SCORE interface card and check that correct signatures are obtained.

+5V - Positive end of C4 - P254/H
OV - Negative end of C4 - 0000/L

Note: If the correct +5V signature is not obtained, carry out the processor card checks given in paras. 33 to 38.

(8) Connect the signature analyser probe, in turn, to the points on the SCORE interface card given in tables 23, 24, 25 and 26 and check that correct signatures are obtained.

(9) Set the front panel POWER switch to OFF.

(10) Set the signature analyser controls as follows:

START pushbutton	OUT (positive edge)
STOP pushbutton	OUT (positive edge)
CLOCK pushbutton	OUT (positive edge)
HOLD pushbutton	OUT (OFF)
SELF-TEST pushbutton	OUT (OFF)

(11) Transfer the signature analyser leads to the following points on the SCORE interface card:

START	ML7 pin 14
STOP	ML7 pin 14
CLOCK	ML9 pin 10
GROUND	ML9 pin 7

Table 23: SCORE Interface Card Signatures 1

	SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)				
			EC	ML12	ML7	ML11	ML17
	0V	0000/L	1,64	1,8	1,8	8	8
	+5V	P254/H	2,63	16	16	16,1	16
*	+15V	P254/H	61	-	-	-	-
	-12V	0000/L	59	-	-	-	-
	IO0	2P0A	19	7	-	6	11
	IO1	4F62	20	6	-	4	12
	IO2	PP2C	21	5	-	3	13
	IO3	P246	22	4	-	11	14
	IO4	HAPP	23	-	7	13	7
	IO5	PC4F	24	-	6	14	6
	IO6	02A7	25	-	5	-	5
	IO7	H710	26	-	4	-	4
	STB11	196P	5	-	-	9	-
	STB12	0000/L	6	-	-	-	-
	STB14	0000/L	8	9	9	-	-
#	FIFO	0000	41	-	-	-	-
	STB10	1FA0	4	3	3	-	-
	STB13	0000	7	-	-	-	-
	STB9	0000	3	-	-	-	-
	CK.INT	P955	44	-	-	-	-

EC denotes Edge Connector

* 15V Logic - use potential divider

\# On later/modified SCORE Boards this signature becomes 0A06.

Table 24: SCORE Interface Card Signatures 2

	SIGNAL	SIGNATURE	TEST POINT		
			EC	ML11	TR COLLECTOR
	Q3	56A6	-	7	
	Q2	7H55	-	5	
	Q1	7H9U	-	2	
	Q4	435U	-	10	
	SAS	8U10	-	12	
	R/L	7463	-	15	
*	W	C4U2	30		TR1
*	X	9U01	29		TR2
*	Y	9UFC	28		TR3
*	Z	A1AC	27		TR4

EC denotes Edge Connector

* Pull-up resistors are required to obtain signature

Table 25: SCORE Interface Card Signatures 3

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)								
		EC	ML16	ML10	ML14	ML9	ML5	ML3	ML1	ML2
0V	0000/L	1,64	4	7	4	7	8	7	5,7,9	7
+5V	P254/H	2,63	1	14	8	14	10,16	14	14	14
INT.CK	P955	44	-	-	-	6	-	-	-	-
CK.IN	0000/L	35	5	-	-	-	-	-	-	-
CK.RTN	0000/L	46	6	-	-	-	-	-	-	-
$\overline{\text{CK.IN}}$	0000/L	-	3	11	-	13	-	-	-	-
CK.IN	P254/H	-	-	10	6	-	-	-	-	-
CK.D	0000/L	-	-	-	7	-	-	-	-	-
CK.E	P254/H	-	-	-	5	1,2	-	-	-	-
EXT.P	0000/L	-	-	1	-	3,12	-	-	-	-
$\overline{\text{EXT.P}}$	P254/H	-	-	2	-	5	-	-	-	-
EXT.SEL	P254/H	-	-	-	-	9,11	-	-	-	-
INT.SEL	0C01	-	-	-	-	8,4	-	-	-	-
SCORE.CK	P955	-	-	13	-	10	9	-	-	-
$\overline{\text{SCORE.CK}}$	0C01	-	-	12	-	-	-	-	3	-
Q4	0000	-	-	-	-		14	1	-	-
SAS	8U10	-	-	-	-	-	-	2	-	-
$\overline{\text{Q4}}$	6H44	-	-	-	-	-	-	3	-	-
STB13	0000/L	7	-	-	-	-	-	-	4,8	-
SIS	0000/L	-	-	-	-	-	-	-	13	9
$\overline{\text{SIS}}$	P254/H	-	-	-	-	-	-	-	12	13
$\overline{\text{SYNC}}$	P254/H	-	-	-	-	-	-	-	-	10,5
SET	8U10	-	-	-	-	-	-	-	6	4
LOAD	9HH1	-	-	-	-	-	-	-	11,1	-
$\overline{\text{LOAD}}$	7U85	-	-	-	-	-	-	-	2	12
RESET	9HH1	-	-	-	-	-	15	-	-	11

Table 26: SCORE Interface Card Signatures 4

SIGNAL	SIGNATURE/ TIP STATE	TEST POINT (PIN NO.)						
		ML12	ML7	ML10	ML2	ML3	ML8	ML15
$\overline{\text{FIFO}}$	U5PA	-	2	9 *	-	-	-	-
DOR	300C	-	14	-	-	-	-	-
$\overline{\text{FE}}$	U5PA	-	-	9 *	2	-	-	-
LOAD	9HHI	-	-	-	1	-	-	-
$\overline{\text{SO}}$	3AIC	-	-	-	3	5,6	-	-
SO	H84U	15	15	-	-	4	9	-
P1	F64H	-	13	-	-	-	7	-
P2	P4H5	-	12	-	-	-	6	-
P3	C6FA	-	11	-	-	-	5	-
P4	4301	-	10	-	-	-	4	-
P5	943A	13	-	-	-	-	13	-
P6	9132	12	-	-	-	-	14	-
P7	UFC6	11	-	-	-	-	15	-
P8	2396	10	-	-	-	-	1	-
CK	0C01	-	-	-	-	-	10	-
Q8	F0U1	-	-	-	-	-	3	3

* ML10 pin 9 is P254 on earlier or unmodified SCORE Boards.

(12) Link the pins of a 26-way plug (para. 2) as listed below and connect to the CONTROL socket on the receiver front panel

Pin D to pin R
Pin H to pin a
Pin K to pin c
Pin M to pin b
Pin P to pin Z

(13) Set the front panel POWER switch to ON.

(14) Connect the signature analyser probe, in turn, to the following points on the SCORE interface and check that correct signatures are obtained.

+5V - Positive end of C4 - CC34/H
0V - Negative end of C4 - 0000/L

(15) Connect the signature analyser probe, in turn, to the points on the SCORE interface card given in table 28 and check that correct signatures are obtained.

(16) Set the front panel POWER switch to OFF.

(17) Disconnect the signature analyser leads.

(18) Remove the extender card and return the SCORE interface card to slot 2.

Table 27: SCORE Interface Card Signatures 5

SIGNAL	SIGNATURE	TEST POINT (PIN NO.)										
		ML8	ML15	EC	ML16	ML17	ML10	ML4	ML6	ML5	ML3	ML20
0V	0000/L	8,11	4	-	4	8	7	8,6	7,8	8	7	7
-12V	0000/L	-	5	-	-	-	-	-	-	-	-	-
+5V	CC34/H	16	-	-	1	16	14	16	14	16	14	14
+12V	CC34/H	-	8	-	-	-	-	-	-	-	-	-
$\overline{CK}$	CC34	10	-	-	-	-	-	-	-	-	-	-
SO	0000	9	-	-	-	-	-	-	-	-	-	-
P8	A486	3	3	-	-	-	-	-	-	-	-	-
DO	1UC2	-	6	53	-	-	-	-	-	-	-	-
CK	0000	-	2	-	-	3	-	1,9	-	1	13	-
CO	CC34	-	7	54	-	-	-	-	-	-	-	-
DI	1UC2	-	-	36	-	-	-	-	-	-	-	-
SI	A486	-	-	-	2	2	5	-	-	-	-	-
$\overline{SI}$	1UC2	-	-	-	-	-	6	7	-	-	-	-
Q3A	4UA4	-	-	-	-	-	-	3,14	-	-	-	-
Q4B	PP9U	-	-	-	-	-	-	2	-	-	-	-
TP5	PP9U	-	-	-	-	-	-	-	3	-	-	-
SYNC	0000	-	-	-	-	-	-	-	1	7	-	-
SYNC	CC34	-	-	-	-	-	-	-	2,11	-	12	-
PS	0000	-	-	-	-	-	-	-	6	6	-	-
PR	0000	-	-	-	-	-	-	-	4	-	11	-
$\overline{LINT}$	0000/L	-	-	-	-	-	-	-	12	-	-	9
$\overline{L/R}$	0000	-	-	-	-	-	-	-	-	-	-	1,2,8
LS	CC34/H	-	-	-	-	-	-	-	-	-	-	10
$L/\overline{R}$	CC34	-	-	-	-	-	-	-	-	-	-	3,5
$\overline{RINT}$	659A	-	-	-	-	-	-	-	-	-	-	6
RS	HPAP	-	-	-	-	-	-	-	-	-	-	4
$\overline{INT}$	659A	-	-	37	-	-	-	-	-	-	-	11