VHF / UHF RECEIVER
MODEL RG - 5545A

INSTALLATION, OPERATION &
MAINTENANCE INSTRUCTIONS

WITH PARTS LIST

VOLUME 1

NZBR 109

VOL 1

VHF/UHF RECEIVER MODEL RG - 5545A

October 1984

By Direction of the
Chief of Naval Staff

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EQUIPMENT MANUAL

INSTALLATION, OPERATION AND MAINTENANCE INSTRUCTIONS WITH PARTS LIST

VHF/UHF RECEIVER
MODEL RG-5545A

THIS DOCUMENT SUPERCEDES ALL PREVIOUS EDITIONS.

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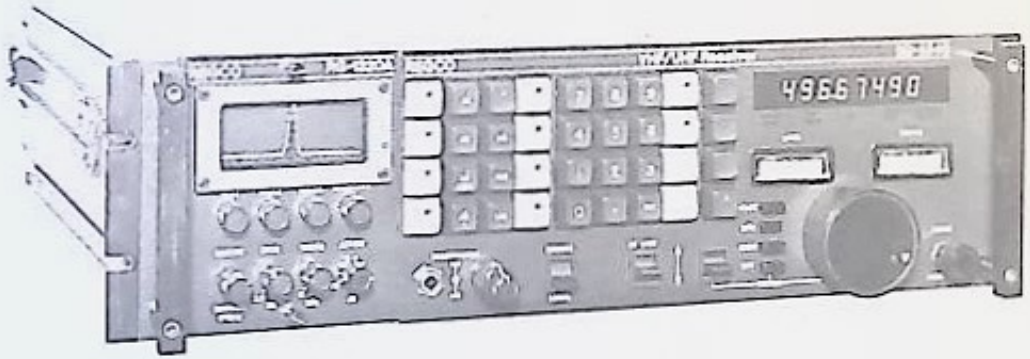

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SECTION I

GENERAL INFORMATION

1-1. SCOPE OF MANUAL

1-2. This manual contains installation, operation, theory of operation, and maintenance instructions, and also includes a parts list and engineering drawings for the VHF/UHF Receiver, Type RG-5545A, (hereinafter referred to as the Receiver) manufactured by Racal Communications, Inc. (RACOMINC) of Rockville, Maryland.

1-3. INTRODUCTION

1-4. The information contained in this section is provided to familiarize installation, operation, maintenance and administrative personnel with the physical and functional characteristics of the Receiver.

1-5. EQUIPMENT DESCRIPTION

1-6. The following paragraphs describe the functional purpose of the Receiver and address operational characteristics associated with the Receiver performance.

1-7. FUNCTIONAL PURPOSE. The Receiver provides radio frequency (RF) reception capabilities within a 20 and 1000 MHz frequency range, to provide demodulated audio signals from amplitude modulated (AM), frequency modulated (FM), and continuous wave (CW) signals. The Receiver is a synthesized, solid state, microcomputer controlled unit, with scan capabilities, a 99 channel memory, and incorporates four IF bandwidths, automatic frequency control (AFC), a carrier operated relay (COR), and three modes of gain control to accommodate operation.

1-8. OPERATIONAL CHARACTERISTICS. The Receiver is equipped for remote control operation when utilizing an optional IEEE-488C-1978 remote control interface (See Appendix A, as applicable), and/or may also be controlled by a Spectrum Surveillance Controller, Type RG-1342 (hereinafter referred to as the Spectrum

Surveillance Controller. In addition, an optional plug-in narrowband Spectrum Display Unit, Type RG-1320B (hereinafter referred to as the Spectrum Display) when equipped with the Receiver, provides an operator with a visual display of signal activity at and around the receiver tuned frequency.

1-9. Receiver frequency tuning, to a resolution of 10 Hz over the 20 to 1000 MHz range, may be accomplished using a ten digit keypad, a tuning control, or a tuning slew switch. Numeric keypad frequency tuning is accomplished by entering the desired frequency on the ten digit (0 to 9) keypad with decimal point. The Receiver automatically tunes to the frequency entered, to a resolution of 10 Hz, when the ENT/EXCL FREQ pushbutton key is pressed. Both the tuning lever and control can be enabled for tuning the Receiver, either up or down in frequency increments of three different rates; FAST (100 kHz), MED (1 kHz), or SLOW (10 Hz).

I-10. The scan capabilities of the Receiver may be operated in five different modes: scanning up, or scanning down over the Receiver frequency limits; automatic scan stop and hold on a preset COR threshold; start frequency at or above the COR threshold; and memory channel scan with automatic stop and hold on a channel pre-set threshold. The scan up or scan down is selected through the numeric keypad along with a rate of scan from 10 Hz to 1000 MHz per second. This rate is selected through the numeric keypad (0 to 9) with 0 providing a scan stop; 1, a 10 Hz rate; 2, a 100 Hz rate; and, so on with 9 providing a 1000 MHz rate. The scan, at the rate selected, is continuous in that the scan is from one frequency limit to the other (up or down), then stepping to the opposite limit and repeating the scan. When scan is operated in the AFC mode, the scan will automatically stop and hold on a frequency that has a signal level at or above a pre-set COR threshold. The AFC will then adjust the frequency to center the signal in the IF passband. When the signal goes below COR threshold and remains there for approximately 0.5 seconds the scan will then continue, or scan may be manually continued with the signal still high, by pressing the CLR pushbutton key-switch. Upper and lower frequency limits are programmed by keying in the frequency, then terminating the key sequence by actuating SCAN UP pushbutton key-switch for the upper limit and SCAN DN for the lower limit. Automatic skip of a frequency at or above the COR threshold is accomplished by storing the frequency in the exclude frequency library memory. The scan may

also be programmed to scan the channels stored in channel memory and to stop and hold on any signal at or above the pre-set COR threshold. Dwell time on each channel is approximately 20 milliseconds unless a signal above the threshold is found.

1-11. Channel memory provides for storage of up to 99 (01 to 99) channels with full Receiver operating parameter set-up in each channel. Any channel may be recalled for viewing or editing without affecting Receiver operation. Any channel recalled may be re-stored after viewing or editing or may be executed to change the Receiver operation as directed by the parameters of the channel executed. Each memory channel may be recalled by channel number (01 to 99) or the slew switch may be used to step through the channels.

1-12. The Receiver contains four IF filter amplifier assemblies with bandpass filters incorporating 10, 20, 50 and 100 kHz bandwidths. Each IF filter amplifier assembly contains a frequency compensated AM and FM demodulator. The IF bandwidths are selectable by keypad entry at the front panel of the Receiver.

1-13. A carrier operated relay (COR), integrated within the Receiver, operates from a preselected threshold of the detected RF signal. The COR may be either enabled or disabled, and the threshold adjusted by actuating a front panel COR THRESHOLD slew switch. The relay contacts provide a low impedance output to the receiver rear panel when closed (enabled and above threshold), and a high impedance output when opened (disabled or below threshold).

1-14. Automatic frequency control (AFC) operates in conjunction with COR and may be enabled or disabled through actuation of the associated pushbutton key-switch on the front panel. When both COR and AFC are enabled and the signal level is above the COR threshold, the frequency is automatically adjusted to center the signal in the IF passband.

1-15. Three modes of gain control are utilized in the Receiver and are selectable from the front panel. The AGC may be operated with a slow or fast time constant, while MGC has a selectable threshold over a minimum 100 dB range.

1-16. Remote control operation of the Receiver operating parameters is accomplished when equipped with an optional IEEE-488C remote control interface

circuit card assembly (A7A9), which permits the Receiver to receive commands from or send status information to a remote controller/computer. The functions which can be controlled from a remote location include; frequency tuning, detection mode, IF bandwidth selection, AGC, attenuation for manual gain, internal/external reference, scan, AFC, COR, channel memory, and frequency excluded library memory. Receiver status may be requested by a remote controller/computer with the Receiver in either a remote or local control mode of operation. In addition, an address switch assembly (S1), comprising a set of 8 DIP switches on the Receiver rear panel (covered), provide for programming the optional remote control interface with the associated IEEE addresses. Surveillance scanning control of the Receiver may be accomplished using an optional Spectrum Surveillance Controller interfaced through an associated FAST SCAN interface connector J15 mounted on the receiver rear panel. The optional Spectrum Display provides the operator with a visual display of signal activity at and around the receiver tuned frequency. The Spectrum Display accepts a 21.4 MHz IF signal generated within the Receiver and displays the input signal spectrum utilizing a cathode ray tube (CRT), and has an adjustable sweep width of 0 to 400 kHz about the receiver tuned frequency.

1-17. FUNCTIONAL OVERVIEW

1-18. The following paragraphs describe the Receiver employed in a typical system application and address Receiver functional organization and principles of operation.

1-19. TYPICAL SYSTEM APPLICATION. Figure 1-1 shows a typical system application block diagram. The typical system may contain a remote computer/position controller and a Spectrum Surveillance Controller, in conjunction with a wide band Spectrum Display, Type HP1311A. This system accommodates three modes of surveillance; bandscan mode, discrete scan mode, and the normal receiver tuning mode. As a result, an operator can view a display of the wide band frequency spectrum within the 20 to 1000 MHz range of the Receiver and the received transmitter activity. The system may be controlled from the remote computer/position controller, the Spectrum Surveillance Controller, or the receiver front panel controls, and allows talk/listen functions between all three control positions. The optional plug-in Spectrum Display is also shown as part of the system and when equipped, provides a narrow band 400 kHz spectrum display of the tuned frequency for viewing at the receiver front panel.

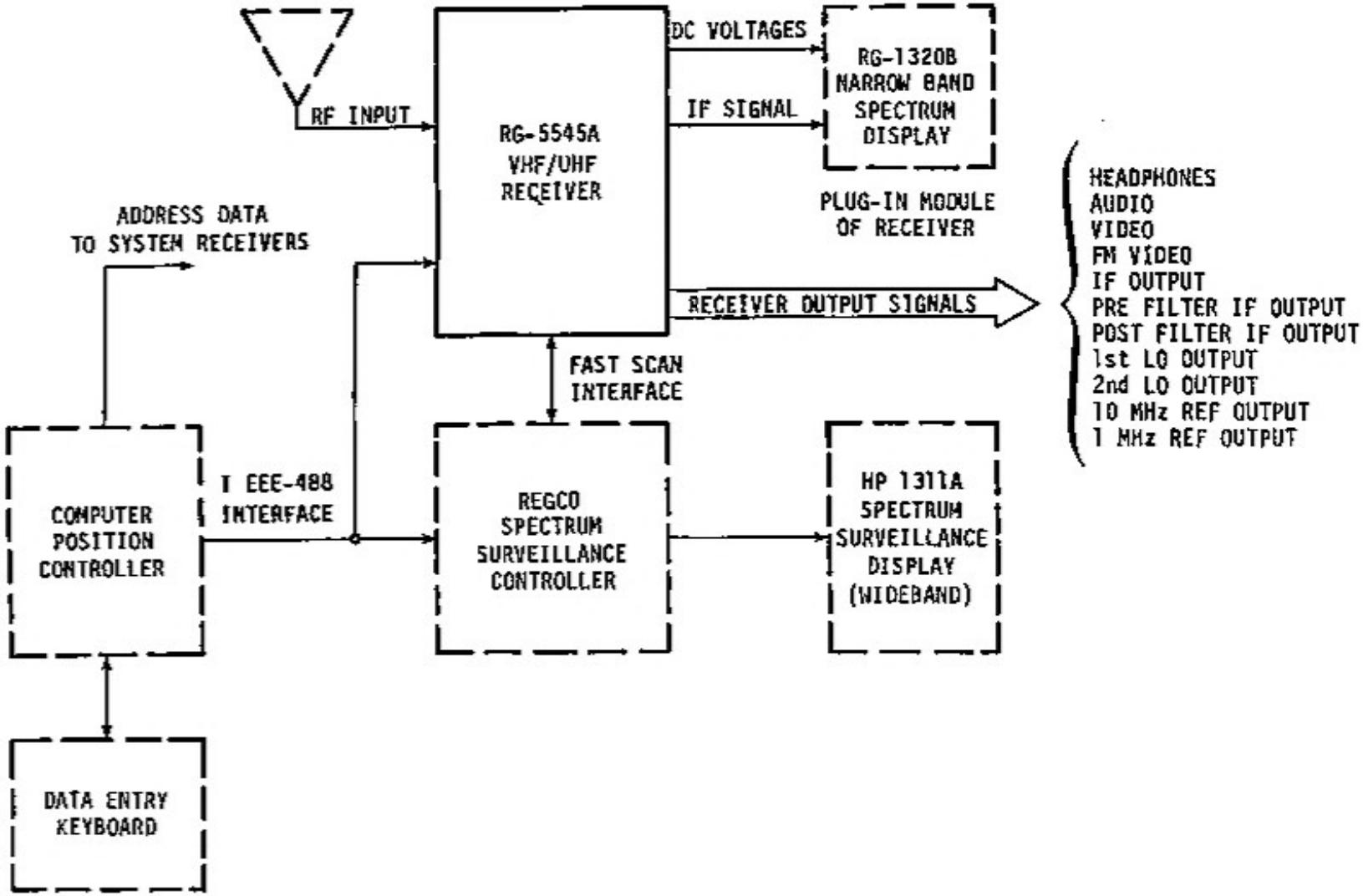


Figure 1-1. Typical System Application

1-20. PRINCIPLES OF OPERATION. Figure 1-2 is a simplified functional block diagram of the Receiver. The functional circuit breakdown is directly related to the module assemblies/circuit card assemblies contained in the Receiver. This description describes the primary signal flow from the RF antenna input to the audio and video outputs, and describes the supporting functions to that primary signal flow. The primary signal flow description includes; the tuner assembly (A3), the IF assembly (A6), and the audio video amplifier/COR assembly (A9). The supporting functions include; the reference generator module assembly (A8), the first LO synthesizer module assembly (A5), the second LO module assembly (A4), the receiver control assembly (A7 and A2), and the power supply module assembly (A1). This description is intended to provide the technician with the basic operating principles of the Receiver. For a more detailed description, refer to Section IV, which presents the same functional breakdown in greater detail.

1-21. PRIMARY SIGNAL FLOW. As shown in Figure 1-2, the RF input signal from the antenna is routed and applied to an RF input limiter (A3A5) before being applied to the corresponding VHF/UHF preselector. The corresponding preselector implements preselection for application to either the VHF or UHF tuner module assemblies (A3A1 and A3A2 respectively), providing first stage conversion within the tuner assembly (A3), by mixing with local oscillator signal frequencies from the first LO synthesizer module assembly (A5). This first conversion stage produces three separate output signals of 661.4, 341.4 and 181.4 MHz. The 661.4 MHz IF signal is produced in the VHF tuner module assembly, by tracking the 20 to 500 MHz RF input signal with a 681.4 to 1161.4 MHz LO signal from the first LO synthesizer module assembly (A5), producing the difference frequency of 661.4 MHz from an associated mixer. The 341.4 MHz difference frequency is produced in the UHF tuner module assembly, by tracking the 500 to 840 MHz input with 841.4 to 1181.4 MHz, providing the 341.4 MHz IF from the mixer. The 181.4 MHz is also produced in the UHF tuner in the same manner; except, that the 840 to 1000 MHz input is tracked with 1021.4 to 1181.4 MHz. One of the three converted frequencies (depending on frequency range), is then coupled to the second converter stage and mixed with a frequency from the second LO module assembly (A4). In the 20 to 500 MHz range, the 661.4 MHz IF is mixed with 60 MHz; in the 500 to 840 MHz range, 341.4 MHz IF is mixed with 320 MHz; in the 840 to 1000 MHz the 181.4 MHz IF is mixed with 160 MHz. In all three frequency ranges, a 21.4 MHz IF signal is produced from a mixer within the second conversion stage.

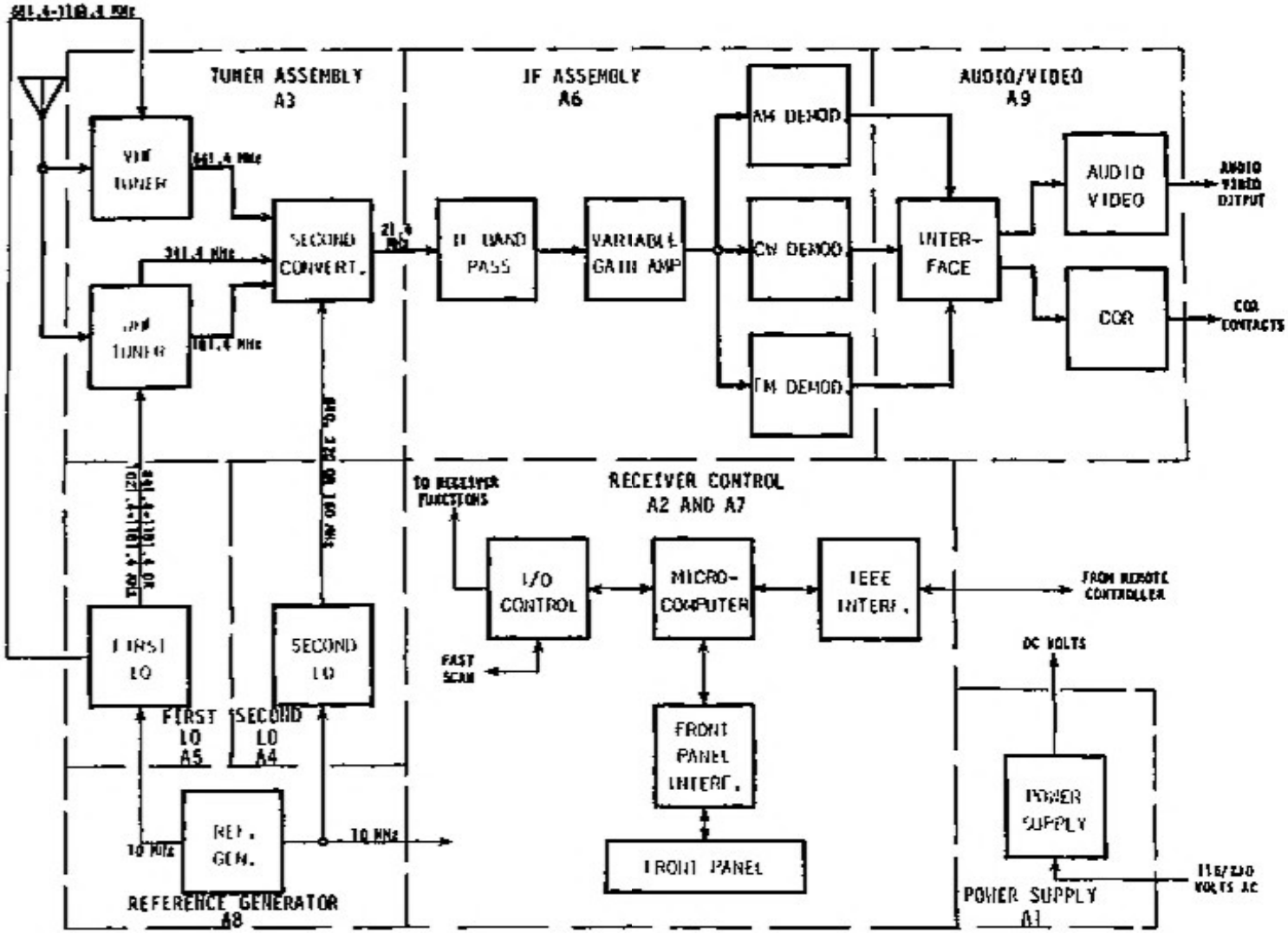


Figure 1-2. Receiver Simplified Functional Block Diagram

1-22. The 21.4 MHz IF signal from the tuner assembly is then coupled to one of four IF bandpass filters in the IF assembly (A6). These filters are selectable from the receiver front panel and provide either 10, 20, 50 or 100 kHz of bandwidth to the IF signal. The signal is then routed to a variable gain amplifier (A6A2) which provides for both automatic (AGC) and manual (MGC) gain control of the IF signal. The gain controlled signal is then detected (AM, FM, or CW) and routed to the audio video amplifier (A9A2) and COR (A9A3). The audio and video signals are routed to the rear panel and to a front panel phones jack for monitoring.

1-23. REFERENCE GENERATOR MODULE ASSEMBLY (A8). The Receiver contains a reference generator oscillator which provides an accurate 10 MHz reference frequency to various receiver circuits. The reference frequency is generated by an internal oven-temperature controlled, crystal oscillator (TCXO), which may be further stabilized by using an external reference frequency of 1, 5 or 10 MHz through rear panel EXT REF INPUT connector J17. A 1 MHz reference monitor signal, derived from the 10 MHz reference, is also available at rear panel 1 MHz REF OUT connector J18.

1-24. SECOND LO MODULE ASSEMBLY (A4). The second LO supplies three separate frequencies to the tuner assembly (A3) for signal conversion utilizing the second converter stage of the three IF signal frequencies generated in the first conversion stage. The second LO operates at 640 MHz and is stabilized through a phase-lock-loop, referenced to the 10 MHz reference frequency. The 640 MHz output of the basic oscillator is used as the second conversion frequency in the 20 to 500 MHz range. The 640 MHz is divided-by-two to provide 320 MHz in the 500 to 840 MHz frequency range; then the 320 MHz is further divided-by-two to provide 160 MHz in the 840 to 1000 MHz frequency range. An output of the second LO is made available at rear panel LO2 connector J6.

1-25. RECEIVER CONTROL ASSEMBLY. The receiver control assembly comprises the functional circuits of the front panel assembly (A2) and receiver control assembly (A7). The front panel assembly contains the controls, displays and indicators physically mounted on the front panel, in addition to decoders for the keyboards. The receiver control assembly consists of a microcomputer, interface, decoder and control sub-modules/circuit card assemblies, and provides for controlling the Receiver from the front panel, from a remote controller/computer, or from an Spectrum Surveillance Controller as may be

applicable. In the local control mode of operation, the Receiver operational parameters are entered at the front panel and routed through the front panel interface circuit card assembly (A7A4) to the microcomputer (A7A2). This information is then processed and routed through control circuits to the appropriate receiver functions. In addition, data is also routed back to the front panel for display. The data flow is timed and controlled by addresses and strobes from the microcomputer and address decoder (A7A6). In the remote control mode of operation, the control function is identical except that the data flow is to and from the remote controller/computer. In an optional fast scan control mode, a microcomputer in the Spectrum Surveillance Controller interfaces with the microcomputer of the Receiver through handshaking lines, and directs receiver functions through the front panel I/O control interface of the Receiver.

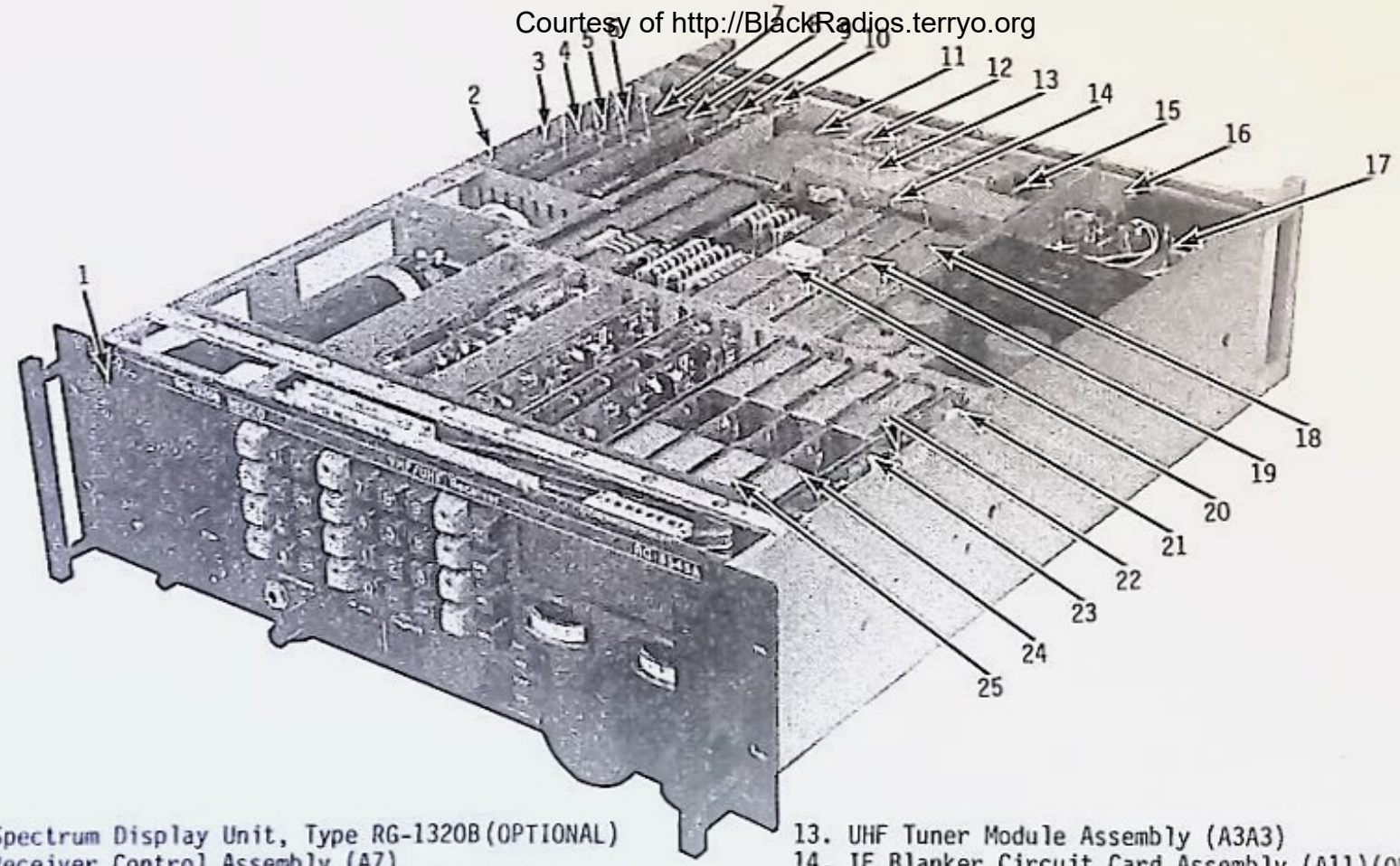
1-26. POWER SUPPLY MODULE ASSEMBLY (A1). The Receiver's power supply will operate from a 115 or 230 volt ac, 47 to 62 Hz power source. A primary power fuse (F1) and input voltage select card is accessible from the rear panel. The dc outputs to receiver control circuits include: regulated -15, -5, +15, and +28 volts dc; and non-regulated -22, +10, and +22 volts dc. In addition, a cooling fan blower motor operates from a secondary winding of the power supply transformer.

1-27. PHYSICAL DESCRIPTION

1-28. The Receiver's physical characteristics and physical/functional associations are described in the following paragraphs.

1-29. RECEIVER ASSEMBLY. The Receiver module assemblies/circuit card assemblies are contained within compartments within an aluminum chassis frame. The second LO (A4), first LO (A5) synthesizer, and IF (A6) assemblies are contained within shielded enclosures with RFI covers to prevent extraneous RF interference. The chassis of the Receiver consists of two side panels, and a rear and front panel. The chassis is 19 inches wide, 20 inches deep, and 5¾ inches high. The front panel is slotted to allow the Receiver to be mounted in a standard 19-inch equipment rack.

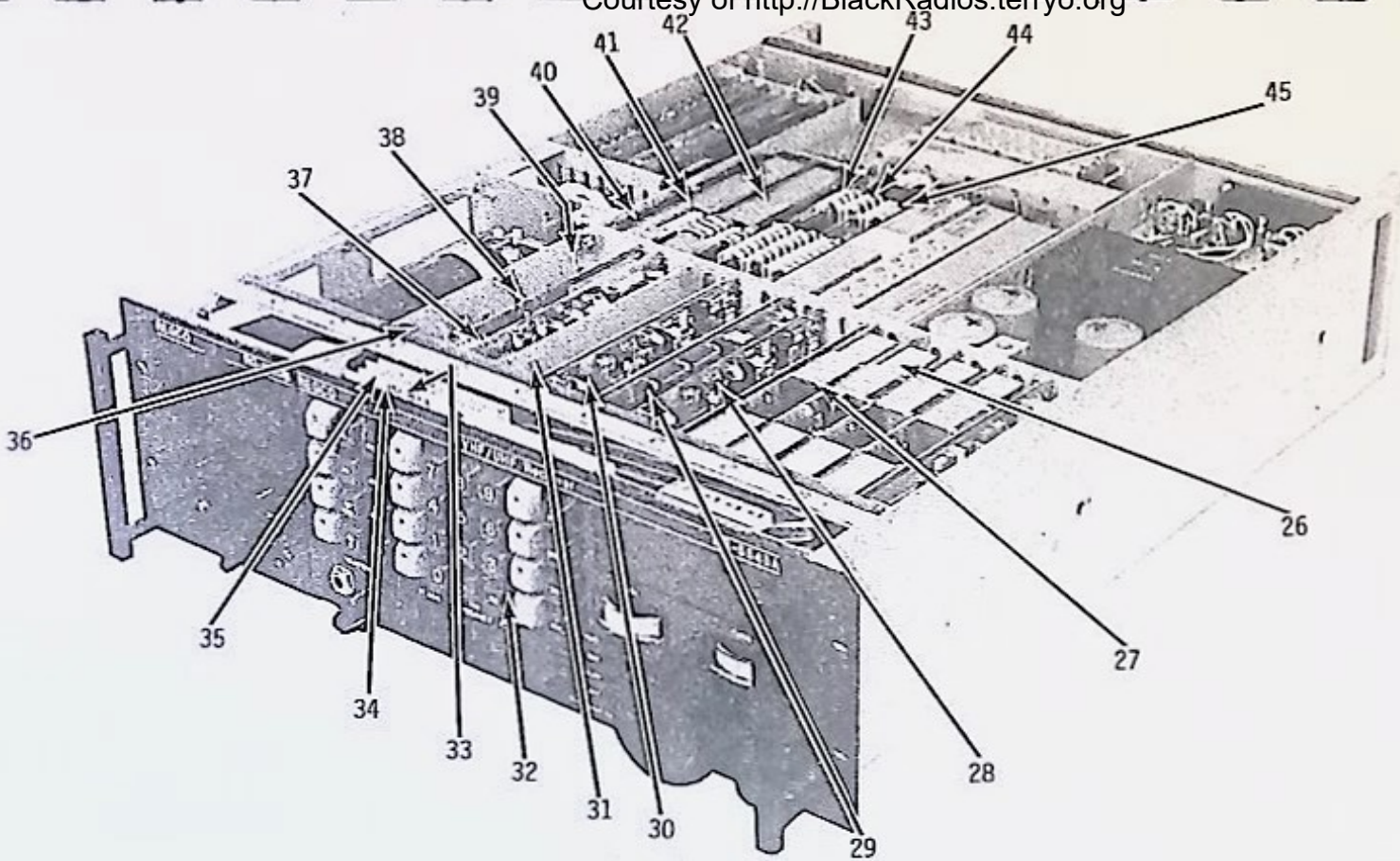
1-30. MAJOR ASSEMBLIES. The Receiver comprises the assemblies/circuit card assemblies as listed in Table 1-1. Refer to Figure 1-3 for identification and location of the major assemblies of the Receiver.



1. Spectrum Display Unit, Type RG-1320B (OPTIONAL)
2. Receiver Control Assembly (A7)
3. Receiver Control Interface Circuit Card Assembly (A7A1)
4. IEEE-488C Remote Control Interface Circuit Card Assembly (A7A9) (OPTIONAL)
5. Converter Circuit Card Assembly (A7A8)
6. Preselector Controller Circuit Card Assembly (A7A7)
7. Address Decoder Circuit Card Assembly (A7A6)
8. Display Driver (A7A5)
9. Front Panel I/O Interface Circuit Card Assembly (A7A4)
10. Microcomputer Circuit Card Assembly (A7A2)
11. Reference Generator Module Assembly (A8)
12. UHF (500-1000 MHz) Preselector Module Assembly (A3A4)
13. UHF Tuner Module Assembly (A3A3)
14. IF Blanker Circuit Card Assembly (A11) (OPTIONAL)
15. RF Input Limiter Module Assembly (A3A5)
16. Power Supply Module Assembly (A1)
17. Power Rectifier Circuit Card Assembly (A1A1)
18. VHF (20-500 MHz) Preselector Module Assembly (A3A2)
19. VHF Tuner Module Assembly (A3A1)
20. Second LO Module Assembly (A4)
21. IF Assembly (A6)
22. IF Control Interface Circuit Card Assembly (A6A7)
23. Variable Gain Amplifier Circuit Card Assembly (A6A2)
24. 100 kHz IF Filter Amplifier Assembly (A6A3)*
25. 50 kHz IF Filter Amplifier Assembly (A6A4)

Figure 1-3. Receiver Chassis, Top View (Sheet 1 of 2)

*NOTE: The 100 kHz IF Filter Amplifier Circuit Card Assembly is standard; 400/20 kHz IF Filter amplifier optional.



26. 20 kHz IF Filter Amplifier Assembly (A6A5)
27. 10 kHz IF Filter Amplifier Assembly (A6A6) (OPTIONAL)
28. USB Demodulator Circuit Card Assembly (A6A7)
29. CW Demodulator Circuit Card Assembly (A6A8)
30. LSB Demodulator Circuit Card Assembly (A6A9) (OPTIONAL)
31. 10 kHz Converter Circuit Card Assembly (A6A10) (OPTIONAL)
32. Front Panel Assembly (A2)
33. Keyboard Assembly (A2A1)
34. Keyboard Decoder Circuit Card Assembly (A2A2)
35. Display Circuit Card Assembly (A2A3)
36. Audio Video Amplifier/COR Assembly (A9)
37. Audio Video Amplifier Circuit Card Assembly (A9A2)
38. COR Circuit Card Assembly (A9A3)
39. Audio Video Control Interface Circuit Card Assembly
40. First LO Synthesizer Module Assembly (A5) (A9A1)
41. VCO B Module Assembly (A5A5)
42. VCO A Module Assembly (A5A1)
43. Programmable Divider Circuit Card Assembly (A5A4)
44. Controller Circuit Card Assembly (A5A2)
45. Digiphase Processor Circuit Card Assembly (A5A3)

Figure 1-3. Receiver Chassis, Top View (Sheet 2 of 2)

Table 1-1. Major Assemblies

REFERENCE DESIGNATION	ASSEMBLY/CIRCUIT CARD ASSEMBLY	REFERENCE DESIGNATION	ASSEMBLY/CIRCUIT CARD ASSEMBLY
A1	Power Supply Module	A6A8	CW Demodulator
A1A1	Power Rectifier	A6A9	LSB Demodulator (Optional)
A2	Front Panel		
A2A1	Keyboard	A6A10	10 kHz Converter (Optional)
A2A2	Keyboard Decoder		
A2A3	Display	A7	Receiver Control
A3	Tuner	A7A1	Receiver Control Output Interface
A3A1	VHF Tuner Module		
A3A2	VHF (20-500 MHz) Preselector	A7A2	Microcomputer
		A7A4	Front Panel I/O Control Interface
A3A3	UHF Tuner Module		
A3A4	UHF (500-1000 MHz) Preselector Module	A7A5	Oisplay Driver
		A7A6	Address Decoder
A3A5	RF Input Limiter Module	A7A7	Preselector Controller
		A7A8	Converter
A4	Second LO Module	A7A9	IEEE-488C Remote Control Interface (Optional)
A4A1	Second LO		
A4A2	Second LO Divider		
A5	First LO Synthesizer Module	A8	Reference Generator Module Assembly
A5A1	VCO A Module		
A5A2	Controller	A8A1	Reference Generator Oscillator
A5A3	Digiphase Processor		
A5A4	Programmable Divider	A8A2	Control Interface
A5A5	VCO B Module	A8A3	Divider
		A8A4	10 MHz Buffer
A6	IF		
A6A1	IF Control Interface	A9	Audio Video Amplifier/ COR Assembly
A6A2	Variable Gain Amplifier	A9A1	Audio Video Control Interface
A6A3	100 kHz IF Filter Amplifier	A9A2	Audio Video Amplifier
A6A4	50 kHz IF Filter Amplifier	A9A3	Carrier Operated Relay (COR)
A6A5	20 kHz IF Filter Amplifier	A10	IEEE-488C Remote Control Interface Adapter (Optional)
A6A6	10 kHz IF Filter Amplifer		
A6A7	USB Demodulator (Optional)	A11	IF Blanker (Optional)

1-31. TECHNICAL PERFORMANCE CHARACTERISTICS

1-32. Technical performance characteristics is a tabulated listing containing the Receiver's most significant characteristics and associated performance criteria. This data is provided in Table 1-2.

Table 1-2. Technical Performance Characteristics

CHARACTERISTICS	PERFORMANCE CRITERIA
Frequency Range	20-1000 MHz
Synthesizer Step Time	5 milliseconds
Synthesizer Phase Noise	10 Hz rms, typical 20 Hz rms maximum, from 200 to 3200 Hz -115 dBc/Hz at 20 kHz offset -127 dBc/Hz at 100 kHz offset
RF Input Impedance	50 ohms
RF Input VSWR	3:1, maximum
RF Input Protection	To 10 V rms
RF Input Noise Figure	12 dB maximum measured to 2nd IF
Intermodulation Distortion, Third Order	0 dBm IP, referenced to the input
Intermodulation Distortion, Second Order	+40 dBm IP, referenced to the input
Image Rejection	90 dB, minimum
IF Rejection	90 dB, minimum
LO Level at RF Input	-107 dBm maximum
Spurious Signals, Internally Generated	-120 dBm signal level referenced to input
Crossing Responses, Externally Generated	70 dB below a -40 dBm input signal
Demodulation Modes	AM, FM, and CW (standard) USB, LSB, and ISB (optional)
Distortion (Standard Bandwidths)	5% typical
IF Bandpass Filter Bandwidths	10 kHz, 20 kHz, 40 kHz and 100 kHz (standard) 2.5:1 shape factor Optional to 500 kHz

Table 1-2. Technical Performance Characteristics (Cont.)

CHARACTERISTICS	PERFORMANCE CRITERIA
Receiver Sensitivity AM, FM	AM and FM sensitivity in dBm at given bandwidths 10 kHz 20 kHz 50 kHz 100 kHz -98 -95 -91 -88 AM--The specified input signal level in dBm, AM modulated 30% tone, will produce a minimum 10 dB signal plus noise to noise (S+N/N) ratio at the audio output. FM--The specified input level in dBm, FM demodulated at a 1 kHz rate with a deviation equal to 40 percent of the IF bandwidth, will produce a minimum 20 dB (S+N/N) ratio at the audio output. (400 Hz modulation is used for the 10 and 20 kHz IF bandwidths.)
Gain Control Range (AGC and MGC)	100 dB minimum
AGC Accuracy	2 dB output variation with 100 dB input charge
Wideband IF Output (Pre-Filter IF)	21.4 MHz, 10 MHz bandwidth, 25 dB above input.
Narrowband IF Output (Post-Filter IF)	21.4 MHz, 400 kHz bandwidth, 25 dB above input
IF Output Level	-10 dBm nominal
Audio Outputs	Phone Jack: 100 mW across 600 ohms Rear Panel: 3 mW across 600 ohms balanced, 100 Hz to 20 kHz bandwidth
Video Output	0.5 Vrms across 93 ohms, 200 Hz to one-half IF bandwidth
FM Discriminator Output	0.5 VRMs across 93 ohms

Table 1-2. Receiver Specifications (Cont.)

CHARACTERISTICS	PERFORMANCE CRITERIA
Frequency Standard	Aging $+5 \times 10^{-9}$ per day $\pm 5 \times 10^{-8}$ per week
Frequency Error	Less than ±100 Hz plus accumulated aging
External Reference	1, 5, or 10 MHz, 50 mV to 5 Vp-p across 50 ohms
Operating Modes	Local, remote and fast scan control
Remote Control Interface	IEEE-488C-1978
Weight	Approximately 60 pounds with signal monitor
Operating Temperature	0° to 50°C
Storage Temperature	-40°C to +70°C
Input Power	115/230 VAC ± 10% 47 to 62 Hz single phase
Sizer	Front panel - 19 inches wide, main chassis 17 inches wide, 5.25 inches high, 20 inches deep excluding connectors handles, controls and indicators.
Power Consumption	120 Watts, approximately.

1-33. ANCILLARY EQUIPMENT/ACCESSORIES

1-34. The Receiver is supplied with a power cord and appropriate connections for ancillary equipment and accessories. However, neither ancillary equipment nor accessories are supplied with the Receiver. To obtain the maximum operational use of the Receiver, the ancillary equipment and accessories listed in Table 1-3 should be obtained (as required) for each specific application.

Table 1-3. Equipment Accessories

EQUIPMENT/ACCESSORY	APPLICATION
Headset	Single channel monitoring
Synthesizer or Standard Source (External Reference)	Injecting an external reference input at 1 MHz, 5 MHz, or 10 MHz
VHF/UHF Antenna	RF signal interception for signal input application to Receiver
Remote Computer/Controller (Computer Position Controller) with Interface Buss Cable	Remote control operation
Spectrum Surveillance Controller, Type RG-1342 with Interface Buss Cable (Fast Scan)	Surveillance scanning control unit providing rate selectable band scanning with selectable band limits, and discrete frequency scanning with selectable thresholds, dwell time and IF bandpass filter bandwidth.
Spectrum Display, Type HP-1311A	Wide band 10 MHz signal display bandwidth monitoring, centered at 21.4 MHz
Spectrum Display Unit, Type RG-1320B (Available as plug-in option to Receiver)	Narrow band 400 kHz signal display bandwidth monitoring, centered at 21.4 MHz

SECTION II

INSTALLATION

2-1. INTRODUCTION

2-2. This section contains instructions pertaining to the Receiver's logistics. These instructions include preparation for use, installation, preparation for storage, and preparation for shipment.

2-3. PREPARATION FOR USE

2-4. Preparation for use includes procedures for unpacking the Receiver, as well as, input power selection, remote control interface addressing (as applicable), and initial checkout. These procedures should be performed on initial receipt of the Receiver and prior to installation.

2-5. UNPACKING AND INSPECTION PROCEDURES. As shown in Figure 2-1, each Receiver shall be unpacked and inspected in accordance with the following procedures.

1. Open top of shipping container (5) and remove technical manual (8) and power cord (7) from container.

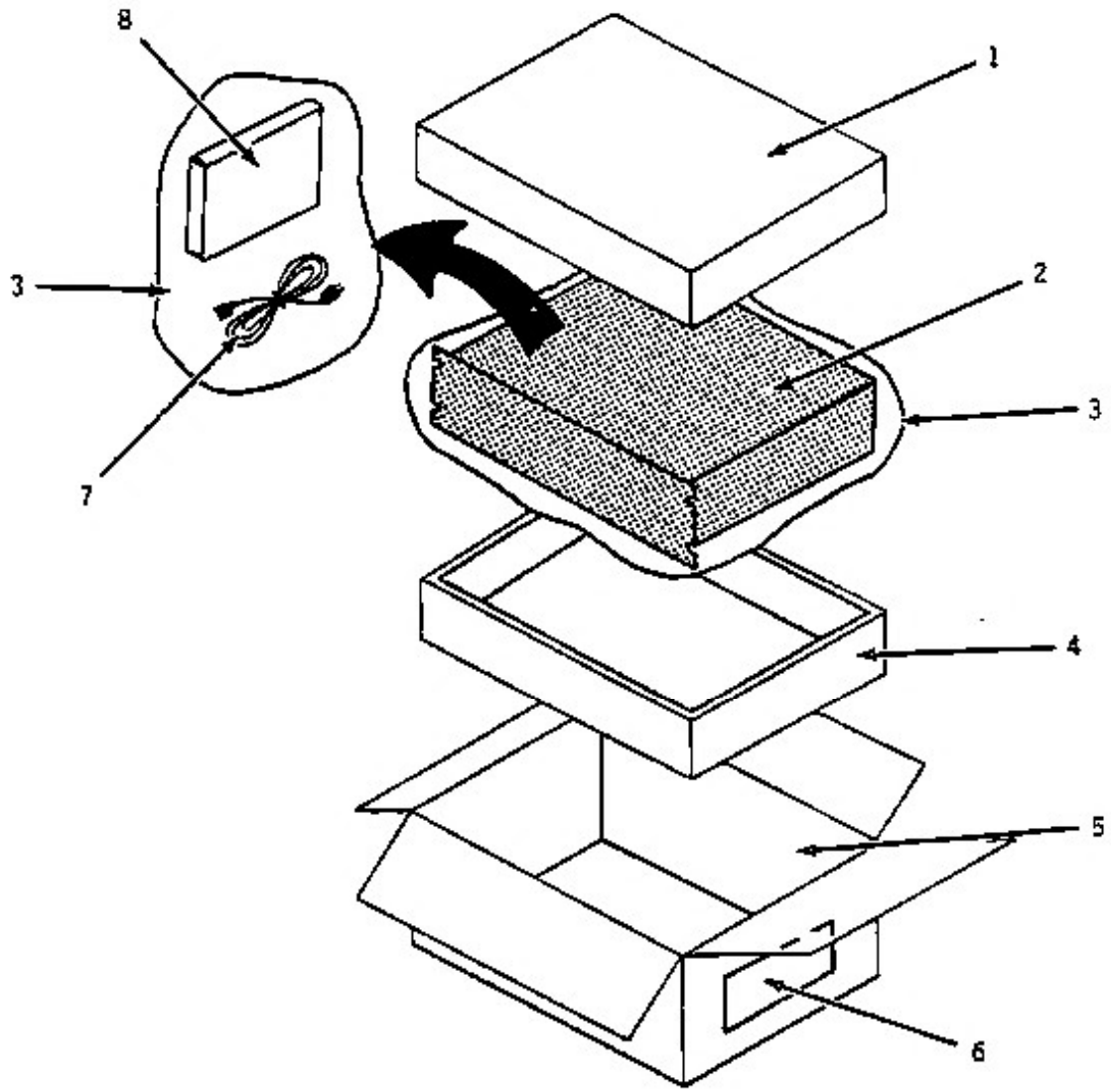
2. Remove top piece (1) from container.

3. Remove Receiver (2) enclosed in a plastic bag from container.

4. Remove Receiver from plastic bag (3).

5. Remove packing slip (6) from plastic envelope on shipping container and check to insure that all items listed on the packing slip were received.

6. Store all packing materials in shipping container and store shipping container for re-use.



1. Top Piece
2. Receiver
3. Plastic Bag
4. Bottom Piece
5. Shipping Container
6. Packing Slip
7. Power Cord
8. Technical Manual

Figure 2-1. Receiver Shipping Container

NOTE

If any item listed on the packing slip was not contained in the shipping container, request disposition instructions from responsible agency.

7. Inspect top and bottom, both sides, and both front and rear panels of equipment for dents, scratches or any visually identifiable structural damage.

8. Inspect controls and indicators on front panel for broken or cracked lenses and for damaged knobs or levers.

9. Inspect jacks and other rear panel mounted devices for damage.

NOTE

If any shipping damage was discovered, request disposition instructions from responsible agency.

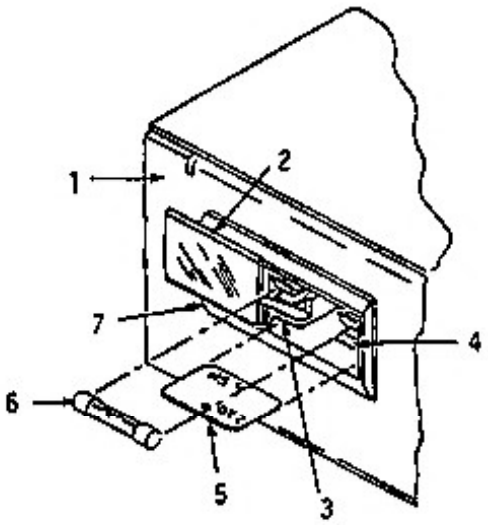
10. When inspection is satisfactorily completed, proceed with minimum performance demonstration.

2-6. INPUT POWER SELECTION. The Receiver can be operated from either a 115 volt or 230 volt primary AC power source. The Receiver is factory strapped for 115-volt operation. As shown in Figure 2-2, to use the Receiver with a 230 volt AC power source, perform steps 1 through 7.

1. Locate AC POWER filter assembly FL1 (7, Figure 2-2) on Receiver rear panel.

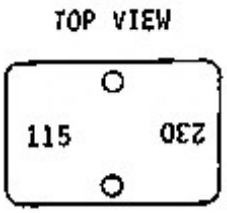
2. Disconnect AC power cord and slide plastic cover (2) fully to left.

3. Push FUSE PULL lever (3) to the left.



DETAIL A
POWER FILTER ASSEMBLY

DETAIL B
CIRCUIT CARD



1. Rear Panel
2. Plastic Cover
3. FUSE PULL Lever
4. Fuse Holder
5. Circuit Card (115/230 VAC)
6. Fuse
7. AC POWER Filter Assembly FL1

Figure 2-2. Input Power Selection

NOTE

One end of the fuse (6) will be ejected as the lever is pushed to the far left position.

4. Remove fuse (6) from fuse holder (4).

5. Insert pointed instrument into hole on circuit card (5) and pull circuit card from slot.

6. As shown in Detail B, Figure 2-2, orient circuit card with desired voltage to left of card and readable (left to right), then insert circuit card fully into slot.

7. Insert correct fuse into fuse holder allowing clearance for FUSE PULL lever (5) to return to right position as fuse is installed.

NOTE

Use 1.25 amp slow-blow fuse for 230 volt operation and 2.5 amp slow-blow fuse for 115 volt operation.

2-7. REMOTE CONTROL INTERFACE ADDRESSING PROCEDURES. The Receiver may be interfaced with a remote controller/computer when fitted with an optional IEEE-488C remote control interface circuit card assembly (A7A9), as applicable. To initialize communication the remote controller/computer must send a binary coded decimal (BCD) address code to the Receiver. This address code is referred to by the mnemonic MLA (my listening address) and preset at equipment.

1. Locate address switch assembly S2 (17, Figure 2-4).

2. Loosen and remove two screws and cover mounted over address switch assembly from receiver rear panel.

NOTE

The following procedures should be implemented using a pointed instrument to facilitate switch setting. In the

following procedures, the ON position is referred to as a logic 1 and the OFF position as a logic 0, however, verify this information in regards to this application with responsible agency at the manufacturer's facility.

3. Position point of instrument/tool on each individual switch 1-8 and set address as required.

4. Align cover over address switch assembly (S2) on receiver rear panel and secure with two screws.

2-8. INITIAL CHECKOUT. Prior to installing the Receiver, the following procedures should be performed to ensure that the Receiver has not been damaged in shipping and to insure operational integrity. (Refer to Figure 3-1 and Table 3-1 for location and function of front panel controls).

1. Depress POWER PUSH/ON switch (26, Figure 3-1) to off.

2. Connect AC power cord between AC POWER filter assembly FL1 on rear panel (30, Figure 2-4) and the proper AC power source as selected in paragraph 2-6.

3. Depress PUSH/ON POWER switch to on, and ensure that front panel indicators illuminate and that a tuned frequency is displayed.

4. Press REMOTE switch to local mode and observe that associated LED indicator is unlit.

5. Press TUNING rate OFF pushbutton switch.

6. Press FM detection mode pushbutton key-switch and observe that associated LED indicator illuminates.

7. Press 10 kHz IF bandwidth pushbutton key-switch and observe that associated LED indicator illuminates.

8. Press AGC FAST pushbutton key-switch and observe that associated LED indicator illuminates.

9. Connect a 600-ohm impedance headset to front panel HEADPHONES jack.

10. Connect a suitable RF antenna to the ANTENNA input connector J1 (3, Figure 2-4) on rear panel.

11. Press TUNING rate FAST pushbutton switch.

12. Press and hold TUNING slew switch lever in either up or down position and tune Receiver to frequency of a local FM station.

13. Monitor audio output using headphones, verify that an audio level is present and can be controlled by associated headphones audio gain control.

14. Press TUNING rate SLOW pushbutton switch.

15. Adjust TUNING control knob in a clockwise (CW) and counter-clockwise (CCW) direction and verify that selected frequency 10 Hz digit changes and that TUNING meter indicates 0 level as station is center tuned.

16. Enter tuned frequency of 100 MHz using numeric (0-9) pushbutton key-switches.

17. Press ENT/EXCL FREQ pushbutton key-switch and ensure that Receiver tunes to 100 MHz as indicated by the frequency display.

18. Depress POWER PUSH/ON switch to off.

19. Disconnect AC power cord from power source and associated antenna, then proceed with installation instructions.

2-9. INSTALLATION INSTRUCTIONS

2-10. To install the Receiver, two sets of procedures must be implemented. These procedures include: installation and cabling. In addition, the Receiver's rear panel components are identified and described.

2-11. INSTALLATION PROCEDURES. The Receiver is designed for rack mounting and is equipped with a standard 19-inch wide, slotted front panel. The Receiver may be installed within an equipment rack on angle supports or by slide mounting, at the option of the using agency. Perform the procedures in paragraph 2-12 or 2-13, as desired, to install the Receiver when using either angle supports or slides, as may be applicable.

NOTE

If the unit is to be installed in an equipment rack, it might be desirable to install the unit with slide mounts. In the event that a slide mount set has not been provided with the unit and seems practical for this installation application (as appropriate), order one set, standard 19-inch Rack Slide Kit, Part Number 81799 from the equipment manufacturer.

2-12. Angle Support Installation - Ensure that angle supports are installed in the equipment rack before proceeding. (See Detail A, Figure 2-3).

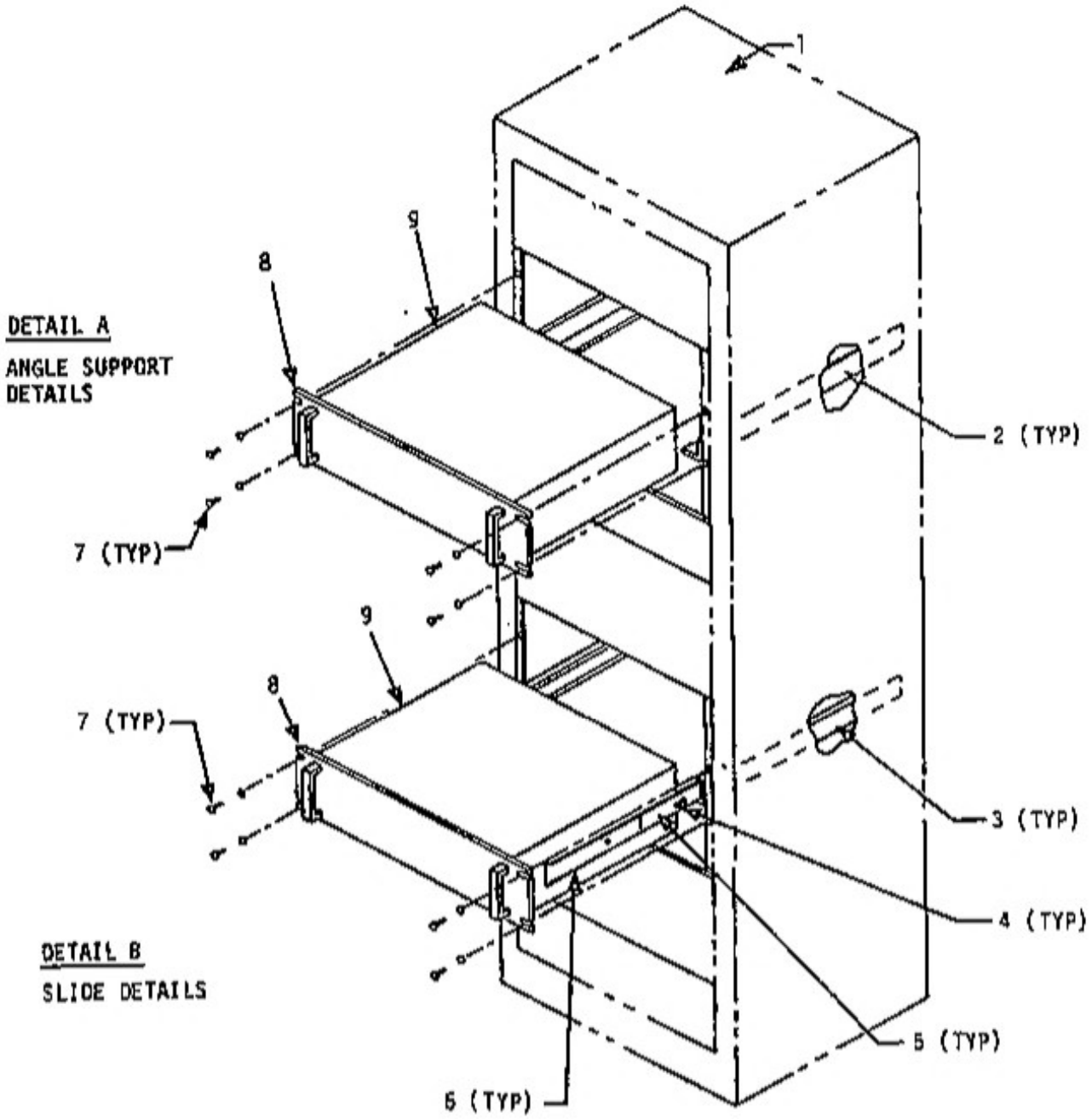
NOTE

In the event that a heat producing unit will be mounted below the Receiver, sufficient cooling fans must be provided, and a minimum of 2 inches of unused space must be allowed directly below the Receiver.

1. Open rear door of equipment rack (1, Figure 2-3) and ensure that cables will not interfere with Receiver installation.

CAUTION

When installing Receiver, be careful not to damage rear panel components.



1. Equipment Rack
2. Angle Support (2)
3. Slide, Stationary Section (2)
4. Spring, Retainer (2)
5. Slide, Intermediate Section (2)
6. Slide, Chassis Section (2)
7. Screw and Washer (4)
8. Front Panel Mounting Holes (4)
9. Receiver

Figure 2-3. Equipment Rack Installation Options

2. Set rear panel side of Receiver squarely on angle supports and slide Receiver (9) into equipment rack (1).

3. Ensure all cables are clear of door and close door on rear of rack.

4. Align front panel mounting holes (8) with threaded mounting holes on both sides of rack, and install four screws and washers (7).

2-13. Slide Installation - This procedure is based on the use of standard three section, straight extension rack slides which can be attached to the Receiver via universal type EIA hole spacings.

1. Attach chassis section slide (6, Figure 2-3) to Receiver and ensure that stationary sections (3) of rack slide are installed in equipment rack (See Detail B, Figure 2-3.)

2. Open rear door of rack and ensure that cables will not interfere with Receiver installation.

CAUTION

When installing Receiver, be careful not to damage rear panel components.

3. Align and insert both intermediate sections (5) of slide into stationary sections (3) and gently slide Receiver (9) into rack until slides catch on spring retainers (4).

4. Release spring retainers and slide Receiver fully into the rack chassis.

5. Ensure all cables are clear of door and close door on rear of rack.

6. Align front panel mounting holes (8) with threaded mounting holes on both sides of rack and install four screws and washers (4).

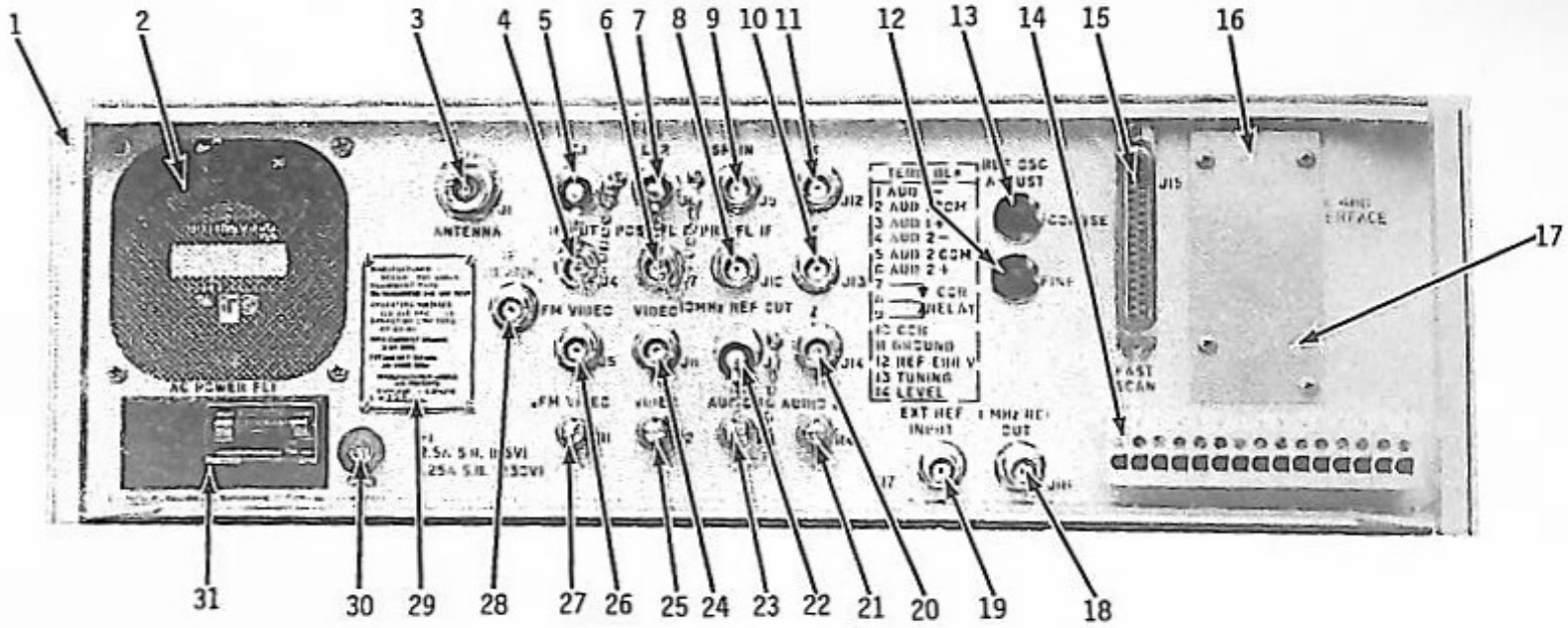
2-14. REAR PANEL COMPONENTS - The rear panel components include: connectors potentiometers, switches, and a terminal block as shown in Figure 2-4; their operational functions are described in Table 2-1.

Table 2-1. Rear Panel Components

FIGURE & INDEX NO.	COMPONENT DESIGNATION	FUNCTION
2-4, 3	ANTENNA J1	Routes RF signal input from associated antenna to receiver circuitry for detection.
5	LO1 J3	Provides a first LO control signal output from the first LO synthesizer module assembly (A5).
4	IF OUT J4	Provides an IF output of 21.4 MHz.
26	FM VIDEO J5	Provides a 93-ohm unbalanced FM video output signal during receiver operation in the FM detection mode.
7	LO2 J6	Provides a second LO control signal output from the second LO module assembly (A4).
6	POST FL IF J7	Provides an IF output centered at 21.4 MHz, from a variable gain amplifier (A6A2) contained within the IF assembly (A6).
24	VIDEO J8	Provides a 93-ohm unbalanced video output signal during receiver operation in any detection mode.
9	SM IN J9	Routes a 21.4 MHz IF signal monitor input to the optional Spectrum Display; the 21.4 MHz IF output of connector J7 is normally jumpered to this input.
8	PRE FL IF J10	Provides a prefiltered IF output signal, centered at 21.4 MHz, from the tuner assembly (A3).
22	10 MHz REF OUT J11	Provides a 10 MHz reference frequency output from the reference generator module assembly (A8); the level of this signal is 50 millivolts to 5 volts peak-to-peak at 50 ohms impedance.
11	X J12	Provides a horizontal deflection output for an external spectrum monitor.
2-4,10	Y J13	Provides a vertical deflection output for an external spectrum monitor.
20	Z J14	Provides a blanking (brightness control) signal output for an external spectrum monitor.
15	FAST SCAN J15	Provides a remote control interface connection to enable a remote Spectrum Surveillance Controller to operate the Receiver in the fast scan mode.

Table 2-1. Rear Panel Components (Cont.)

FIGURE & INDEX NO.	COMPONENT DESIGNATION	FUNCTION
16	IEEE-488 INTERFACE J16	Provides a remote control interface connection to enable a remote controller/computer to control the Receiver through use of digital command words.
17	Address Switch Assembly (S2) (Covered)	Provides for selection of various remote control interface system receiver addresses.
14	TERM BLK TB1	Provides for two balanced audio 1 and 2 outputs, carrier operated relay contact, reference error voltage, and tuning and level signal interconnection to ancillary processing equipments.
19	EXT REF INPUT J17	Routes an external reference frequency standard at 1 MHz, 5 MHz, or 10 MHz to be used in place of 10 MHz reference oscillator generated within the reference generator module assembly (A8).
18	1 MHz REF OUT J18	Provides a 1 MHz reference frequency output from the reference generator module assembly (A8).
27	FM VIDEO R1	Potentiometer used to adjust the output level of the FM video signal which is output from connector J5.
25	VIDEO R2	Potentiometer used to adjust the output level of the video signal which is output from connector J8.
23	AUDIO 1 R3	Potentiometer used to adjust the output level of the audio 1 (USB) signal which is output at terminals 1, 2, and 3 of terminal block (TERM BLK) TB1.
21	AUDIO 2 R4	Potentiometer to adjust the output level of the audio 2 (LSB) signal which is output at terminals 4, 5 and 6 of terminal block (TERM BLK) TB1.
13	REF OSC ADJUST - COARSE	Potentiometer used to course adjust the frequency of the reference oscillator contained within the reference generator module assembly (A8).
12	REF OSC ADJUST - FINE	Potentiometer used to fine adjust the frequency of the reference oscillator contained within the reference generator module assembly (A8).



1. Handle (2)
2. Blower-Fan Assembly
3. ANTENNA Input Connector J1
4. IF OUT Connector J4
5. LO1 Output Connector J3 with Cap
6. POST FL IF Output Connector J7
7. LO2 Output Connector J6 with Cap
8. PRE FL IF Output Connector J10
9. SM IN Connector J9
10. Y-Vertical Deflection Signal Output Connector J13
11. X-Horizontal Deflection Signal Output Connector J12
12. REF OSC ADJUST - FINE Control
13. REF OSC ADJUST - COARSE Control
14. TERM BLK Audio/Control Signal Designation/Pin Out Chart and Connector TB1
15. FAST SCAN Remote Control Interface Connector J15
16. IEEE-488 Remote Control Interface Connector J16 (OPTIONAL)
17. Address Switch Assembly S2 (OPTIONAL)
18. 1 MHz REF OUT Connector J18
19. EXT REF INPUT Connector J17
20. Z Blanking Signal Output Connector J14
21. AUDIO 2 Output Level Potentiometer R4
22. 10 MHz REF OUT Connector J11 with Cap
23. AUDIO 1 Output Level Potentiometer R3
24. VIDEO Output Connector J8
25. VIDEO Output Level Potentiometer R2
26. FM VIDEO Output Connector J5
27. FM VIDEO Output Level Potentiometer R1
28. IF Blank Connector (OPTIONAL)
29. Receiver Nameplate
30. GND Terminal (E1)
31. AC POWER Filter Assembly FL1

Figure 2-4. Receiver Rear Panel Details

2-15. CABLING PROCEDURES - There are three sets of cabling associated with providing receiver operation: input power and signal cabling, output signal cabling, and special cabling. Input power and signal cabling, and output signal cabling must be implemented to complete the Receiver electrical installation as specified by this procedure. Cabling associated with optional operating applications may be implemented as described by Receiver operating instructions (See Figure 2-5 and 3-2).

1. Connect ground wire AWG No. 10, with lugs on both ends, between GND terminal on receiver rear panel and equipment rack chassis ground (as appropriate).

2. Connect AC power cord between AC POWER filter assembly FL1 (30, Figure 2-4) on receiver rear panel and equipment rack 115 volt ±10%, 47 to 62 Hz, AC power receptacle.

NOTE

The following step is to be implemented only when the Receiver is fitted with the optional IEEE-488C remote control interface circuit card assembly (A7A9), otherwise proceed to step 4.

3. Connect IEEE-488C remote control interface buss cable between IEEE-488 remote control interface connector J16 (as applicable) on receiver rear panel and remote controller/computer terminal.

NOTE

Input and output signal cables required for cabling interconnections are not provided with the Receiver. Use compatible cables with the proper impedance matching.

4. Connect input signal cables (as required) between interfacing equipment and appropriate signal input connectors in accordance with Figure 2-5.

5. Connect output signal cables (as required) between appropriate signal output connectors and interfacing equipment in accordance with Figure 2-5.

6. Ensure all cables are clear of door and close door on rear of rack chassis.

2-16. PREPARATION FOR STORAGE

2-17. There are no unique procedures or special circumstances to be considered when preparing the Receiver for storage other than those associated with good commercial practices. Good commercial practices require a degree of protection to prevent the Receiver from incurring physical damage and to prevent deterioration from excessive moisture. For best results, it is suggested that the Receiver be stored in a structure which will sustain a temperature betwen -40° C and +70° C, and maintain a relative humidity of 10 to 95 percent, non condensing. The Receiver may be repackaged in its original shipping container for storage, as shown in Figure 2-1, or at the discretion of the using agency.

2-18. PREPARATION FOR SHIPMENT

2-19. There are no special circumstances to be considered when preparing the Receiver for shipment. The Receiver, properly packaged in its original shipping container or in accordance with other good commercial practices, may be transported by common carrier truck, rail, ship or aircraft, at the discretion of the using agency.

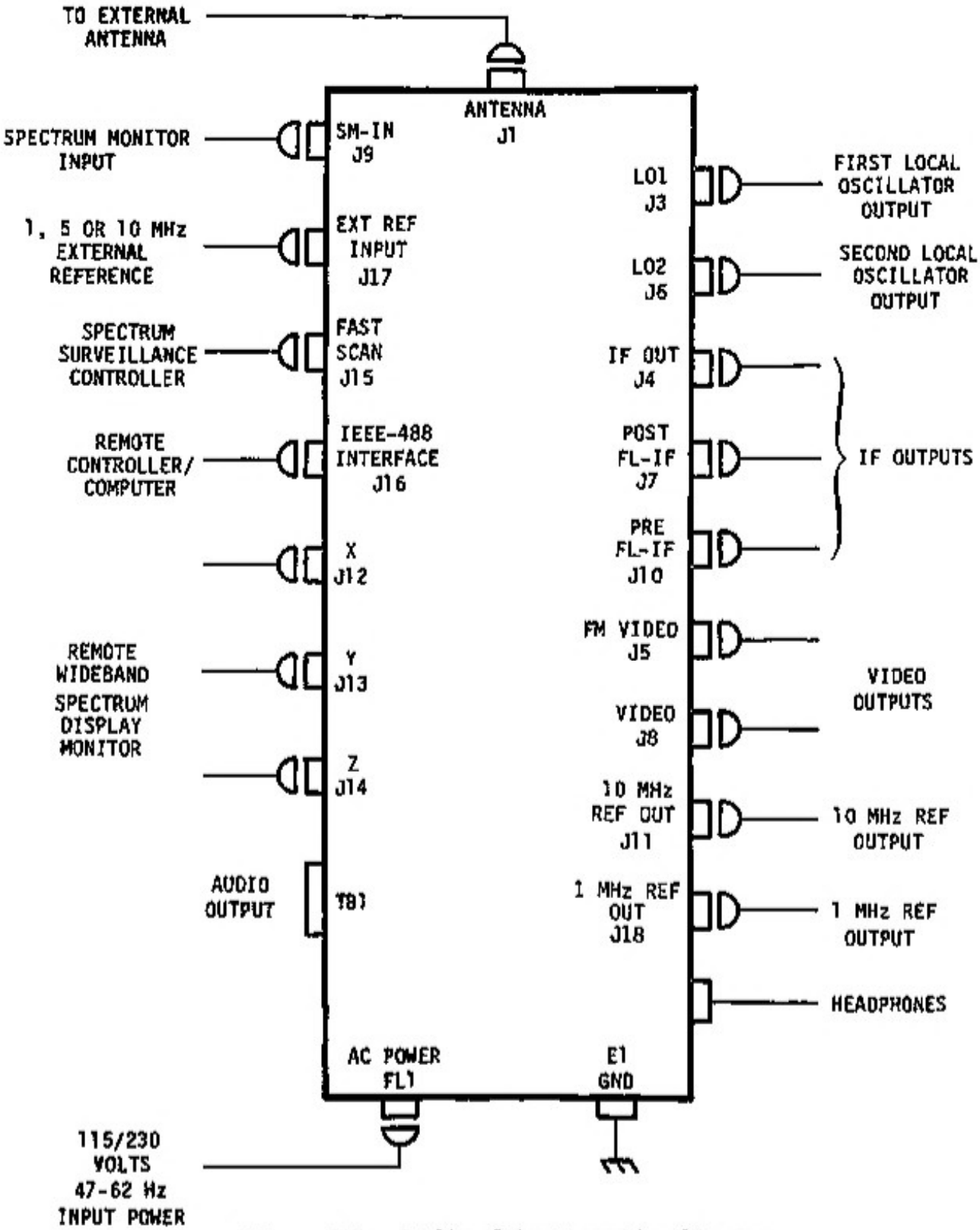


Figure 2-5. Cabling Interconnection Diagram

SECTION III

OPERATION

3-1. INTRODUCTION

3-2. This section provides an operational overview of the Receiver and identifies and describes the functions of the Receiver's controls, indicators, and operator's adjustments. In addition, instructions are included or both normal and special operational applications. It should be noted, however, that operating instructions for the Spectrum Display are not provided within the scope of this manual. However, if the Spectrum Display is integrated within the Receiver, the using agency must refer to the instruction manual for that equipment.

3-3. OPERATIONAL OVERVIEW

3-4. In order to use the complete functional capabilities of the Receiver, an operator must become proficient in understanding and manipulating the controls which comprise the Receiver. Initially, an operating mode must be selected then any available operating parameters of the selected mode may be chosen. For the purpose of this section, it is assumed that sufficient peripheral devices are electronically interfaced with the Receiver, so that command signals, intelligence, and responses may be sent and received within the system, thus allowing commands issued, received, and functional control signals to be generated within the operational system. Such electronic informational exchanges supply drive signals for indicators, displays and meters to provide visual surveillance and monitoring, and byte serial and bit parallel data for control and analysis. Thus, the operator must choose between local or remote control mode of operation, when fitted with the IEEE-488C remote control interface circuit card assembly (A7A9), as may be applicable. Then, a detection mode must be selected and a method of tuning determined, as well as, automatic (AGC) or manual gain control (MGC). A frequency range of RF signal evaluation is then programmed by the selection of an IF bandpass filter bandwidth. At this point, the operator can then manipulate the controls that utilize channel and exclude frequency library memories, therefore, scanning the RF either to detect signals by chance or by design.

3-5. CONTROLS AND INDICATORS

3-6. Front panel controls and indicators are identified on Figure 3-1 and their operational functions are described in Table 3-1. Potentiometers that are located on the rear panel are shown on Figure 2-4; their operational functions are described in Table 2-1.

Table 3-1. Controls and Indicators

FIGURE& INDEX NO.	CONTROL/INDICATOR	FUNCTION
1	100 kHz Pushbutton Key-Switch with LED Indicator	Selects an IF bandpass filter bandwidth of 100 kHz and associated LED indicates that bandwidth has been selected.
2	50 kHz Pushbutton Key-Switch with LED Indicator	Selects an IF bandpass filter bandwidth of 50 kHz and associated LED indicates that bandwidth has been selected.
3	20 kHz Pushbutton Key-Switch with LED Indicator	Selects an IF bandpass filter bandwidth of 20 kHz and associated LED indicates that bandwidth has been selected.
4	10 kHz Pushbutton Key-Switch with LED indicator	Selects an IF bandpass filter bandwidth of 10 khz and associated LED indicates that bandwidth has been selected.
5	FM Pushbutton Key-Switch with LED Indicator	Selects the FM detection mode and associated LED indicates that FM detection mode has been selected.
6	AM Pushbutton Key-Switch with LED Indicator	Selects the AM detection mode and associated LED indicates that AM detection mode has been selected.
7	Blank Pushbutton Key-Switch	No function assigned; reserved for optional ISB function.
8	AFC Pushbutton Key-Switch with LED Indicator	Alternately pressing enables and disables the AFC mode and associated LED indicates when enabled.
9	AGC FAST Pushbutton Key-Switch with LED Indicator	Selects and indicates the automatic RF gain mode. It provides a fast rate of gain adjustment and is the gain mode recommended for most receiver operations.

Table 3-1. Controls and Indicators (Cont.)

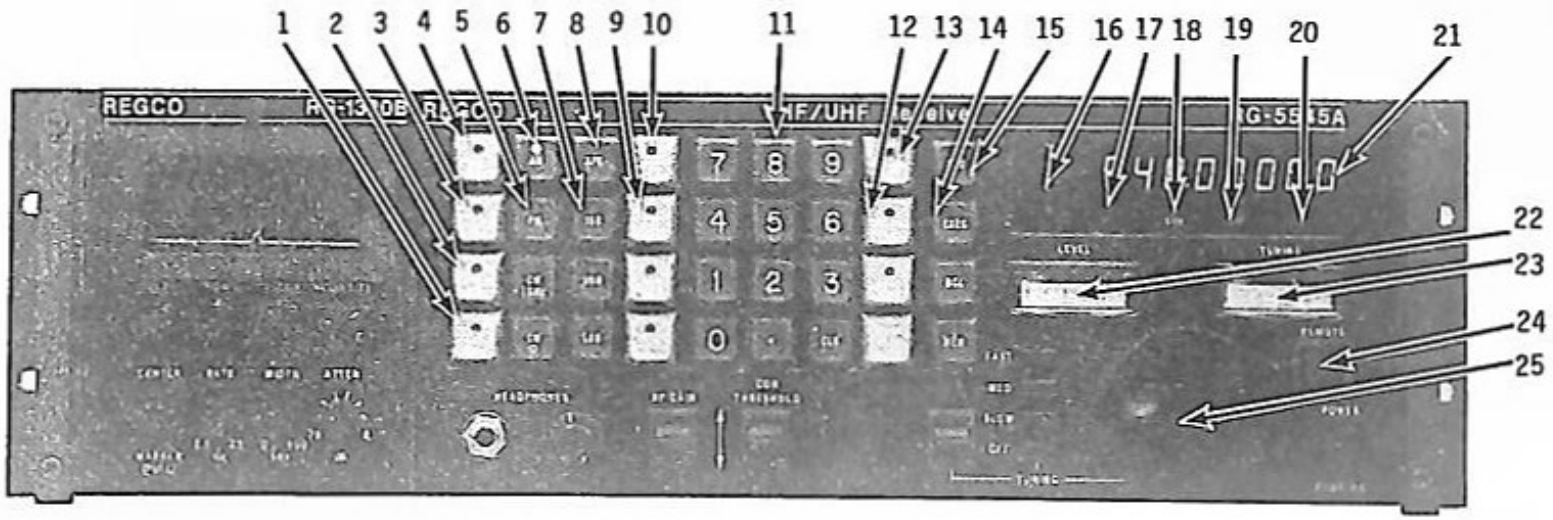
FIGURE & INDEX NO.	CONTROL/INDICATOR	FUNCTION
10	EXT REF Pushbutton Key-Switch with LED Indicator	Selects and indicates that the external reference frequency mode is functional when a 1 MHz, 5 MHz or 10 MHz input frequency is connected to the receiver rear panel; the external reference mode locks the receiver's internal frequency standard to the external frequency reference.
11	Numeric Pushbutton Key-Switches	Contains the digits 0 through 9 and decimal point (.); used to enter selected tuning frequency in tuning mode, start-stop frequencies for scan mode, exclude frequencies for scan exclude frequency mode, channel selection in memory mode, and scan rate selection in scan mode.
12	SCAN UP Pushbutton Key-Switch with LED Indicator	Selects or terminates scan up modes with digit rates from 0 to 9 and associated LED indicates that mode has been selected.
13	SCAN DN Pushbutton Key-Switch with LED Indicator	Selects or terminates scan down modes with digit rates for 0 to 9 and associated LED indicates that mode has been selected.
14	EXEC Pushbutton Key-Switch	Executes the displayed channel in memory mode for operation.
15	STO Pushbutton Key-Switch	Selects and stores programmed channels in memory when used in conjunction with memory mode.
16	MEMORY DISPLAY Annunciator	Indicates the stored channel number most recently called during memory mode.
17	COR THRESHOLD Annunciator	Indicates when COR THRESHOLD is enabled through COR THRESHOLD slew switch.
18	COR Annunciator	Indicates when signal level equals or exceeds pre-set threshold.
19	FAST SCAN Annunciator	Indicates when an optional Spectrum Surveillance Controller has control of Receiver functions.

Table 3-1. Controls and Indicators (Cont.)

FIGURE & INDEX NO.	CONTROL/INDICATOR	FUNCTION
20	REFERENCE UNLOCKED Annunciator	Indicates by flashing on and off in the external reference frequency mode that the internal reference frequency is not locked to the external reference.
21	Frequency Display	Indicates selected tuned frequency to a resolution of 10 Hz with decimal indicating MHz; eight digit LED display.
22	LEVEL Meter	Provides a visual indication of the RF power level at the antenna input.
23	TUNING Meter	Provides a visual indication of relative frequency signal level to which the Receiver is tuned.
24	REMOTE Control Switch	Provides alternate selection between the remote and local control modes.
25	TUNING Control Knob	Used to tune Receiver selected frequency, up or down, at a rate selected by the TUNING rate FAST, MED, or SLOW pushbutton switch.
26	POWER PUSH/ON Switch	Provides on/off control of ac power source to the Receiver.
27	FAST TUNING Rate (100 kHz) Pushbutton Switch	These four pushbutton switches control the tuning rate (in Hz) at which the TUNING switches and TUNING control knob tune the Receiver; OFF disables both tuning controls.
28	MED TUNING Rate (1 kHz) Pushbutton Switch	
29	SLOW TUNING Rate (10 Hz) Pushbutton Switch	
30	OFF TUNING Rate Pushbutton Switch	
31	RCL Pushbutton Key-Switch	Provides for recall of channels stored in channel memory.
32	MEM Pushbutton Key-Switch with LED Indicator	Selects and indicates the channel memory scan mode.
33	TUNING Slew Switch	Used to tune Receiver selected tuning frequency, up or down, at a rate selected by the TUNING mode FAST, MED, or SLOW pushbutton switch.
34	CHAN SCAN Pushbutton Key-Switch with LED Indicator	Selects and indicates the channel memory scan mode.

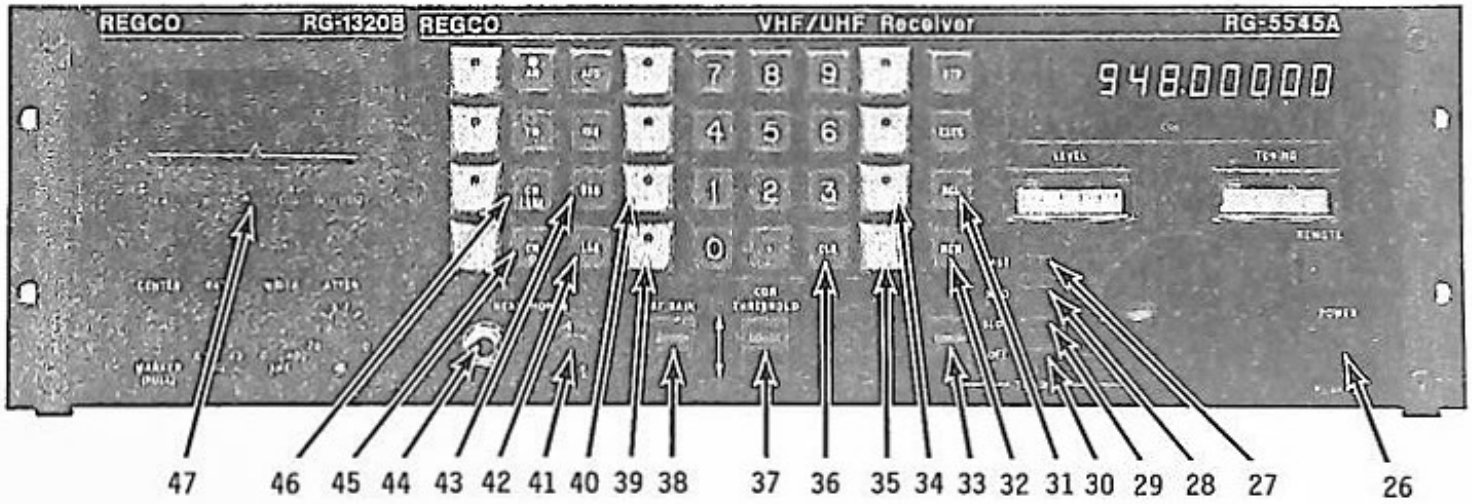
Table 3-1. Controls and Indicators (Cont.)

FIGURE & INDEX NO.	CONTROL/INDICATOR	FUNCTION
35	ENT/EXCL FREQ Pushbutton Key-Switch	Enters selected tuning frequency or frequencies into the exclude frequency memory library.
36	CLR Pushbutton Key-Switch	Clears digits entered but not yet executed with the enter pushbutton key-switch; terminates memory mode, and continues scan when scan has locked on a COR threshold signal.
37	COR THRESHOLD Slew Switch	Enables the carrier operated relay (COR) and adjusts the threshold at which it operates.
38	RF GAIN Slew Switch	Adjusts receiver gain in MGC mode.
39	MGC Pushbutton Key-Switch with LED Indicator	Selects and indicates the manual gain control (MGC) mode.
40	AGC SLOW Pushbutton Key-Switch with LED Indicator	Selects and indicates the slow automatic gain control (AGC) mode
41	HEADPHONES Audio Gain Controls (USB and LSB)	Adjusts the audio level to the headphones jack.
42	Blank Pushbutton Key-Switch	No function assigned; reserved for optional LSB function.
43	Blank Pushbutton Key-Switch	No function assigned; reserved for optional USB function.
44	HEADPHONES Jack	Provides audio signal output for 600 ohm headset.
45	CWD Pushbutton Key-Switch with LED Indicator	Selects and indicates the CW detection mode with 0 offset.
46	CW 1 KHz Pushbutton Key-Switch with LED Indicator	Selects and indicates the CW detection mode with 1 KHz offset.
47	Spectrum Display	Refer to equipment manual for Spectrum Display Unit, Type RG-1320B
	Address Switch Assembly (Covered)	Provides for selection of various protocol interface specifications (See Table 2-2).



1. 100 KHz Pushbutton Key-Switch
2. 50 KHz Pushbutton Key-Switch
3. 20 KHz Pushbutton Key-Switch
4. 10 KHz Pushbutton Key-Switch
5. FM Pushbutton Key-Switch
6. AM Pushbutton Key-Switch
7. ISB Pushbutton Key-Switch (Optional)
8. AFC Pushbutton Key-Switch
9. AGC FAST Pushbutton Key-Switch
10. EXT REF Pushbutton Key-Switch
11. Numeric 0-9, decimal point (.) Pushbutton Key-Switches
12. SCAN UP Pushbutton Key-Switch
13. SCAN DN Pushbutton Key-Switch
14. EXEC Pushbutton Key-Switch
15. STO Pushbutton Key-Switch
16. MEMORY DISPLAY LED Indicator with Annunciator
17. COR THRESHOLD Annunciator
18. COR Annunciator
19. FAST SCAN Annunciator
20. REFERENCE UNLOCKED Annunciator
21. Frequency Display
22. LEVEL Meter
23. TUNING Meter
24. REMOTE Switch
25. TUNING Control Knob

Figure 3-1. Front Panel Controls and Indicators (Sheet 1 of 2)



26. POWER PUSH/ON Switch
27. TUNING Rate FAST Pushbutton Key-Switch
28. TUNING Rate MED Pushbutton Key-Switch
29. TUNING Rate SLOW Pushbutton Key-Switch
30. TUNING Rate OFF Pushbutton Key-Switch
31. RCL Pushbutton Key-Switch
32. MEM Pushbutton Key-Switch
33. TUNING Slew Switch
34. CHAN SCAN Pushbutton Key-Switch
35. ENT/EXCL FREQ Pushbutton Key-Switch
36. CLR Pushbutton Key-Switch
37. COR THRESHOLD Slew Switch
38. RF GAIN Slew Switch
39. MGC Pushbutton Key-Switch
40. AGC SLOW Pushbutton Key-Switch
41. HEADPHONES Gain Control
42. LSB Pushbutton Switch (Optional)
43. USB Pushbutton Switch (Optional)
44. HEADPHONES Jack
45. CW 0 Pushbutton Key-Switch
46. CW 1 KHz Pushbutton Key-Switch
47. Spectrum Display Unit*

*NOTE: Refer to Spectrum Display Unit, Type RG-1320B equipment manual for front panel controls and indicators.

Figure 3-1. Front Panel Controls and Indicators (Sheet 2 of 2)

3-7. OPERATING INSTRUCTIONS

3-8. These operating instructions are designed to familiarize the operator with the different operational parameters within operating modes available. The Receiver may be operated from the front panel (local control), from a remote controller/computer (remote control), or from a Surveillance Controller (fast scan control), as may be applicable. In either the local or remote modes, the Receiver may be operated in any detection mode, using any one of four IF bandpass filter bandwidths, and AGC modes and scan modes. In addition, the channel memory and exclude frequency library memory may be programmed, stored, recalled or executed in both the local and remote modes of operation. In the fast scan control mode, a Spectrum Surveillance Controller, connected to the Receiver, directs all Receiver operations. The operating instructions are provided in three control modes of operation; local, remote and fast scan. The operator should familiarize himself with the local operating techniques before attempting remote or fast scan operation. The local operating instructions provide detailed operating techniques and descriptions, while remote and fast scan instructions describe operating format, commands and interface requirements.

NOTE

Operational expertise using the Receiver in the local control mode of operation is suggested prior to attempting operation in the remote control mode, as may be applicable. The operator must first connect the primary AC power source to the Receiver, turn power on, and then select local control mode of operation by depressing the REMOTE switch. When the Receiver is functioning in the remote control mode, the associated LED indicator will be on, whereas when the Receiver is in the local control mode the associated LED indicator will be off.

3-9. LOCAL OPERATION CONTROL MODES. Paragraphs 3-10 through 3-18 describe the basic operating parameters for the Receiver. Because of the various modes and conditions in which these parameters may be used, the following descriptions are not intended as operating procedures but to familiarize the operator with the various operating parameters. If they are used in conjunction with local operation, power must be turned on, and the REMOTE switch must be set for local operation. For typical local control operating instructions refer to paragraph 3-19.

3-10. Detection Modes. The Receiver provides several detection modes which include: AM, FM, CW with 0 offset, CW with 1 kHz offset, USB, LSB, and ISB, as may be applicable. Selection of either of the available modes of operation is made by pressing the appropriate mode selection pushbutton key-switch located on the front panel of the Receiver. When a mode is selected, the associated LED indicator will illuminate. It should also be noted, that selection of a detection mode will automatically disable the previous detection mode, and therefore only a single mode of detection can be made operable or selectable at any given time. The available detection modes and associated criteria are as follows:

a. AM Mode - Amplitude Modulation

   1. Press AM pushbutton key-switch to select AM mode.

   2. Select desired IF bandwidth by pressing 10 kHz, 20 kHz, 50 kHz, or 100 kHz pushbutton key-switch.

   3. Select desired gain control mode by pressing MGC, AGC SLOW, or AGC FAST pushbutton key-switch.

b. FM Mode - Frequency Modulation; a demodulated FM signal will produce the carrier, or center frequency; that carrier plus the frequency of modulation as a higher frequency; that carrier minus the frequency of modulation as a lower frequency; and, the modulation as a transmitted frequency. However, the latter signal frequency will not be within the passband of the Receiver.

1. Press FM pushbutton key-switch to select FM mode.

NOTE

Although any bandwidth can be selected, a band slightly greater than the maximum carrier deviation should be used to ensure a full scale output without distorting the signal.

2. Select desired IF bandwidth by pressing 10 kHz, 20 kHz, 50 kHz, or 100 kHz pushbutton key-switch.

NOTE

The AGC SLOW gain control mode is not recommended for use during FM signal detection.

3. Select desired gain control by pressing either AGC FAST or MGC pushbutton key-switch.

c. CW 0 - Carrier Wave; if an unmodulated carrier is received, the IF signal of that carrier will be at 21.4 MHz, and the audio signal associated with that carrier will not be present in either the headphones or ancillary speaker output.

CW 1 kHz - Carrier Wave; when this mode is selected, audio monitoring is available, in conjunction with a 1 kHz tone in the headphones and ancillary speaker, due to the 1 kHz offset in processing the audio signals.

NOTE

The CW0 mode utilizes a fixed CW detection mode and the CW 1 kHz mode utilizes a 1 kHz offset CW detection mode.

1. Press CW 0 or CW 1kHz pushbutton key-switch to select desired CW mode of operation.

2. Select an IF bandwidth that will permit sufficient offset to produce a tone frequency from the HEADPHONES output jack.

3. Monitor audio signal output from HEADPHONES output jack and tune Receiver to frequency slightly offset from the carrier frequency to produce an audio signal tone.

d. USB (Optional) - Upper Sideband; by convention, selection of upper sideband is higher in frequency than the carrier frequency and is in the frequency band 3200 kHz wide, which begins 200 kHz higher than the carrier frequency. Selection of the USB detection mode allows evaluation of the sideband that is located within that band of frequencies.

NOTE

When the USB detection mode is selected, audio signal tones of a lower sideband (LSB) signal will not be heard in either the headphones or speaker outputs. To monitor a LSB signal with audio, it is necessary to select the independent sideband (ISB) detection mode. Refer to sub-paragraph f.

1. Press USB pushbutton key-switch to select USB mode.

2. Select desired IF bandwidth by pressing either 10 kHz, 20 kHz, 50 kHz, or 100 kHz pushbutton key-switch, as appropriate.

3. Select desired gain control by pressing either MGC, AGC SLOW, or AGC FAST pushbutton key-switch.

e. LSB (Optional) - Lower Sideband; by convention, the lower sideband is lower in frequency than the carrier wave frequency, and is in the frequency band 3200 kHz wide, which begins 200 kHz lower than the carrier wave frequency. Selection of the LSB detection mode allows evaluation of the sideband that is located within that band of frequencies.

NOTE

When the LSB detection mode is selected, audio signal tones of an upper sideband (USB) signal will not be heard in either the headphones or speaker outputs. To monitor a USB signal with audio, it is necessary to select the independent sideband (ISB) detection mode. Refer to sub-paragraph f.

1. Press LSB pushbutton key-switch to select LSB mode.

2. Select desired IF bandwidth by pressing either 10 kHz, 20 kHz, 50 kHz, or 100 kHz pushbutton key-switch, as appropriate.

3. Select desired gain control by pressing either MGC, AGC SLOW, or AGC FAST pushbutton key-switch.

f. ISB (Optional) - Independent Sideband; the independent sideband is not a sideband signal, however, selection of the ISB detection mode allows an audio signal tone of either LSB or USB to be monitored while operating the Receiver in the opposite sideband detection mode. Refer to sub-paragraphs d and e.

1. Press ISB pushbutton key-switch to select ISB mode.

2. Select desired IF bandwidth by pressing either 10 kHz, 20 kHz, 50 kHz, or 100 kHz pushbutton key-switch, as appropriate.

3. Select desired gain control by pressing either MGC, AGC, SLOW, or AGC FAST pushbutton key-switch.

3-11. Frequency Tuning. With the Receiver in the local control mode of operation, four methods of tuning are available to the operator which include: manual tuning using the TUNING control knob; manual tuning using the TUNING slew switch; manual tuning using the 10 digit (0-9) numerical pushbutton key-switches with decimal point (.) and ENT/EXCL FREQ (enter excluded frequency) pushbutton key-switch; and, automatic scanning (up or down) of the entire frequency range of the Receiver. It should also be noted, that when using either the manual or automatic tuning method, the selected tuning frequency may be changed at a fast (100 kHz), medium (1 kHz), or slow (10 Hz) rate.

NOTE

The four TUNING rate pushbutton key-switches labeled FAST, MED, SLOW, and OFF do not operate independently of each other. If one of the switches is pressed, any other switch that had been pressed will be reset. Therefore, it is only capable to have a single tuning rate operational at any one time.

a. TUNING Slew Switch

1. Select desired tuning rate by pressing either FAST, MED, or SLOW TUNING rate pushbutton switch.

2. Set and hold TUNING slew switch in up position to increase frequency or down position to decrease frequency, and observe corresponding change on frequency display.

3. Release TUNING slew switch when frequency display indicates desired frequency.

4. Press TUNING rate OFF pushbutton switch to lock Receiver at desired frequency and disable tuning controls.

NOTE

When using the TUNING rate FAST pushbutton switch, the 100 kHz digit, located immediately to the right of the decimal point, will change; when using the MED pushbutton switch the 1 kHz digit, the third digit to the right of the decimal point will change; when using the SLOW pushbutton switch, the 10 Hz digit, the fifth digit to the right of the decimal point will change. These changes occur as the receiver is tuned manually either using the tuning control knob or tuning slew switch lever.

b. TUNING Control Knob

1. Select desired tuning rate by pressing either FAST, MED OR SLOW TUNING rate pushbutton switch.

2. Adjust TUNING control knob in a clockwise (CW) direction to increase frequency or counterclockwise (CCW) to decrease frequency and observe that frequency changes on frequency display.

3. Discontinue adjusting TUNING control knob when frequency display indicates desired frequency.

4. Press TUNING rate OFF pushbutton switch to disable TUNING control knob and lock Receiver at desired frequency.

c. Tuning using 10 Digit (0-9) with Decimal Point (.) Numerical Pushbutton Key-Switches.

1. Enter desired frequency by pressing appropriate pushbutton key-switches sequentially selecting significant to least significant digits.

NOTE

For example for a frequency of 204.06088, press 2, 0, 4,. (decimal point), 0, 6, 0, 8 and in that order. If an incorrect digit is selected during tuning frequency entry, press CLR pushbutton key-switch to erase entries, then reselect the desired frequency.

2. Press ENT/EXCL FREQ pushbutton key-switch to tune Receiver.

d. Scan Tuning - See paragraph 3-16.

3-12. Gain Control Modes. The Receiver can be operated in either manual gain control (MGC) or automatic gain control (AGC) modes.

a. Manual Gain Control (MGC)

1. Press MGC pushbutton key-switch to set Receiver in manual gain control mode.

2. Set and hold RF GAIN slew switch in up or down position to obtain desired level as indicated by front panel LEVEL meter. Press lever switch up to increase gain, down to decrease gain, in addition, the level meter indicates relative attenuation when in the MGC mode.

b. Automatic Gain Control (AGC)

1. Selected desired AGC time constant by pressing either AGC FAST or AGC SLOW pushbutton key-switch.

3-13. IF Bandwidth - One of four IF bandwidths may be selected during Receiver operation; however, the narrowest bandwidth to incompass the detected signal should be used, such as in the FM mode where the bandwidth depends on maximum carrier deviation.

1. Select desired IF bandwidth by pressing either 10 kHz, 20 kHz, 50 kHz or 100 kHz pushbutton key-switch.

3-14. Carrier Operated Relay (COR) - This function is activated through the COR THRESHOLD slew switch. The switch has two functions which include; to activate the COR THRESHOLD annunciator, in conjunction with displaying the threshold level on the LEVEL meter, and to adjust the COR threshold level.

1. Set and hold COR THRESHOLD slew switch in up or down position and release.

2. Observe that COR THRESHOLD annunciator appears and a threshold level is indicated on LEVEL meter.

NOTE

The COR THRESHOLD annunciator will remain on for two seconds when the switch is actuated for the first time. It must be actuated, up or down, a second time within the two second period to adjust the COR Threshold.

3. Within two seconds, press the COR THRESHOLD slew switch down (to increment) or up (to decrement) to appropriate level indicated on LEVEL meter.

NOTE

It should be noted that the incrementing or decrementing will be variable so that the longer the switch is held in either position the faster the threshold level will change. In addition, the COR THRESHOLD annunciator will disappear after the COR THRESHOLD slew switch has

been in the center position for two seconds and COR annunciator will appear when the receiver signal level or the MGC attenuation level exceeds the set threshold.

3-15. Automatic Frequency Control (AFC) - This function operates in conjunction with the COR threshold, so that when the COR line asserts, the receiver tuned frequency will be centered in the IF passband.

1. Press AFC pushbutton and observe that associated LED indicator illuminates.

NOTE

In scan mode, if AFC cannot lock on a signal, the AFC LED indicator will blink three times and the scan will continue.

2. Press AFC pushbutton a second time to disable AFC mode and observe that AFC indicator goes out.

3-16. Scan Modes - The Receiver may be operated in any one of five different scan modes which include: scan up or down to the Receiver frequency limits; scan up or down with preset frequency limits; automatic stop and hold on a preset COR threshold level; automatic skip of a preset COR threshold level; (excluding frequencies) and, memory channel scan with automatic stop on a preset COR threshold level.

a. Scan Up or Down to Receiver Frequency Limits.

NOTE

If frequency limits have been previously set for the scan mode, then the Receiver limits will have to be entered (see sub-paragraph b).

1. Press SCAN UP pushbutton key-switch and observe that associated LED indicator illuminates and a flashing zero occurs in the left most digit.

2. Press numeric pushbutton key-switch 1 and observe that frequency indicated increases at 10 Hz per second rate.

3. Press numeric pushbutton key-switch 8 and observe that frequency increases at 100 MHz per second rate and that scan occurs to Receiver upper frequency limit, then skips to lower limit and begins over again.

NOTE

If the Receiver is scanned in the AFC mode, the highest scan rate will be either 5 or 6, depending on the IF bandwidth selected.

4. Press numeric pushbutton key-switch 0 and observe that scan stops, and that Receiver remains in scan up mode.

5. Press SCAN UP pushbutton key-switch and observe that associated LED indicator goes out.

NOTE

The Receiver is no longer in the scan mode. Repeat steps 1-5 for scan down mode by pressing SCAN DN pushbutton key-switch and selecting any numeric rate from 0 to 9.

b. Scan with Pre-Set Frequency Limits.

NOTE

If scan limits have not been programmed or the memory has been dumped, the upper and lower limits will be the Receiver frequency limits.

1. Press SCAN UP pushbutton key-switch and observe that associated LED indicator illuminates and a frequency is displayed with a flashing 0 as left most digit.

NOTE

This frequency is the upper scan limit.

2. Press SCAN DN pushbutton key-switch and observe that associated LED indicator illuminates and a frequency is displayed, with a flashing 0 as left most digit.

3. Remove Receiver from scan mode of operation by pressing SCAN DN pushbutton key-switch and observe that associated LED indicator goes out.

4. Enter 800 MHz using numeric pushbutton key-switches, then press SCAN UP pushbutton key-switch, and observe that associated LED indicator does not come on.

NOTE

Step 4 enters the upper frequency limit but does not display it on the frequency display. To display the frequency limit repeat step 1.

5. Enter 400 MHz using numeric (0-9) pushbutton key-switches, then press SCAN DN pushbutton key-switch, and observe that associated LED indicator does not illuminate.

NOTE

Step 5 enters the lower frequency limit but does not display it on the frequency display. To display the frequency limit repeat step 2.

6. To scan between the frequency limits set in steps 4 and 5 refer to paragraph 3-16a.

c. Scan with Automatic Stop on Pre-Set COR Threshold

NOTE

Verify that COR threshold level has been established in the Receiver (see paragraph 3-14).

1. Select scan mode, either up or down, at a 1 MHz rate (numeric pushbutton key-switch 6).

2. Press AFC pushbutton key-switch and observe that associated LED indicator illuminates.

NOTE

Verify that the scanning stops on a frequency where the signal level is above the pre-set COR threshold. The AFC action will lock Receiver tuning to the received carrier. If the signal level drops below the pre-set threshold and remains there for 0.5 seconds, scanning will automatically resume.

3. To manually resume scan, press CLR pushbutton key-switch.

NOTE

This disables the AFC function for a frequency range of four times the selected IF bandwidth; however, if the signal remains above the threshold the scan will again stop on this frequency on its next scan.

4. To terminate AFC function, press AFC pushbutton key-switch and observe that associated LED indicator goes out.

NOTE

Scanning will resume from a locked condition when AFC is terminated.

d. Excluding Frequencies from the AFC Function

1. Set up Receiver in scan mode as described in sub-paragraph c above.

NOTE

When the scanning stops on a pre-set threshold signal, and it is desired to exclude this frequency from a scan stop, implement step 2.

2. Press ENT/EXCL FREQ pushbutton key-switch.

NOTE

Observe that the scan continues and that it skips (four times the IF bandwidth selected) this frequency on subsequent scans. As many as 300 frequencies may be entered into the exclude frequency library. To review or modify this library refer to paragraph 3-17.

e. Memory Channel Scan

NOTE

Before proceeding, ascertain that the Receiver set-ups have been loaded into the channel memory and that channels have been activated for channel scan (see paragraph 3-18).

1. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator illuminates.

NOTE

Observe that the channel numbers on the MEMORY DISPLAY are incrementing upward to the highest active channel, then start over again from the lowest active channel with approximately a 20 millisecond pause on each channel. In addition, channel scanning will stop when a channel is found with its signal level above the preset threshold. To resume channel scanning, proceed to step 2.

2. Press CLR pushbutton key-switch and observe that Receiver steps to next channel in memory.

NOTE

To terminate channel scanning, proceed to step 3.

3. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator goes out.

3-17. Exclude Frequency Library - The exclude frequency library is programmed to accept and store frequencies for exclusion in the AFC scan mode. The library has a memory capacity for up to 300 frequencies and can be reviewed and/or modified using the front panel controls, or from a remote controller/computer. The exclude frequency will be a frequency range that is four times the IF bandwidth selected. The exclude frequency library is operated in the memory mode at channel 00.

1. Press MEM pushbutton key-switch and observe that associated LED indicator illuminates.

2. Press TUNING slew switch to step memory to channel 00, then press RCL pushbutton key-switch to recall exclude frequency library.

NOTE

The exclude frequencies are stacked in numerical order. When frequencies are added or removed they are automaticlaly filed in numerical order. When the exclude frequency library is recalled, the lowest frequency in the stack is recalled and displayed. If no frequencies are filed the display will be blank.

3. Enter 385.76540 MHz using numerical pushbutton key-switches, then press ENT/EXCL FREQ pushbutton key-switch.

NOTE

Observe that this frequency is displayed as a new entry to the library.

4. Press TUNING slew switch lever up or down to step through exclude frequency library, then return to frequency entered in step 3.

5. Press CLR pushbutton key-switch and observe that 385.76540 MHz is no longer displayed but that next higher frequency in library is displayed.

NOTE

Any frequency may be added to the library as demonstrated in step 3 or removed as in step 5. The library stack will always be sorted in numerical order.

3-18. Channel Memory - The channel memory can accept and store up to 99 (01 to 99) channels with a full operating parameter set-up. The channels may be recalled, reviewed, edited or stored without affecting Receiver operation or any channel may be executed to change the Receiver set-up.

1. Press MEM pushbutton key-switch and observe that associated LED indicator and MEMORY DISPLAY annunciator illuminate, and that a channel number is indicated.

NOTE

The TUNING slew switch may be used to step through (address) the memory channels. Channel 00 is not a valid channel for Receiver set-ups. This channel is used for addressing the exclude frequency library (see paragraph 3-17).

2. To view contents of a channel, address channel and press RCL pushbutton key-switch.

NOTE

The contents of the memory channel will be transferred to the front panel. The MEMORY DISPLAY will blink on and off to indicate to the operator that the front panel displays do not necessarily reflect the current operating conditions.

NOTE

The contents of the channel may now be altered by changing the Receiver set-up in the same manner as would be used under normal receiver operation; however, only the front panel displays will be altered without affecting receiver operation.

3. To store contents of channel, as indicated by the front panel display, press STO pushbutton key-switch.

4. To change receiver current operating condition to that indicated for channel memory, press EXEC pushbutton key-switch.

5. To activate a channel for channel scanning, press CHAN SCAN pushbutton key-switch and note that associated LED indicator illuminates for approximately 1 second and goes off.

NOTE

Only the active channels will be scanned in the memory mode.

6. If a channel is already active, CHAN SCAN LED indicator will light when channel is recalled.

7. To de-activate a channel, press CHAN SCAN pushbutton key-switch and observe that associated LED indicator goes out.

3-19. TYPICAL LOCAL CONTROL MODE OPERATING INSTRUCTIONS - These instructions are designed to provide the operator with a familiarization of the local control mode of operation for the Receiver. These instructions are not intended to cover all the various combinations of Receiver operation. The operator should familiarize himself with the local operation control modes described in paragraphs 3-9 through 3-18 before attempting to perform this procedure.

1. Depress POWER PUSH/ON switch and observe that a frequency display is present and that various front panel indicators are illuminated.

NOTE

The Receiver integrates a RAM memory retention system which will cause the Receiver to return to the last operating set-up before power was turned off.

2. Observe REMOTE switch and if illuminated, press switch to obtain local control operation, and observe that associated LED indicator goes out.

3. Press AM pushbutton key-switch and observe that associated LED indicator illuminates and all other detection mode pushbutton key-switch LED indicators are off.

4. Press 10 kHz pushbutton key-switch to select narrowest IF bandwidth and observe that associated LED indicator illuminates.

NOTE

Observe that all other IF bandwidth indicators are off.

5. Press numeric pushbutton key-switches 8, 5, 0, .(decimal point), 5, 4, 3, 2, and 1 in sequence, then press the ENT/EXCL FREQ key and observe that Receiver tunes to 850.54321 MHz.

6. Press MGC pushbutton key-switch and observe that associated LED indicator is on and that both AGC FAST and AGC SLOW LED indicators are off.

7. While observing LEVEL meter, press and hold RF GAIN slew switch in either up or down position to adjust a threshold for MGC.

NOTE

Level meter indicates approximate reading in decibels (dB).

8. Press TUNING rate FAST pushbutton key-switch, then press and hold TUNING slew switch in down position and observe that Receiver frequency decreases at a fast (100 kHz) rate.

9. Tune Receiver to a known FM station.

10. Press TUNING rate SLOW pushbutton key-switch, observe TUNING meter and adjust TUNING control knob until 0 indication is obtained.

11. Press TUNING rate OFF pushbutton key-switch and verify that the TUNING slew switch and control knob are disabled.

12. Connect a 600 ohm headset to the front panel HEADPHONES jack, then verify that an audio signal is present and that the audio signal level can be adjusted with associated gain control.

13. Momentarily press COR THRESHOLD slew switch either up or down, then release and observe that COR THRESHOLD annunciator appears and LEVEL meter is operational.

NOTE

The COR THRESHOLD annunciator will remain activated for approximately two seconds and then disappears, unless the COR THRESHOLD slew switch is activated a second time.

14. With COR THRESHOLD annunciator activated, press COR THRESHOLD slew switch either up or down to obtain a low COR threshold level of 20 dB.

15. Enter 600 MHz using numeric pushbutton key-switches and press SCAN UP pushbutton key-switch to set an upper scan limit.

16. Enter 100 MHz using numeric pushbutton key-switches and press SCAN DN pushbutton key-switch to set a lower scan limit.

17. Press AFC pushbutton key-switch and observe that associated LED indicator illuminates.

18. Press SCAN UP pushbutton key-switch, then enter a scan rate of 6 (1 MHz per second) using numeric pushbutton key-switches and observe that Receiver begins scanning from 100 MHz toward 600 MHz in steps of 1 MHz per second.

NOTE

The scan will automatically stop when it reaches a frequency with a signal level above the pre-set threshold.

19. Press CLR pushbutton key-switch and observe that Receiver resumes scanning.

NOTE

When scanning stops on pre-set threshold signal, press ENT/EXCL FREQ pushbutton key-switch and observe that the scan continues, and that it skips (four times the selected IF bandwidth) this frequency on subsequent scans.

20. Press 0 numeric pushbutton key-switch and observe that Receiver stops scanning but remains in scan up mode.

21. Press SCAN DN pushbutton key-switch, then press numeric pushbutton key-switch 6 and observe that Receiver scans down in 1 MHz steps per second.

22. Press SCAN ON pushbutton key-switch a second time and observe that Receiver de-activates scan mode.

23. Press MEM pushbutton key-switch and observe that associated LED indicator and MEMORY DISPLAY annunciator is on, and that a channel number is indicated.

24. Press and hold TUNING slew switch lever in up or down position to step to channel number 24.

25. Press RCL pushbutton key-switch and observe that front panel displays and indicators show parameter set-up contained for channel 24, and that MEMORY DISPLAY annunciator is blinking on and off.

NOTE

The blinking MEMORY DISPLAY annunciator reminds the operator that the front panel of the Receiver now displays the contents in memory of channel 24 instead of the operating set-up of the Receiver. The channel set-up may now be altered with any front panel controls without affecting receiver operation.

26. After desired channel set-up is accomplished, press STO pushbutton key-switch to store contents of channel 24.

27. Press and hold TUNING slew switch lever in the up or down position to step through channels 01 to 99.

28. When a channel number is reached with desired Receiver set-up, press EXEC pushbutton key-switch and observe that channel set-up is Receiver operating condition.

NOTE

Any number of the 99 channels may be programmed in the channel scan, however, only those numbers activated will be scanned. The scan will be up from one active number to the next with approximately a 20 millisecond delay on each active channel; however, if the signal level of any channel is above its pre-set threshold, the scanning will stop and hold on that channel until the signal drops below the threshold or the CLR pushbutton key-switch is pressed.

29. Select channel to be activated, then press CHAN SCAN pushbutton key-switch and observe that associated indicator illuminates for approximately 1 second and goes out to indicate instruction was received.

NOTE

If a channel is already activated, the CHAN SCAN indicator will illuminate when that channel is recalled.

30. To deactivate a channel, press CHAN SCAN pushbutton key-switch when associated LED indicator illuminates.

31. Press MEM pushbutton key-switch and observe that associated LED indicator goes out.

32. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator illuminates and that Receiver begins scanning active memory channels with approximately a 20 millisecond delay on each channel.

33. When scan stops on a channel pre-set threshold, press CLR pushbutton key-switch and observe that scan continues.

34. Press CHAN SCAN pushbutton key-switch a second time and observe that associated LED indicator goes out and Receiver is deactivated from channel scan mode.

NOTE

This concludes the typical local operating procedure, turn Receiver power off.

3-20. REMOTE CONTROL OPERATION - The Receiver may be operated from a remote controller/computer when fitted with the optional IEEE-488C remote control interface circuit card assembly (A7A9). This is accomplished by inputting command words into the remote controller/computer for both controlling the Receiver and requesting status data from the Receiver. Communication between the remote controller/computer and the Receiver is accomplished through a string of data words. Each word consists of a letter (including the function) and several numbers (identifying the value). Each string of data words must be prefixed with the Receiver identifying address for either the talker or listener function as defined by the IEEE-488C-1978 specifications, and then terminated with a line feed to indicate the end of a message. The Receiver may be set for remote control operation and the IEEE address switch assembly on the rear panel must be properly programmed. The remote controller/computer may override the REMOTE switch.

3-21. Command Words For Listener - When the remote controller/computer commands the Receiver to function as a listener, the command words as shown in Table 3-2 are used. A single command word may be sent or several commands may be formatted to form a string of words. For example, F100 CRLF (carriage return-line feed) will cause the Receiver to tune to 100 MHz without changing any other operating parameter. The command F200.567 D2 I17 CRLF will cause the Receiver to tune to 200.567 MHz in the FM mode with a 50 kHz IF bandpass filter. As indicated in the first example, no extraneous data, such as leading and trailing zeros, spaces or unnecessary decimal points, need be sent. If an invalid command is sent (for example, specifying an operating parameter that is not compatible with the selected mode), the command will be ignored. All commands (word or string of words) must be terminated with a line feed (LF) to indicate end of message.

Table 3-2. Command Words for Listener

RECEIVER FUNCTION	COMMAND LETTER(S)	COMMAND NUMBER	COMMAND WORD EXAMPLES
Frequency Set-up	F	Any number from 20 to 1000 (MHz) with decimal point if required.	F785.697 = 785.697 MHz
Detection Modes	D	1 = AM 2 = FM 3 = CW 0 4 = CW 1 kHz 5 = ISB (as applicable) 6 = LSB (as applicable) 7 = USB (as applicable)	D3 = CW detection mode with zero offset
IF Bandwidth	I	10 = 10 kHz 13 = 20 kHz 17 = 50 kHz 20 = 100 kHz/200 kHz/ 400 kHz	I17 = 50 kHz IF bandwidth
Gain Control Mode	M	1 = AGC FAST 3 = AGC SLOW 4 = MGC	M4 = Manual gain mode (see IF attenuation--A.
IF Attenuation	A	Any number between 0 and 255 (0 corresponds to maximum gain)	A125 = 50 dB of gain, approximately
Scan Mode	SM	From 0 to +9 and 0 to -9	SM5 = scan up at 100 kHz per second SM 7 = scan down at 10 MHz per second SM0 = stop scan but still in scan mode
Scan Kill	SK	None frequency set-up	SK = Removes the Receiver from scan mode
Scan Mode Start Frequency	FU	Same as for frequency set-up	FU28.5 = 28.5 MHz
Scan Mode Stop Frequency	FD	Same as for frequency set-up	FD680 = 680 MHz
AFC On	AF	1	AF1 = AFC on
AFC Off	AF	0	AF0 = AFC off
COR Threshold	CO	Any number between 0 and 255	C065 = COR threshold level (0 = minimum)

Table 3-2. Command Words for Listener

RECEIVER FUNCTION	COMMAND LETTER(S)	COMMAND NUMBER	COMMAND WORD EXAMPLES
Channel Store	C(N)S (Data string)	N=channel number from 01 to 99 Data string = receiver set-up for channel	C32SF125D1I13M2A100 AF0C0120 = Store channel 32 with receiver set-up as shown
Channel Recall	C(N)R or C(N)?	N=channel number from 01 to 99	C16R=Recall channel 16 C25?=Recall channel 25
Store Receiver Operating Set-up	C(N)SX	N=channel number from 01 to 99	C88SX = Store current Receiver operating set up into channel 88
Transfer Channel to Receiver Operation	C(N)X	N=channel number from 01 to 99	C45X = Transfer contents of channel 45 to Receiver operation
Activate Channels for Scanning	E(N);	N=channel number from 01 to 99	E14;20;25;50; = activate channels 14, 20, 25 and 50 for scanning
Deactivate Channels from Scanning	K(N);	N=channel number from 01 to 99	K15;21;26;51 = deactivate channels 15, 21, 26 and 51 from scanning
Deactivate Channels from Scanning	KX	None	Deactivates all channels from scanning
Execute Channel Scan	P	1	P1 = enables channel scan
Kill Channel Scan	P	0	P0 = disables channel scan
Store Exclude Frequency	FL (Freq.)S	Frequency to be excluded	FL251.673S = Exclude frequency of 251.673 MHz
Kill Exclude Frequency	FL(Freq.)K	Exclude frequency to be killed	FL125K = Kill exclude frequency of 125 MHz
Kill all Exclude Frequencies	FLX	None	FLX = Deactivate all exclude frequencies

Table 3-2. Command Words for Listener

RECEIVER FUNCTION	COMMAND LETTER(S)	COMMAND NUMBER	COMMAND WORD EXAMPLES
Receiver Local Control	S	0	S0 = Set Receiver for local control operating mode
Receiver Remote Control	S	1	S1 = Set Receiver for remote control operating mode
All Receivers out of DF mode	S	2	S2 = Remove all Receivers from DF mode
HF Receiver in DF mode	S	3	S3 = Place HF Receiver in DF mode
VHF/UHF Receiver	S	4	S4 = Place VHF/UHF Receiver in DF mode
Internal Reference	S	5	S5 = Select inernal reference frequency
External Reference	S	6	S6 = Select external reference frequency
Master/Slave Gain Bit Set	S	7	S7 = Set master/slave gain bit
Master/Slave Gain Bit Clear	S	8	S8 = Clear master/ slave gain bit

Table 3-3. Command Words for Talker

RECEIVER MONITOR FUNCTION	MONITOR COMMAND	EXAMPLES OF RECEIVER RESPONSE
All Receiver Functions	G?	F123.456780I13M1A120L1205120 AF1CO120T12SM-1FD12.34FU56.78 ACO-234;1-459-982IP10;13;17;20 CRLF
Frequency	F?	F328.46875 CRLF
Detection Mode	D?	D2 CRLF
IF Bandwidth	I?	I13 CRLF
Gain Control Mode	M?	M3 CRLF
Attenuation	A?	A120 CRLF
Scan Start Frequency	FU?	FU27.87654 CRLF
Scan Stop Frequency	FD?	FD385.64282 CRLF
AFC Status	AF?	AF1 CRLF
COR Level	CO?	CO90 CRLF
Channel Recall	C(N)?	C23(Receiver set-up string as indicated for G)E1
Channel Scan Active Status	E(N)?	C23E1 CRLF
Exclude Frequencies	FL?	FL(All frequencies in exclude library, in numerical order with each separated by a semicolon). This inquiry should be used alone because its response could be lengthy.
Receiver Signal Level	L?	L120 CRLF
IF Poll	IP?	IP10;113;1;7;20 CRLF
Test Status	T(N)	T63 CRLF

Table 3-3. Command Words for Talker

RECEIVER MONITOR FUNCTION	MONITOR COMMAND	EXAMPLES OF RECEIVER RESPONSE
Summary Error Indication	None, data sent at end of each monitor response	S1-S64 reprints seven error indications but are sent as a sum of seven bits as shown S1 = Receiver operating in remote control S2 = Synthesizer out-of-lock S4 = Receiver in DF mode S8 = Last command sequence had data error S16 = Master/slave gain bit S32 = Remote reference oscillator S64 = COR Example: If S59 is sent; subtract 32 from 59 = 17 subtract 16 from 17 = 1 then S1,S16 and S32 is status information

3-22. FAST SCAN CONTROL OPERATION - The fast scan operating mode requires a Spectrum Surveillance Controller to be connected to the FAST SCAN interface connector J15 on the rear panel of the Receiver. The Spectrum Surveillance Controller then directs control of the Receiver, blanking the front panel display, except for the FAST SCAN annunciator, and overriding the REMOTE control switch. For operating instructions in the FAST SCAN mode, refer to the Spectrum Surveillance Controller equipment manual provided by the manufacturer.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This section contains the theory of operation for the VHF/UHF Receiver, Type RG-5545A (Receiver). The theory is divided into three sections including functional capabilities, overall functional circuit operation, and detailed circuit description to best describe the Receiver functions. Functional capabilities provide an operator with an overview of the Receiver's control functions and operating parameters. The overall functional circuit operation provides a functional overview of primary circuit stage operation and signal flow within the Receiver at the major functional block diagram level. The detailed circuit description describes operation of the major functional circuits at the simplified schematic/logic level, in conjunction with an associated circuit block diagram to aid the technician/operator in understanding the various functions.

4-3. FUNCTIONAL CAPABILITIES

4-4. The Receiver is microcomputer controlled with reception capabilities between 20 and 1000 MHz and provides AM, FM and CW demodulation. Operation may be controlled from either the receiver front panel, a remote computer/controller, or from a Spectrum Surveillance Controller, Type RG-1342. Controllable functions include: detection mode (AM, FM, or CW); frequency tuning by keypad entry, tuning knob or slew switch in 10 Hz, 100 kHz and 1 MHz rates; four selectable IF bandwidths of 10, 20, 50 and 100 kHz; three selectable gain control modes of AGC FAST, AGC SLOW or MGC with adjustable threshold; a carrier operated relay (COR) with adjustable threshold and automatic frequency control (AFC); scan capabilities that include scan up or scan down over the Receiver frequency limits, with start and stop limits, with automatic stop on signals above a pre-set COR threshold; exclusion of frequencies for the automatic stop; and the ability to scan pre-selected channels stored in the channel memory with automatic stop on channel signals above a pre-set COR threshold. The channel memory can store up to 99 channels with a full operating parameter set-up in each channel. A level meter on the front panel provides a

dB readout for adjusting MGC threshold or the COR threshold whereas a tuning meter aids in tuning the Receiver to center frequency when not in the COR-AFC mode. An optional plug-in Spectrum Display Unit, Type RG-1320B, which forms an integral part of the Receiver front panel, will provide the operator with a visual display of signal activity at and around the Receiver tuned frequency.

4-5. OVERALL FUNCTIONAL CIRCUIT OPERATION

4-6. Figure 4-1 shows a functional block diagram of the Receiver. Control of all the Receiver operating functions is effected through microcomputer based control circuits contained on the front panel (A2) and receiver control (A7) assemblies. This receiver control operates diode switches in the tuner assembly (A3) for different frequency bands, tunes the first LO in 10 Hz increments for frequency tuning, selects one of three outputs of the second LO for different frequency bands, controls various circuits in the IF assembly (A6) and audio video amplifier/COR assembly (A9) for IF bandwidths, detection modes, gain modes, COR and AFC, and controls memory for scan, exclude frequency library and channel memory. Selection of an external reference and detection of a lock or unlocked condition with the internal reference is also effected by receiver control.

4-7. The tuner assembly translates the 20 to 1000 MHz RF signals, received from an external RF antenna, to a 21.4 MHz IF signal. This is accomplished by separately mixing the RF signal from the antenna with two different local oscillators in three frequency bands. In the first band, the first LO tracks 20 to 500 MHz with 681.4 to 1161.4 MHz, to provide a 661.4 MHz IF, which is then mixed with 640 MHz from the second LO to produce the 21.4 MHz IF. In the second band, the first LO tracks 500 to 840 MHz with 841.4 to 1181.4 MHz, to provide a 341.4 MHz IF, which is then mixed with 320 MHz from the second LO to produce the 21.4 MHz IF. In the third band, the first LO tracks 840 to 1000 MHz with 1021.4 to 1181.4 MHz, to provide a 181.4 MHz IF, which is then mixed with 160 MHz from the second LO to produce the 21.4 MHz IF. In all frequency bands, Receiver control provides selection of the associated bands, pre-select filtering for the RF input, and bandpass filtering for the IF frequencies.

4-8. The 21.4 MHZ IF signal is further processed through the IF assembly (A6), which provides three primary functions; bandwidth control and selection, manual

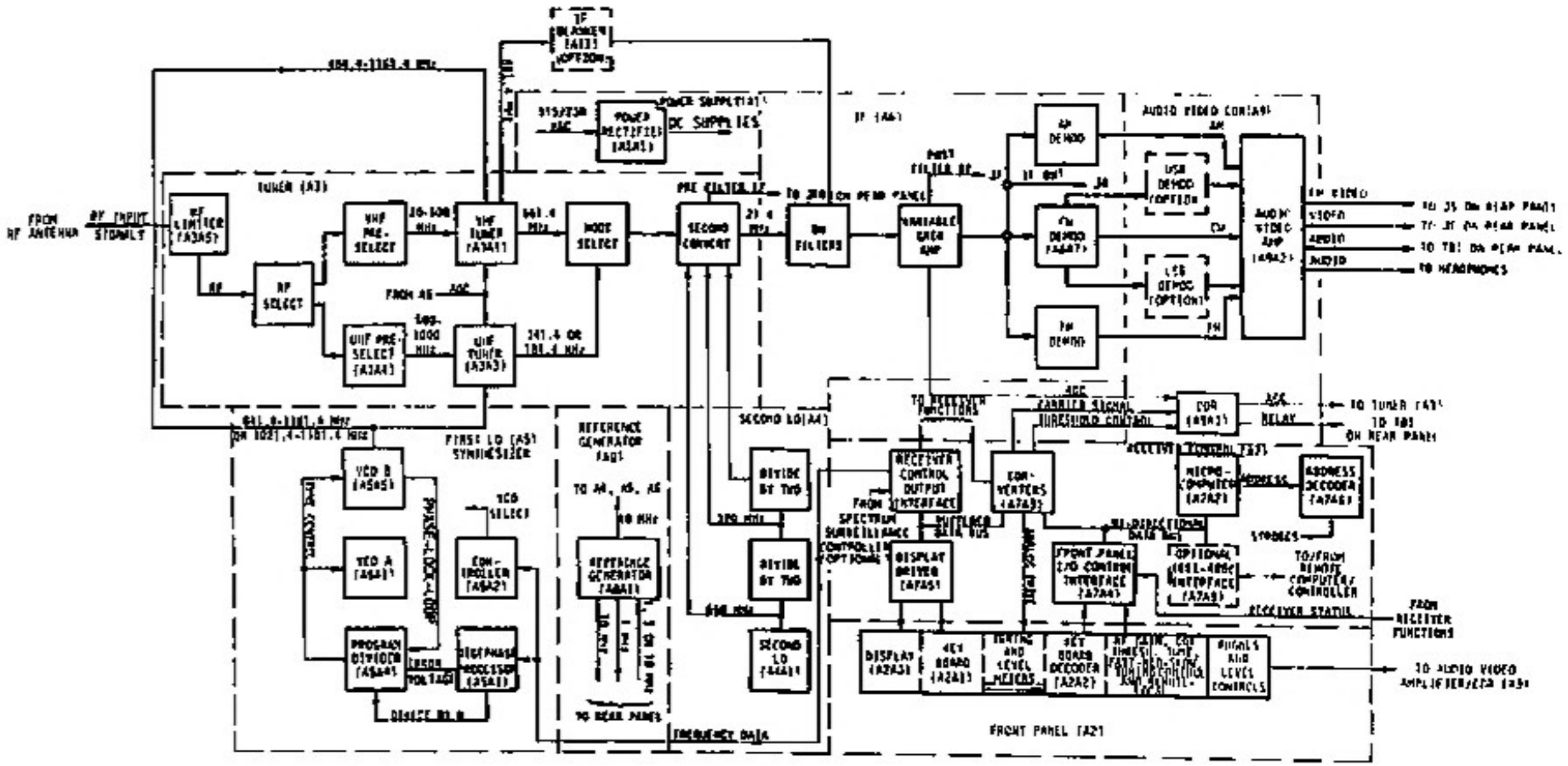


Figure 4-1. Receiver Overall Functional Block Diagram

or automatic gain control, and demodulation. The IF signal is first routed to one of four selectable IF bandwidth filters; 10, 20, 50 and 100 kHz (contained on four separate circuit cards), which are selected through receiver control. This bandwidth controlled signal is then provided gain control, either manual or automatic, which is selectable and microcomputer controlled. The gain controlled signal is then routed to three separate demodulators (AM, FM and CW). The AM and FM demodulators each consist of four demodulators, designed for the specific bandwidth of 10, 20, 50 or 100 kHz. These demodulators are contained on their respective bandwidth IF filter amplifier circuit card assemblies (A6A3-A6A6) and are automatically selected through front panel control. The CW signal is produced either with zero offset or with 1 kHz offset, selectable through receiver control.

4-9. The outputs of all three demodulators are routed to an audio video amplifier/COR assembly (A9) with separate amplifiers for FM video, video, audio 1, audio 2, headphones tip and headphones ring. The demodulated signals are selected and switched to the various amplifiers through receiver control, then routed either to the headphones jack on the front panel, or to connectors on the rear panel of the Receiver with level controls for the various functions.

4-10. The carrier operated relay (COR) circuits are also contained within the audio video amplifier/COR assembly. These circuits receive the RF gain signal from the variable gain amplifier circuit card assembly (A6A2), compare it with a threshold signal from receiver control, then provide the drive for a relay coil. A delay circuit keeps the relay coil energized for approximately 0.5 seconds when the signal drops below the pre-set threshold.

4-11. A reference generator module assembly (A8) provides an accurate 10 MHz reference frequency to various receiver circuits. The 10 MHz reference signal is generated by an internal oven-temperature controlled, crystal oscillator which may be further stabilized by an external reference of either 1, 5, or 10 MHz applied to a phase-lock-loop within the internal oscillator. The 10 MHz reference and a derivative of 1 MHz is output to the rear panel of the Receiver for external use.

4-12. The first LO synthesizer module assembly (A5) supplies the first LO input to the tuner assembly (A3), for translating the 20 to 1000 MHz RF signals to three different first IF signals of 661.4 MHz (20 to 500 MHz), 341.4 MHz (500 to 840 MHz) and 181.4 MHz (840-1000 MHz). The first LO synthesizer, comprising five sub-modules/circuit card assemblies , makes use of six separate VCOs (voltage controlled oscillators), which are controlled by a frequency control word from receiver control. This digital word is derived by receiver control which receives instructions through frequency selection at the front panel or from a remote controller/computer. In the first frequency band (20-500 MHz), the first LO synthesizer frequency output is the tuned frequency (F) + 661.4 MHz. In the second frequency band (500-840 MHz), the output is F + 341.4 MHz, while in the third frequency band (840-1000 MHz), the output is F + 181.4 MHz. Each of the six VCOs operates in a particular band of frequencies with the appropriate oscillator selected through receiver control. A phase-lock-loop, referenced from the 10 MHz reference generator oscillator, provides frequency stability. The output of the synthesizer is also routed to the rear panel of the Receiver for external monitoring or as required.

4-13. The second LO module assembly (A4) supplies frequency outputs to the tuner assembly (A3) second converter stage for translating the three first IF signals to a single second IF of 21.4 MHz. To accomplish this function, the second LO outputs three frequencies that are 21.4 MHz below each of the three first IF frequencies. Receiver control selects the appropriate second LO frequency at the same time it selects the frequency bands for implementing first conversion. The second LO produces three frequency outputs from a VCO and two divide-by-two circuits. The direct output of the VCO provides the 640 MHz for the first frequency band (681.4 MHz), then is divided-by-two, to produce the 320 MHz for the second frequency band (341.4 MHz), and further divided-by-two, to produce the 160 MHz for the third frequency band (181.4 MHz). In all three frequency bands, the 21.4 MHz second IF is produced for output from the second converter stage. The basic oscillator is stabilized through a phase-lock-loop referenced to the 10 MHz reference generator oscillator. The output of the second LO is also routed to the rear panel for external monitoring or as required.

4-14. Receiver control comprising the front panel assembly (A2) and the receiver control assembly (A7), controls Receiver operation through a

microcomputer (A7A2) which evaluates input instructions, then sends control instructions to the appropriate Receiver circuits. In the local control mode of operation, instructions are entered at the front panel and routed to the microcomputer, through a front panel I/O interface (A7A4), which then routes control signals to change Receiver operation as instructed. At the same time, instructions are routed through a display driver (A7A5) to update the front panel readouts and keypad LEDs. In the remote control mode, a remote computer/controller is interfaced to the microcomputer through an IEEE-488C remote control interface (A7A9) which can request Receiver status information in either the remote or local operating modes. In the optional fast scan mode, the Spectrum Surveillance Controller controls Receiver operation, directing the microcomputer into a standby state. Program sequence is controlled through microcomputer addresses, read and write signals, and from strobes generated by an address decoder (A7A6). Receiver operation is controlled through both a converter (A7A8) and a receiver control output interface (A7A1). Most of the microcomputer RAM memory is used for the exclude frequency library and the channel memory functions. Up to 300 frequencies may be stored in the exclude frequency library, where as up to 99 channels, with full Receiver operating parameter set-up, may be stored in channel memory.

4-15. The Receiver power supply may be operated from either 115 or 230 volts ac, which is card selectable from the rear panel. The power supply provides both regulated and unregulated dc voltages to various receiver circuits. The Receiver cooling fan blower operates from a secondary winding of the power transformer, contained in the power supply, which supplies the blower motor with 115 volts ac when using either a 115 or 230 volt ac power source.

4-16. DETAILED CIRCUIT DESCRIPTION

4-17. The detailed circuit description is divided into eight circuit divisions to best describe the Receiver's circuits. The circuit divisions and reference designator for each division are listed below in the order that they are described.

CIRCUIT DIVISION	REF DESIG.	PARAGRAPH
Tuner Assembly	A3	4-17
IF Assembly	A6	4-28
Audio Video Amplifier/ COR Assembly	A9	4-40
Reference Generator Module Assembly	A8	4-45
First LO Synthesizer Module Assembly	A5	4-47
Second LO Module Assembly	A4	4-60
Receiver Control	A2 and A7	4-63
Power Supply Module Assembly	A1	4-83

4-18. TUNER ASSEMBLY (A3). The tuner assembly translates the 20-1000 MHz RF input, from an external RF antenna, to a 21.4 MHz IF signal by mixing it with frequencies from the first LO synthesizer (A5) and second LO (A6). Figure 4-2 shows a functional block diagram of the tuner assembly. The tuner assembly consists of an RF limiter (A3A5), a VHF (20-500 MHz) preselector (A3A2), VHF tuner (A3A1), UHF (500-1000 MHz) preselector (A3A4), and UHF tuner (A3A3). After RF limiting and preselect filtering, the VHF tuner translates the 20 to 500 MHz RF input signals to a 661.4 MHz IF, by mixing with the first LO frequency which ranges from 681.4 MHz (20 MHz) to 1161.4 MHz (500 MHz). The difference frequency of 661.4 MHz is then routed through an amplifier, filter, and a select switch to a second mixer. In this frequency band, the second LO adds 640 MHz to the mixer to produce the 21.4 MHz IF. The 500 to 840 MHz input is switched through the UHF preselector to the UHF tuner, where it is translated to 341.4 MHz by mixing it with a 841.4 MHz (500 MHz) to 1181.4 MHz (840 MHz) from the first LO. This 341.4 MHz IF is then switched through to the second mixer in the VHF tuner. In this frequency band, the second LO adds 320 MHz to the mixer to produce the 21.4 MHz IF. The 840 to 1000 MHz input is also switched through the UHF preselector to the UHF tuner where it is translated to 181.4 MHZ by mixing with 1021.4 MHz (840 MHz) to 1181.4 MHz (1000 MHz) from the first LO. This 181.4 MHz is routed to the second mixer in the VHF tuner where it is mixed with 160 MHz from the second LO to produce the 21.4 MHz IF. The selecting and routing of the various frequencies through their appropriate circuits is

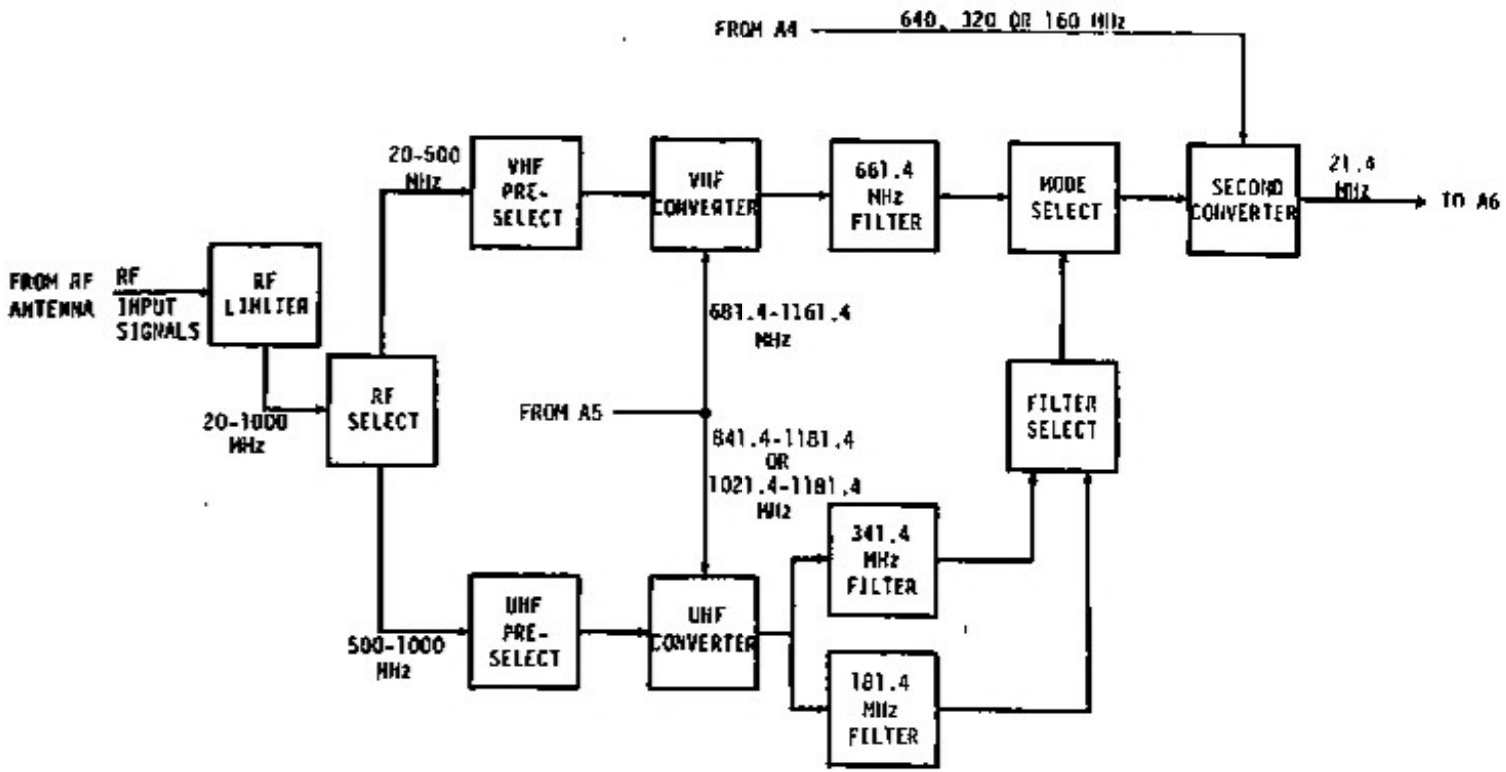


Figure 4-2. Tuner Assembly (A3) Functional Block Diagram

accomplished through diode switches that are controlled from decoder circuits in the tuner assembly. The decoders receive their instructions from the microcomputer (A7A2) which then controls the switches for selecting and routing the various signals.

4-19. RF Limiter (A3A5). The RF limiter provides protection to the tuner assembly (A3) by limiting the RF input from the antenna or other sources. The RF limiter is designed to receive RF signals up to 10 volts rms (2 watts), with its output basically limited to +17 dBm (50 milliwatts), however, limiting actually begins with a +13 dBm input with a 1 dB insertion loss up to the +18 dBm level. The +17 dBm output will then remain constant over the +18 dBm to 10 volts rms range. The RF limiter is connected to the ANTENNA input connector J1. This unit is sealed and should be returned to the factory for any needed repairs.

4-20. VHF (20-500 MHz) Preselector (A3A2). The VHF preselector provides band filtering for the 20 to 500 MHz RF input from the antenna. This filtering is provided for eight different bands, in the 20-500 MHz range, with a separate set of filters for each band. Figure 4-3 shows a functional block diagram of the VHF preselector and decoder driver, in addition to the frequency range of each band of filters. The preselector decoder driver provides for selecting the appropriate filter for the band that the Receiver is tuned to. Figure 7-8A shows the schematic diagram of the VHF (20-500 MHz) preselector. The RF signal input is routed to a group of eighteen diode switches which are paired and coupled to a set of filters (band 9 is the 20-500 MHz range and is unfiltered) with the same diode switch arrangement on the output of the filters. Each set of filters is designed to reject all frequencies outside the respective band. A particular filter is selected when a select signal from the decoder driver goes low (from positive to negative), reversing the bias on the pair of diodes on each end of the filter, allowing the RF to pass through. For instance, when the Receiver is tuned to 25 MHz, band 1 is enabled, which biases the four diodes (CR33-CR36) in a reverse manner (from positive to negative), and the RF signal passes through the 20-28 MHz filter. This filtered RF is then routed to the VHF tuner (A3A1).

4-21. Figure 7-9 shows the associated decoder driver schematic diagram. The decoder driver receives data from the microcomputer, decodes it and provides the select signals and drive for band select. The frequency information from receiver control is routed to two decoders U8 and U9. Decoder U8 provides the

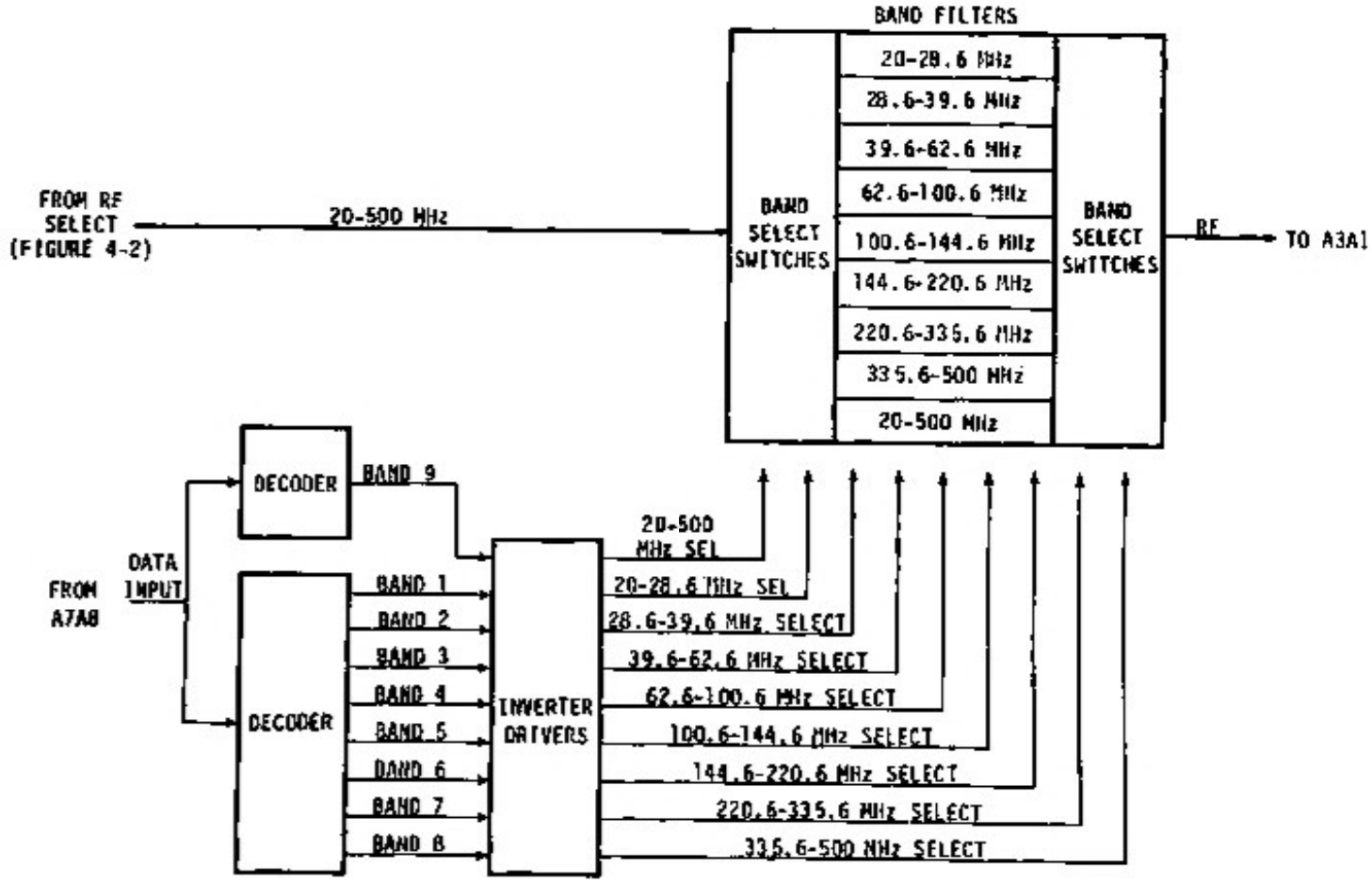


Figure 4-3. VHF (20-500 MHz) Preselector and Decoder Driver (A3A2) Functional Block Diagram

eight select outputs for the eight bands of frequencies in the 20 to 500 MHz range. These select signals are routed through inverters (U6A-U6F and U7A-U7B) to driver amplifiers (U2A and B to U4A and B). Decoder U9 provides the select signal for band 9 (20-500 MHz range) through inverter U7C and driver amplifier U5A.

4-22. VHF Tuner (A3A1). The VHF tuner converts the 20-500 MHz RF signal to a 661.4 MHz IF signal and then converts either the 661.4 MHz signal, 341.4 MHz, or 181.4 MHz signals from the UHF tuner to a 21.4 MHz second IF signal. Figure 4-4 shows a functional block diagram of the VHF tuner. The RF signal from the VHF preselector (A3A2) is coupled through RF amplifiers, an attenuator, and a low pass filter to the first mixer. The first LO output is also coupled to this mixer and tracks the 20-500 MHz input with 681.4 to 1161.4 MHz. The difference output of 661.4 MHz is routed through a first IF amplifier and bandpass filter, to a select switch, that is controlled from the decoder driver on the UHF tuner (A3A3). In the 20-500 MHz frequency band, this switch selects the 661.4 MHz signal and routes it to the second mixer. In the other two frequency bands (500-840 MHz and 840-1000 MHz), the switch selects the output of the UHF tuner (either 341.4 or 181.4 MHz). The second LO is also input to the second mixer and provides 640 MHz when the 661.4 MHz is selected, 320 MHz when the 341.4 MHz is selected, and 160 MHz when the 181.4 MHz is selected. In all three frequency bands, a 21.4 MHz difference is produced by the mixer and routed through buffer amplifiers and a filter to a two-way power divider. This power divider provides the two outputs of the tuner assembly which are then routed to the IF module assembly (A6) and to the rear panel PRE FIL IF connector J10.

4-23. Figure 7-7A shows the schematic diagram of the VHF tuner. The 20-500 MHz RF from the VHF preselector is routed through RF amplifier U15, to variable attenuator U14, which is controlled by the AGC signal. The AGC signal, from AGC control of the IF assembly (A6), is applied to an attenuator through amplifiers U10A, U10B and U10C, and a linearizing circuit consisting of diodes CR5, CR5 and CR7. The AGC controlled signal from attenuator U14 is coupled through buffer amplifier U13 to a low pass filter (C24-C29, L12-L16 and R45-R47). This filter, with trimmer capacitors, is designed for image and IF rejection into the first mixer. The second input to this mixer is the first LO frequency (681.4-1161.4 MHz) and is routed from the first LO synthesizer module assembly (A5) through buffer amplifiers U9 and U8. The 661.4 MHz difference from the first mixer is routed through IF amplifier U7 and a 661.4 MHz bandpass filter

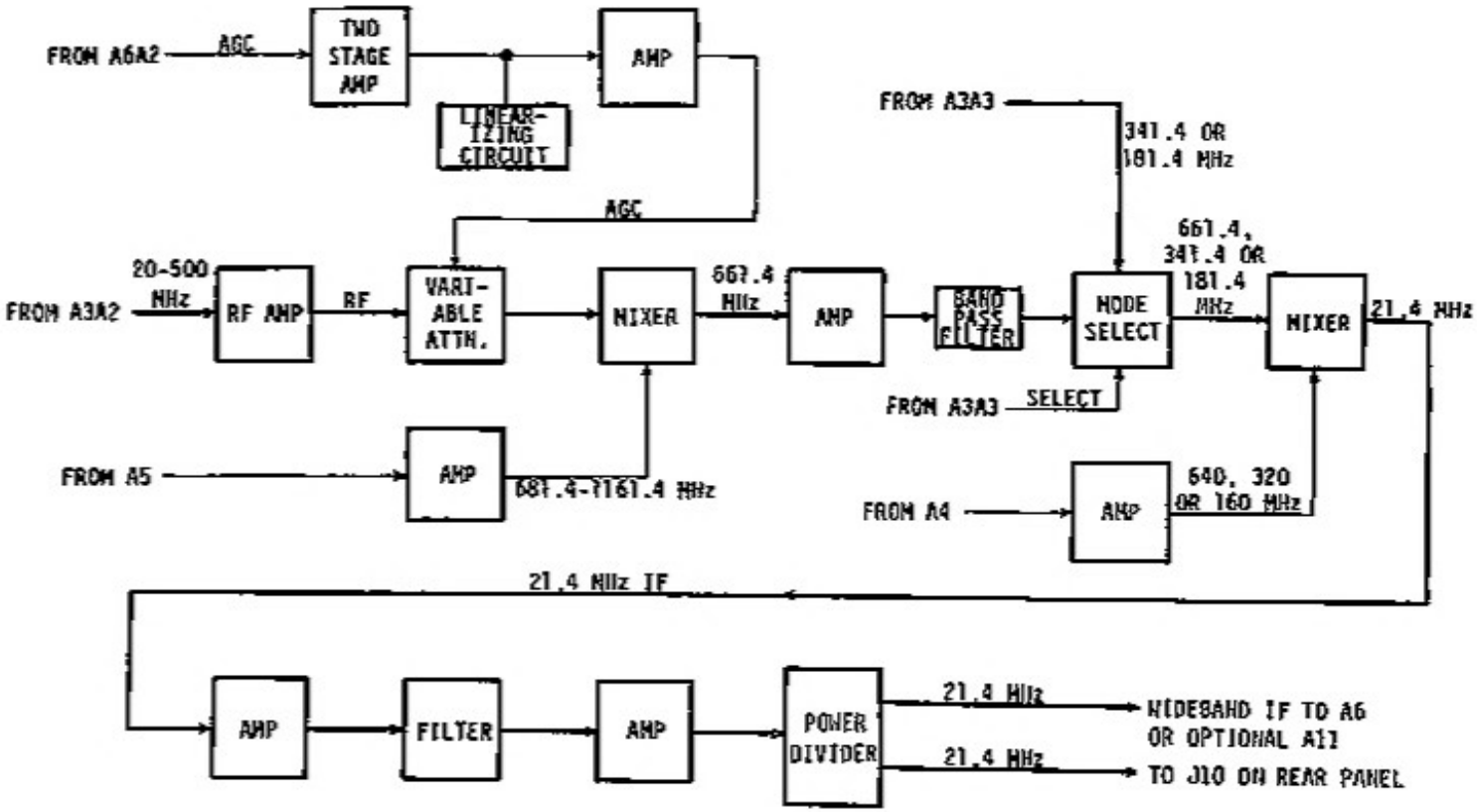


Figure 4-4. VHF Tuner (A3A1) Functional Block Diagram

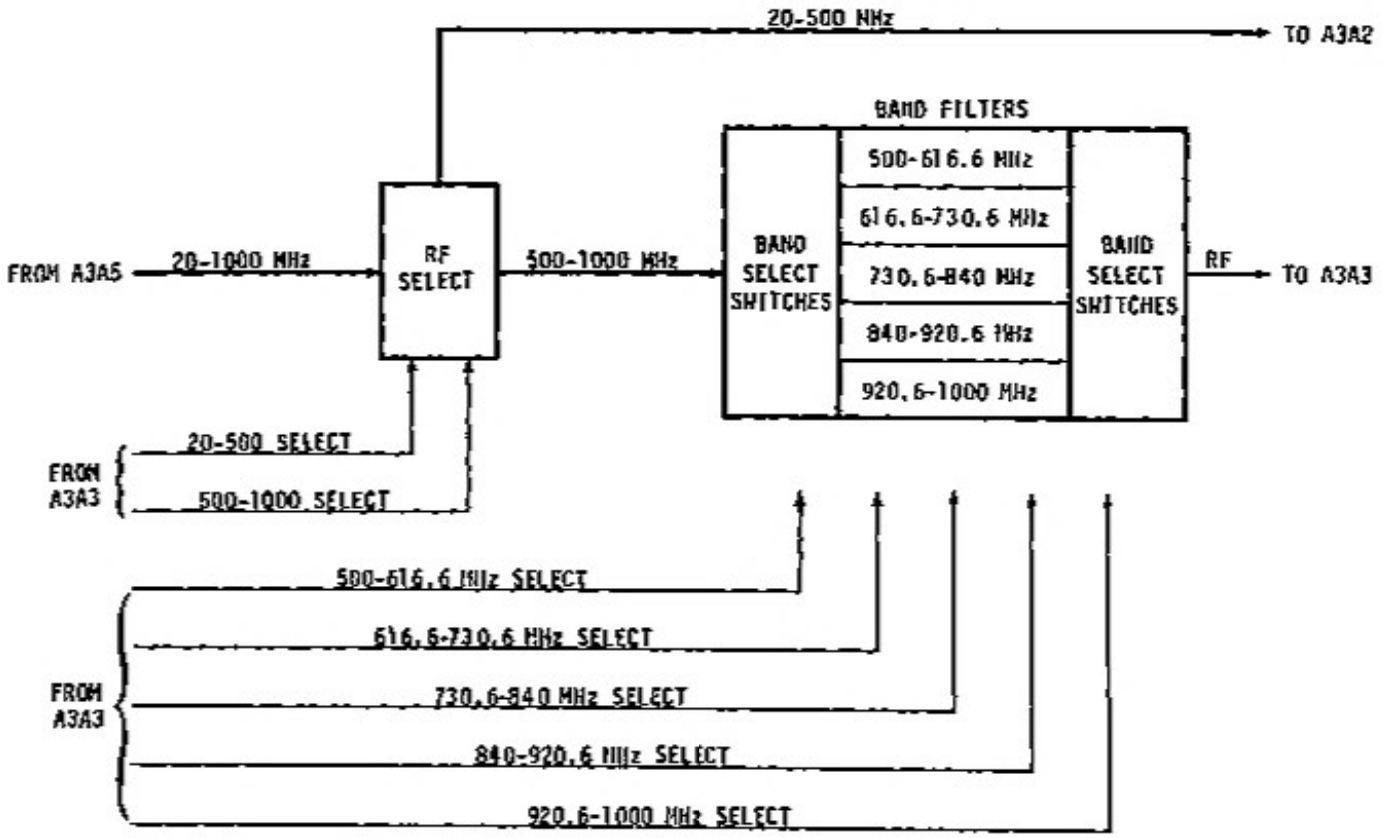


Figure 4-5. UHF (500-1000 MHz) Preselector (A3A4) Functional Block Diagram

4-26. UHF Tuner (A3A3). The UHF tuner converts the 500-1000 MHz RF input, from the UHF (500-1000 MHz) preselector (A3A4), to either 341.4 MHz (500-840 MHz) or 181.4 MHz (840-1000 MHz). Figure 4-6 shows a functional block diagram of the UHF tuner and associated decoder driver that controls the diode switches contained in the tuner and preselector. The RF input from the preselector is routed through RF amplifiers, an attenuator, a filter and diode switch to the mixer. The first LO output is also connected to this mixer and tracks the 500-840 MHz input with 841.4 to 1181.4 MHz. These two separate tracks produce the 341.4 MHz and 181.4 MHz IF from the mixer. Each of these frequencies are routed through their respective bandpass filters, selected in the associated frequency band, to the VHF tuner. The decoder driver decodes frequency instructions from receiver control and provides select signals to the various diode switches in the UHF tuner and UHF preselector for the respective frequency band.

4-27. Figure 7-10A shows the schematic diagram for the UHF tuner. The RF signal from the preselector is routed through RF amplifier U1 to attenuator U2. This attenuator is controlled from the AGC linearizing circuit on the UHF decoder driver which provides gain control to the RF signal. The output of the attenuator is routed through a series of filters and a diode switch to the mixer. Coils L1-L3, in conjunction with trimmer capacitors C2-C5, provide image rejection into the mixer; coil L4 and trimmer capacitor C6 act as a 181.4 MHz trap, while coil L5 and trimmer capacitor C7 act as a 341.4 MHz trap. Diode switches CR1-CR2, controlled by a select line from the decoder driver, passes the RF signal to the mixer. Diode switches CR3-CR4 are used for extended frequency range and are not used in this application. The second input to the mixer is the first LO frequency routed from the first LO synthesizer (A5) through buffer amplifiers U5 and U6. In the 500-840 MHz frequency band, the first LO input is from 841.4 to I181.4 MHz, and produces a 341.4 MHz difference from the mixer. In the 840-1000 MHz band, the first LO input is from 1021.4 to 1181.4 MHz, and produces a 181.4 MHz difference from the mixer. The output of the mixer is routed to two bandpass filters, each selectable through diode switches controlled from the decoder driver. In the 500-840 MHz band, the 341.4 MHz filter is selected through diodes CR7, CR8, CR11 and CR12. In the 840-1000 MHz band, the I81.4 MHz filter is selected through diodes CR5, CR6, CR9 and CR10. The output of the selected filter is then routed to the VHF tuner (A3A1) for second conversion of the signal.

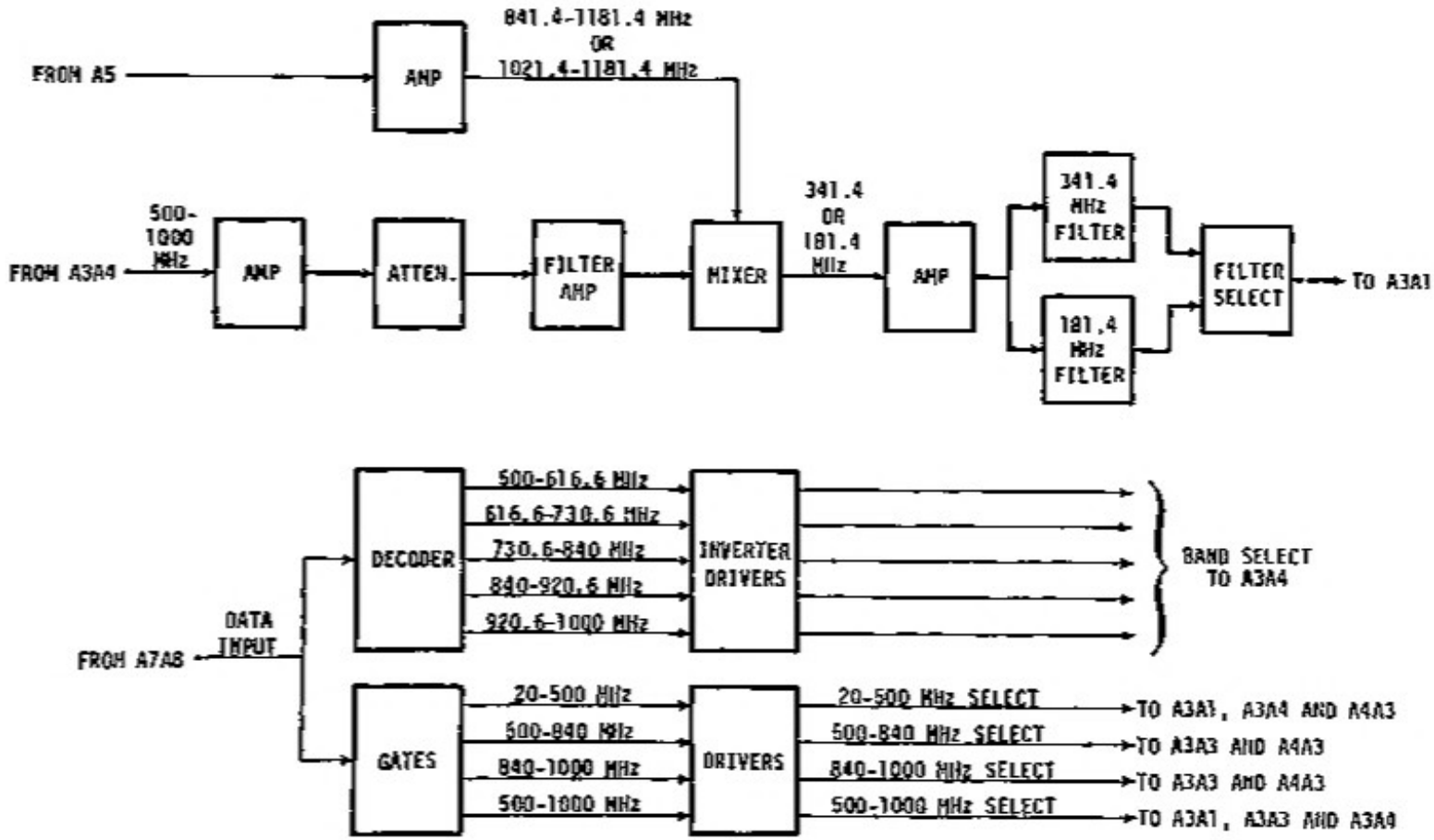


Figure 4-6. UHF Tuner and Decoder Driver (A3A3) Functional Block Diagram

4-28. Figure 7-11 shows a schematic diagram of the associated decoder driver. Frequency data input from receiver control is routed to a decoder on data input lines A-E. The five outputs of the decoder are inverted through inverters U2A to U2E and routed to drive amplifiers U6A, U6B, U7A, U7B and U18A. The output of these five amplifiers then selects the filters in the UHF preselector (A3A4) for the proper frequency range within 500-1000 MHz. Data input, from receiver control, on data input lines x, y and z, are gated to provide selection for three frequency bands; either 20-500 MHz, 500-840 MHz, or 840-1000 MHz. Data on line y and z is combined through NAND gate U9A and AND gate U14C and routed through amplifier U18B to provide select signals to the second LO and the 181.4 MHz bandpass filter in the 840-1000 MHz band. Data on line x and z is combined through NAND gate U9B and AND gate U14B and routed through amplifier U17B to provide a select signal to the second LO in the 500 to 840 MHz band. The outputs of U14B and U14C, are combined through NOR gate U1A and routed through amplifier U5A, to provide a select signal to the second LO in the 20-500 MHz band. Data line y and the output of U14B, are combined through exclusive OR gate U3C and routed through amplifier U5B, to provide select signals for routing the RF signals to and from the UHF (500-1000 MHz) preselector in the 500 to 1000 MHz band. The outputs of U14A and U14B, are combined through exclusive OR gate U3A, whose output is further combined with the output of U14C through exclusive OR gate U3B, and routed through amplifier U15A, to provide a select signal that selects the UHF tuner output for the second mixer of the VHF tuner (A3A1) in the 500-1000 MHz band. The outputs of U3C and U9C, are combined through exclusive OR gate U3D, inverted by U9D, and then routed through amplifier U15B to provide select signals for the extended frequency range, unused in this application. The output from U3B is inverted by U9C and routed through amplifier U16A to provide select signals for routing the RF input to the VHF (20-500 MHz) preselector (A3A2) and selecting the 661.4 MHz IF in the 20-500 MHz band. Data line z and the output of U3C, are combined through AND gate U14D and routed through amplifier U16B, to provide select signals for the 341.4 MHz filter in the 500-840 MHz band. The 20-500 MHz select output of U9C is also routed to two sets of transistor switches, which control power input to the VHF tuner for this frequency band. Transistors Q6 and Q8 switch the +5 volts, while transistors Q5 and Q7 switch the +15 volts. The 500-1000 MHz select output of U3C also controls transistor switches for controlling power to the UHF tuner (A3A3). Transistors Q2 and Q4 control the +5 volts, while Q1 and Q3 control the +15 volts.

4-29. IF ASSEMBLY (A6). Figure 4-7 shows an overall functional block diagram of the signal flow through the associated circuits. The IF assembly contains six sub-assemblies/modules (A6A2-A6A6, A6A8) with plug-in slots available for an optional upper (USB) and lower (LSB) sideband demodulators (A6A7 and A6A9 respectively). These six assemblies provide for IF bandwidth selection, automatic or manual gain control, AM and FM demodulation, and CW demodulation. Assemblies A6A3 through A6A6 are identical except for the bandwidth filter and frequency dependent components in the AM and FM demodulators. The bandwidth filter is selected through receiver control which selects the appropriate IF filter amplifier (A6A3-A6A6) for the bandwidth selected.

4-30. IF Filter Amplifiers (A6A3-A6A6). Figure 4-8 shows a functional block diagram of one of the IF filter amplifiers. These IF filter amplifiers accommodate the four selectable IF bandwidths of the Receiver and the bandwidth sensitive AM and FM demodulators. Each contains one of the four selectable bandwidth filters and an associated AM and FM demodulator (A6A3-100 kHz, A6A4-50 kHz, A6A5-20 kHz and A6A6-10 kHz). During actuation, three of the IF filter amplifiers will be kept isolated from signal flow while the appropriate one is switched into the signal flow as directed by the bandwidth selected through receiver control. This is accomplished through the diode switching logic contained on each IF filter amplifier.

4-31. Figure 7-22 shows a schematic diagram of an IF filter amplifier. The 21.4 MHz signal from the tuner assembly (A3) is coupled to the bandwidth filter circuits on each of the four IF filter amplifiers. The filters on all four IF filter amplifiers are isolated from the IF signal by diode switches CR1-CR2, while the output of the filter is isolated by diode switches CR3-CR4. The diode switches of only one IF filter amplifier will be biased on as directed by receiver control, allowing the signal to flow through the bandwidth filter selected. This bandwidth controlled signal is then routed to the variable gain amplifier (A6A2).

4-32. The gain controlled IF signal from the variable gain amplifier is routed back to all four IF filter amplifiers. The AM and FM demodulators (on all four IF filter amplifiers) are isolated from the IF signal by diode switches CR1-CR2. The diode switch (located on the same amplifier as the selected bandwidth filter) will be biased on, connecting the signal to the appropriate AM and FM

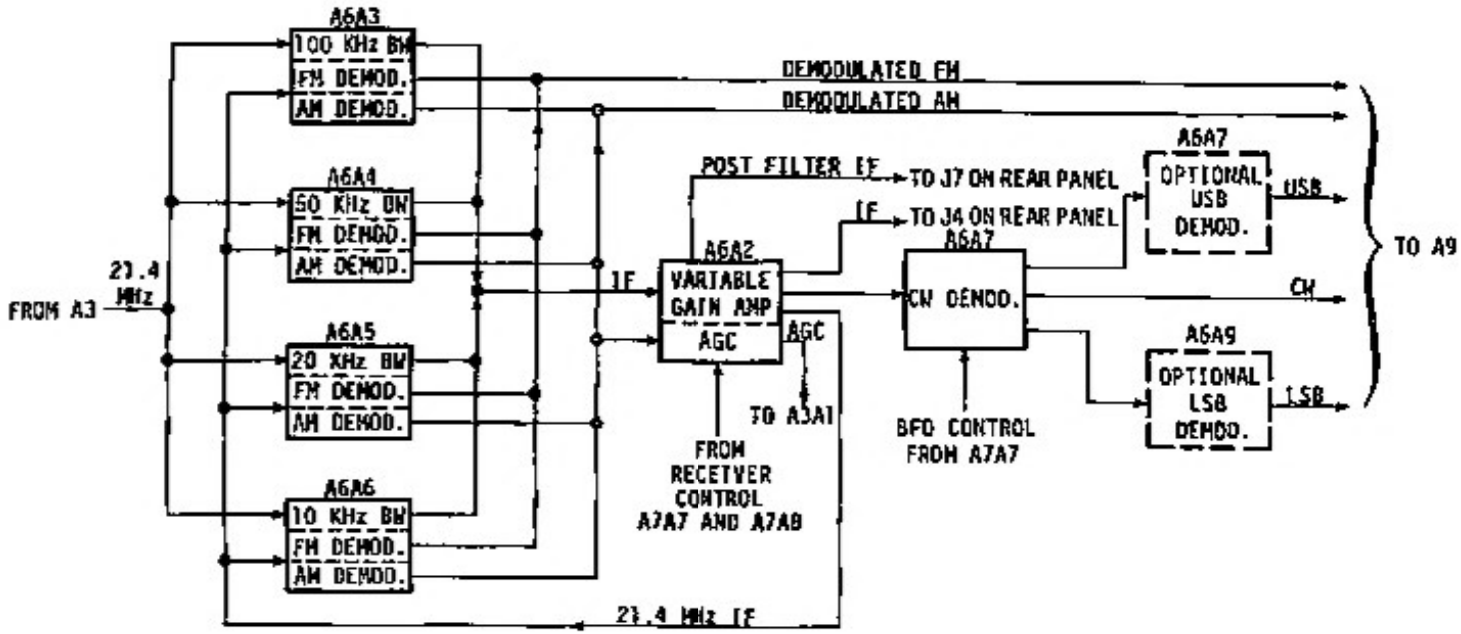


Figure 4-7. IF Assembly (A6) Functional Block Diagram

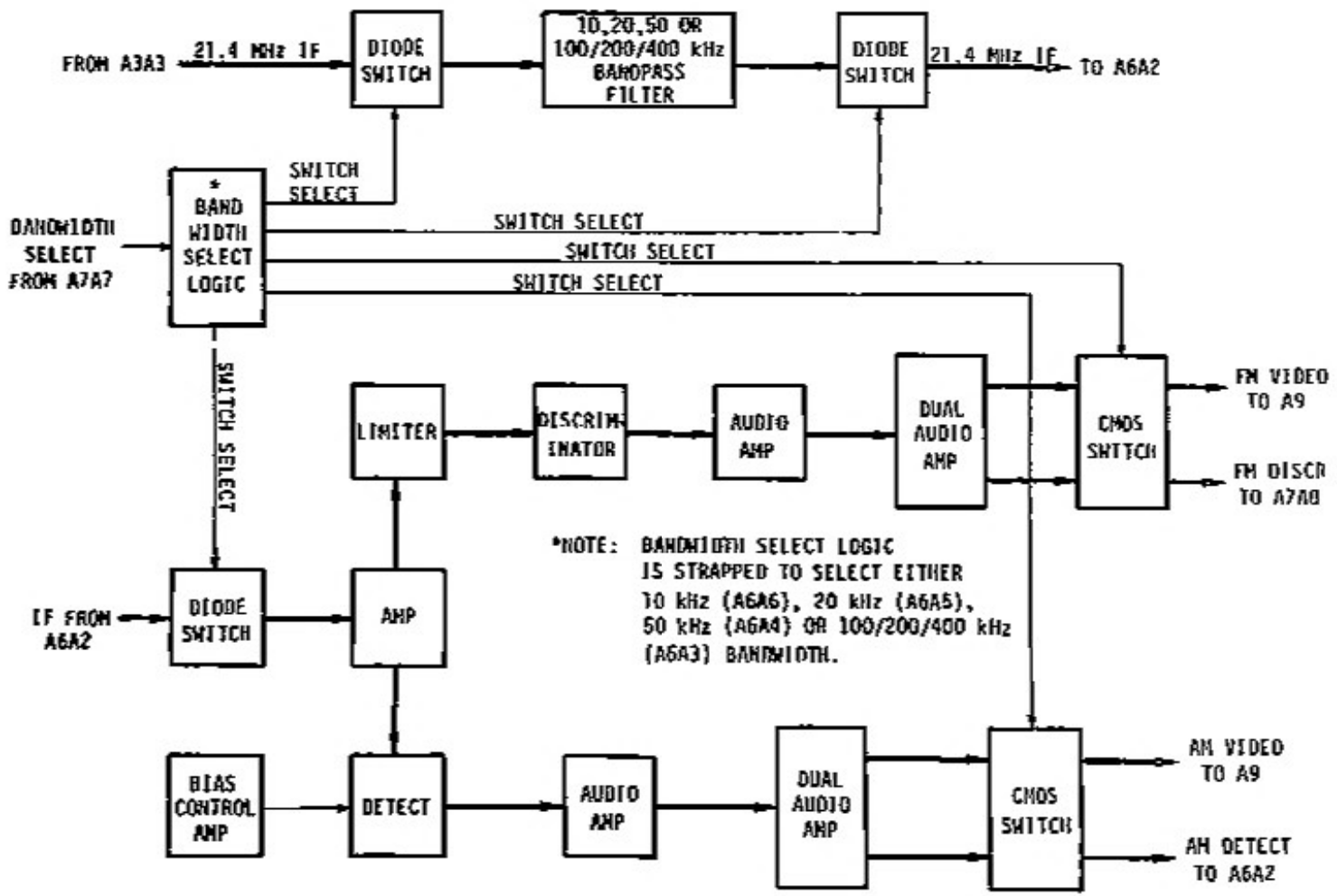


Figure 4-8. IF Filter Amplifier (A6A3-A6A6) Functional Block Diagram

demodulators. Power to the AM detector bias control and to the FM limiter will be turned on by transistor switch Q1. The switched IF signal is coupled to amplifier Q1 which divides the signal and routes it to both the AM detector and FM limiter/discriminator.

4-33. The AM component of a signal is detected by a detector circuit, consisting of diodes CR3-CR7, whose bias is controlled through bias control amplifier U1A. The detected AM is then routed through audio amplifiers U1B, U2A, U2C, and U2D to a CMOS switch U3. This switch, inhibited by the same select signal as for bandwidth, couples the signal to the audio video amplifier/COR assembly (A9), as the AM video, and to the variable gain amplifier (A6A2) for AGC drive.

4-34. Demodulation of an FM component of a signal is accomplished by passing the signal first through a separate limiter, then a discriminator. The audio output of the discriminator is then amplified through U8B, U8A, and U8D and routed to CMOS switch U4. This switch is inhibited in the same manner as the other select switches and routes the signal to the audio video amplifier/COR assembly (A9), as the FM video, and to the receiver control assembly (A7) for receiver control.

4-35. The IF select signal selects diode and CMOS switches that control the signal into and out of the four IF filter amplifiers (A6A3-A6A6). Each select signal is connected separately from receiver control which routes a select signal to only the amplifier corresponding to the bandwidth selected. This IF select signal is level controlled through level translators U5C, U5E and U5F, and is then routed to drive amplifiers U6A-U6D. The output of U6A and U6D controls the diode switch which controls the signal to the AM and FM demodulators. The output of U6B drives transistor switch Q1, which controls a voltage regulator supplying voltage to the AM bias control amplifier and to the FM limiter. Level translators U5A and U5B control the CMOS switches which control the output of the AM and FM demodulated signal. The IF select signal is also routed to a diode arrangement (arranged differently on each IF filter amplifier), which forms a code for receiver control. This code tells receiver control which bandwidth has been selected.

4-36. Variable Gain Amplifier (A6A2). Figure 4-9 shows a functional block diagram of the variable gain amplifier. This amplifier provides manual or

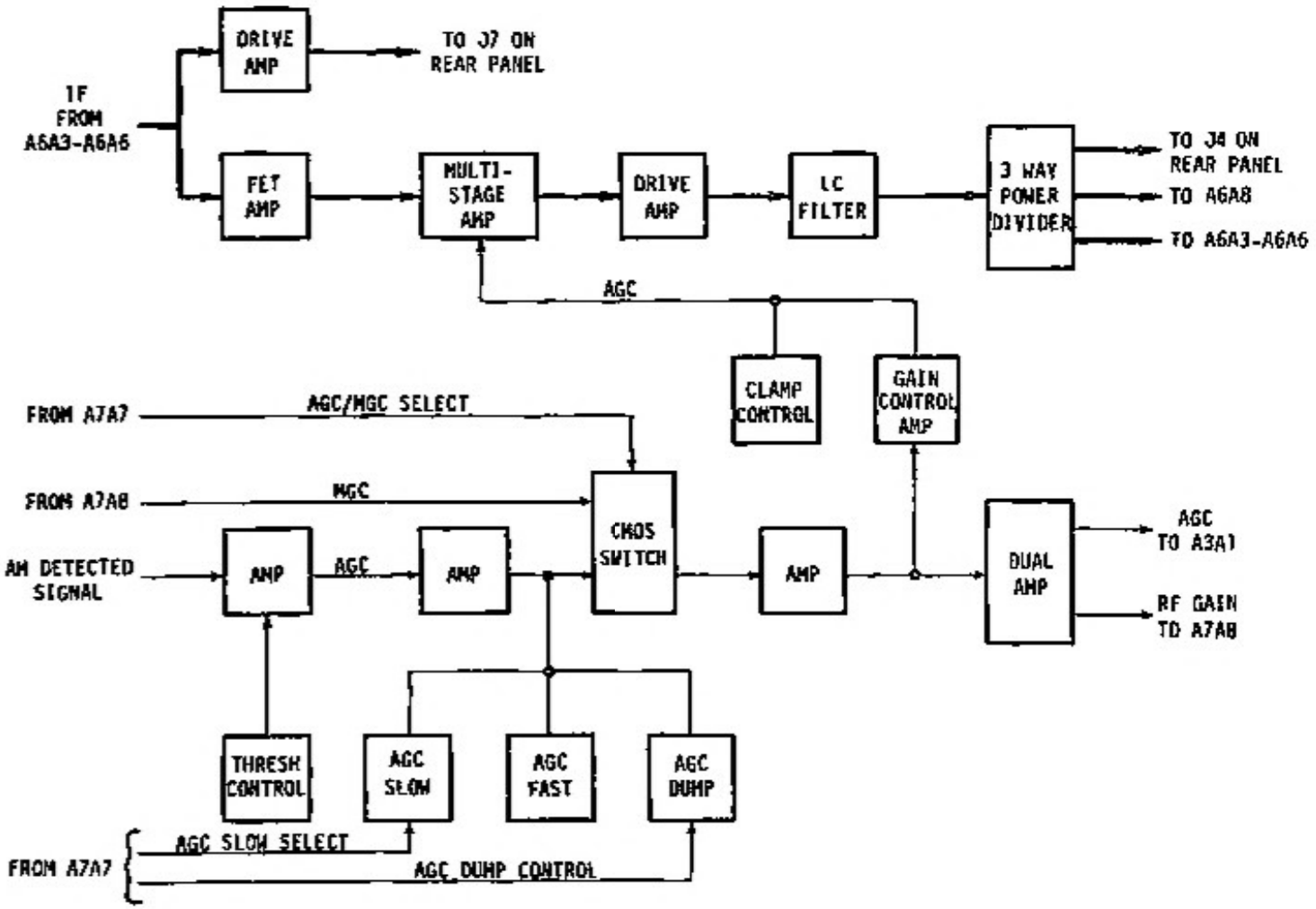


Figure 4-9. Variable Gain Amplifier (A6A2) Functional Block Diagram

automatic controlled gain to the IF signal and gain control to the tuner, and supplies the signal for COR operation. The 21.4 MHz IF is routed through various IF amplifiers with AGC controlling the gain of several stages of amplification. The AGC operates from the AM detected signal, when in the automatic mode, and from an analog signal from receiver control, when in the manual mode. Three modes of gain control are provided in the AGC circuits; AGC FAST, AGC SLOW and MGC (manual gain control). These modes are controlled through receiver control, which also controls an AGC dump circuit, used to speed up the AGC signal for large changes in amplitude.

4-37. The schematic diagram for the variable gain amplifier is shown in Figure 7-21. The input signal from the selected IF filter amplifier drives amplifier Q1 and FET amplifier Q2. The output of Q1 is the POST FL IF available at rear panel connector J7. The output from Q2 is coupled to a three stage differential amplifier (U1, U2 and U3). The differential amplifier modifies the signal gain in accordance with the gain control input from the gain control circuits. The gain controlled signal is routed through coupling transformer T1 to buffer-drive amplifier U10. This amplifier is used to drive the signal through a high pass filter (C57-C63 and coils L18-20) to a three way power output divider (U4). The three outputs from U4 are routed to: the AM and FM demodulators on the selected IF filter amplifier, the CW demodulator, and the rear panel IF OUT connector J4.

4-38. The gain control circuits mode of operation, AGC FAST, AGC SLOW or MGC, is controlled from receiver control. When either of the AGC modes is selected, gain mode C from receiver control is high, causing the switch between pins 5 and 6 of U7 to close. This closed switch routes the AM detector signal through amplifier U6C, part of U9, and diode CR4 to amplifier U6B. In MGC mode, gain mode C is low, and the MGC analog signal from receiver control is routed through the switch between pins 9 and 10 of U7 and U6B. Capacitor C28 is connected to the cathode of diode CR4, and with the constant current source provided by the circuit of U8B, is charged or discharged to a level in relation to the gain signal appearing at diode CR4. This gain-compensated signal is coupled, through amplifier U6B and gain control amplifier U8A to the three-stage amplifier (described in paragraph 4-36) for gain control of the IF signal. In AGC FAST, gain mode 2 (applied to transistor Q7), is high and capacitor C28 is discharged at a fast rate through diode CR5 and the circuit of U8C. In AGC SLOW, gain

mode 2 is high, transistor Q7 is cut off and the discharge time constant is slow. When the gain mode is changed from manual to automatic, capacitor C28 which may be charged to a high level is discharged to a starting level by the DMP signal from receiver control. This input through transistor Q5 and Q6, operational amplifier U8D and transistors Q3 and Q4 causes capacitor C28 to rapidly discharge through transistor Q3. The output of amplifier U6B is also routed to the tuner through amplifier U6A and to receiver control through U6D.

4-39. CW Demodulator (A6A8). Figure 4-10 shows a functional block diagram of the CW demodulator. The CW demodulator provides a demodulated continuous wave (CW) output with zero beat (CW0 mode), or an output with a 1 kHz offset from zero beat (CW 1 kHz mode). In addition, the CW demodulator generates a 2 MHz and 80 kHz reference frequency from the 10 MHz reference for use on an optional upper sideband (USB), lower sideband (LSB), 10 kHz converter circuit card assemblies (A6A7, A6A9, and A6A10 respectively). The 21.4 MHz input to the CW demodulator is mixed with a 19.4 MHz signal from a phase-locked voltage-controlled oscillator. The 2 MHz difference frequency from this mixer is routed through a four way power divider to outputs for the optional circuits previously described, and to a second mixer contained on the CW demodulator. The second input to this mixer is from a phase locked oscillator (controlled by CW offset data from receiver control) that is either 2.000 MHz or 2.001 MHz. This then results in the CW signal without offset or with 1 kHz offset.

4-40. Figure 7-23 shows the schematic diagram of the CW demodulator. The 21.4 MHz IF from the variable gain amplifier (A6A2) is routed through an RLC filter, for removing frequencies outside the bandwidth, to mixer U1. The second input to this mixer is the 19.4 MHz derived from the VCO (Q6-Y1). This VCO is controlled by a closed phase-lock-loop, which is referenced to the 10 MHz reference from the reference generator (A8), and counted down to 100 MHz by the divide-by-100 U10 circuitry. The mixer output is the 2 MHz IF (difference between 21.4 MHz IF and 19.4 MHz). This 2 MHz signal drives the four way power divider U2. Three of the 2 MHz outputs are used to drive optional circuits. The fourth output is one input to mixer U13. The second input to mixer U13 is either the 2.000 MHz (for CW 0 mode) or 2.001 MHz (for CW 1 kHz mode) derived from the VCO (Q8-U2). This VCO is controlled by the phase-lock-loop, which is referenced to an 8 kHz frequency reference, counted down from the 2 MHz frequency reference by a divide-by-25 circuit U11 and divide-by-10 circuit U23.

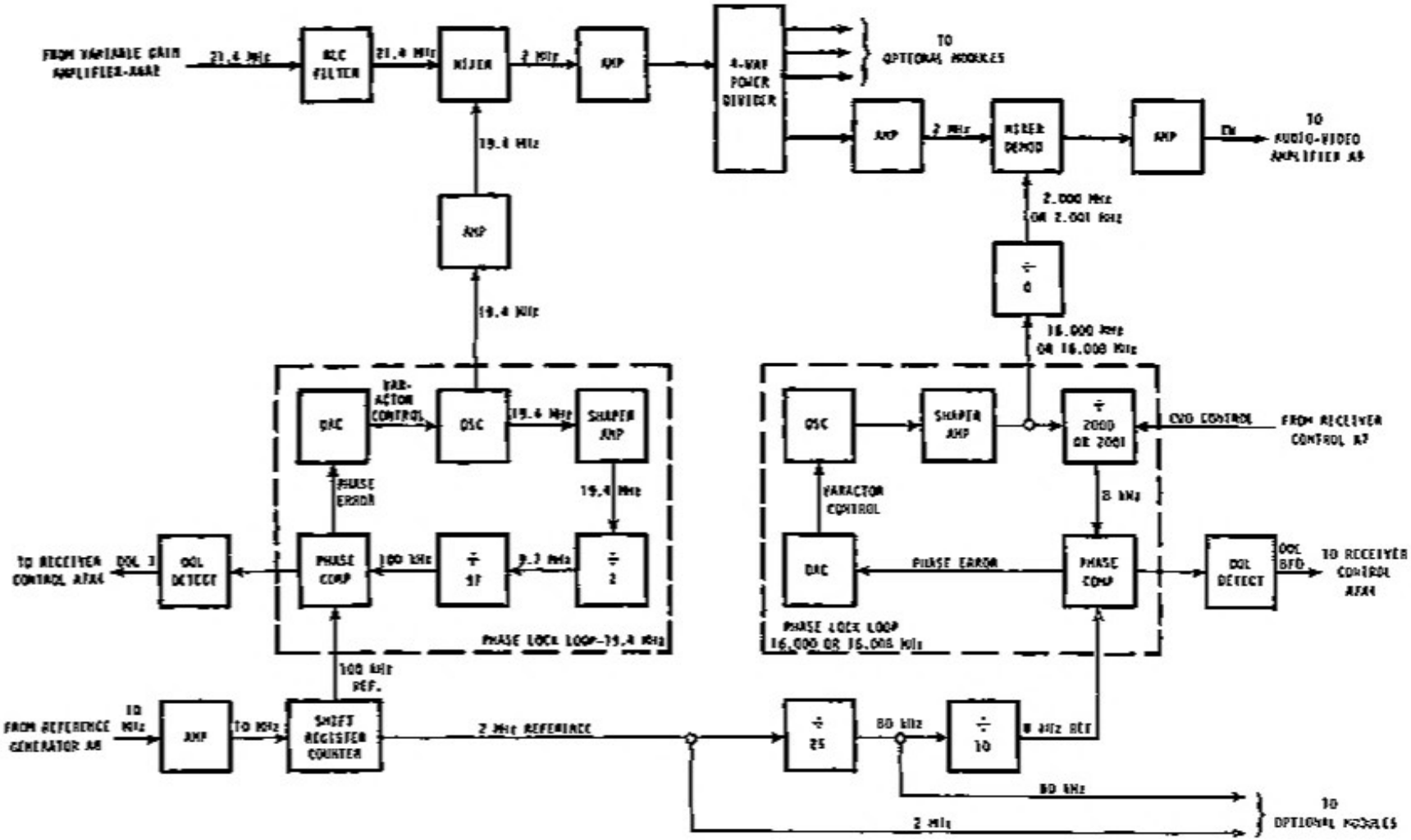


Figure 4-10. CW Demodulator (A6A8) Functional Block Diagram

The phase-lock-loop contains a counter which is counted down by either 2000 to 2001 (U18, U19, U20) dependent on the CW O signal from receiver control. This CW O selects either the CW O or the CW 1 kHz mode. The difference is output from mixer U13 as the CW video signal which is routed to the audio video amplifier/COR assembly (A9). The 2 MHz reference frequency and the 80 kHz reference from divide-by-25 counter U11 are used by the previously mentioned optional circuits.

4-41. AUDIO VIDEO AMPLIFIER/COR ASSEMBLY (A9). The audio video amplifier/COR circuit contains an control interface (A9A1), an audio video amplifier (A9A2), and a carrier operated relay (COR) (A9A3) circuit. The control interface interfaces audio signals from the demodulators to the audio video amplifier; COR and AGC signals from receiver control back to COR; and, receiver control signals to both the audio video amplifier and COR.

4-42. Audio Video Amplifier (A9A2). Figure 4-11 shows a functional block diagram of the audio video amplifier. This circuit receives the AM, FM, CW and optional USB and LSB components of the demodulated IF signal, selects these signals and applies them through amplifiers to headphones, jacks or terminals for monitoring. The audio video amplifier contains six sets of amplifiers for FM video, video, audio 1 and audio 2, headphones tip and headphones ring, two 4-circuit CMOS switches, and a decoding circuit used to control the CMOS switches. These switches select the demodulated input signals and apply them to the appropriate amplifiers for drive and output to the headphones or rear panel connections.

4-43. Figure 7-34 shows the schematic diagram of the audio video amplifier. The FM, AM, CW and optional USB and LSB inputs from the IF assembly (A6) are connected to switches U23 and U24. The switch outputs are controlled by signals from receiver control. The mode signals (2^0, 2^1, 2^2, and 2^3) are connected to decoder U2. Depending on the receiver output mode selected, the control signal A, B, or C is input to decoder U2 and one of the outputs from the decoder actuates the appropriate output switch. The SCAN signal from the digital control circuits is applied, during fast scan mode of operation, through gate U4B, and controls the FM VIDEO output through switch U23. This FM VIDEO output is blocked during fast scan mode of operation. The SCAN signal is routed through gates U4B, U5A, and U5B, to deactivate the decoder (U2). Thus, all

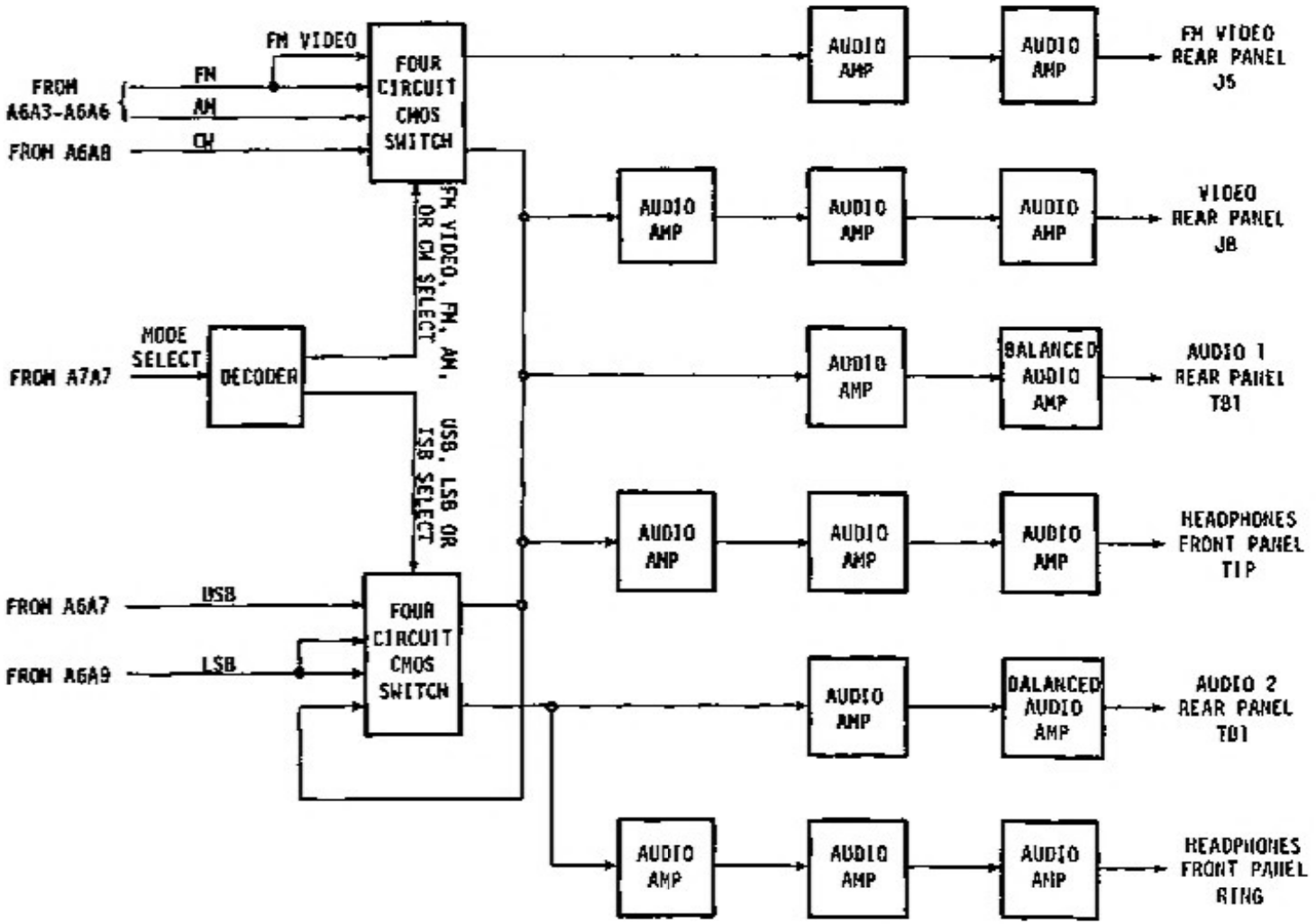


Figure 4-11. Audio Video Amplifier (A9A2) Functional Block Diagram

outputs are blocked during fast scan operations. The A, B, and C outputs from switches U23 and U24 connect to the output amplifiers. The A output is applied through operational amplifiers U8 and U9. The gain of amplifier U8 is controlled by the FM VIDEO adjustment (R1) located on the rear panel of the Receiver. The U9 amplifier output is routed to the FM VIDEO output at rear panel connector J5. The B output is applied to the three separate amplifier chains to provide the VIDEO, AUDIO 1 and HEADPHONES 1 outputs. The VIDEO output amplifier chain consists of operational amplifiers U10, U11 and U12. The gain of amplifier U10 is controlled by the VIDEO adjustment (R2) located on the rear panel of the Receiver. The U12 amplifier output is available at the receiver rear panel connector J8 as the VIDEO output. The AUDIO 1 output amplifier chain receives the B input into operational amplifier U13. The gain of U13 is controlled by the AUDIO 1 (USB) adjustment R3 located on the rear panel of the Receiver. The output of U13 drives both operational amplifiers U14A and U14B. These two amplifiers provide the drive for the balanced AUDIO 1 (USB) outputs. These signals are connected to terminal board TB1 at terminals 1, 2 and 3 on the rear panel of the Receiver. The HEADPHONES 1 output amplifier chain consists of operational amplifiers U17, U18, and U19. The gain of amplifier U17 is controlled by the HEADPHONE (USB) audio level control adjustment located on the front panel of the Receiver. The U19 amplifier output is connected to the HEADPHONE 1 (tip) on the receiver front panel. The C output from switch U24 is applied to the two separate amplifier chains which provide the AUDIO 2 and HEADPHONES 2 outputs. The AUDIO 2 output amplifier chain receives the C input which is routed to operational amplifier U15. The gain of the operational amplifier is controlled by the 10 K AUDIO (LSB) adjustment R4 located on the rear panel of the Receiver. The output of the operational amplifier drives both operational amplifiers U16A and U16B. These two amplifiers provide the drive for the balanced AUDIO 2 outputs. These are connected to receiver rear panel terminal board TB1 at terminals 4, 5 and 6. The HEADPHONES 2 output amplifier chain consists of operational amplifiers U20, U21 and U22. The gain of amplifier U20 is controlled by the HEADPHONES (LSB) audio level control adjustment located on the front panel of the Receiver. The U22 amplifier output is connected to HEADPHONES 2 (ring) on the Receiver front panel.

4-44. Carrier Operated Relay (COR) (A9A3). Figure 4-12 shows a functional block diagram of the COR. The basic carrier RF gain drive signal, from DAC 3 in receiver control, is coupled to a (threshold) comparator to which the threshold

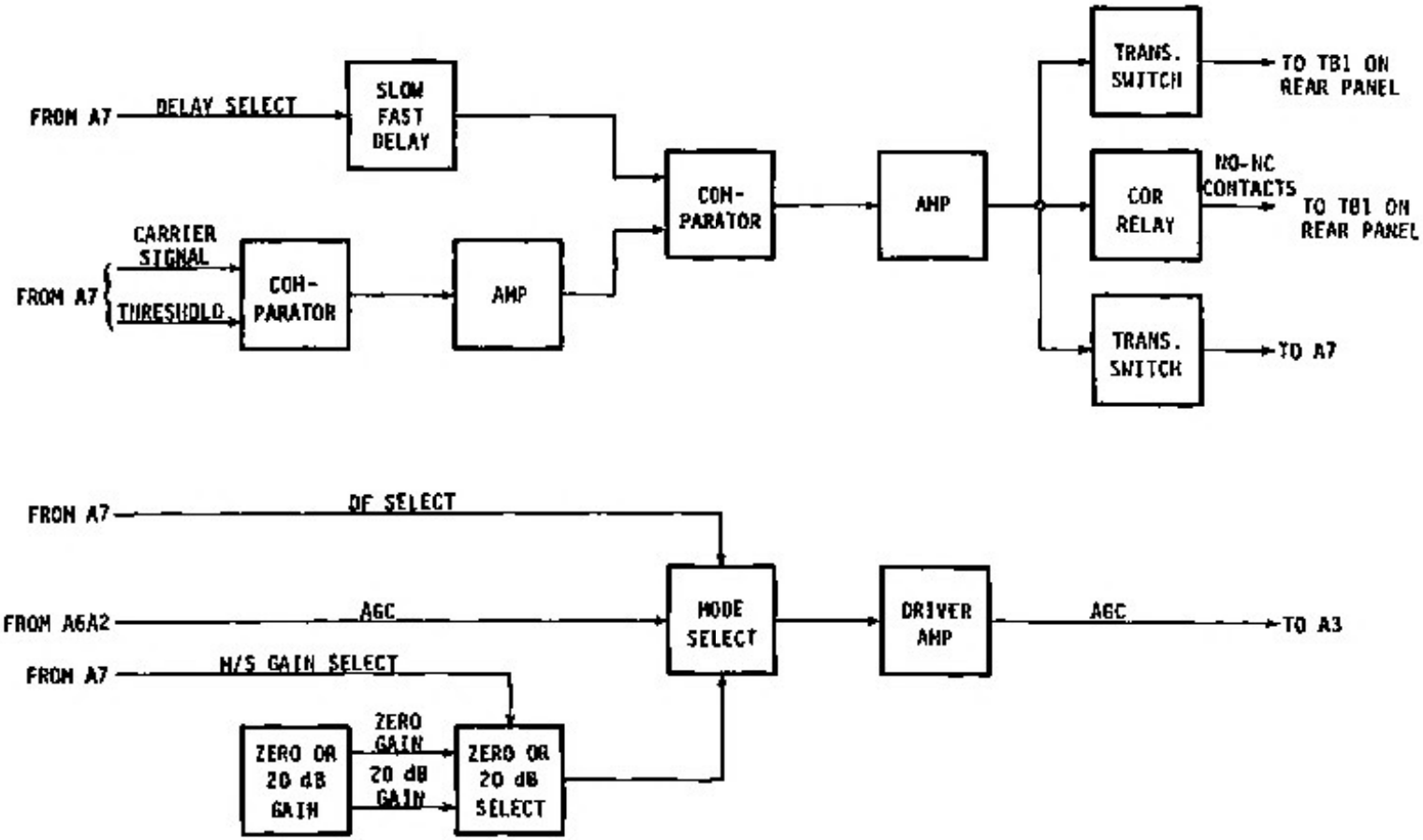


Figure 4-12. Carrier Operated Relay (A9A3) Functional Block Diagram

control signal from DAC 2 is also connected. The comparator determines the level that the carrier drive signal will operate the relay. The threshold comparator signal is amplified and then coupled to a delay comparator to which fast or slow delay is added. This circuit will keep the relay energized for approximately two seconds (SLOW) or less than 0.5 seconds (FAST), after the input carrier signal drops below the pre-set threshold. This output signal is then routed through a drive amplifier to the relay coil and to two transistor switches. Both the transistor switch and the contacts of the relay are output on the rear panel. The transistor switch will sink 250 milliamps of current at 50 volts.

4-45. Figure 7-35 shows the schematic diagram of the COR circuits. Comparator U2A receives both the COR threshold level signal and the RF gain signal from receiver control. If the RF gain signal exceeds the COR threshold level, comparator U2A is turned on, causing the output of transistor Q1 to go low which in turn rapidly discharges capacitor C4 through U2D. With the negative input of U2C near ground potential and its positive input held high by U2D, emitter follower Q2 is switched on providing drive for the COR output circuits. If the RF gain signal drops below the COR threshold, comparator U2A is turned off causing the output of transistor Q1 to go high. Capacitor C4 begins charging through resistors R12 and R13, holding the negative input to U2C below its crossover point for approximately two seconds (SLOW mode). When the crossover point of U2C is reached, it will switch off causing Q2 to turn off, which in turn switches off the COR drive circuits. In the FAST, mode comparator U2D holds capacitor C5 at near ground potential which changes the crossover point of U2C, thus operating Q2 fast. The COR drive circuits consist of transistors Q3, Q4 and Q5, and relay RL1. Transistor Q3 is used to drive the coil of relay RL1 with its normally open and normally closed contacts output to terminals 7, 8 and 9 of terminal board TB1 on the rear panel. Transistor Q4 provides for a current sink of 250 milliamps at 50 volts and is output to terminal 10 of terminal board TB1 on the rear panel. Transistor Q5 provides a COR output signal to receiver control. An AGC control circuit is also contained within this circuit stage. In normal modes of operation, the AGC input from the variable gain amplifier (A6A2) is routed through CMOS switch U1A and drive amplifier U3 to the tuner AGC circuits. In the optional DF (direction finding) mode, the AGC from the variable gain amplifier is disconnected from drive amplifier U3 and either

maximum gain or an adjustable gain is selected by CMOS switch U1B. The adjustable gain is provided by variable resistor R3 in series with R2 and R4. Maximum gain is provided by grounding the positive input of drive amplifier U3. The control signals for both U1A and U1B are applied from receiver control.

4-46. REFERENCE GENERATOR MODULE ASSEMBLY (A8). Figure 4-13 shows a functional block diagram of the reference generator. The reference generator provides a 10 MHz reference frequency used by assemblies A4, A5 and A6 as references to oscillator phase-lock-loops. The reference generator contains an oven temperature-controlled crystal oscillator which can operate independently or be further stabilized through an external reference to a phase-lock-loop for the internal oscillator.

4-47. Figure 7-32 shows the reference generator schematic diagram. The 10 MHz reference oscillator output is coupled to drive amplifier Q9 which drives a four way power divider U10. The four outputs of this power divider are routed to A4A1, A5A4, A6A7 and to a rear panel 10 MHz REF OUT connector J11. A portion of the signal from amplifier Q9 is also routed to shaper amplifier Q3-Q4 and connected through inverter U1A to divide-by-10 circuit U5. The resultant 1 MHz signal is then routed to rear panel 1 MHz REF OUT connector J16. If no external reference is used, no other circuitry on the reference generator is used except DC supply voltages. When an external reference is used, Receiver control selects and connects the crystal oscillator into a phase-lock-loop circuit. The external reference, either 1, 5 or 10 MHz is coupled through shaper amplifier Q1-Q2 and inverter U1C to a strapable divider circuit U2. This circuit must be strapped to provide either a divide-by-10 for a 10 MHz input, a divide-by-5 for a 5 MHz input, or the circuit bypassed for a 1 MHz input. The 1 MHz signal is coupled to one clock of the phase comparator U3 while the divided-by-10 oscillator frequency (1 MHz) is coupled as the second clock input. The phase comparator detects phase error between the two signals and routes it to a digital-to-analog converter (DAC) Q6, Q7, and Q8. The analog output of the DAC is routed through amplifier U8A and U8B and CMOS switch U9 to control the frequency of the oscillator. A portion of the phase difference signal from the phase comparator is used to drive an out-of-lock (OOL) detector (U4C, U1B and U6). The output of this detector drives a LED indicator DS1 and is also routed to receiver control.

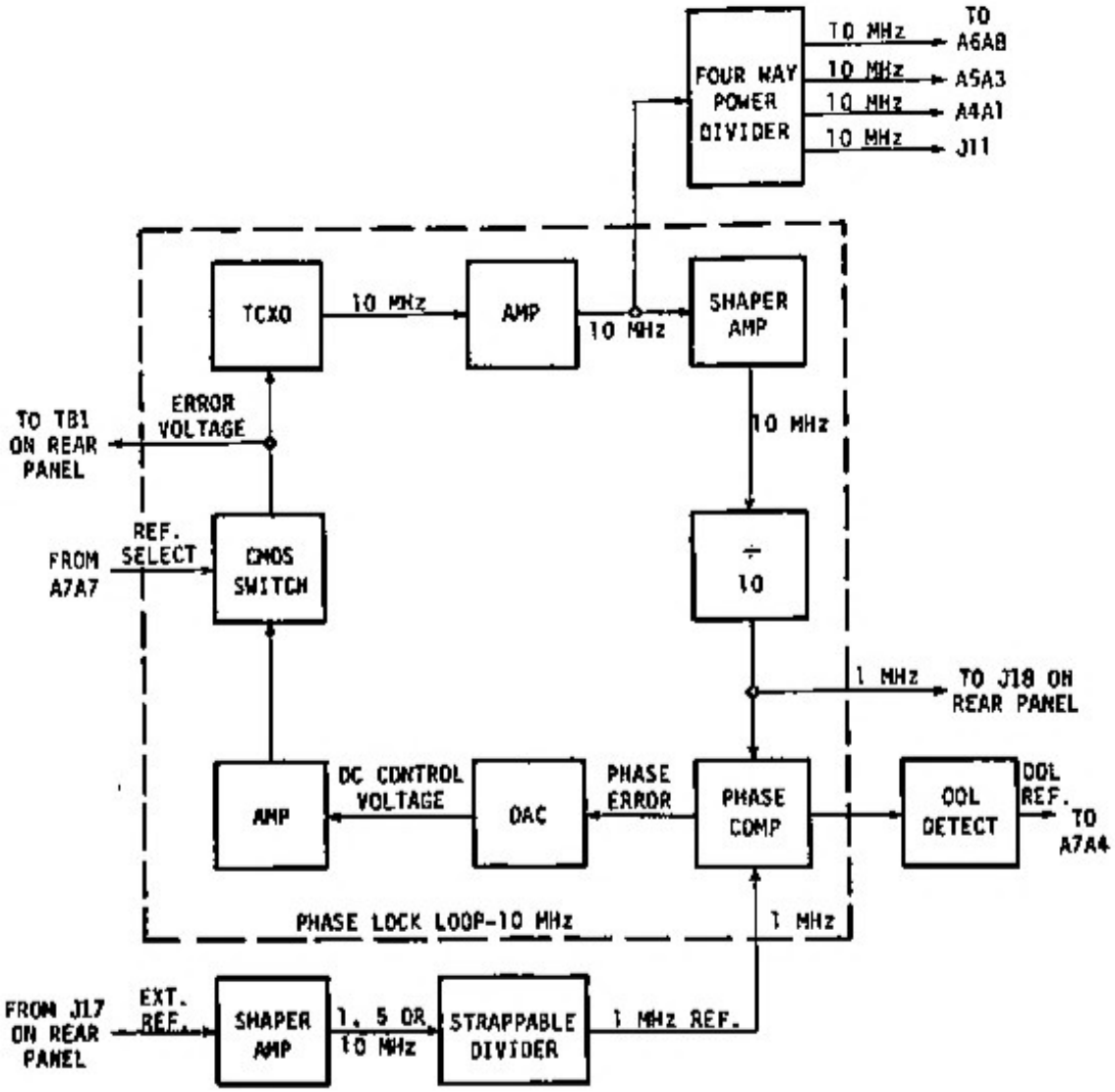


Figure 4-13. Reference Generator (A8) Functional Block Diagram

4-48. FIRST LO SYNTHESIZER MODULE ASSEMBLY (A5). Figure 4-14 shows an overall functional block diagram of the first LO synthesizer. The first LO synthesizer provides the first LO signal (681.4 to 1181.4 MHz) to the tuner assembly (A3). The first LO synthesizer circuit contains five sub-modules/circuit card assemblies; VCO A (A5A1), VCO B (A5A5), controller (A5A2), digiphase processor (A5A3), and programmable divider (A5A4). Each VCO contains three separate oscillators (total of six), each covering a different range of frequencies within the 681.4 to 1181.4 MHz range (refer to Table 4-1). The controller contains the VCO select circuitry that automatically, through receiver control, selects the appropriate VCO for the required frequency range. A coarse tuning circuit for the Spectrum Surveillance Controller is also contained on the controller. The digiphase processor contains circuitry for computing the divide-by-N control word. The programmable divider contains the phase-lock-loop circuits that keep the selected VCO locked on frequency.

4-49. Frequency Control-Phase Lock Loop. The six VCOs cover a frequency range of 500 MHz between 681.4 and 1181.4 MHz with each VCO covering an 80 to 85 MHz range (refer to Table 4-1). Each VCO can be further controlled to operate in 20 to 22 MHz increments, over its range through a band selection technique, then this range is still further controlled to a resolution of 10 Hz, through a phase-lock-loop, that provides a tuning voltage to the varactor of the selected VCO.

4-50. The phase-lock-loop that tunes the selected VCO to a resolution of 10 Hz is accomplished by comparing the oscillator output frequency to an accurate stable reference frequency, developing an error voltage from any phase difference and then driving the oscillator varactor with that error voltage to correct oscillator frequency. To accomplish this, a reference from the temperature-controlled crystal oscillator is used and divided by ten, to provide a 1 MHz reference for better sensitivity to phase difference. The oscillator output frequency must then be divided to correspond to this 1 MHz reference. Since the oscillator frequency can vary between 681.4 and 1181.4 MHz, the divide-by number must be variable, and to accomplish a resolution of 10 Hz it must be fractional. This can be more clearly demonstrated by using the formula N=Fo divided by Fr; where N is the divide-by number, Fo the oscillator frequency, and Fr the reference frequency. Assume that Fo is 701.234670 MHz and the reference frequency is 1.0 MHz, then using the above formula the result is:

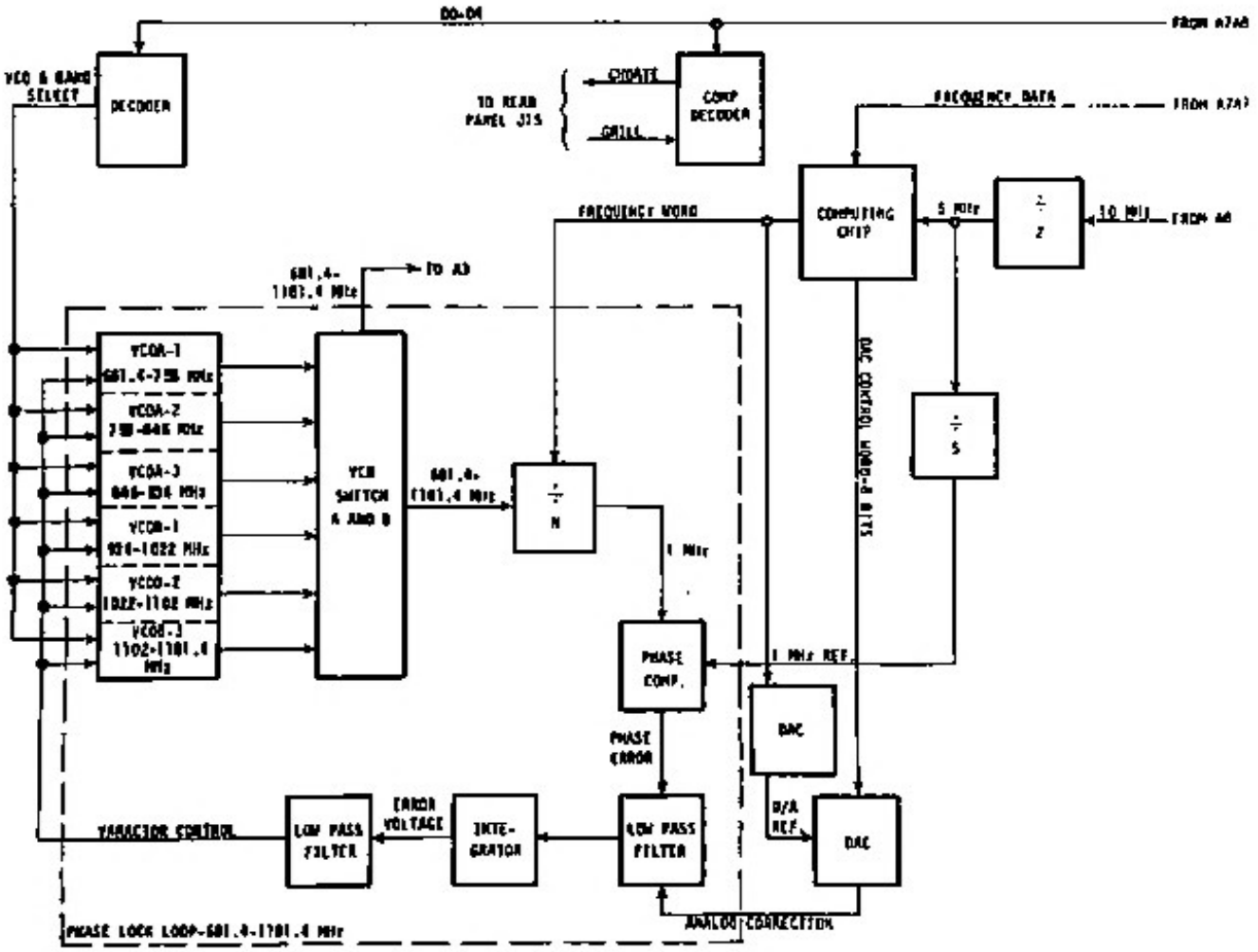


Figure 4-14. First LO Synthesizer (A5) Functional Block Diagram

701.234670(Fo) divided by 1.0(Fr) = 701.234670(N). If we split this number into its integer part and its decimal part, the result is a three-decade integer and a six-decade decimal number. Generating the non-integer part as an actual frequency is done by considering a portion of the frequency spectrum of interest, between 701 MHz and 702 MHz, where this finally generated frequency will occur. Thus, it is possible to generate any signal between these two frequencies by an averaging technique; that is to say if the signal at 702 MHz is sampled 234,670 times and the signal at 701 MHz is sampled 765,330 times (1,000,000-234,670) then the average or apparent signal produced by this sampling would occur at the frequency of interest at 701.234670 MHz. This type of sampling produces a large number of sampling sidebands on the main output frequency. These can be removed, however, by a correction signal equal and opposite to these predictable sidebands and adding this to the oscillator control signal, effectively nullifying the production of these sidebands. Since the first LO synthesizer generates frequencies to within 10 Hz, the decimal part need only contain five decades.

4-51. As shown in Figure 4-14, the computing chip provides the frequency word to the divide-by-N circuit which varies the N number to produce 1 MHz from the oscillator frequency. If the oscillator drifts off frequency or the frequency is changed through receiver control, the output of the divide-by-N will be either 1 MHz plus or minus, depending on direction of change. The phase error between this divided oscillator frequency and the reference frequency will be detected by the phase comparator and applied to an integrator. The computing chip also provides a digital correction for nullifying the unwanted sidebands and applies it to a digital-to-analog converter (DAC). The analog correction signal from the DAC is also applied to the integrator which integrates the signals to produce an error voltage. This error voltage is routed to the oscillator's varactor. Frequency data from the computer is also coupled to a binary decoder which supplies the VCO and band select signals which select the appropriate oscillator and its band to within 22 MHz of the selected frequency. The phase lock loop, with its divide-by-N controlled by the frequency word, then causes the oscillator to adjust to the frequency selected.

4-52. VCO A and VCO B (A5A1 and A5A5). Figure 4-15 shows a functional block diagram of both VCO A and VCO B, while Figures 7-15 and 7-19 show the schematic

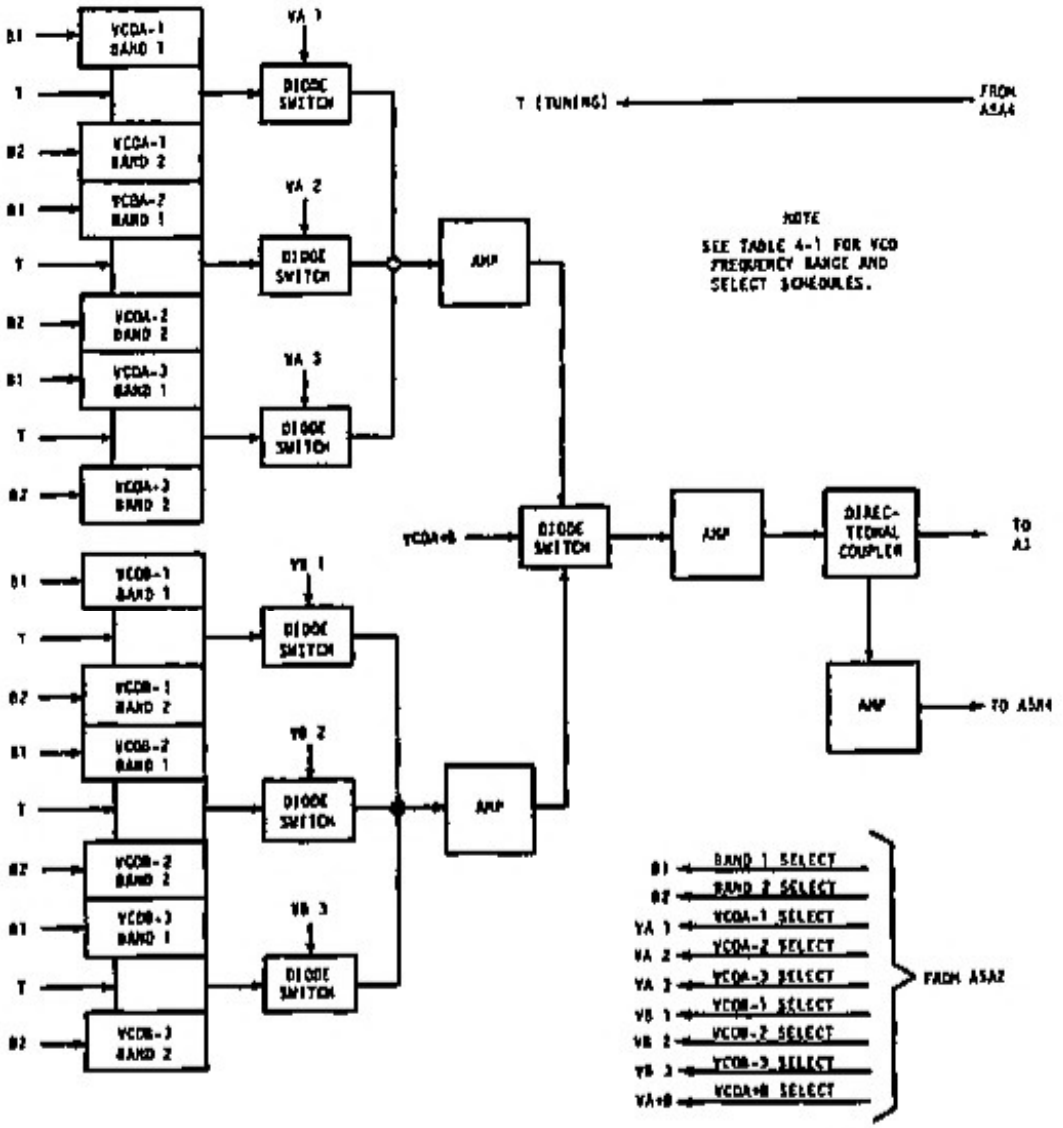


Figure 4-I5. VCO A (A5A1) and VCO B (A5A5) Functional Block Diagram

diagram of each. Each VCO contains an oscillator Q1, with a tuned tank circuit consisting primarily of inductors Z1, Z2 and Z3, and varactor CR3. Inductors Z2 and Z3 can be switched in and out of the tuned tank, by band 1 and band 2 selection, through diode switches CR1 and CR2 respectively. The frequency between each band will be approximately 20 MHz; however, the actual band range will depend on the VCO and band selected (refer to Table 4-1). The band selection can select neither band (VCO low frequency), band 2 (VCO low frequency plus approximately 20 MHz), band 1 (VCO low frequency plus approximately 40 MHz) or both band 1 and band 2 (VCO low frequency plus approximately 60 MHz). The varactor, receiving its control voltage from the phase-lock-loop, provides for tuning the oscillator between the bands as described in paragraph 4-50. The VCO selection controls the bias of diode switches that select the appropriate VCO for the frequency range selected. Since the six VCOs are contained on two modules (three on each), a select signal (VCO A or VCO B) selects the appropriate VCO by biasing a diode switch located at the LO output (A5A5). The LO output is then coupled through a buffer amplifier and direction coupler to the tuner (A3).

4-53. Controller (A5A2). Figure 4-16 shows a functional block diagram of the controller. The controller provides the decoding, from microcomputer input data, for VCO selection, and band selection within each oscillator. In addition, the cathode also contains a coarse tune circuit that alerts the Spectrum Surveillance Controller (when being used with the Receiver) to abrupt tuning changes in the VCO.

4-54. Figure 7-16 shows the schematic diagram of the controller. Data lines D0 through D3, from receiver control, are each routed to its own shift register U8, U9, U13 and 14 respectively. Inverted data line D4 and the write strobe are routed through NAND gate U3B and inverter U4 to provide the clock input to all four shift registers, while inverted data line D0, data line D4, and the write strobe are routed through NAND gate U3A to provide the clear for all four shift registers. The output of the shift registers are decoded by binary decoder U18 which produces 8 bits (D0-D7) of output data. This data is then routed to 8 bit latch U19. The write strobe and data lines D0 and D4 through NAND gate U3C clock the data through data latch U19. Data lines D0 and D1 from the latch are routed through inverters U15A, U15B, U15C and U15D to their separate amplifiers for BAND 1 and BAND 2 select signals for the VCOs. Data lines D2 through D5 are

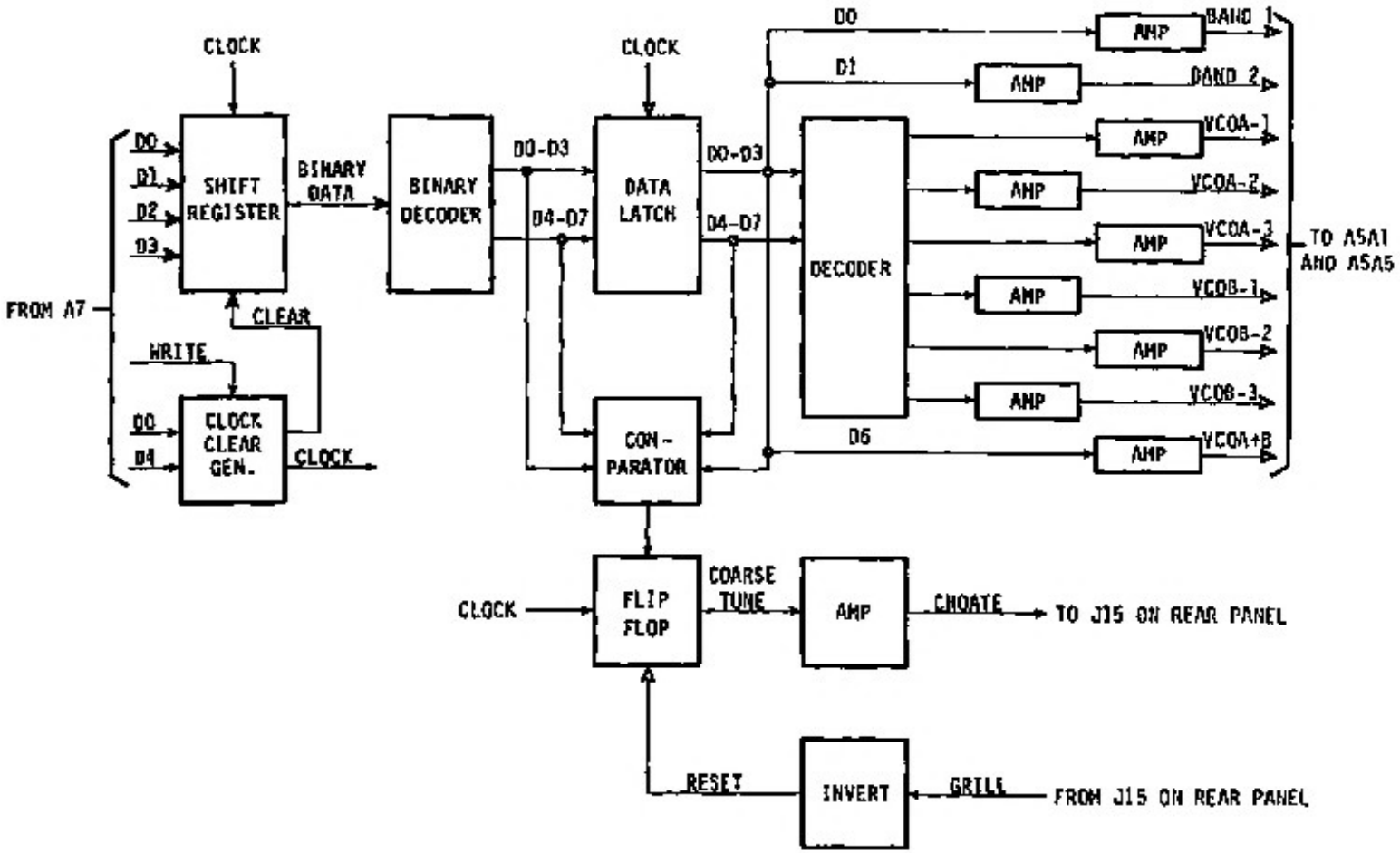


Figure 4-16. Controller (A5A2) Functional Block Diagram

Table 4-1. VCO Truth Table

BAND (MHZ)	VCO A 1 2 3	VCO B 1 2 3	BAND 1 2	VCO A&B	"N" INPUT 20 MHz DIV 8 2^3	DIV 7 2^2	DIV 6 2^1	DIV 5 2^0	200 MHz DIV 12 2^3	DIV 11 2^2	DIV 10 2^1	DIV 9 2^0
681.4 - 698	1 0 0	0 0 0	0 0	1	0	0	1	0	0	1	0	0
698 - 718	1 0 0	0 0 0	0 1	1	0	0	1	1	0	1	0	0
718 - 738	1 0 0	0 0 0	1 0	1	0	1	0	0	0	1	0	0
738 - 758	1 0 0	0 0 0	1 1	1	0	1	0	1	0	1	0	0
758 - 780	0 1 0	0 0 0	0 0	1	0	1	1	0	0	1	0	0
780 - 802	0 1 0	0 0 0	0 1	1	0	1	1	1	0	1	0	0
802 - 824	0 1 0	0 0 0	1 0	1	1	0	0	0	0	1	0	0
824 - 846	0 1 0	0 0 0	1 1	1	1	0	0	1	0	1	0	0
846 - 868	0 0 1	0 0 0	0 0	1	0	0	0	0	0	1	0	1
868 - 890	0 0 1	0 0 0	0 1	1	0	0	0	1	0	1	0	1
890 - 912	0 0 1	0 0 0	1 0	1	0	0	1	0	0	1	0	1
912 - 934	0 0 1	0 0 0	0 1	1	0	0	1	1	0	1	0	1
934 - 956	0 0 0	1 0 0	0 0	0	0	1	0	0	0	1	0	1
956 - 978	0 0 0	1 0 0	0 1	0	0	1	0	1	0	1	0	1
978 - 1000	0 0 0	1 0 0	1 0	0	0	1	1	0	0	1	0	1
1000 - 1022	0 0 0	1 0 0	1 1	0	0	1	1	1	0	1	0	1
1022 - 1042	0 0 0	0 1 0	0 0	0	1	0	0	0	0	1	0	1
1042 - 1062	0 0 0	0 1 0	0 1	0	1	0	0	1	0	1	0	1
1062 - 1082	0 0 0	0 1 0	1 0	0	0	0	0	0	0	1	1	0
1082 - 1102	0 0 0	0 1 0	1 1	0	0	0	0	1	0	1	1	0
1102 - 1122	0 0 0	0 0 1	0 0	0	0	0	1	0	0	1	1	0
1122 - 1142	0 0 0	0 0 1	0 1	0	0	1	1	1	0	1	1	0
1142 - 1162	0 0 0	0 0 1	1 0	0	0	1	0	0	0	1	1	0
1162 - 1181.4	0 0 0	0 0 1	1 1	0	0	1	0	1	0	1	1	0

NOTE: 1. VCO A1, A2, A3, B1, B2, B3 and VCO A&B:
+15 VDC @ 5 MA = LOGICAL 1
-15 VDC @ 5 MA = LOGICAL 0

2. BANDS 1 & 2:
+15 VDC @ 60 MA = LOGICAL 1
-15 VDC @ 60 MA = LOGICAL 0

3. "N" input data shown simulates BCD normally provided by the Programmable Divider (A5A4) as shown in Figure 7-18.

routed to 1 of 10 decoder U10. This decoder is controlled by data lines D2 through D5 through BCD to decimal decoder U5, and data lines D0 and D1 through transistors Q1 and Q2 respectively. The six outputs of decoder U10 drive inverters and amplifiers to provide the select lines to the six VCOs. Data line D6, from data latch U19, is routed through inverters U17C and U17D and amplifier U11B to provide the VCO (A+B) select.

4-55. The frequency data that is clocked through data latch U19 is compared and routed through a flip-flop and transistor amplifier to the Spectrum Surveillance Controller (when used with the Receiver) as coarse tune information. Two comparators compare the data lines D0 through D3 while comparator U21 compares data lines D4 through D7. The compared data of U20 is also compared by U21 which outputs its data to flip-flop U15 and is clocked by the inverted clock signal to data latch U19. The Q output of the flip-flop is then routed through transistor amplifier Q1 to the Spectrum Surveillance Controller. Flip flop U15 is set when previous and new information is different, stopping the scan of the surveillance controller while the synthesizer relocks on the new band. A GRILL signal from the Spectrum Surveillance Controller is inverted by U4 and used to reset the flip-flop, after allowing sufficient time for relock.

4-56. Digiphase Processor (A5A3). Figure 4-17 shows a functional block diagram of the digiphase processor. The digiphase processor receives frequency data from receiver control and generates the frequency word (divide-by-N control word) which is routed to the controller (A5A2) and to the programmable divider (A5A4). In addition, the digiphase processor generates the analog correction signal for correcting the frequency control word on the programmable divider.

4-57. Figure 7-17 shows the schematic diagram of the digiphase processor. The frequency data from receiver control is processed by computing chip U7. The frequency data (D0-D4) is a string of ten 5-bit characters and are strobed into U7 by strobe W from receiver control. The computing chip computes the digital BCD value of N and outputs this data as the DIV 1 - DIV 11 outputs. The DIV 1 - DIV 4 outputs are routed through quad latch U3 to the programmable divider as divide-by-N control word 2 MHz. The DIV 5 - DIV 11 outputs are routed through level translators U5 to the programmable divider as divide-by-N control words 20 MHz (DIV 5 - DIV 8) and 200 MHz (DIV 9 - DIV 11), and to digital-to-analog converter U6. The computing chip also supplies an eight-bit digital word (DA 1 - DA 8), to multiplying digital to analog converter U8, for an analog

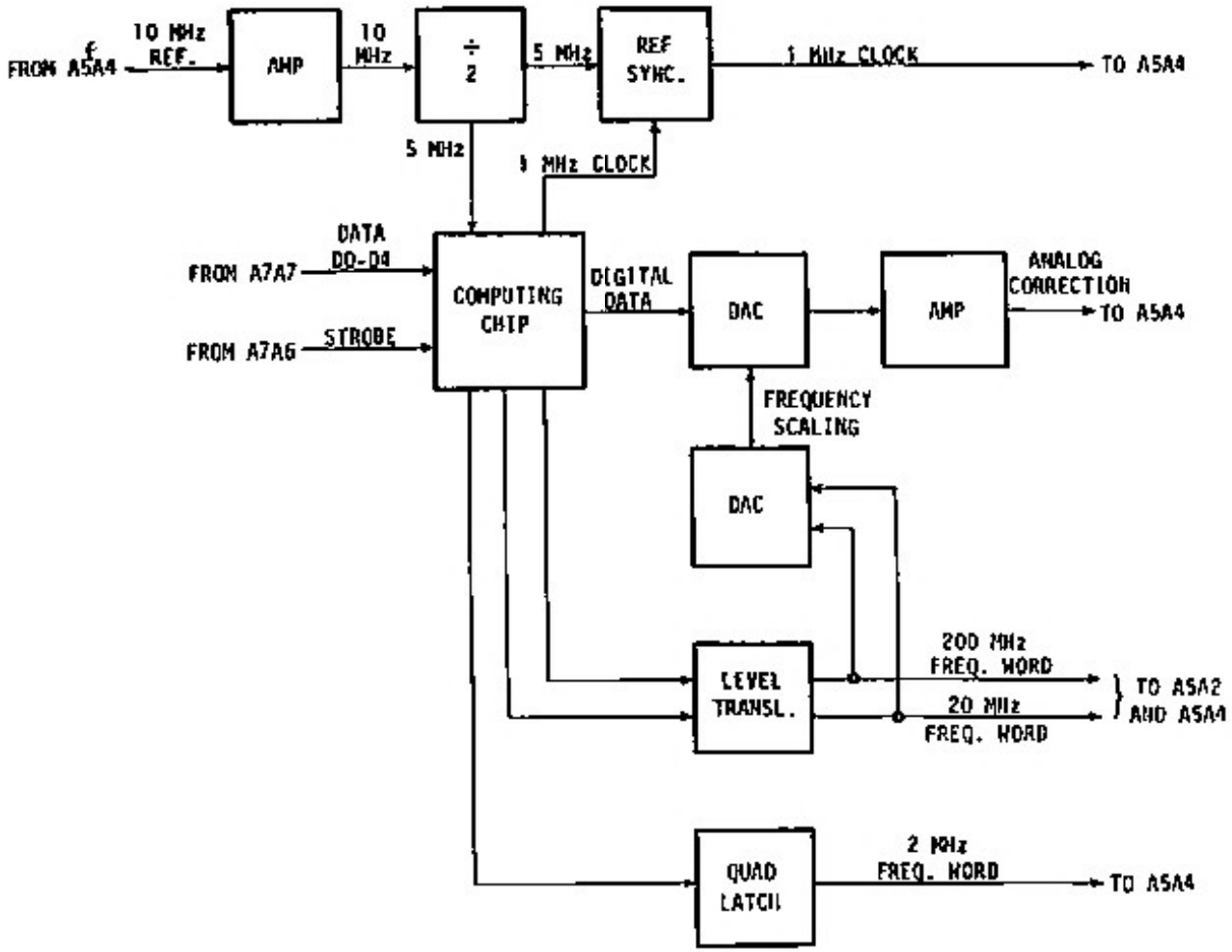


Figure 4-17. Digiphase Processor (A5A3) Functional Block Diagram

correction signal used in the programmable divider. Digital-to-analog converter U8 also receives an analog reference signal from U6 through operational amplifier U10B. This amplifier scales the analog correction voltage according to the value of N. This signal was derived from the divide-by-N control words routed to and converted by U6. The analog correction signal from U8 is routed to the programmable divider through operational amplifier (U10A). The computing chip (U7) requires a clock signal which is derived from the 10 MHz reference frequency. The 10 MHz reference frequency routed from the programmable divider is coupled through a low pass filter (C1-C3 and L1), transistor amplifier Q1, and buffer amplifiers U1A, U1B and U1C to the clock input of flip-flop U4A. The 5 MHz output from U4A is routed through transistor Q2 to the clock input of U7. The 5 MHz outputs of U4A also drives the clock of flip-flop U4B while the 1 MHz clock output of U7 drives its D input. The output of U4B is a 1 MHz reference and is routed to the programmable divider.

4-58. Programmable Divider (A5A4). Figure 4-18 shows a functional block diagram of the programmable divider. The programmable divider provides the phase-lock-loop for the VCO frequency. The VCO frequency received, is divided as directed by the divide-by-N control word from the digiphase processor (A5A3), phase compared to a reference frequency, and then integrated into an error voltage tuning the VCO.

4-59. Figure 7-18 shows a schematic diagram of the programmable divider. The 1st LO signal from the selected VCO drives amplifier U1, which in turn drives the prescaler U2, which divides by either 20 or 22. The prescaler contains a divide-by-2 counter followed by a divide-by-10 or 11 counter. The counter control input to the prescaler determines whether the counter divides by 10 or 11. A binary coded decimal (BCD) counter is formed by U3, U4 and U5; U3 containing unit digits; U4 tens digits; and, U5 hundreds digits. The preset inputs to this counter are the N value DIV1-DIV11 from the digiphase processor. These inputs are labeled 2 MHz, 20 MHz and 200 MHz because of the divide-by-2 in prescaler U2.

4-60. The prescaler U2 drives (for countdown) the units counter (U3) and the interconnected tens and hundreds counter (U4 and U5) separately; that is, the output of the units counter U3 does not connect to the input of the tens counter U4. Thus, during countdown, while there are values greater than zero in the units counter, the counter control zero detect circuit (flip-flop U6A) sets prescaler U2 to count by 11. Each output of the prescaler decrements both the

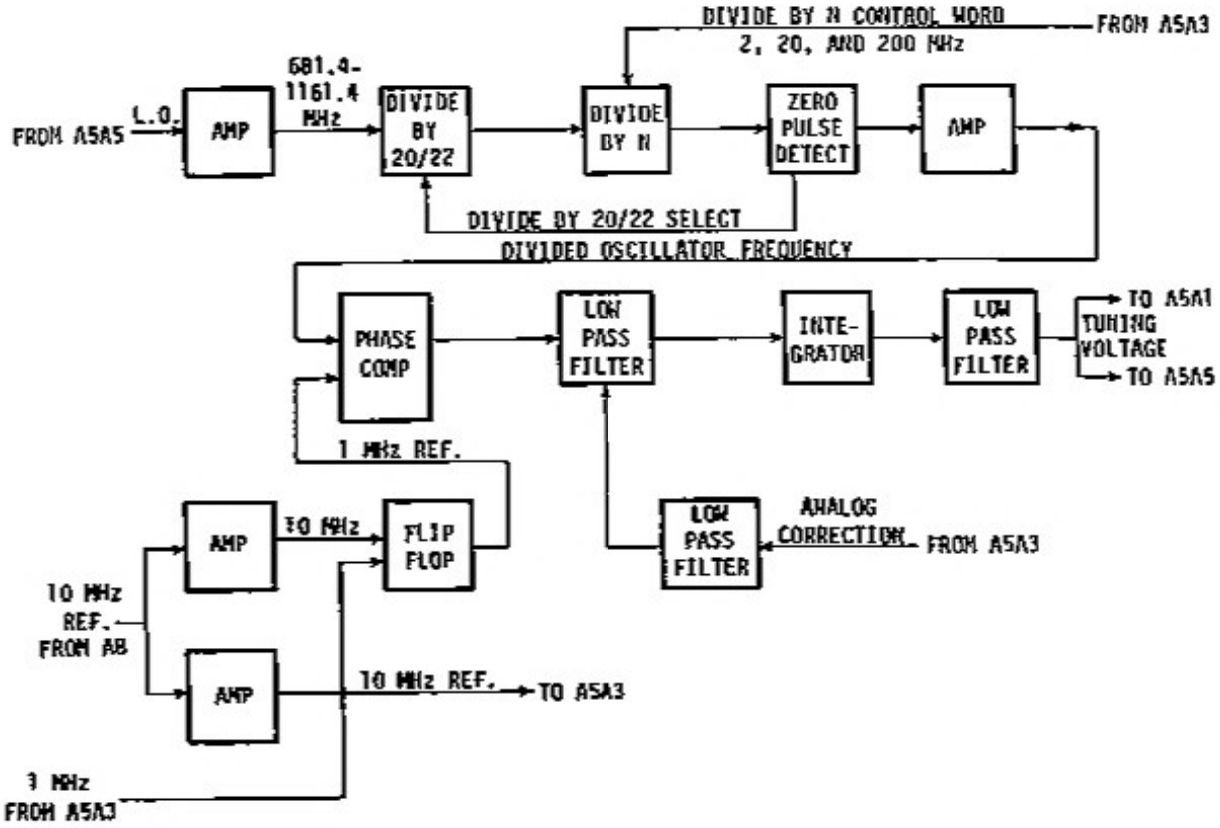


Figure 4-18. Programmable Divider (A5A4) Functional Block Diagram

units section and tens and greater section of the programmable counter by 1. This effectively subtracts 11 from the programmable counter. When the units section counts down to zero, the counter control zero detector U6A sets the prescaler to count by 10 (after divide-by-2). Each output now decrements the tens and greater sections of the programmable counter by one, effectively subtracting 10 from the counter. When the counter has counted down to zero (N counts), the flip-flop U6B is set. At the next input pulse (from the prescaler) the programmable counter is loaded to start another count cycle and flip-flop U6N is set. At the next input pulse (from the prescaler) the programmable counter is loaded to start another count cycle and flip-flop U6B is set. At the next input pulse (from the prescaler) the programmable counter is loaded to start another count cycle and flip-flop U6N is reset. Thus Q and $\overline{Q}$ outputs produce a pulse for each N count. The Q output of U6B drives the clock input of phase detector flip-flop U7A through transistor Q1. Phase detector flip-flop U7B is driven by the 1 MHz reference (described later). The $\overline{Q}$ outputs from phase detector flip-flop U7A and U7B drive NAND gate flip-flops U8A - U8D. Thus, pulses will be obtained from the $\overline{Q}$ outputs of U7A and U7B whose relative phase and widths will indicate the phase error between the VCO output and the reference signal. The phase error pulse signal from the phase comparator is then coupled through a low pass filter (C22-C25, L3-L6 and R18-R24) to an integrator network (C26, C27, CR1-CR4, R25, R26 and U10). This circuit also receives the analog correction signal from the digiphase processor (A5A3), and integrates this signal with the phase error signal, and provides a DC error voltage output. This error voltage is then routed through a low pass filter (C30, C31, L7, R30 and R73) to the voltage controlled oscillators for tuning. The 1 MHz reference used by the phase comparator is derived from the 10 MHz reference generator and the 1 MHz clock reference from the digiphase processor. The 10 MHz reference is routed through transistor amplifier Q2 to the clock input of flip-flop U9A. The 1 MHz clock reference from the digiphase processor is coupled to the data input of this same flip-flop so that it is clocked through the flip-flop every tenth pulse of the 10 MHz reference. This technique provides a clean 1 MHz reference, with transitions synced to the operation of the digiphase processor, which is then routed the phase comparator. The 10 MHz reference signal is also routed through FET isolation amplifier Q3 to the digiphase processor.

4-61. SECOND LO MODULE ASSEMBLY (A4). Figure 4-19 shows a functional block diagram of the second LO. The second LO generates the 640 MHz, 320 MHz, and

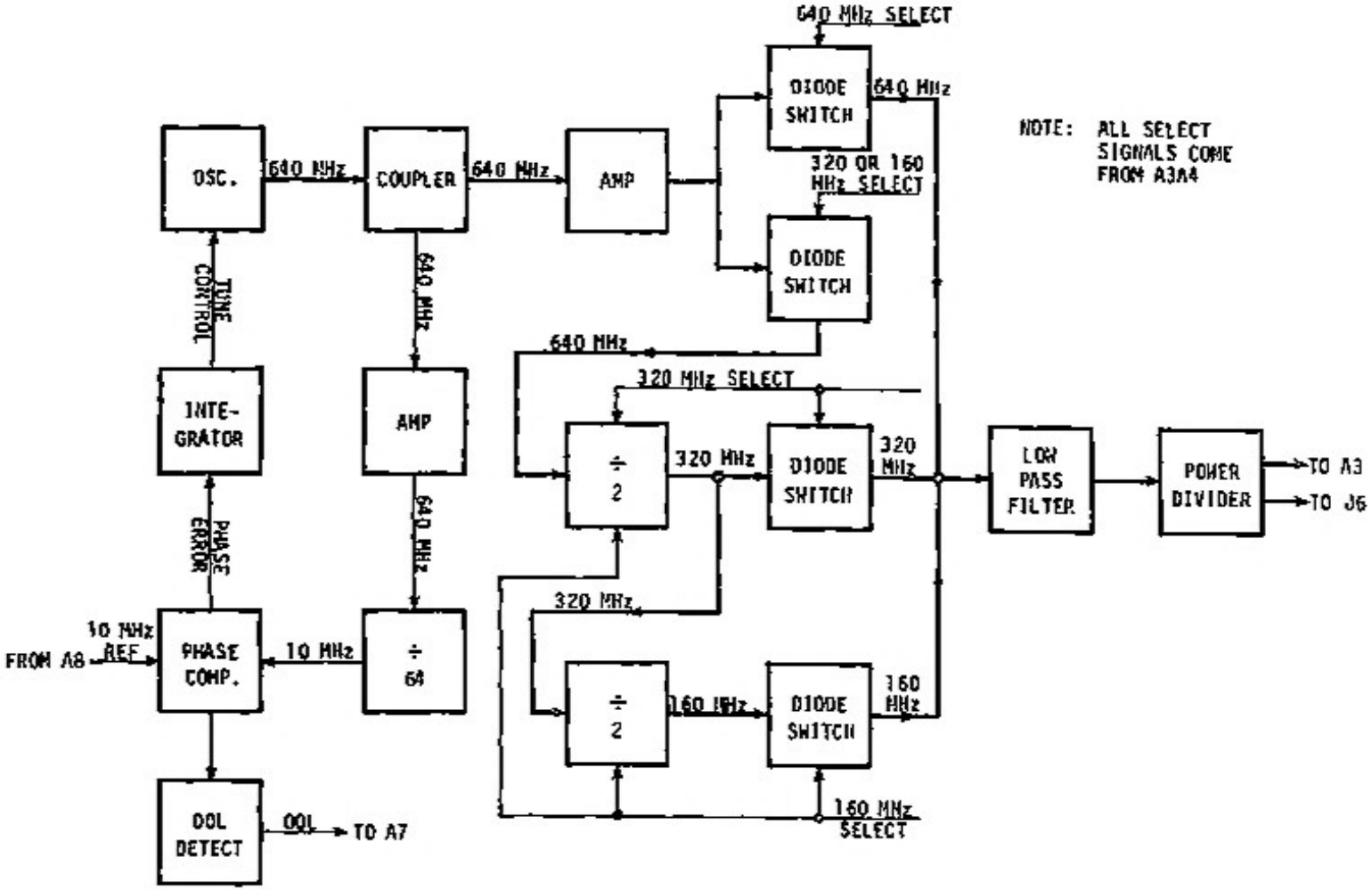


Figure 4-19. Second LO (A4) Functional Block Diagram

160 MHz signals used for second conversion in the tuner (A3). The circuit consists of a voltage controlled oscillator (VCO), with a phase-lock-loop circuit to maintain oscillator stability, and two divide-by-2 circuits with switching circuits, to select either 640, 320 or 160 MHz output to the tuner.

4-52. Figure 7-13 shows the schematic diagram of the second LO. The oscillator Q101 generates the basic 640 MHz second LO frequency. This basic frequency is routed through directional coupler Z101 and buffer amplifier U101 to a low pass filter (C215-C217 and L205-L206) and power divider (X201), either directly or through one or two divide by two circuits depending on the frequency band). The route of the 640 MHz is directed by diode switches which are controlled by frequency band selection from the tuner (A3). In the 640 MHz (20-500 MHz) band, a select line to the cathode of diode switch CR205 is held high (positive), preventing the 640 MHz from being routed to the divide-by-2 circuits, while at the same time a select line to the cathodes of diode switches CR201 and CR204, through inverter driver U203A, goes low (from positive to negative) allowing the 640 MHz to be routed to the filter and power divider. In the 320 MHz (500-840 MHz) and 160 MHz (840-1000 MHz) bands, the select line to diodes CR201 and CR204 is high while the select line to diode switch CR205, through inverter driver U203F (320 MHz) or U203E (160 MHz) goes low allowing the 640 MHz to be routed to divide-by-2 circuit U201. The 320 MHz output of U201 is routed to diode switch CR202 and to divide by two circuit U202. The 160 MHz output of U202 is routed to diode switch CR203. Divide-by-2 circuit U201 is enabled by both the 320 MHz and 160 MHz select lines, through inverter drivers U203F and U203E respectively, while U202 is enabled by the 160 MHz select line only, through inverter driver U203D. In the 320 MHz band, the select line to diode switch CR202, through inverter driver U203B, goes low routing the 340 MHz to the filter and power divider. In the 160 MHz band, the select line to diode switch CR203, through inverter driver U203C, goes low routing the 160 MHz to the filter and power divider. The two outputs of the power divider are routed through connector J3 to the rear panel and connector J2 to the tuner assembly.

4-53. The 640 MHz oscillator frequency is stabilized through a phase-lock-loop. This phase-lock-loop contains a frequency phase comparator, integrator, divide-by-64 oscillator reference and a 10 MHz reference from the reference generator (A8). A portion of the 640 MHz oscillator frequency is coupled from directional coupler Z101 through isolation amplifier Q102 to the input of divide-by-64 circuit U303. The 10 MHz output of U303 is then coupled to one clock input of

dual flip-flop U304B. The other clock input is from the 10 MHz reference generator to flip-flop U304A. The 10 MHz reference is passed through a filter network (C309-C310, U306A and B, L301 and R307-R309) to provide a clean 10 MHz square wave. The dual flip-flop and the combination NAND gates and flip-flops of U305A to U305D make up the phase comparator. When the oscillator frequency is in phase with the 10 MHz reference the two outputs of the phase comparator are balanced square waves 180 degrees opposite in phase with a 50 percent duty cycle, but if the oscillator drifts off frequency the phase detector outputs become unbalanced, one greater and one less than 50 percent duty cycle. These signals are then integrated through integrator U307 and associated components which produce a drive signal to the varactor in the oscillator circuit; thus correcting the oscillator drift. An out-of-lock (OOL) circuit, consisting of NAND gate U306C, transistor Q301 and associated components, is used to detect and send this information to the microcomputer (A7A2) when the oscillator is not locked to the 10 MHz reference frequency.

4-64. RECEIVER CONTROL (A2 and A7). Figure 4-20 shows an overall functional block diagram of receiver control. The circuits of receiver control comprise two assemblies: front panel (A2) and receiver control (A7). The front panel assembly contains tune and RF gain controls, COR threshold control, remote/local select, phones jack and associated level control, tuning and level meters, power switch, keyboard and associated decoder and displays. The receiver control assembly comprises the receiver control output interface (A7A1), microcomputer (A7A2), front panel I/O control interface (A7A4), display driver (A7A5), address decoder (A7A6), preselector controller (A7A7), converter (A7A8), and IEEE-488C remote control interface (A7A9).

4-65. Receiver control is a microcomputer based control distribution center for all Receiver functions. This control can be initiated manually from and through the front panel; from a remote computer/controller through the IEEE-488C remote control interface module; or from a Spectrum Surveillance Controller through the receiver control output interface. Control parameters entered at the front panel are directed through the front panel I/O control interface (A7A4) to the microcomputer data bus. This data flow is controlled by strobes from the microcomputer address decoder. Information on the data bus is processed by the microcomputer and strobed through the converter, and the receiver control output interface and display drivers to the appropriate Receiver functions. When the Receiver is operated in the remote control mode, control data is routed through

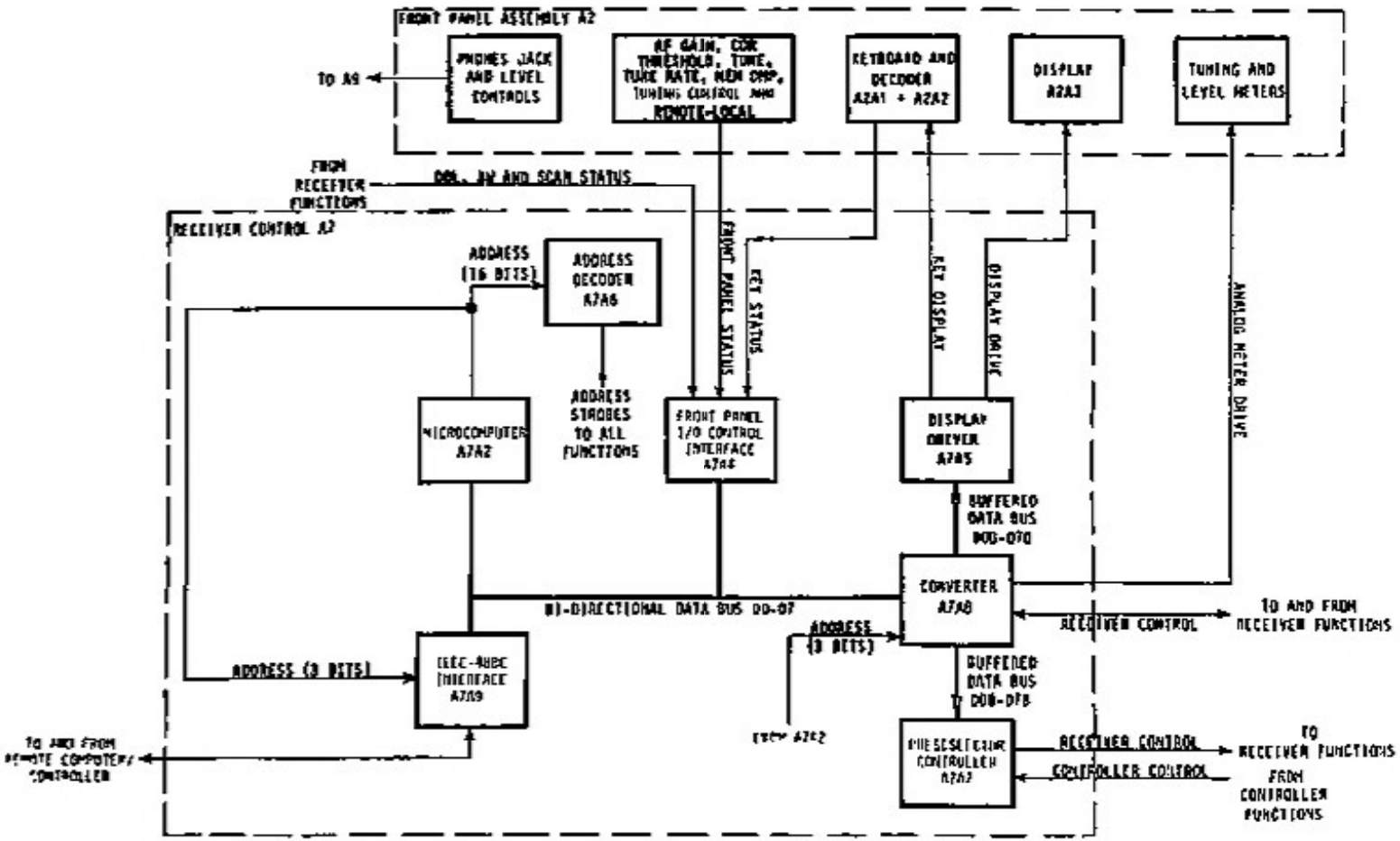


Figure 4-20. Receiver Control (A2 and A7) Overall Functional Block Diagram

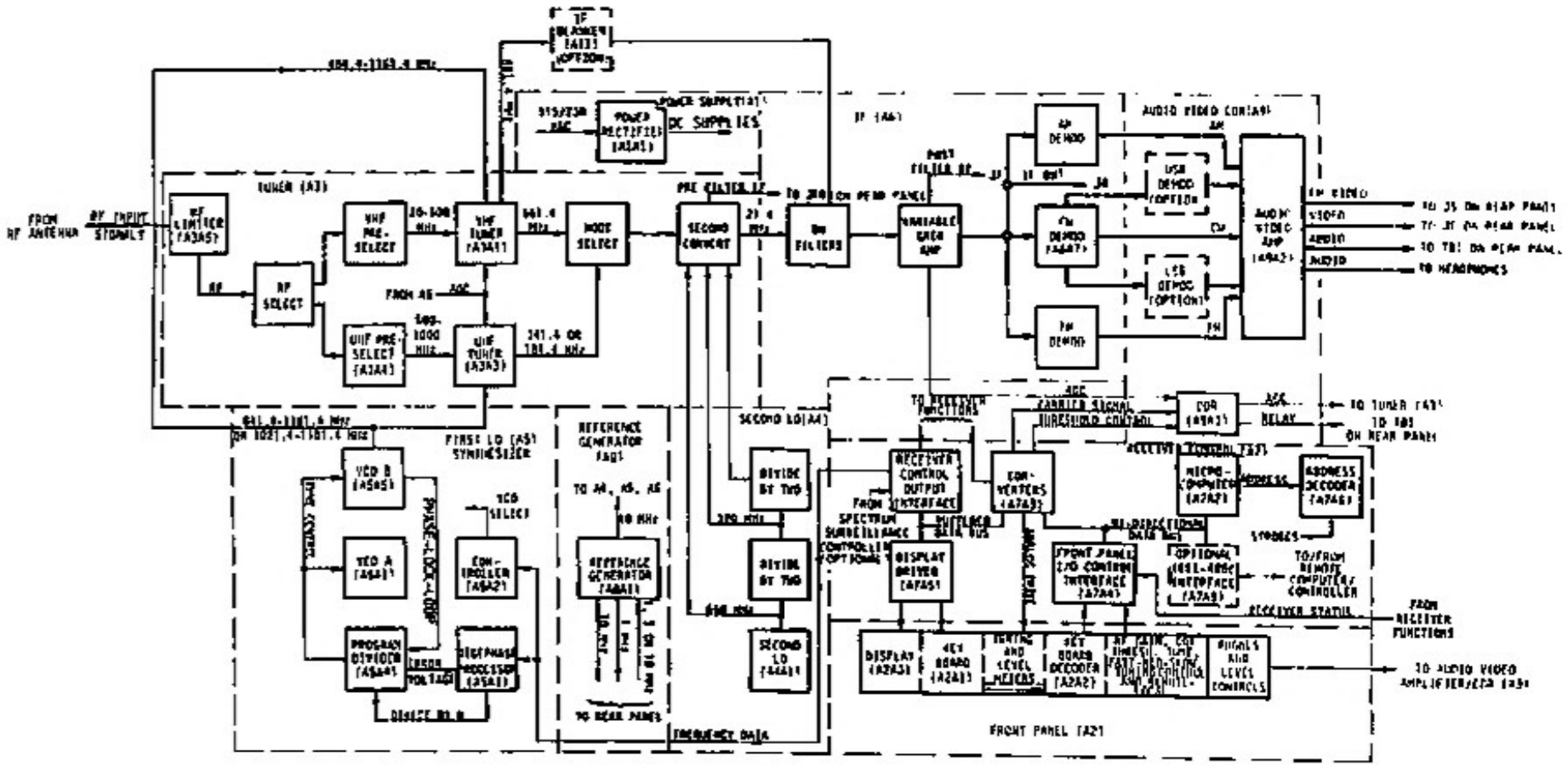


Figure 4-1. Receiver Overall Functional Block Diagram

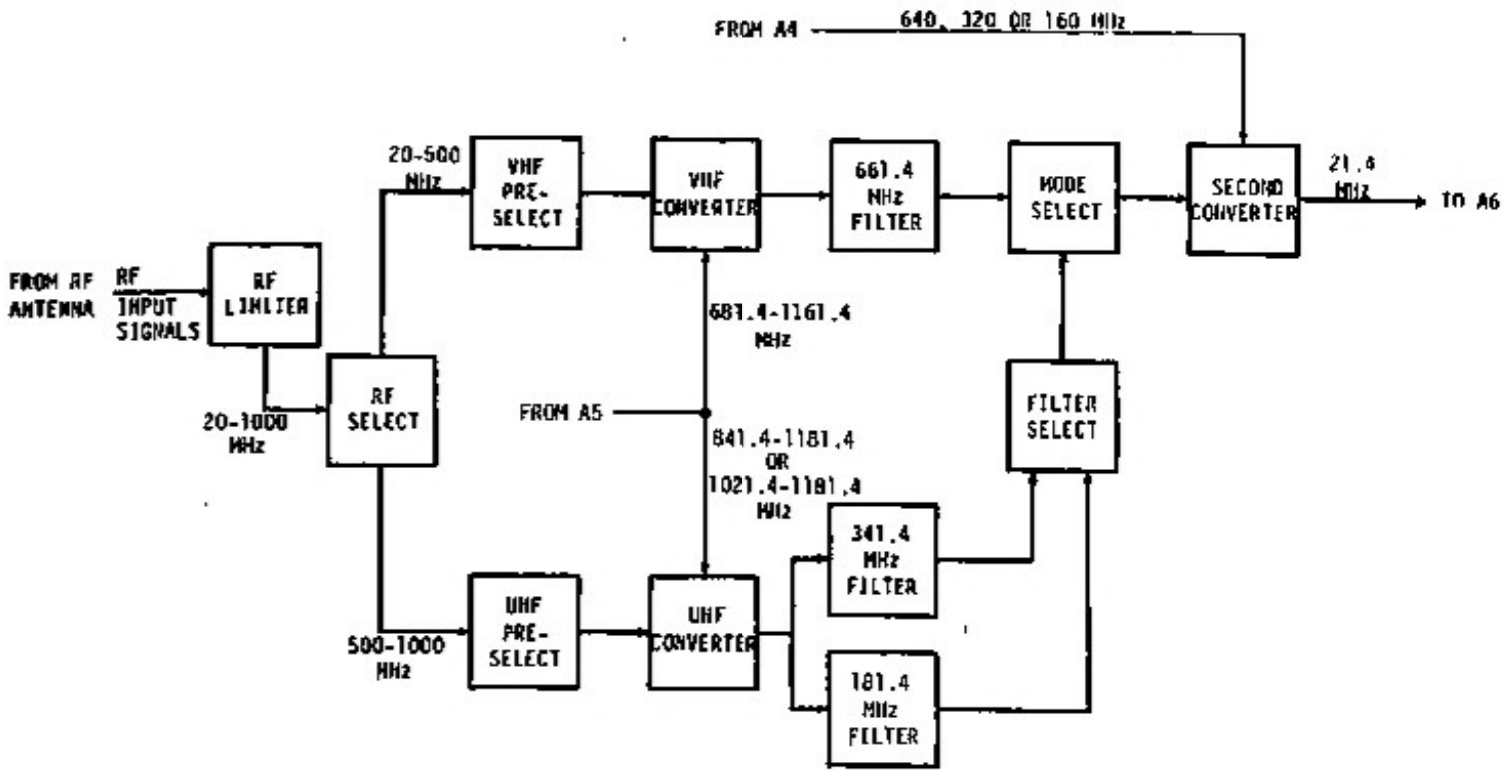


Figure 4-2. Tuner Assembly (A3) Functional Block Diagram

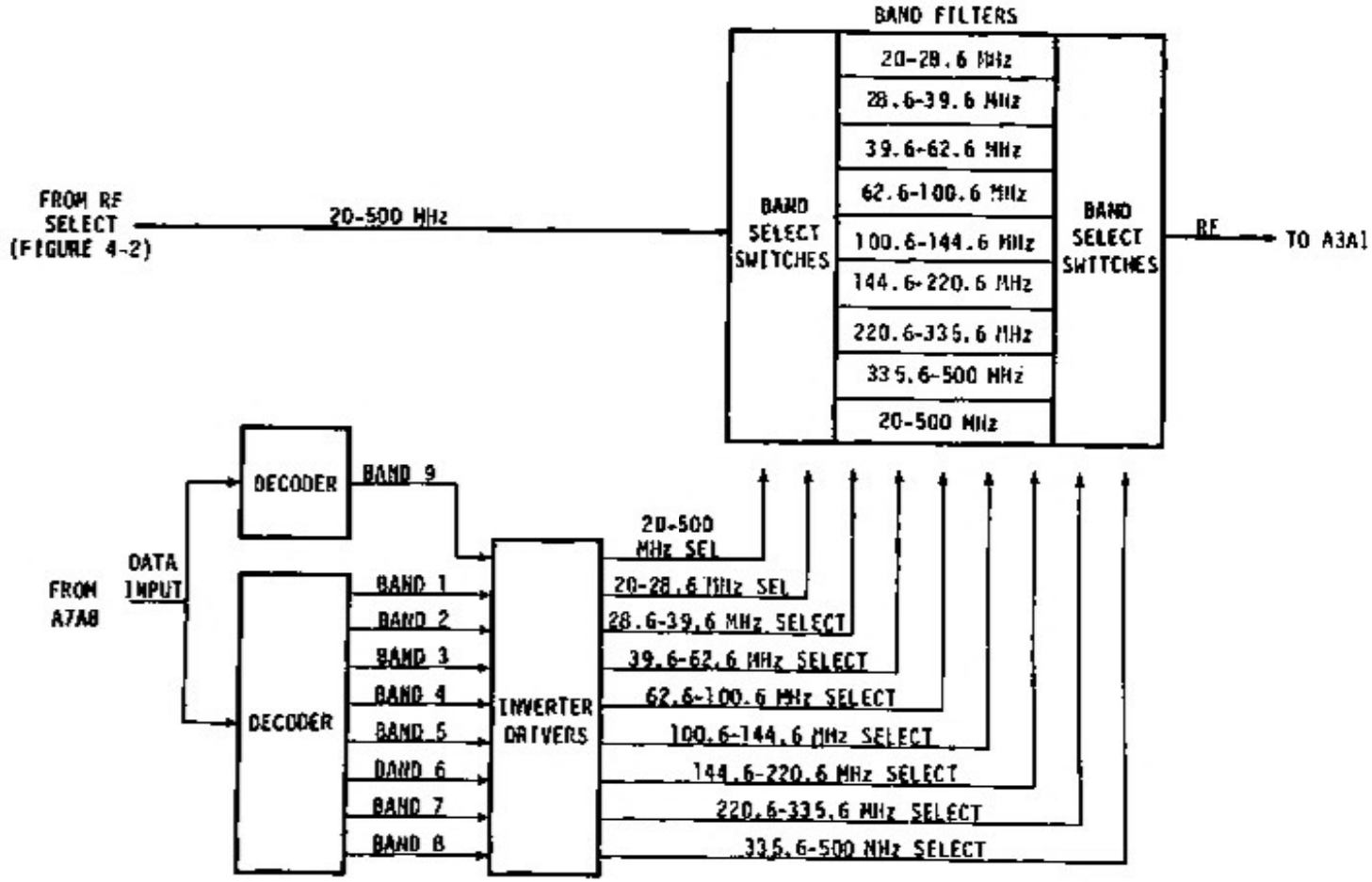


Figure 4-3. VHF (20-500 MHz) Preselector and Decoder Driver (A3A2) Functional Block Diagram

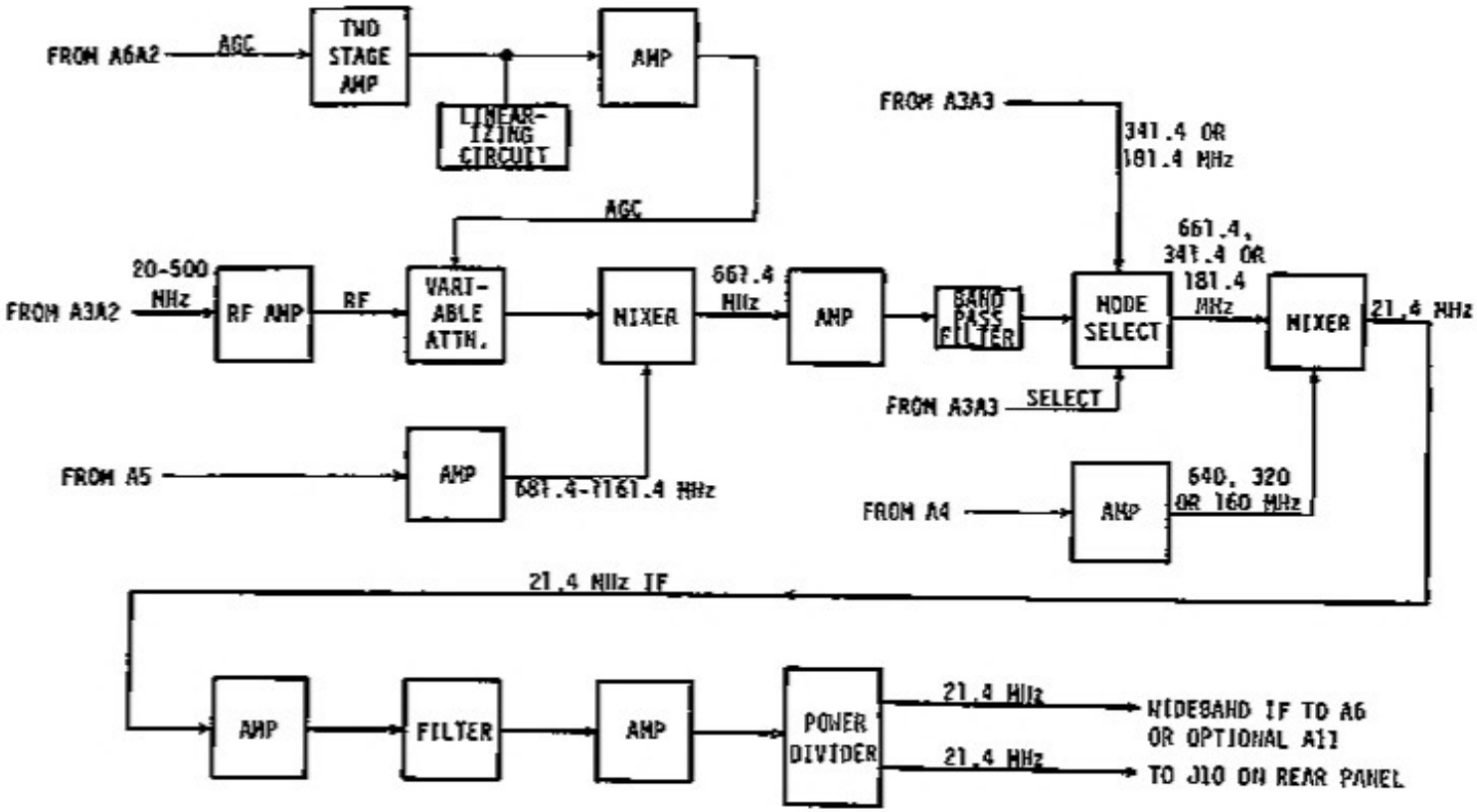


Figure 4-4. VHF Tuner (A3A1) Functional Block Diagram

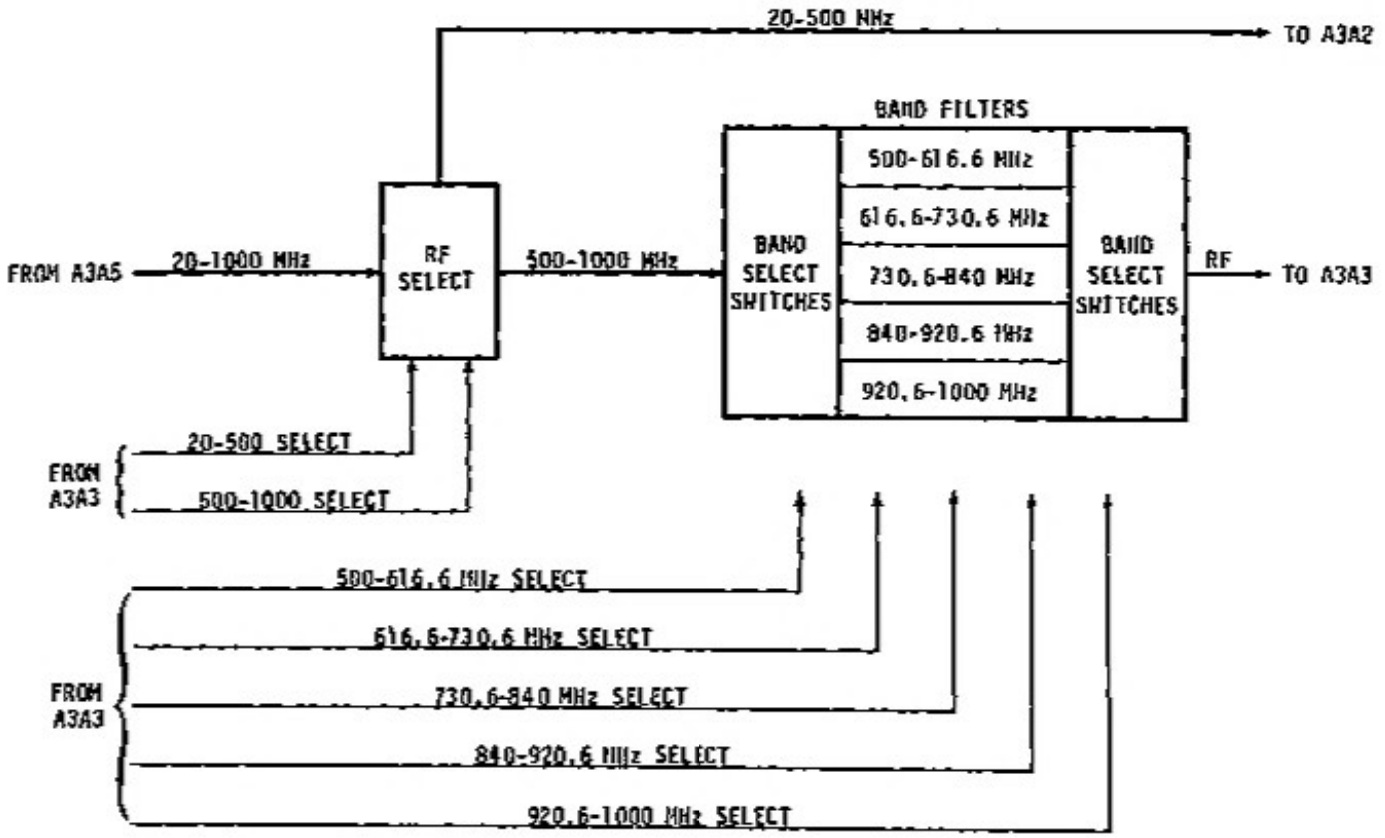


Figure 4-5. UHF (500-1000 MHz) Preselector (A3A4) Functional Block Diagram

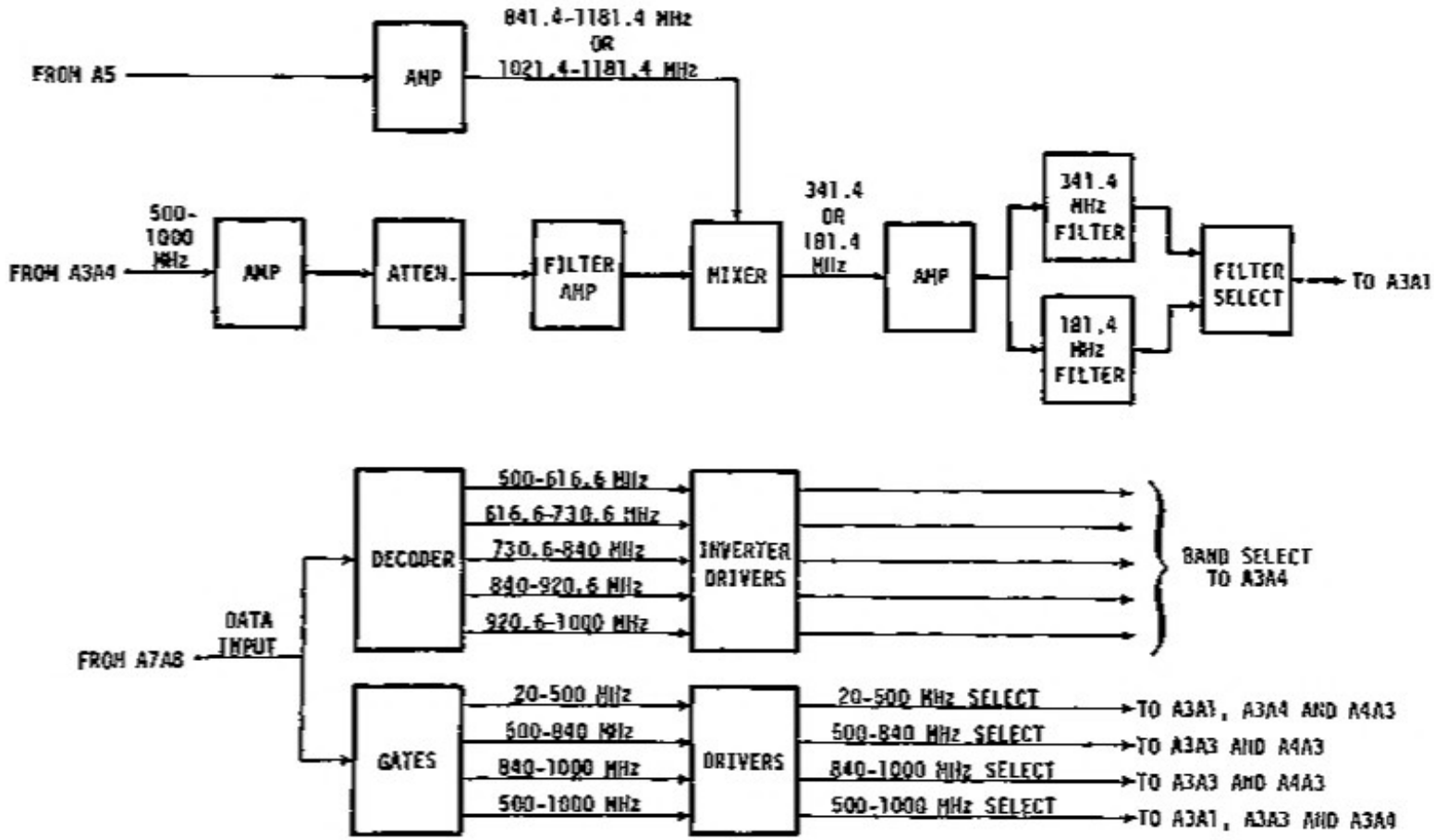


Figure 4-6. UHF Tuner and Decoder Driver (A3A3) Functional Block Diagram

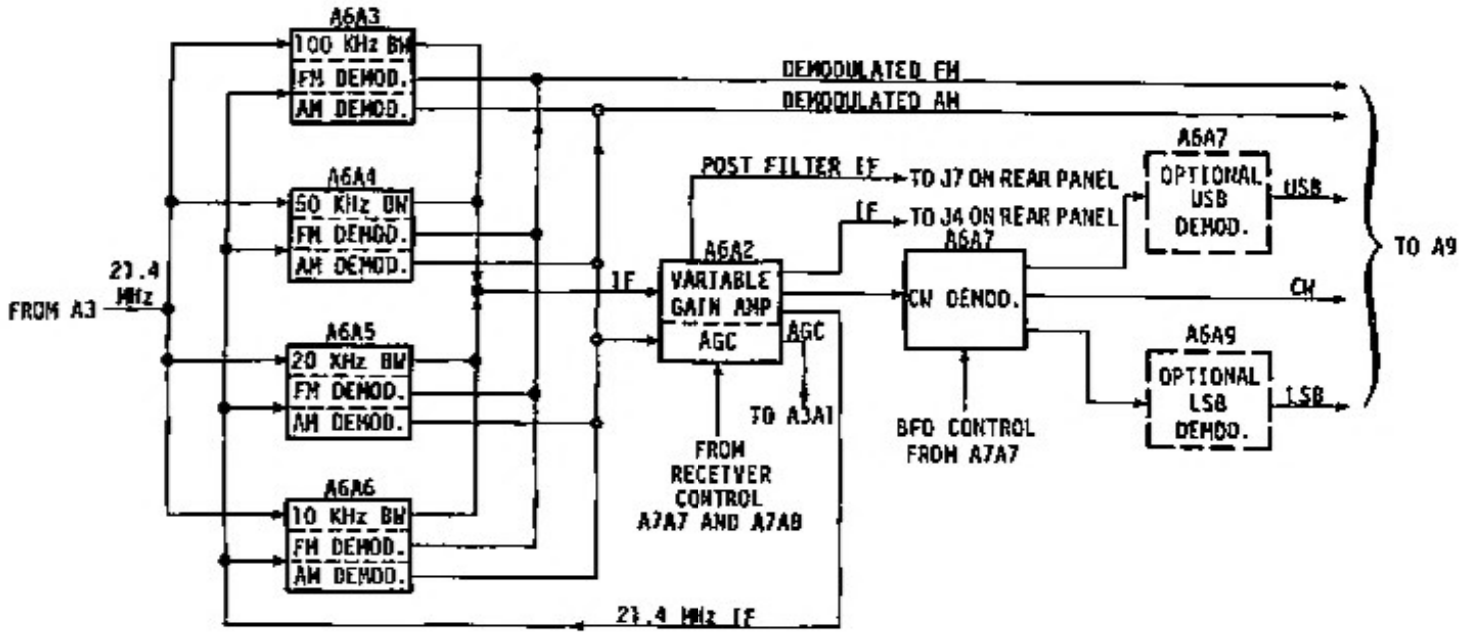


Figure 4-7. IF Assembly (A6) Functional Block Diagram

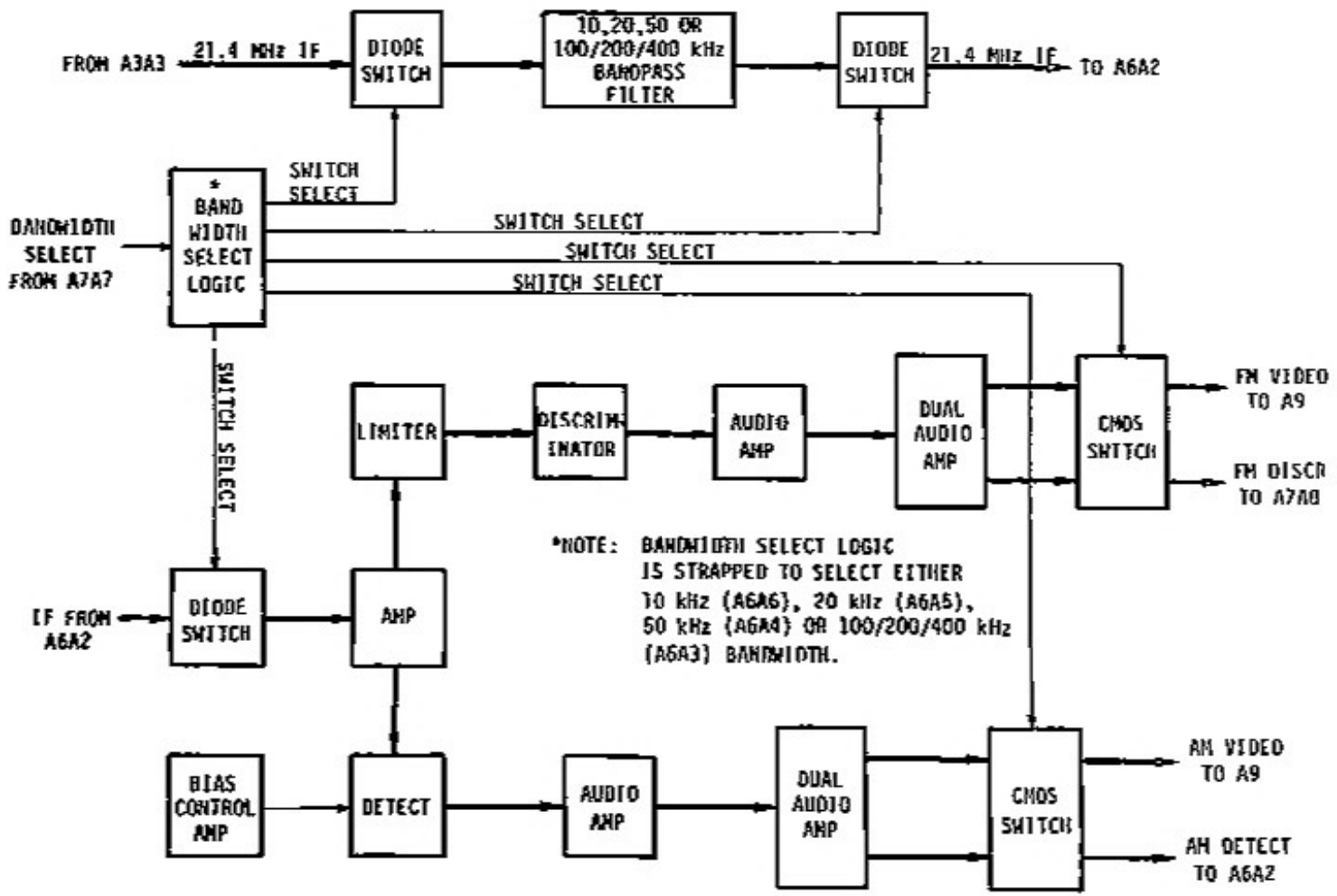


Figure 4-8. IF Filter Amplifier (A6A3-A6A6) Functional Block Diagram

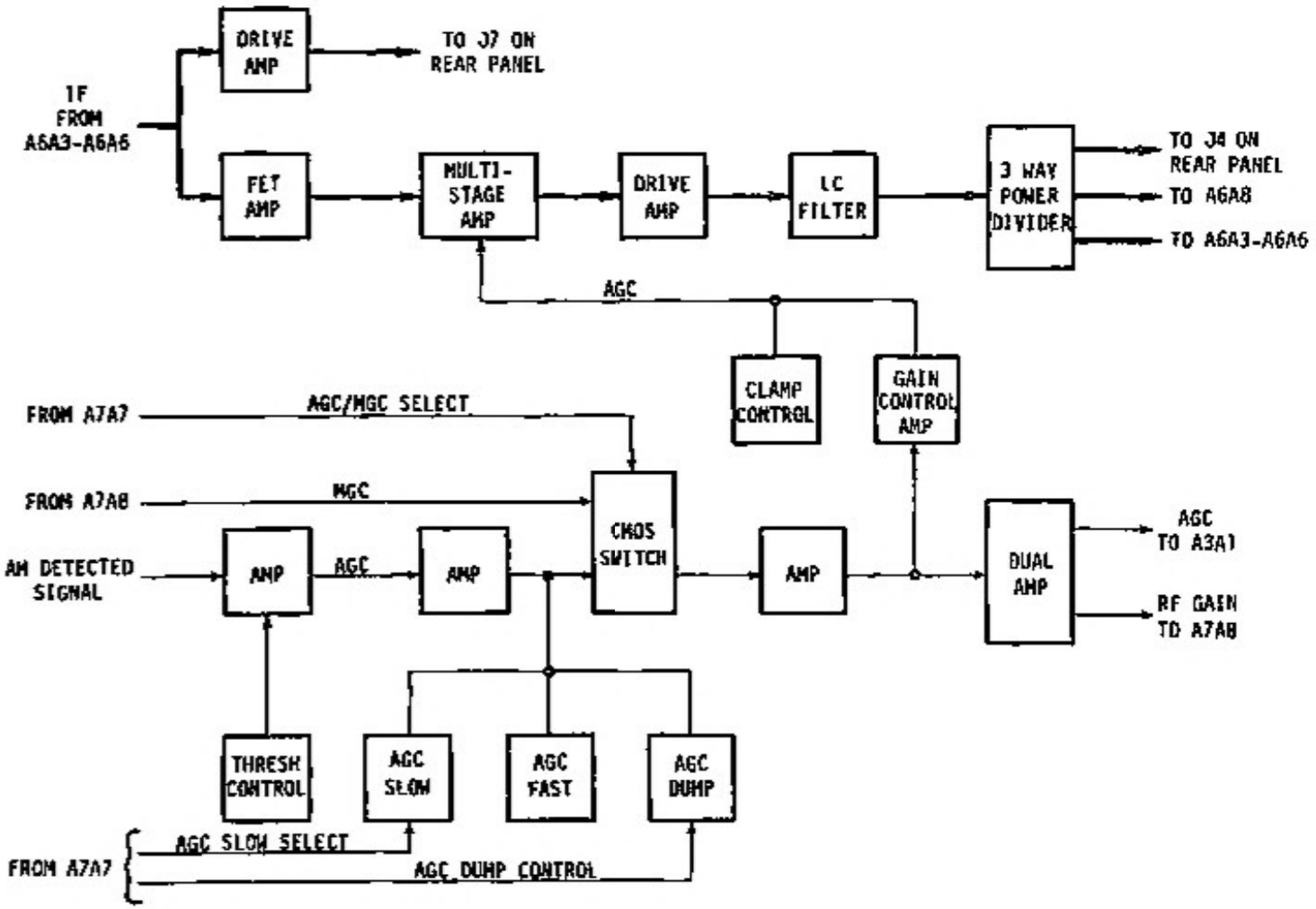


Figure 4-9. Variable Gain Amplifier (A6A2) Functional Block Diagram

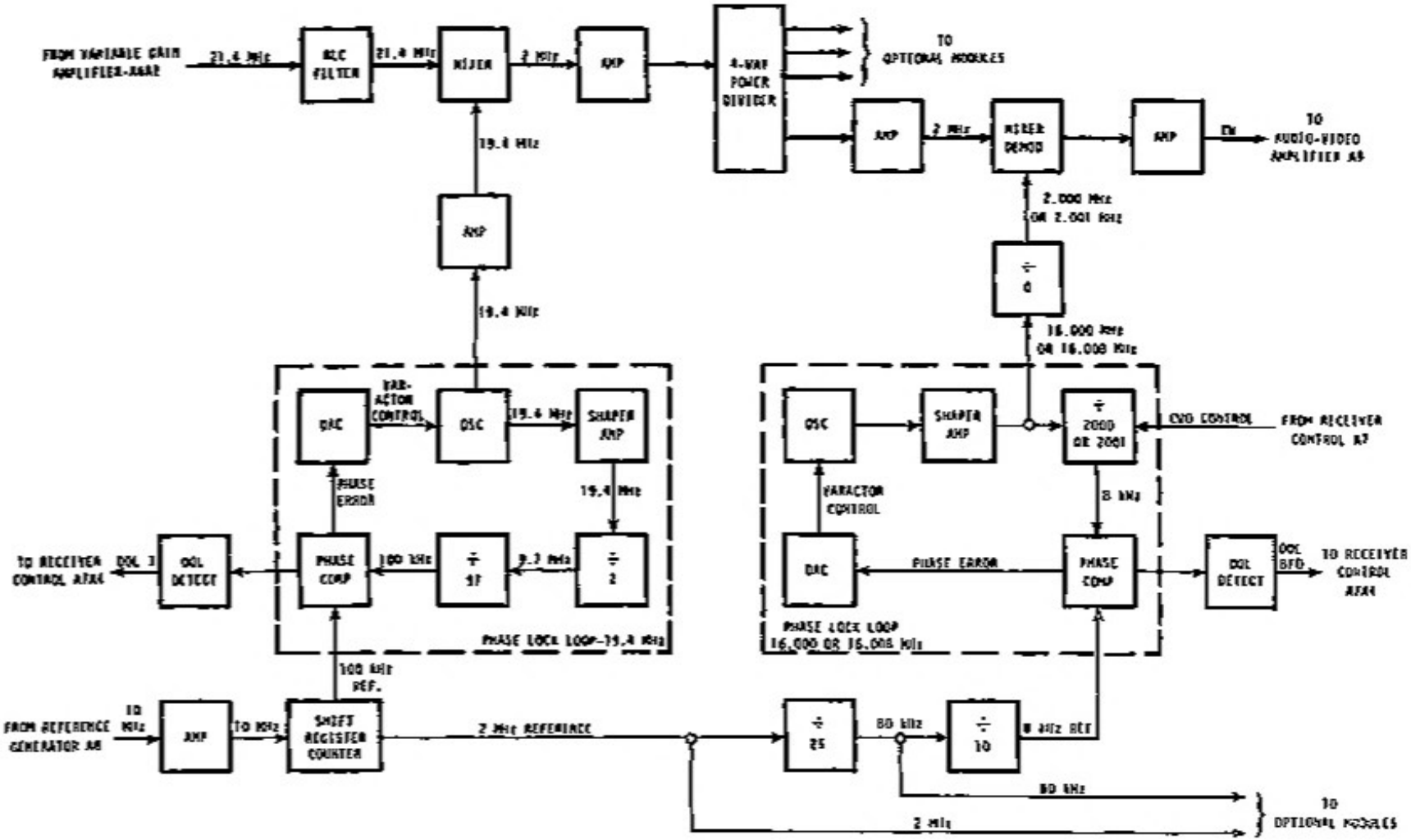


Figure 4-10. CW Demodulator (A6A8) Functional Block Diagram

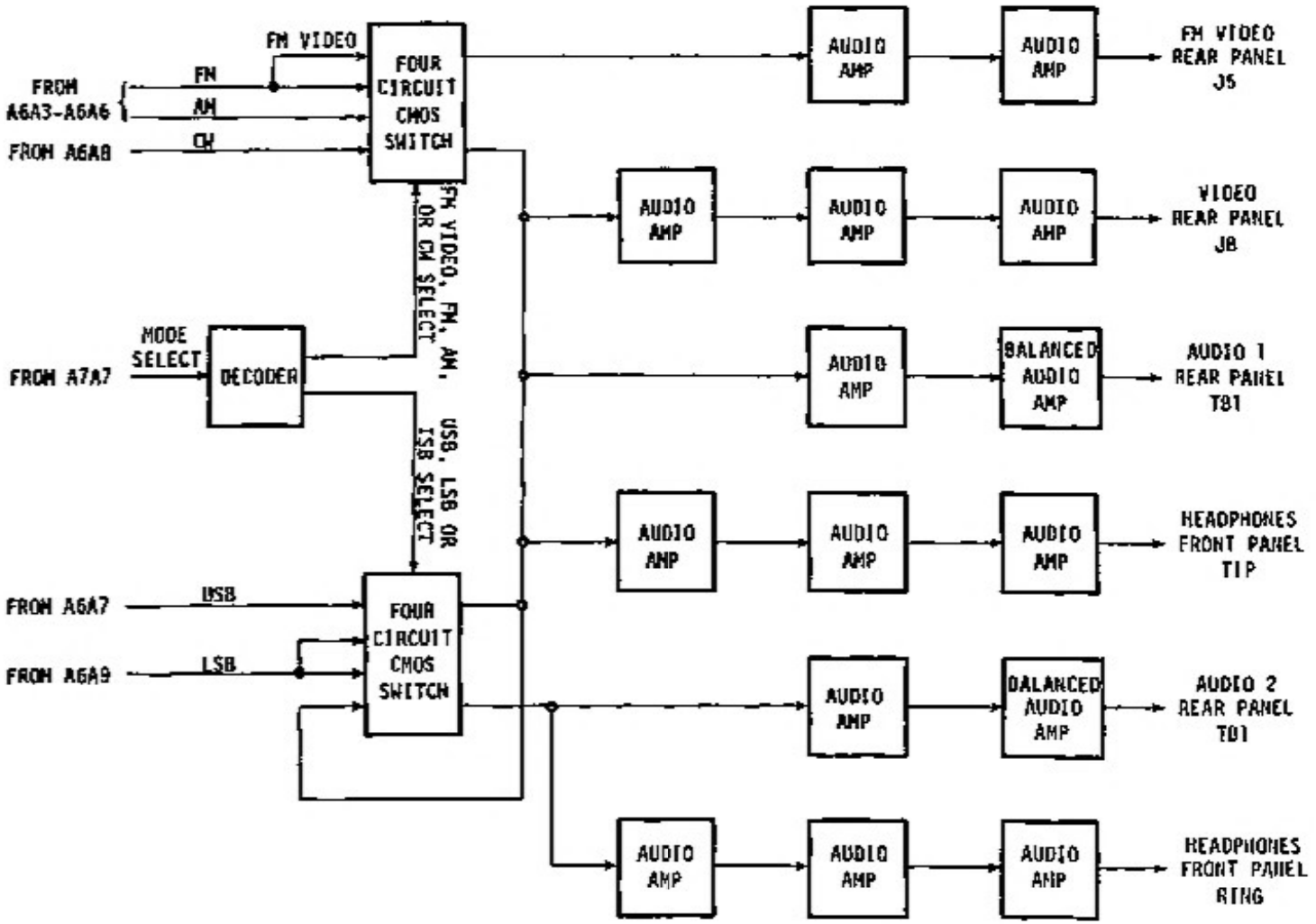


Figure 4-11. Audio Video Amplifier (A9A2) Functional Block Diagram

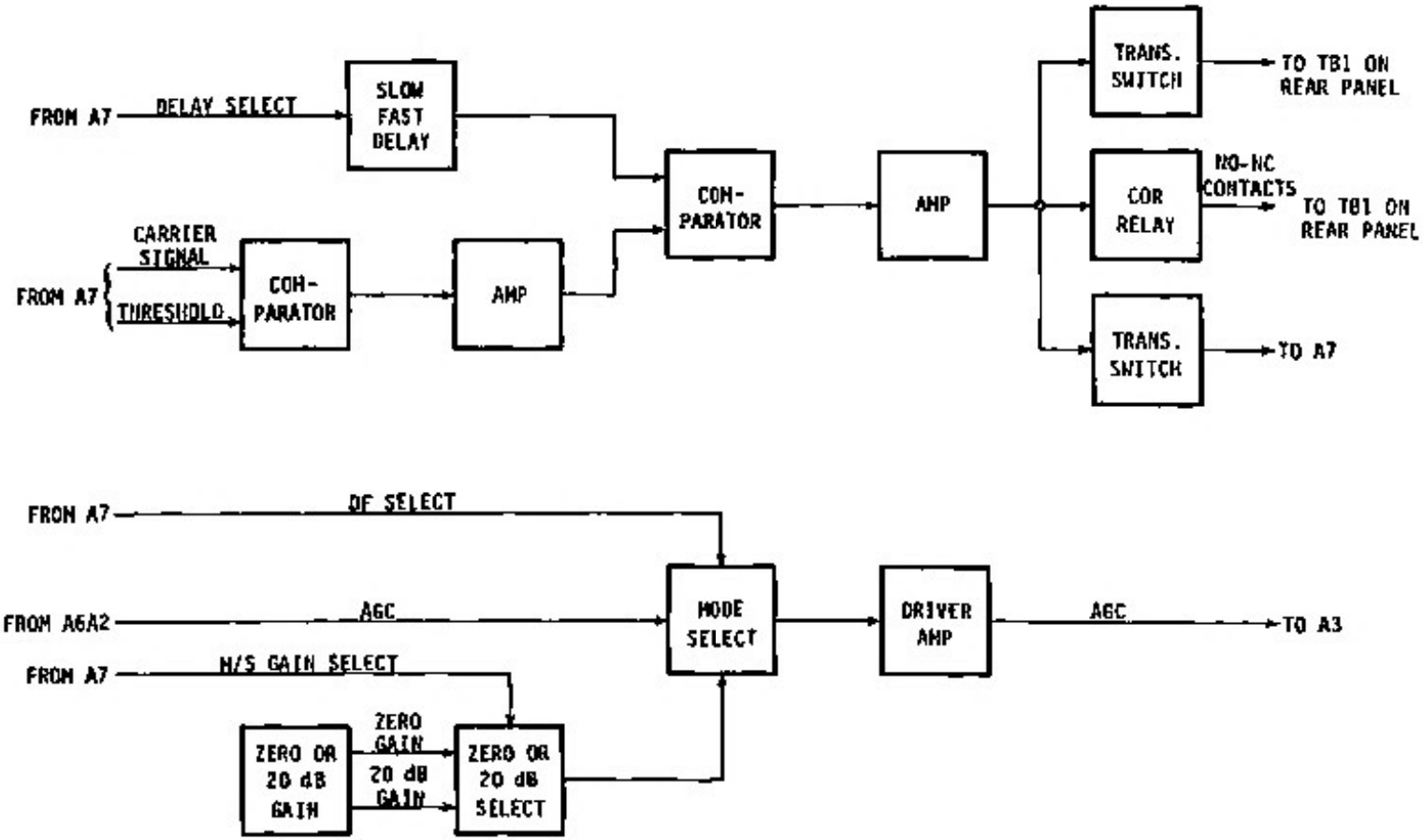


Figure 4-12. Carrier Operated Relay (A9A3) Functional Block Diagram

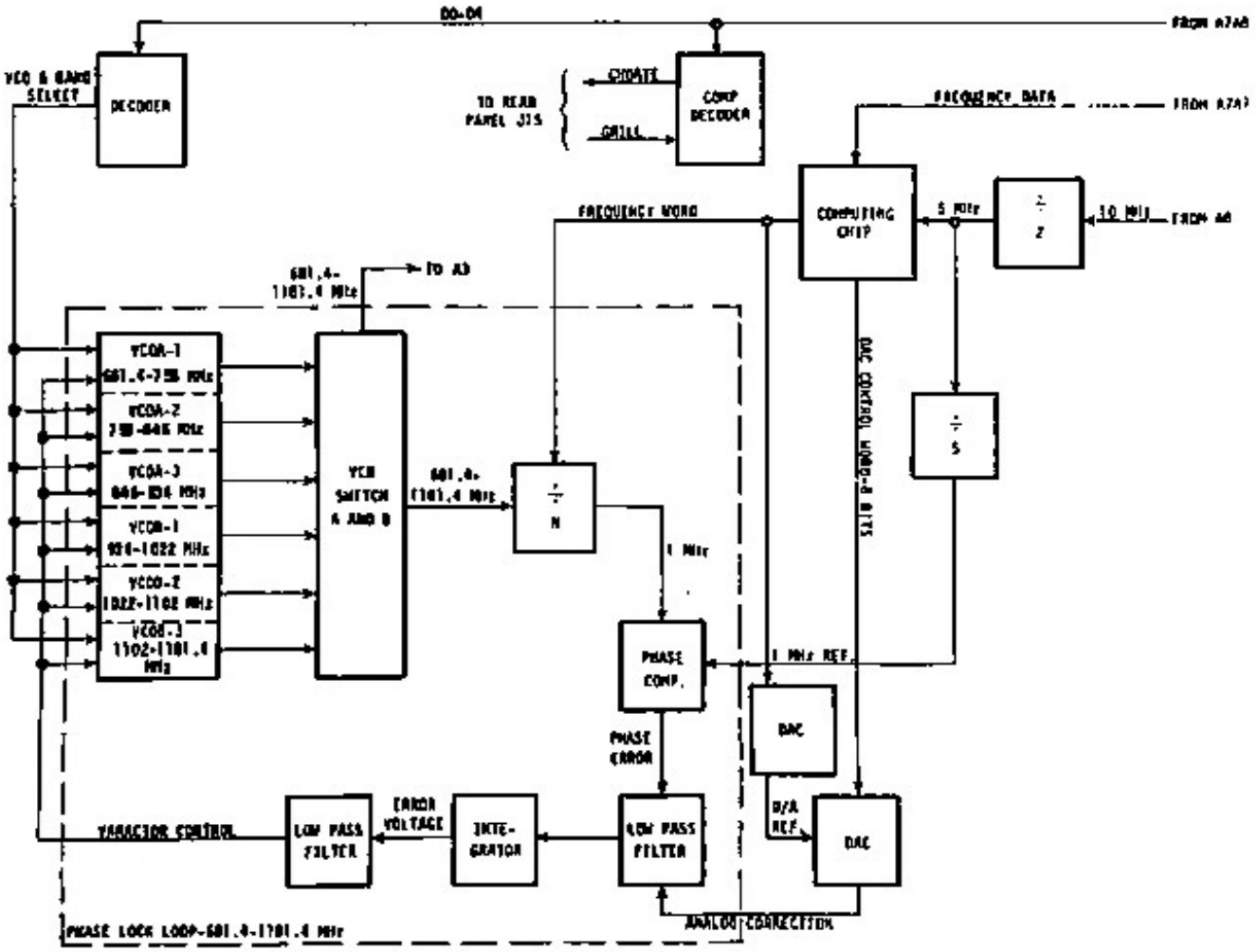


Figure 4-14. First LO Synthesizer (A5) Functional Block Diagram

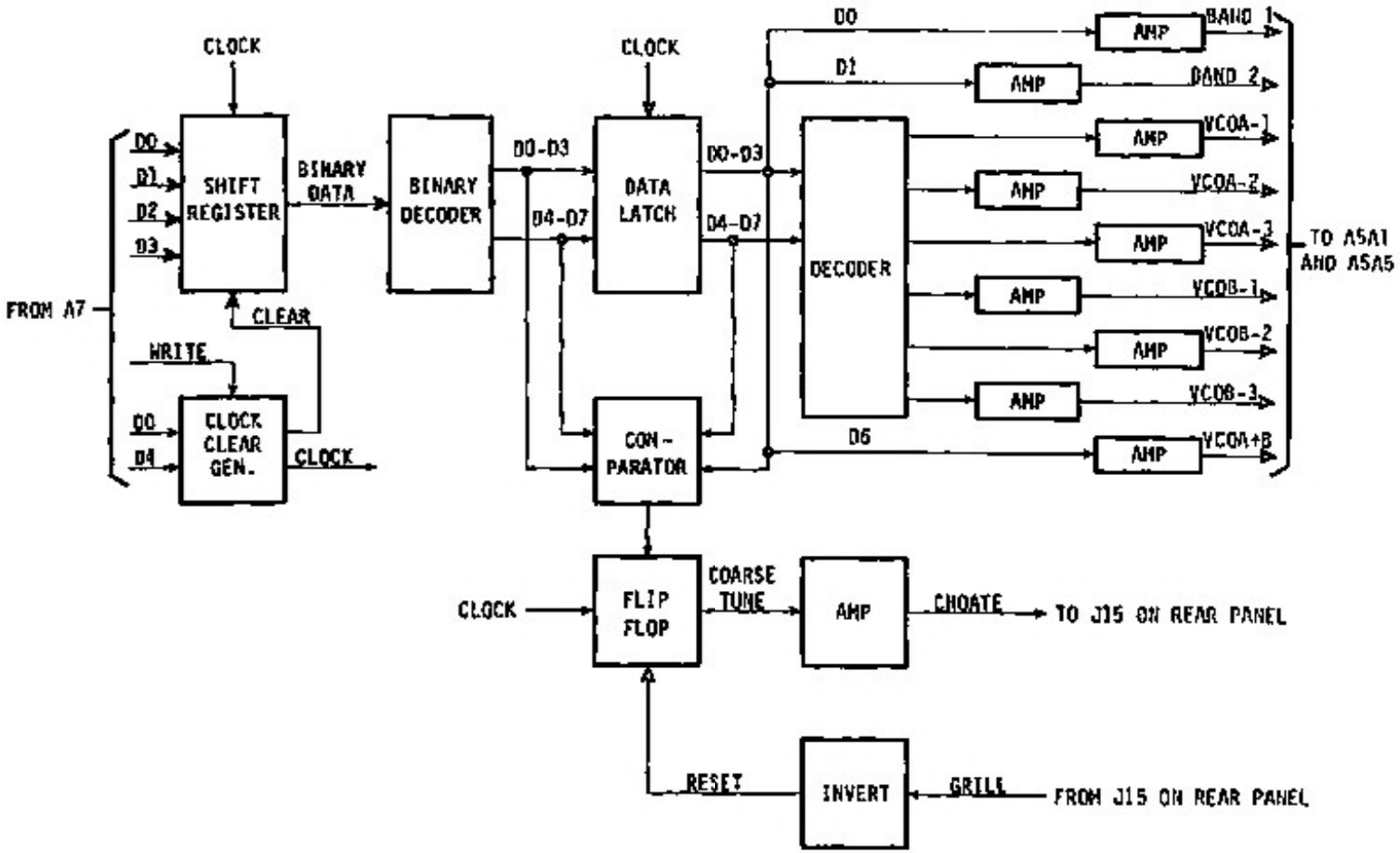


Figure 4-16. Controller (A5A2) Functional Block Diagram

Table 4-1. VCO Truth Table

BAND (MHZ)	VCO A 1 2 3	VCO B 1 2 3	BAND 1 2	VCO A&B	"N" INPUT 20 MHz DIV 8 2^3	DIV 7 2^2	DIV 6 2^1	DIV 5 2^0	200 MHz DIV 12 2^3	DIV 11 2^2	DIV 10 2^1	DIV 9 2^0
681.4 - 698	1 0 0	0 0 0	0 0	1	0	0	1	0	0	1	0	0
698 - 718	1 0 0	0 0 0	0 1	1	0	0	1	1	0	1	0	0
718 - 738	1 0 0	0 0 0	1 0	1	0	1	0	0	0	1	0	0
738 - 758	1 0 0	0 0 0	1 1	1	0	1	0	1	0	1	0	0
758 - 780	0 1 0	0 0 0	0 0	1	0	1	1	0	0	1	0	0
780 - 802	0 1 0	0 0 0	0 1	1	0	1	1	1	0	1	0	0
802 - 824	0 1 0	0 0 0	1 0	1	1	0	0	0	0	1	0	0
824 - 846	0 1 0	0 0 0	1 1	1	1	0	0	1	0	1	0	0
846 - 868	0 0 1	0 0 0	0 0	1	0	0	0	0	0	1	0	1
868 - 890	0 0 1	0 0 0	0 1	1	0	0	0	1	0	1	0	1
890 - 912	0 0 1	0 0 0	1 0	1	0	0	1	0	0	1	0	1
912 - 934	0 0 1	0 0 0	0 1	1	0	0	1	1	0	1	0	1
934 - 956	0 0 0	1 0 0	0 0	0	0	1	0	0	0	1	0	1
956 - 978	0 0 0	1 0 0	0 1	0	0	1	0	1	0	1	0	1
978 - 1000	0 0 0	1 0 0	1 0	0	0	1	1	0	0	1	0	1
1000 - 1022	0 0 0	1 0 0	1 1	0	0	1	1	1	0	1	0	1
1022 - 1042	0 0 0	0 1 0	0 0	0	1	0	0	0	0	1	0	1
1042 - 1062	0 0 0	0 1 0	0 1	0	1	0	0	1	0	1	0	1
1062 - 1082	0 0 0	0 1 0	1 0	0	0	0	0	0	0	1	1	0
1082 - 1102	0 0 0	0 1 0	1 1	0	0	0	0	1	0	1	1	0
1102 - 1122	0 0 0	0 0 1	0 0	0	0	0	1	0	0	1	1	0
1122 - 1142	0 0 0	0 0 1	0 1	0	0	1	1	1	0	1	1	0
1142 - 1162	0 0 0	0 0 1	1 0	0	0	1	0	0	0	1	1	0
1162 - 1181.4	0 0 0	0 0 1	1 1	0	0	1	0	1	0	1	1	0

NOTE: 1. VCO A1, A2, A3, B1, B2, B3 and VCO A&B:
+15 VDC @ 5 MA = LOGICAL 1
-15 VDC @ 5 MA = LOGICAL 0

2. BANDS 1 & 2:
+15 VDC @ 60 MA = LOGICAL 1
-15 VDC @ 60 MA = LOGICAL 0

3. "N" input data shown simulates BCD normally provided by the Programmable Divider (A5A4) as shown in Figure 7-18.

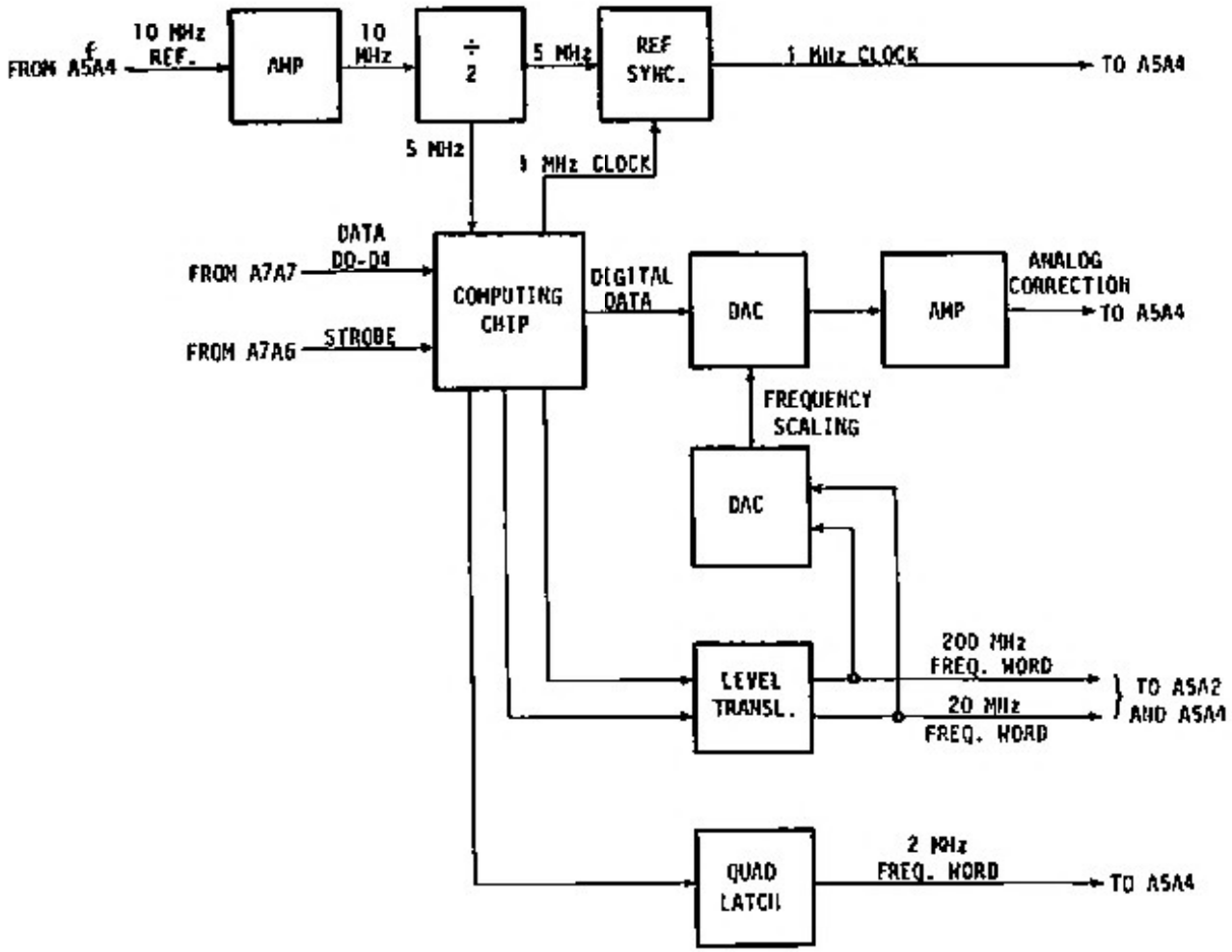


Figure 4-17. Digiphase Processor (A5A3) Functional Block Diagram

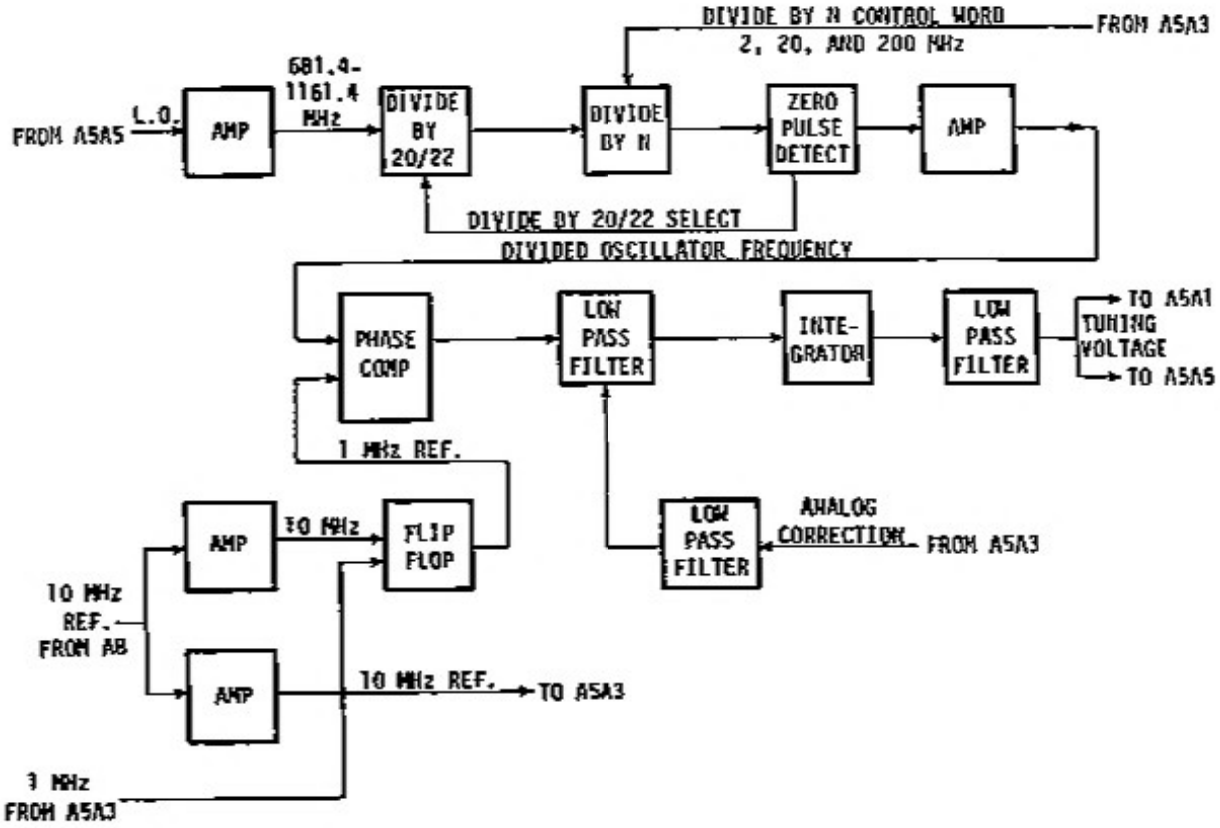


Figure 4-18. Programmable Divider (A5A4) Functional Block Diagram

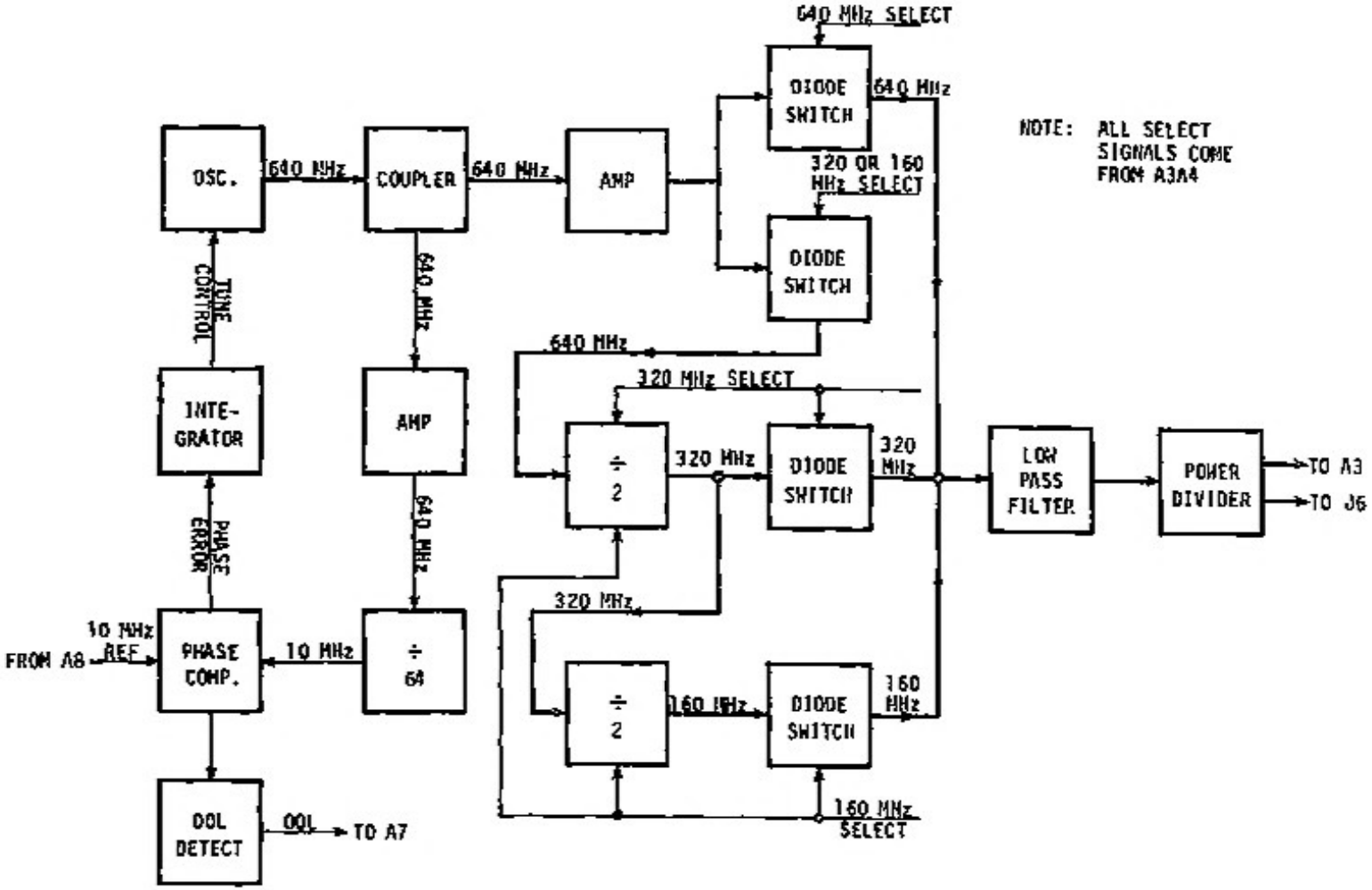


Figure 4-19. Second LO (A4) Functional Block Diagram

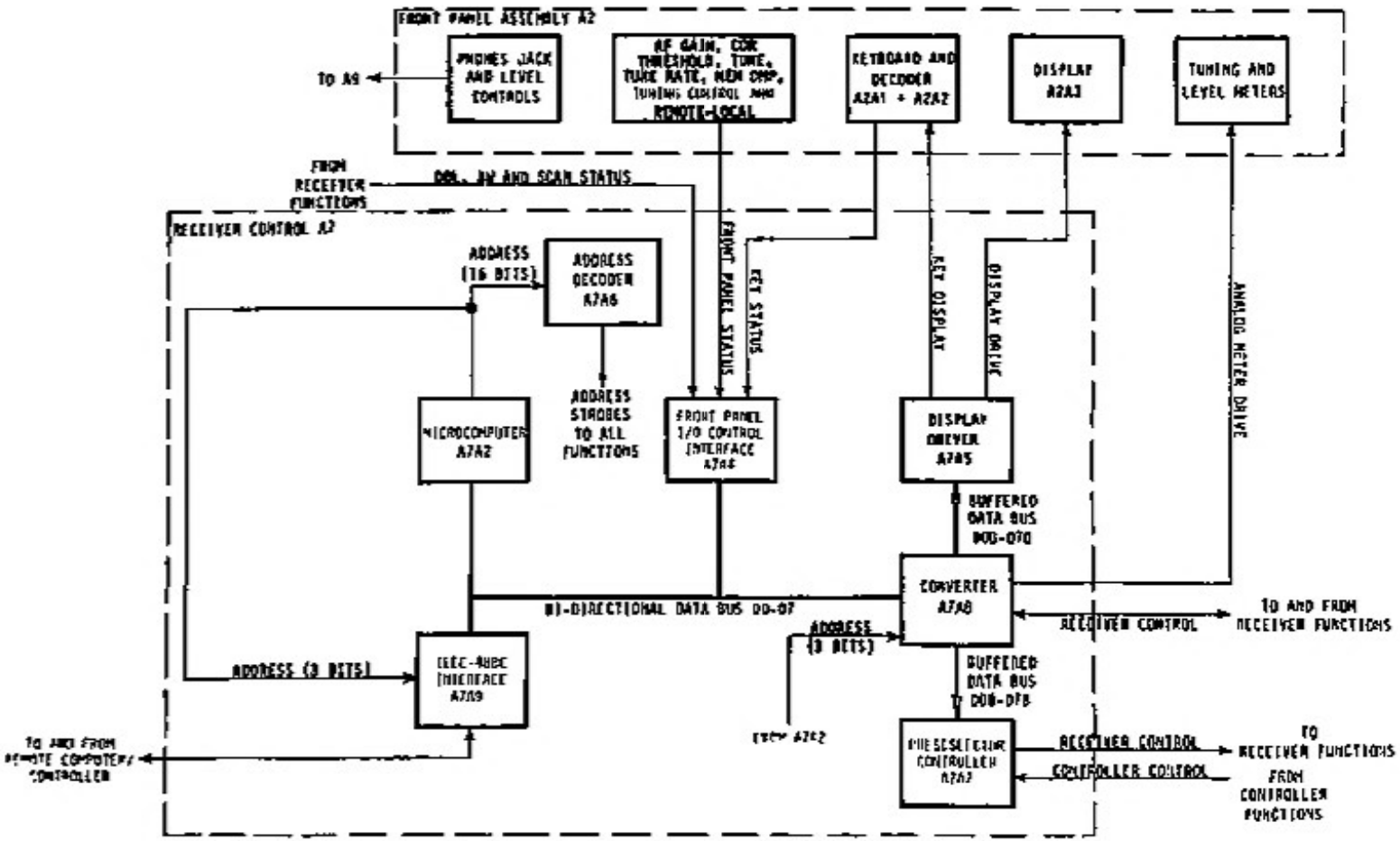


Figure 4-20. Receiver Control (A2 and A7) Overall Functional Block Diagram

the IEEE-488C remote control interface to the microcomputer, which processes the data and routes it to Receiver functions in the same manner as data received from the front panel. Receiver status information is sent to the remote computer/controller through the same interface upon request. When the Receiver is operated in the fast scan mode, through a Spectrum Surveillance Controller, control is effected through the receiver control output interface. A FAST SCAN strobe, from the Spectrum Surveillance Controller is routed to the microcomputer through the front panel I/O interface to override remote or local control of operation during this mode. RAM is used mainly for strobing up to 99 channels with full Receiver set up and up to 300 frequencies in the exclude frequency library. The ROM is used for microprocessor (CPU) program storage.

4-66. The microcomputer in conjunction with other receiver control circuits performs the following functions:

a. Initializes circuits upon application of power.

b. Retains Receiver operating parameters in memory during power off.

c. Determines priorities of command request.

d. Reads front panel commands in local mode of operation.

e. Reads remote computer controller commands in remote mode of operation.

f. Overrides remote/local control mode and reads commands from Spectrum Surveillance Controller in fast scan mode of operation.

g. Computes and directs Receiver operating parameters.

h. Updates front panel display in both remote and local modes.

i. Sends remote computer/controller Receiver status information upon request.

When power is turned on, the microcomputer starts the initialization process by executing the stored program. Initialization includes setting all circuitry to starting conditions and setting receiver controls and displays to values retained in memory. After initialization, the microcomputer operates a

continuous background program to monitor for out-of-lock conditions. During this background program, the microcomputer will respond to interrupt requests. The interrupt will request the microcomputer to stop the background program and service the interrupt. For example, for a change in a front panel setting in local control mode of operation, the interrupt service program reads the front panel settings, stores the latest settings in memory, computes the new Receiver parameter control data and sends this data to the appropriate Receiver circuits. After completion of the service program, the microcomputer returns to the background program or responds to the next interrupt. The interrupt requests (IRQ) serviced by the microcomputer, in their order of ascending priority, are:

a. IN0. Tuning Control. The tuning control is an optical encoder that generates two square wave outputs with a $\pm 90^{\circ}$ phase difference depending upon direction of rotation. When the shaft is rotated, the signal TNGWHL (IN0) is asserted to the priority interrupt controller (PIC), the processor will then examine the direction of rotation (D0) and the tuning speed (D1-D3) using strobe 1C18R. Using this data, it will increment or decrement the tuned frequency as required, reset the interrupt request using strobe 1C01W, and return.

b. IN1. Slew Switches. There are three slew switches: COR, RF, GAIN, and the tuning/MEMORY slew switch. Each of these switches will, when actuated, assert the signal SLWSWT (IN1) to the PIC. The processor will then read the data bus using strobe 1C1AR to determine which direction. It will then increment or decrement the indicated parameter as required and repoll the data bus to determine if the switch is still actuated. If the switch is still actuated, the process repeats; if not, the interrupt request is cleared using strobe 1C02W and the program returns.

c. IN2. Keyboard. When any pushbutton key-switch is pressed, the signal KBD (IN1) is asserted. The processor then reads the data bus, using strobe 1C19R, to determine which key was pressed. Depending upon which key was pressed and on the current operating status, the processor will perform the required function, clear the interrupt request using strobe 1C03W, and return.

d. IN3. Fast Scan (Optional). When an external Spectrum Surveillance Controller wishes to take control, it will assert the signal FSTSCN (IN3). The processor will light the FAST SCAN annunciator, blank the frequency display, zero the tuning and signal strength meters, set the gain mode to MGC, set the gain to 3/4 gain (64_h), and set the IF and LO multiplexer to external, using strobe 1C08 and data (FF_h). The processor will then poll the state of FSTSCN

using the 1C18R (D5). When FSTSCN is released by the Spectrum Surveillance Controller, the processor will restore the original operating conditions and return.

e. IN4. Remote/Local. Whenever the remote/local condition is changed, the signal REMLCL (IN4) is asserted. The processor will read the state of the remote line using strobe 1C18R (D4) and enter the appropriate program section (1 = Remote, 0 = Local).

f. IN5. Address Pass. When the IEEE-488C remote control interface (A7A9) receives a valid talk or listen address followed by a valid mnemonic, it will assert IN5. The processor will then read the interrupt status register in the 488 controller, clearing IN5, and take appropriate action. This IRQ is inhibited in the remote mode, and enabled in the local mode.

g. IN6. Display. A 500 Hz timer will assert IN6 approximately every 2 milliseconds. The processor will fetch the next display data from memory, erase the old display, display the new data and clear the interrupt request. The seven segment displays modules are commutated in pairs; IN6 is cleared by strobe 1C05W.

4-67. Microcomputer (A7A2). Figure 4-21 shows a functional block diagram of the microcomputer. The microcomputer contains a central processing unit (CPU), read only memory (ROM), random access memory (RAM), priority interrupt controller (PIC), memory retention and reset circuitry, a clock, and in and out gates. The CPU (processor) directs operations in accordance with the program sequences permanently stored in ROM, while RAM is used for temporary data storage during processing. The CPU reads from, or writes to, the other units of the digital control during programmed sequences. This is done through the bi-directional 8-bit data bus (D0-D7), by addressing the appropriate circuits through the 16-bit address bus (A0-A15), and the address decoded strobes from the address decoder (A7A6). At power turn on, a $\overline{\text{RESET}}$ is applied to the CPU. This causes the CPU to go to FFFEH and get the starting address in the ROM where the initialization program sequence starts. The ROM supplies instructions to the CPU to carry out the initialization sequence. When the sequence is completed, the CPU then goes to its background program and will now respond to the interrupt request (IRQ) received from the PIC. The PIC receives the seven interrupt reqeusts IRQ 0-6, as shown in Figure 4-21. When any of these requests are made, the PIC sends the IRQ to the CPU. When the CPU is ready to receive the interrupt

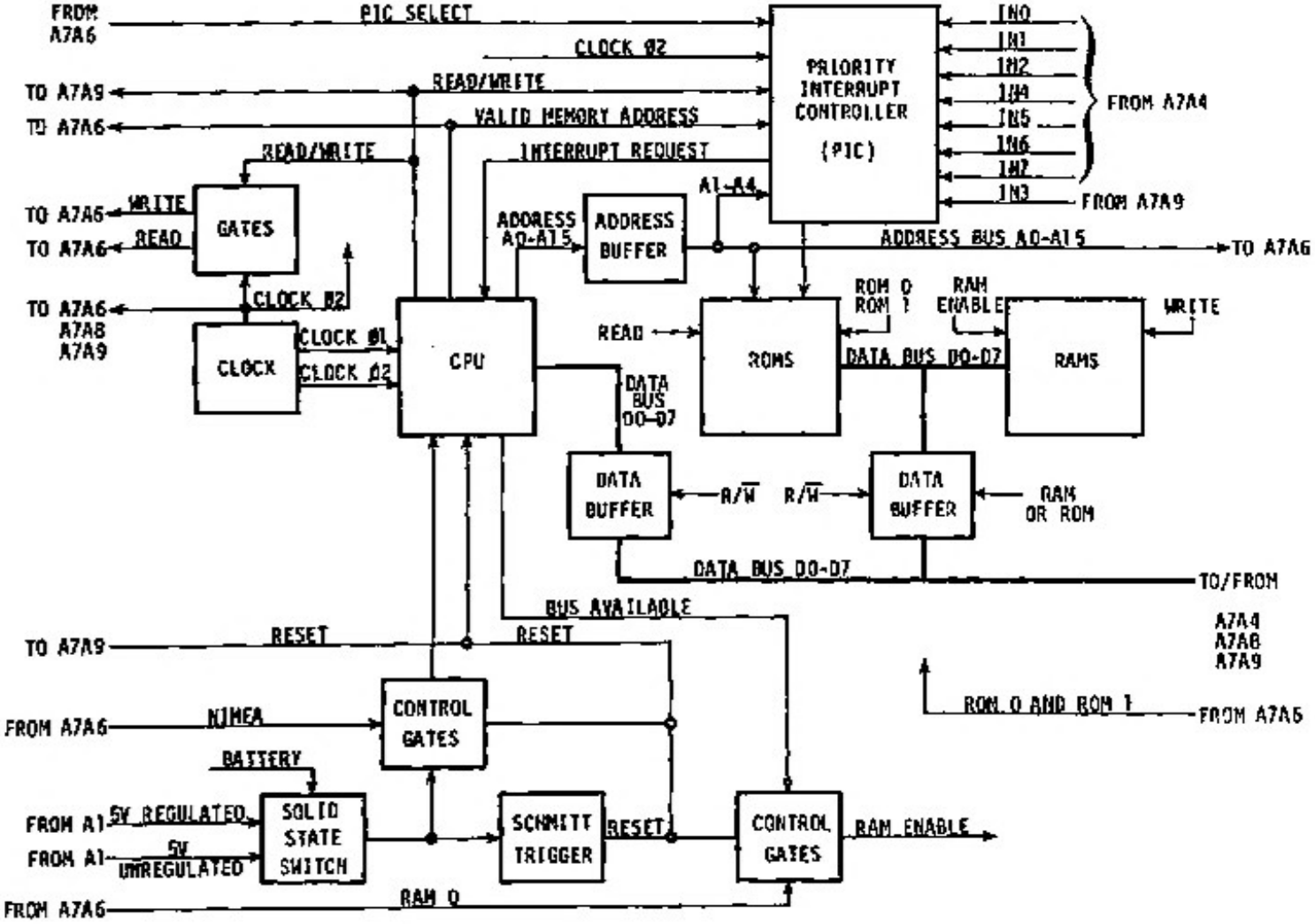


Figure 4-21. Microcomputer (A7A2) Functional Block Diagram

request, the PIC is allowed to place the starting program address of the highest priority interrupt request on the address bus. This address is the starting address of the interrupt servicing sequence stored in ROM. Thus, the CPU receives the instructions from the ROM to carry out the interrupt service routine. At power turn-off, the non-maskable interrupt ($\overline{NMI}$) is sent to the CPU which causes it to go into its power down sequence. This also causes the RAM to operate in a very low power drain state although still capable of retaining memory. The stand-by battery supplies power to the RAM while external power is off and is charged when external power is supplied.

4-68. Figure 7-25 shows the schematic diagram of the microcomputer. Data flow in and out of the CPU (U5) is accomplished through the 8-bit bi-directional data bus (D0-D7), while CPU commands to all functions are accomplished through the 16 bit-address bus (A0-A15), read write ($R/\overline{W}$) strobe, valid memory address (VMA) strobe, and bus available (BA) strobe. CPU timing is achieved through clock signals (Ø1 and Ø2) from clock U1. The CPU receives an interrupt request from the PIC (U5) which determines priorities from its seven interrupt requests. PIC is selected in program sequence from CPU addresses through the address decoder (A7A6). The PIC also routes address lines A1-A4 to the appropriate ROM area which then outputs its stored data onto the data bus. All address lines are connected from the CPU through non-inverting buffers U16 and U17 to various Receiver circuits. The ROM (U9 and U12) each hold up to 8 K times 8-bit words, and contains the program memory, while the RAM (U7, U10, and U11) can contain up to 6 K times 8-bit words of working memory. Both the ROM and RAM are enabled from decoded addresses and read and write strobes. VMA from the CPU strobes both the PIC and memory enable in timed sequence with CPU clock Ø2. The read strobe is obtaned from the CPU-$R/\overline{W}$ strobe, timed through NAND gate (U4) by clock Ø2. The write strobe is obtained in the same manner as the read strobe except the $R/\overline{W}$ strobe is inverted by U13 before being clocked through its NAND gate U4. This strobe is used to enable the RAM. The read and write strobes are also routed to the address decoder while the CPU $R/\overline{W}$ strobe is routed to the IEEE-488C remote control interface (A7A9). Data bus lines to and from the CPU are buffered through non-inverting transceiver U6. Data from the CPU, ROMS, RAMS, the front panel I/O control interface (A7A4), the converter (A7A8), and the IEEE-488C remote control interface (A7A9) are strobed onto the data bus in program sequence by the decoded address signals, while data on the data bus is strobed, also in program sequence, to the CPU, RAM and the converter and IEEE-488C remote control interface. This data is further processed and routed to the appropriate Receiver functions.

4-69. The microcomputer also contains a memory retention and reset circuit, to retain memory in the otherwise volatile memory of the RAM, and to provide a reset signal to the CPU and to the IEEE-488C remote control interface when power is turned on. At power on, C2 will begin to charge though R1. The charge time of capacitor C2 assures that the +5 V supply will stabilize throughout the microcomputer circuitry, and U1 is working for at least eight clock cycles. When C2 is charged to a CMOS high level, then U15 pin 9 will go high, causing U3 pin 5 to release the reset and actuate the microcomputer initialization routine to start program operations. The reset line also sets U15 pin 6 to a low level to enable the RAMS. In the initialization routine, signal NMIENA is strobed low and sets U3 pin 8 to a high level. This allows U14 to monitor the unregulated +5 V for a power interruption. When power is interrupted, the output of U14 will go high and be inverted by U4, and will give the CPU a non-maskable interrupt ($\overline{\text{NMI}}$). This will cause the CPU to go into its power down program, and put all variables away into the RAMS. The CPU will then go into a wait state, causing a bus available signal (BA) to be supplied by the CPU and set U15 pin 6 to a high level, thus disabling the RAMS. When power is down, Q1 will relinquish the control of power from the RAMS to the battery BT1.

4-70. All data temporarily stored in the RAMS may be cleared in an emergency (channel memory). This can be accomplished by pulling out on the POWER PUSH/ON switch located on the front panel. The receiver can be reinitialized to default parameters by turning it off and then back on.

4-71. Address Decoder (A7A6). Figure 4-22 shows a functional block diagram of the address decoder and Figure 7-28 shows the associated schematic diagram. The address decoder receives addresses from the microcomputer on the 16-bit address bus, the valid memory address (VMA) signal, read and write strobes, and clock Ø1 signal. The address decoder decodes and clocks through these addresses to provide; strobes for ROM and RAM enable, PIC select, and non-maskable interrupt enable ($\overline{\text{NMIENA}}$) to the microcomputer; an analog-to-digital converter select ($\overline{\text{ADCST}}$) strobe to the converter (A7A8); a remote select ($\overline{\text{REMSL}}$) to the IEEE-488C remote control interface (A7A9); write strobes to the front panel I/O control interface (A7A4), the display driver (A7A5), the preselector controller (A7A7), and the converter (A7A8); and, read strobes to the front panel I/O control interface and converter. All strobes are generated through decoder demultiplexers and gates that output the strobes in timed sequence with placement of the corresponding address on the address lines, VMA enable, and clock Ø2 from the CPU.

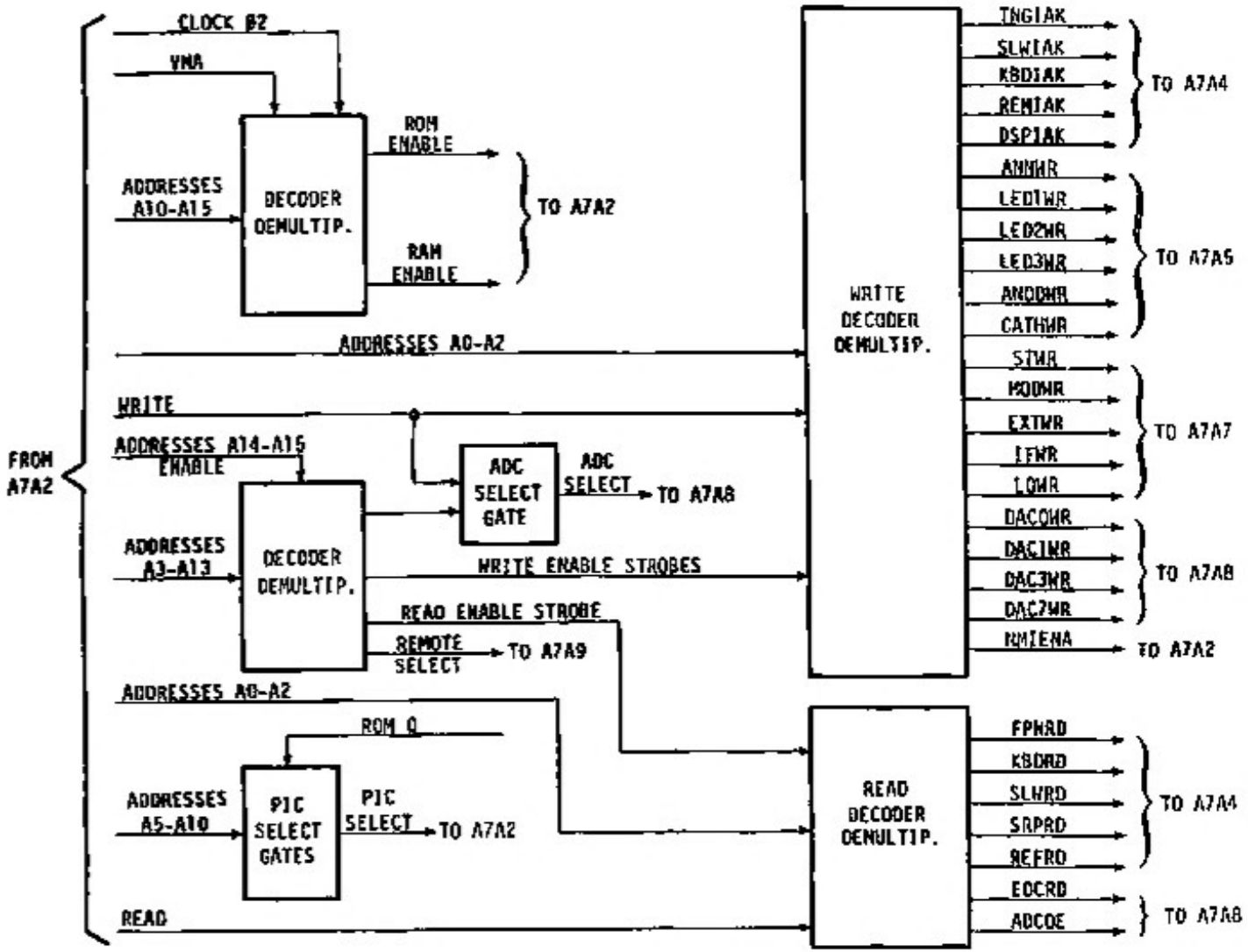


Figure 4-22. Address Decoder (A7A6) Functional Block Diagram

4-72. Front Panel I/O Control Interface (A7A4) and Assembly (A2). Figure 4-23 shows a functional block diagram of the front panel I/O control interface and front panel assembly. All inputs from the front panel assembly except the phones jack and associated level control, are routed through the front panel I/O control interface to the microcomputer data bus. The only data routed to the front panel assembly is the analog drive, from the converter (A7A8) for tuning and level meters, and the display drives, from the display driver (A7A5) for the front panel displays (see paragraph 4-75).

4-73. The front panel keyboard (A2A1) (Figure 7-3) contains 36 pushbutton key-switches which are routed to five 8-input priority encoders (U1-U5) (See Figure 7-4). The three normal outputs of these five encoders are connected in parallel to form the coded key outputs K0 to K2. The G5 output of each of the five encoders are routed to five inputs of the sixth priority encoder whose three normal outputs form the coded key outputs K3 to K5. Outputs K0 to K5 form a two digit octal code (K0-K2 = LSC, K3-K5 = MSD) that is used by the microcomputer to identify the specific pushbutton key-switch depressed. The G5 output of this encoder forms an interrupt request ($\overline{IRQ}$) which is routed to the front panel I/O control interface (Figure 7-26) and is used to clock data flip flop U8A. When clocked, the Q output of U8A goes low and sends IRQ level 2 ($\overline{IRQ2}$) to the PIC. Upon receipt of the interrupt request, the microcomputer asserts $\overline{KBORD}$ then reads the two digit octal code, as set-up by the depressed pushbutton key-switch, on data lines through buffer U3. The microcomputer then sets $\overline{KBDIAK}$ which resets the Q output of U8A ($\overline{KBD}$) high; thus, removing the interrupt request $\overline{IRQ2}$. Timer U4 provides a timed interrupt ($\overline{IRQ6}$) approximately every 2 milliseconds through flip flop U16A-U16B by setting $\overline{DSPLY}$ low. The microcomputer reads the displays on each request and asserts DSPIAK each time to reset the flip flop. Flip flop U16C-U16D is used to clear RAM memory. The $\overline{CLR}$ input to the flip flop is made low by pulling out on the POWER ON/OFF switch located on the front panel. This asserts MEMCLR ($\overline{IRQ7}$). The microcomputer then clears the RAM memory and resets flip flop U16C-U16D through CLRIAK.

4-74. The remote or local control mode of operation is determined by flip-flop U9C-U9D (Figure 7-26) which routes its status to the clock input of U8B. The $\overline{Q}$ output of U8B represents the remote control mode and is routed to a three state buffer U58, and to the clock input to data flip-flop U10B. The local status from the Q output of U8B is routed to the clock input of U10A. The inputs of RS

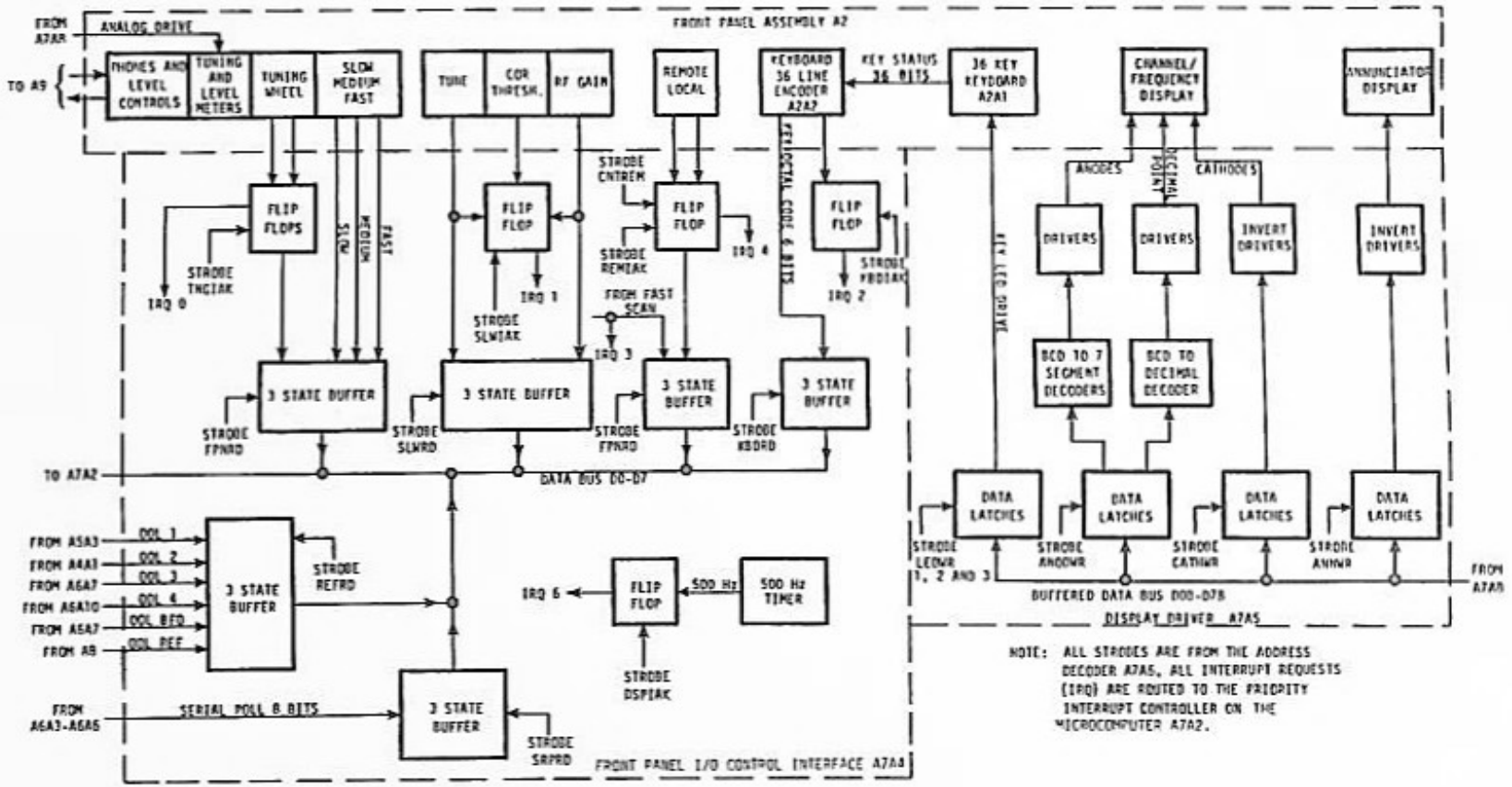


Figure 4-23. Front Panel Assembly (A2) and I/O Control Interface (A7A4) and Display Driver (A7A5) Functional Block Diagram

flip flop U9C-U9D are connected to the normally open (LOCAL) and normally closed (REMOTE) contacts of the REMOTE switch (S1), located on the front panel. The reset of data flip flop U8B is controlled by a remote computer/controller (CNTREM) through inverter U15D while its set input is controlled by control clear (CNTCLR) through NAND gate U9B. When there is no request for remote control from a remote computer/controller or fast scan, flip flop U8B can be toggled between its Q (clock high-local) and $\overline{Q}$ (clock low-remote) outputs with the front panel REMOTE switch through RS flip flop U9C-U9D. The Q output U8B (local) is connected to data flip flop U10A while its $\overline{Q}$ output (remote) is connected to data flip flop U10B. The outputs of these flip flops, coupled through NOR gate U11A, provide an interrupt (IRQ4) through REMLCL when the REMOTE switch is toggled between remote and local, or between local and remote. Upon receipt of the interrupt request, the microcomputer sets FPNRD low, which permits it to read data lines D4 and D5, connected to the output of buffer U5B. If the REMOTE switch is set for remote control operation, the Q output of U8B connected to the input of U5B will be high, causing data line D4 to be high. If the REMOTE switch is set for local control, data line D4 will be low. In the remote mode, the $\overline{Q}$ output of U8B also drives transistor Q1 to light LED DS1 in the front panel REMOTE switch. After the microcomputer determines remote/local status, it responds by setting REMIAK low, which resets U10A and U10B through inverter U15C, removing the interrupt through REMLCL. If a remote computer/controller requests remote operation through CNTREM, the reset input to U8B is held high which prevents the clock input to U8B (from the REMOTE switch) from toggling the flip flop out of its remote conditon. When the CNTCLR goes low, it provides a high to the set input of U8B, through NAND gate U9B, which sets the flip flop to the local condition. If an optional Spectrum Surveillance Controller is connected to the Receiver it provides a low to the input of buffer U5B through FSTSCN. This causes data line D5 to be low which is read along with data line D4 (remote/local status) when the microcomputer responds to the REMLCL interrupt (IRQ4). When the microcomputer determines that a Spectrum Surveillance Controller is present it overrides any remote/local requests from the front panel or a remote computer/controller and turns control over to the Spectrum Surveillance Controller.

4-75. The status of TUNE, COR THRESHOLD and RF GAIN controls is strobed onto the data bus through buffers U1 and U2B (Figure 7-26) by strobe SLWRD, while its IRQ1 is developed through AND gates U12A, U12B and U12C and flip-flop U7-U9A.

When any control is depressed, up or down, the output ($\overline{SLWSWT}$) of flip flop U7-U9A is set low which asserts an interrupt ($\overline{IRQ1}$) to the PIC. The microcomputer responds by setting $\overline{SLWRD}$, to buffers U1 and U2B low, and reading outputs D1-D7, to determine which switch was asserted and whether it was up or down. Program control assigns priority to the switches as follows: S3U, S3D, S2U, S2D, S1U, S1D. Switch S4 is not used in the Receiver. When more than one switch is depressed, the one with the highest priority is recognized and the others ignored. After determining which switch was depressed, the microcomputer causes $\overline{SLWIAK}$ to be set low, which resets flip flop U7-U9A, and causes $\overline{SLWSWT}$ to return to the high state removing the interrupt to the PIC. The tuning control operates through flip flops U6A and U6B and buffer U5A. The two outputs (A and B) of the tuning control are two identical square waves, 180 degrees out of phase, with frequency determined by the rate at which the control is turned. When turned clockwise (increase frequency), pulse A leads pulse B, when turned counter clockwise, pulse B leads pulse A. The A output is connected to the data input of flip flop U6A, while the B output is connected to the clock inputs of U6A and U6B. Each time the B pulse goes high the Q output ($\overline{TNGWHL}$) goes low sending an interrupt ($\overline{IRQ0}$) to the PIC. The microcomputer then reads data lines D0-D3, whose condition is controlled by buffer U5A, by setting $\overline{FPNRD}$ low. When pulse A leads pulse B (clockwise rotation), the Q output of U6A is always high, but when pulse B leads pulse A (counter-clockwise rotation), the same output is always low. The microcomputer then determines direction of rotation by the high or low condition of data lines D0. Front panel TUNING rate switches (SLOW, MEDIUM and FAST), control data lines D1-D3 through buffer U5A. These data lines set the frequency digit to be changed by the tuning control; SLOW (data line D1 low) controls the tens digit; MEDIUM (data line D2 low) controls the 1 K digit; FAST (data line D3 low) controls the 100 K digit. The rate at which the tuning control changes any one of these digits is determined by the rate that pulse B (tuning control rate) sends an interrupt to the PIC through flip flop U6B. The microcomputer resets flip flop U6B after each B pulse by asserting $\overline{TNGIAK}$ through inverter U15E.

4-76. Display Driver (A7A5). Figure 4-23 shows a functional block diagram of the display drivers and the front panel displays (A2A3). The display drivers are used to drive the front panel displays which consist of a nine digit, seven segment LED frequency readout, a two digit channel memory readout, five anunciators, and LED indicators of the pushbutton key-switches. Data from the

buffered data bus D0B and D7B (Figure 7-28) is latched through three data latches (U15-U17), in program sequence, by LED write strobes LEDWR1, LEDWR2, and LEDWR3. The output of the latch is routed through an inverter driver to drive the appropriate key-switch LED. The buffered data bus is also strobed through data latch U1, by ANODWR, and routed to two 7-segment decoders (U2 and U3), and to decimal point decoder U4 through NAND gates U27A - U27D. The seven segment decoders drive the frequency display LED anodes through transistor drivers Q1 - Q14. The decimal point decoder drives the display decimal points through transistor drivers Q15 - Q23. Another data latch U11, strobed by CATHWR, routes the latched data through inverter drivers U12 and U13 to the cathodes of the display. The five annunciators are driven from data on the buffered data bus, which is latched through data latch U18 by strobe ANNWR. The latched data is routed through inverter drivers on integrated chip U22.

4-77. Converter (A7A8). Figure 4-24 shows a functional block diagram for the converter. The converter contains an analog -to-digital converter (ADC), to convert analog gain information from the Receiver to digital inputs for the microcomputer, and eight digital-to-analog converters (DAC), to convert digital gain, tuning and COR threshold data from the microcomputer to analog signals for various Receiver circuits. The ADC selects various analog inputs (as directed by the microprocessor addresses and strobes), converts them to digital words and places the digital words on the data bus at the appropriate times, by the strobes from the address decoder (A7A6). Figure 7-31 shows the schematic diagram for the converter. The data bus D0 to D7 is clocked through data latch U14, by inverted CPU clock Ø2, and becomes the buffered data bus D0B to D7B. This buffered data is used to drive the DACs and is also routed to the display driver (A7A5) and preselector controller (A7A7). Only five of the DACs outputs are used; DAC 0 (U13) to the level meter; DAC 1 (U12) to the tuning meter, DAC 2 (U11) for COR threshold; DAC 3 (U10) to manual gain control (MGC) on the variable gain amplifier (A6A2); and, DAC 7 (U6) to the Spectrum Surveillance Controller through rear panel FAST SCAN connector J15. Each DAC receives its eight bit digital data from the buffered data bus, in program sequence through strobes DAC 0 WR, DAC 1 WR, DAC 2 WR, DAC 3 WR, and DAC 7 WR respective to the DAC outputs. The output of each DAC is routed through a driver amplifier which drives the circuits as described above.

4-78. The converter also contains the analog-to-digital converter U15. The ADC receives eight separate analog inputs (ADC0-ADC7) and converts the selected

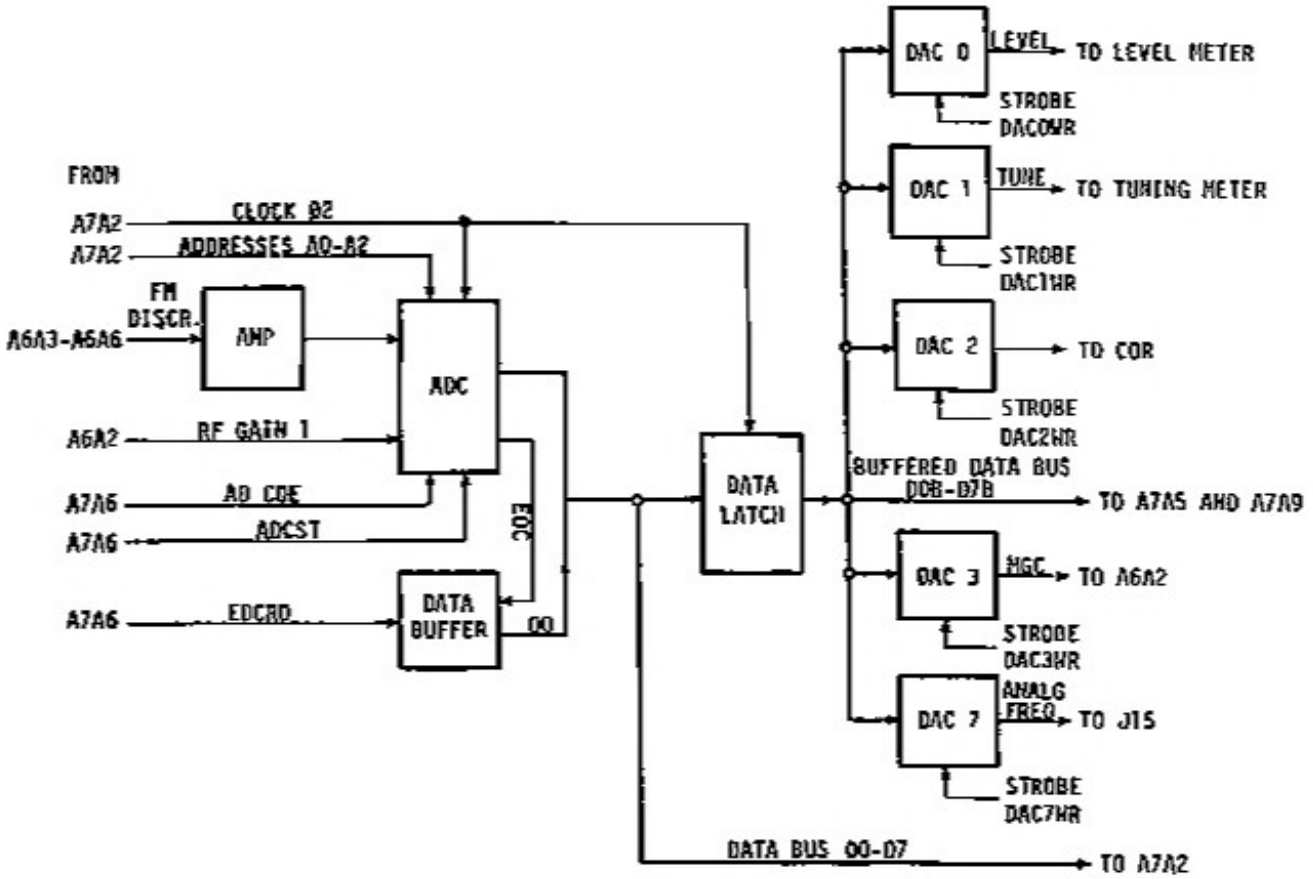


Figure 4-24. Converter (A7A8) Functional Block Diagram

inputs (one at a time in the program) to an 8-bit digital word, which is output on the data bus. The input to be converted is selected through the address lines A1-A2. The strobe signals $\overline{\text{ADCOE}}$ (enable), $\overline{\text{ADCST}}$ (conversion start) and $\overline{\text{EOCRD}}$ (end of conversion read) are supplied from the address decoder (A7A6). The conversion start signal ($\overline{\text{ADCST}}$) initiates the conversion of the selected inputs. The $\overline{\text{EOCRD}}$ strobe places the end-of-conversion (EOC) signal on the data bus line (D0) through three state buffer U16. The microcomputer will read the digital output after the conversion by asserting the enable $\overline{\text{ADCOE}}$. Only the ADC1 and ADC0 inputs to the ADC are used by the Receiver. ADC1 input, from the FM discriminator, is filtered by a unity gain, inverting, 10 Hz, low pass filter amplifier U5A, then given a +2.5 volt DC offset and further filtered by unity gain, inverting, 1 kHz low pass filter amplifier U5B. The output of U5B is a smoothed offset version of the discriminator output signal within the 0 to +5 volt range. The ADC0 input is RF gain 1 from variable gain amplifier (A6A2) and is an AM detected version of the IF amplifier output signal. The converter digital data from either of these two signals is processed by the microcomputer and used for either gain or COR threshold applications.

4-79. Preselector Controller (A7A7). Figure 4-25 shows a functional block diagram of the preselector controller. The preselector controller receives the processed data from the Receiver microcomputer and/or from the Spectrum Surveillance Controller, then is multiplexed or latched to Receiver circuits through program timed strobes. The outputs of the preselector controller select receiver bandwidth (IF select) and receiver frequency bands, tunes the synthesizer (LO OUT), selects the CW or CW1 kHz mode (BFO) and reference select mode (REF SEL), provides scan ($\overline{\text{SCN}}$), mute ($\overline{\text{MUT}}$), and squelch ($\overline{\text{SQU}}$) signals to the audio video amplifier/COR (A9), dump ($\overline{\text{DMP}}$) control to the AGC on the variable gain amplifier (A6A2), selects gain MGC, AGC fast or AGC slow (GAIN MODE), and selects detector mode (DET MODE).

4-80. Figure 7-29 shows the controller schematic diagram. The buffered data bus D0B-D7B (from the converter A7A8) is connected to each of the latches U1 through U5. The data on the bus is strobed through each of the latches at the appropriate program times by the strobes ($\overline{\text{LOWR}}$, $\overline{\text{IFWR}}$, $\overline{\text{EXTWR}}$, $\overline{\text{MODWR}}$ and $\overline{\text{STWR}}$) from the address decoder (A7A6). The outputs from U1, which are the LO (synthesizers) control word bits from the microcomputer (A7A2), are routed to one set of inputs on the analog multiplexers (U14 and U15). Similarly, the outputs from U2, which are the IF filter select control word bits (from the

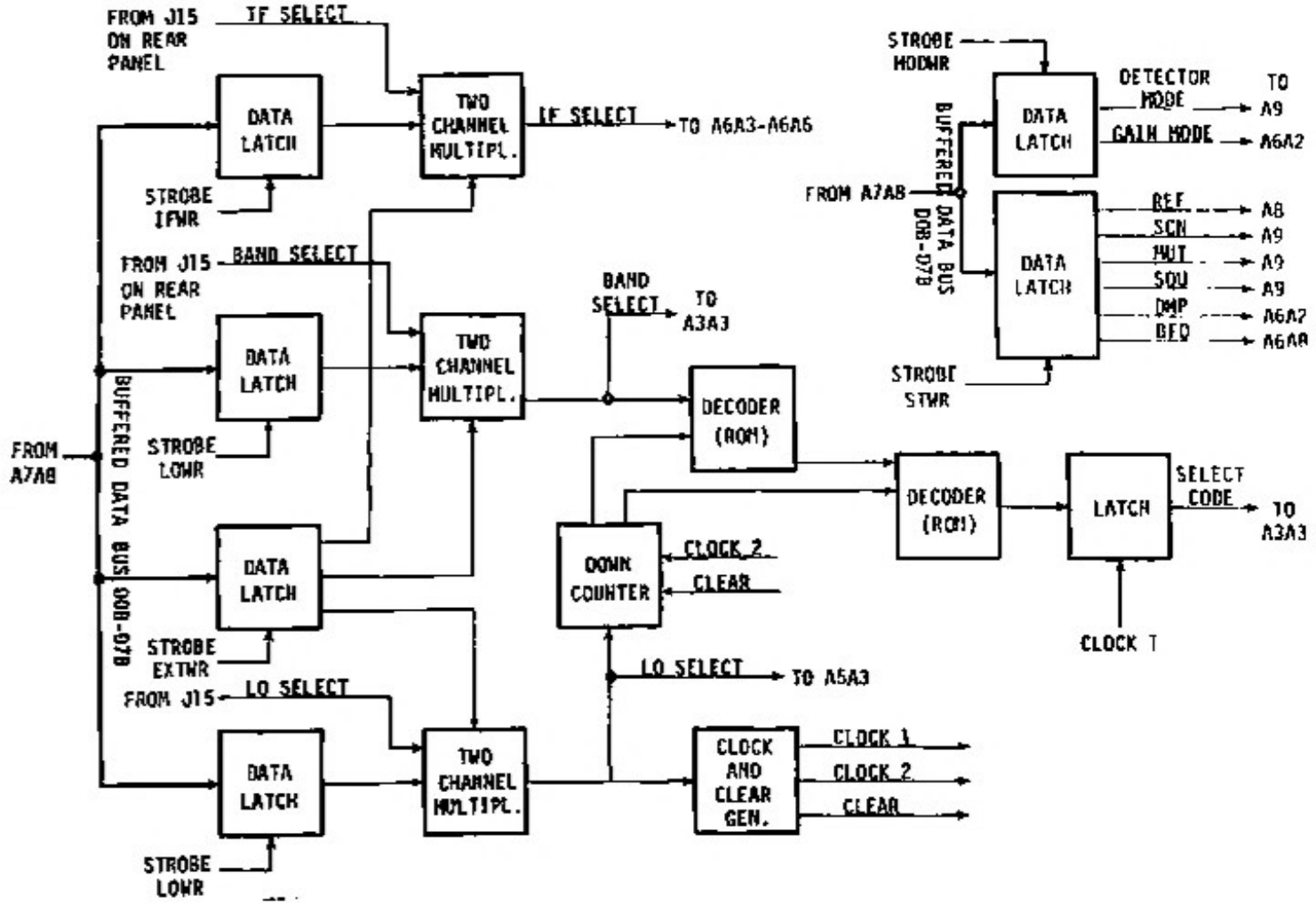


Figure 4-25. Preselector Controller (A7A7) Functional Block Diagram

Receiver microcomputer), are one set of inputs to the analog multiplexers (U10, U11 and U12). Band select control words are output from both U1 and U3 to analog multiplexers U12 and U13. The second set of inputs to these analog multiplexers is the LO control word, band select, and IF select control word from the FAST SCAN input connector J15 (from the external Spectrum Surveillance Controller). The U3 outputs are routed to the multiplexers (U10 through U15) and control the selection of either the microcomputer inputs or the Spectrum Surveillance Controller inputs. The multiplexer U10 through U15 outputs are then routed as the LO, band and IF select control words to the first LO synthesizer (A5), tuner (A3), and IF filter amplifiers (A6A3-A6A6). Latch U4 relays the detector and gain mode control signals to the Receiver circuits. Latch U5 relays the REF (external reference to reference generator), BFO (CHO or 1 kHz offset), $\overline{\text{DMP}}$ (dump to AGC), and $\overline{\text{SCN}}$ (at FAST SCAN, inhibiting of audio video output) signals to the receiver circuits. The band and LO select signals are routed through decoder circuits to provide select codes to the tuner (A3).

4-81. IEEE-488C Remote Control Interface (A7A9). Figure 4-26 shows a functional block diagram of the optional IEEE-488C remote control interface. The IEEE-488C remote control interface, when remote control mode of operation is utilized, connects to an IEEE-488C remote control interface adaptor (A10), and interfaces the microcomputer (A7A2) to the remote computer/controller through the IEEE-488C interface bus. The IEEE-488C remote control interface contains a general purpose interface adapter (GPIA) which is connected directly to the microcomputer data bus and to the bi-directional IEEE-488C interface bus through transceivers. When the GPIA is addressed (according to its preset address on the address switch) by the remote computer/controller, it sends an interrupt request (IRQ-5) to the PIC for servicing of the remote command. When the microcomputer services the request, it receives and carries out the remote command. The GPIA then relays any status data sent from the microcomputer to the remote computer/controller. The GPIA is also reset at power on and is set up at initialization by the microcomputer.

4-82. Figure 7-31 shows the IEEE-488C remote control interface schematic diagram. The sixteen IEEE-488C signal bus lines, to and from the remote computer/controller, are connected via the Receiver rear panel IEEE-488C remote control interface connector J16. These lines consist of the eight data lines (DIO1-DIO8) and the bus management and handshaking lines (REN, ATN, NRFD, SRQ, DAV, NDAC, EOI and IFC). These inputs are routed through the GPIA adapter to

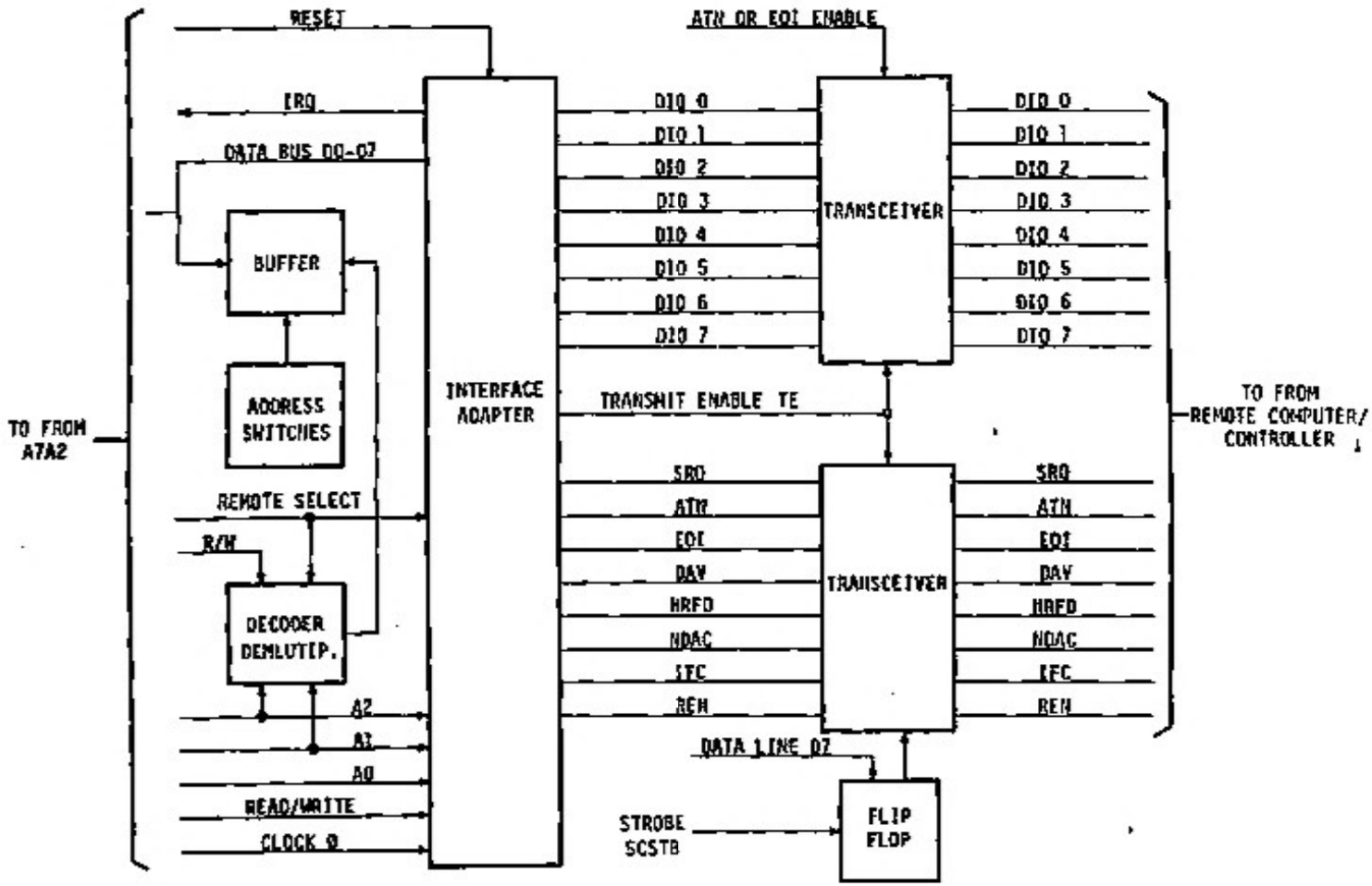


Figure 4-26. IEEE-488C Remote Control Interface (A7A9) Functional Block Diagram

two 8-line transceivers U4 and U5. Signal flow direction through the transceivers is controlled by the TE lines from the GPIA U8. The IEEE-488C signal bus lines, through the transceivers, are connected to their corresponding terminals on the GPIA. Microcomputer connections (from the CPU) to the GPIA are made through connector P1. These connections include: data bus lines D0-D7, clock Ø2, read/write (R/$\overline{W}$), address lines (A0, A1 and A2), $\overline{RESET}$, chip select ($\overline{REMSEL}$), and interrupt request (IRQ). Initialization for the GPIA is activated through the $\overline{RESET}$ line. GPIA operation is controlled through 14 internal registers which are written to and read from by the microcomputer, being addressed through $\overline{REMSEL}$, A0, A1, and A2. At initialization, the microcomputer sets the appropriate GPIA registers to the start states required for operation.

4-83. The remote computer/controller will address the Receiver as a listener or talker. When the GPIA is addressed, it asserts an interrupt request $\overline{IRQ5}$. The microcomputer receives the interrupt through the priority interrupt controller (PIC) and initiates the interrupt service routine. When addressed as a listener, the GPIA generates TE and the interface circuit accepts remote computer/controller commands and data from the IEEE-488C interface bus. Data on lines DIO1-DIO8 interconnect from the remote computer/controller to the GPIA. The handshaking lines are set up accordingly; the GPIA transfers all subsequent data (in the message) from the remote computer/controller to the microcomputer under program control. When addressed as a talker, the GPIA TE line is low and the IEEE-488C remote control interface sends data from the GPIA to the IEEE-488C interface bus and remote computer/controller. Data on lines DIO1 to DIO8 is routed from the GPIA to the IEEE-488C interface bus. The handshaking lines are set up accordingly; the GPIA transfers subsequent data from the microcomputer to the remote computer/controller under program control.

4-84. POWER SUPPLY MODULE ASSEMBLY (A1). Figure 4-27 shows the functional block diagram for the power supply. The power supply supplies the various DC voltages used throughout the Receiver. The Receiver operates from either 115 or 230 volts a,c which is card selectable from the AC POWER FL1 filter/connector on the rear panel. The power supply contains a multi-secondary step down transformer, rectifiers, filters and regulators used to supply dc voltages from -22 volts to +28 volts used by the Receiver. One secondary winding of the transformer supplies 115 volts ac to the Receiver cooling fan blower motor for either 115 or 230 volt input operation.

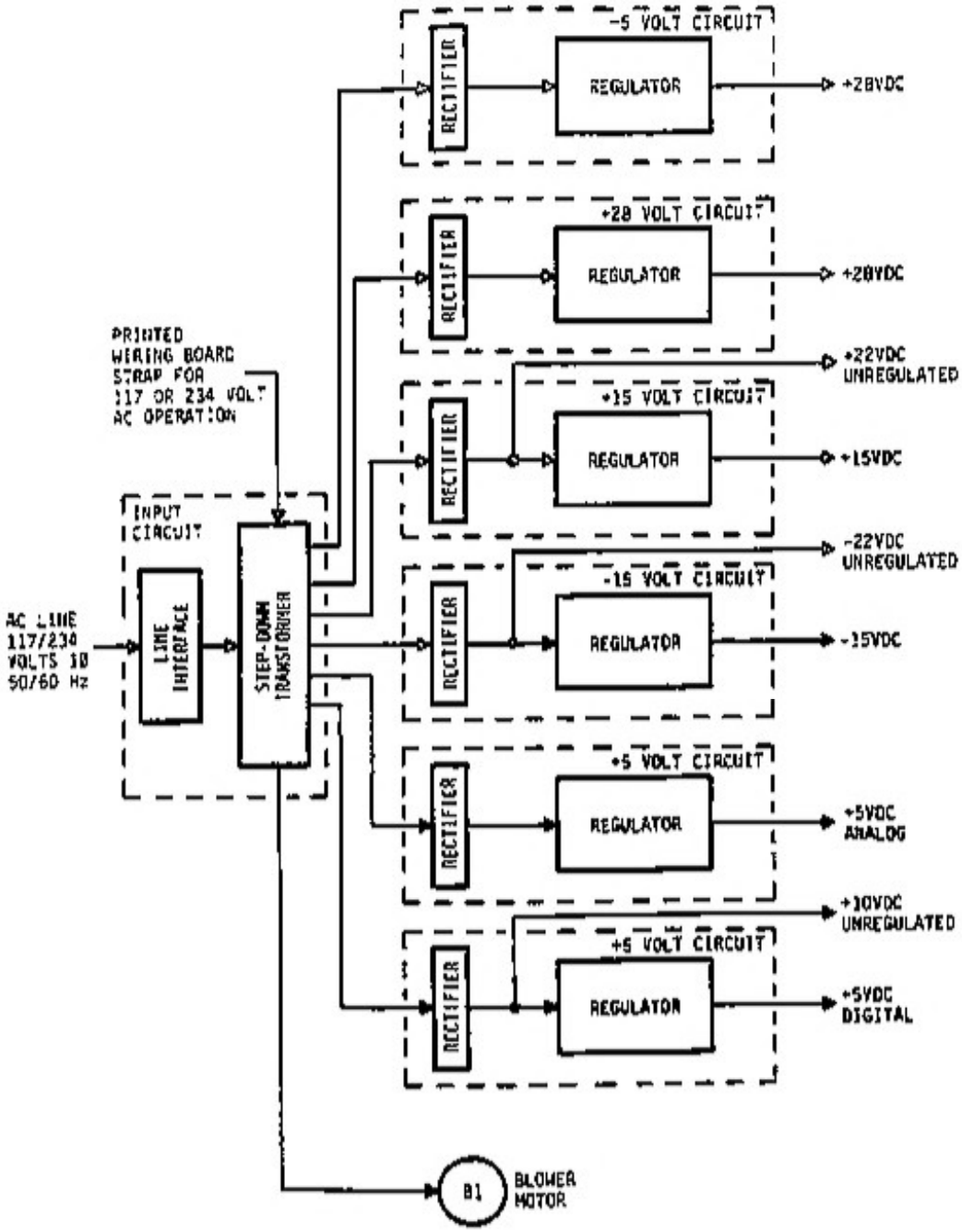


Figure 4-27. Power Supply (A1) Functional Block Diagram

4-85. Figure 7-1 shows the schematic diagram of the power supply. Input power is routed through a fuse F1, a filter FL1, the front panel POWER switch (S1), and the card select switch to the primary winding of the transformer. Six secondary windings of the transformer are used to produce six different dc voltages through full wave rectifiers CR1-CR12. These dc voltages are filtered through filter capacitors C1-C6 to smooth the pulsating dc voltages. Three of these voltages are fused and routed to Receiver circuits as -22, +10 and +22 volts dc unregulated. All six of the voltages are routed through voltage regulators U1-U6 and then routed to Receiver circuits as -15, -5, +5 analog, +5 digital, +15 and +28 volts dc-regulated.

SECTION V

MAINTENANCE INSTRUCTIONS

5-1. INTRODUCTION

5-2. This section contains maintenance instructions for the VHF/UHF Receiver, Type RG-5545A (Receiver). These instructions include: maintenance schedules, list of test equipment, preventive maintenance instructions, performance tests, troubleshooting procedures and adjustment procedures.

5-3. MAINTENANCE SCHEDULE

5-4. The preventive maintenance schedule in Table 5-1 shows the frequency that the instructions in this section should be performed. A number of the instructions, such as alignment, should be performed only when it is required to re-establish performance through adjustments. This would be shown in the Maintenance Schedule, under the "as required only" column.

Table 5-1. Maintenance Schedule

MAINTENANCE	AS REQUIRED ONLY	DAILY	WEEKLY	MONTHLY	SEMI-ANNUALLY	ANNUALLY
Cleaning	X				X	
Damage Inspection	X				X	
Performance Test					X	
Troubleshooting Procedure	X					
Adjustment Procedure	X					
Disassembly/ Reassembly	X					

5-5. TEST EQUIPMENT

5-6. The test equipment required for performing maintenance alignment of the Receiver is shown in Table 5-2.

Table 5-2. Test Equipment Required

ITEM	EQUIPMENT	MODEL NO.	MANUFACTURER
1	Digital Voltmeter	8010A	Fluke
2	Oscilloscope	565B	Tektronix
3	Signal Generator (2)	86480PT02	Hewlett-Packard
4	Frequency Doubler	FK-5	Mini-circuits
5	Computer/Controller	4051	Tektronix
6	Synthesizer/Function Generator	3325A	Hewlett-Packard
7	Tracking Generator	8444A	Hewlett-Packard
8	Spectrum Analyzer	141T/8554B/ 8552B	Hewlett-Packard
9	RMS Voltmeter	8920A	Fluke
10	Synthesized Signal Generator	8662A	Hewlett-Packard
11	Spectrum Analyzer	3585A	Hewlett-Packard
12	Frequency Counter	9919	Racal-Dana
13	Variac	GR-W5MT3AW	General Radio
14	Power Converter	251TCA	California Instruments
15	Power Divider/Combiner	PD-1000-2SMA	American Microwave
16	Stopwatch	H-1595	Heuer
17	Low Pass Filter, 3400 Hz	JW33-1910A	Sprague
18	Distortion Analyzer	339A	Hewlett-Packard
19	Pre-amp/Filter	75052/77025	Regco
20	Headset, Stereo		

Table 5-2. Test Equipment Required (cont.)

ITEM	EQUIPMENT	MODEL NO.	MANUFACTURER
21	PC Card Extractor	5851	REGCO
22	Resistor, Termination	50 ohm	-
23	Resistor, Termination	91 ohm	-
24	Resistor, Termination	600 ohm	-
25	Isolation Transformer	LL-010	Torotel
26	Spectrum Surveillance Controller	RG-1342	Regco
27	Spectrum Display	HP1311A	Hewlett-Packard
28	Test Plug*	227	M. M. Smith
29	Computer/Controller	4051	Tektronix
30	PC Card Extender	EB-123 Rev. 1 (Analog) EB-122 Rev. A (Digital)	Regco

*Attach two 6-inch lengths of RG-55/U cable, terminated with UG-88/U BNC Connectors.

5-7. PREVENTIVE MAINTENANCE

5-8. Preventive maintenance for the Receiver consists of maintenance tasks to detect potential malfunction or failure of components. In addition, preventive maintenance defines the necessary cleaning, operational checks, and minor calibrations required to maintain operational performance standards.

5-9. CLEANING. The Receiver should be inspected and cleaned to maintain cleanliness and good general appearance. The maintenance schedule in Table 5-1 shows the frequency that the following inspection and cleaning procedures should be accomplished.

1. Remove dust and dirt from front and rear using a lint free cloth moistened in tap water.

NOTE

If cleaning requires removal of oil or grease, use isopropyl alcohol, specification TT-I-1735, grade A instead of tap water.

2. Clean blower motor assembly as follows:

WARNING

Rotating blades of the blower motor can cause injury. Always disconnect the Receiver power cord before cleaning the blower motor filter.

a. Remove four phillips-head screws securing filter and filter cover to Receiver rear panel.

b. Remove filter from cover by lifting out, as required.

c. Clean filter and cover in a solution of mild detergent and tap water.

d. Dry filter with low pressure (5 to 10 psig) compressed air.

e. Re-install clean filter in cover.

f. Attach cover to Receiver rear panel with four phillips-head screws, as required.

3. Remove top and bottom covers from Receiver by loosening eight (8) quarter turn fasteners and lifting covers off.

CAUTION

Do not use bristle brushes or cloths to clean circuit cards. This material may create static electricity which can damage CMOS integrated circuits.

4. Inspect interior for dust and dirt collection.

5. Use a vacuum device to remove dust and other loose matter.

WARNING

The filter capacitors used in the power supply will retain an electrical charge after power is removed. The capacitors should be discharged slowly by shorting the terminals through a protected resistive device.

6. Inspect and clean power supply as described in steps 4 and 5.

5-10. DAMAGE INSPECTION. The Receiver should be inspected for damage, missing parts and general deterioration. The maintenance schedule in Table 5-I provides the necessary time interval between inspection for which the following procedures should be accomplished.

1. Inspect knobs, switches, controls and indicators on Receiver front panel for damage, tightness, freedom to operate, and replace damaged or missing items, as required.

2. Inspect connectors on Receiver rear panel for bent or broken pins, damaged shells, and replace or repair, as required.

3. To inspect interior of Receiver, remove top and bottom cover by loosening eight (8) quarter-turn fasteners.

4. Inspect internal modules/circuit card assemblies and components for signs of excessive heat, corrosion, damaged circuits, loose connections, or other signs of damage, and repair or replace, as required.

5. Inspect tuning control (knob) assembly for freedom of operation and general appearance.

6. Tuning control should operate and spin freely, and check that encoder disk is tight on shaft and free of wobble as it is rotated.

7. Inspect fuse (F1) and power filter assembly (FL1) circuit card strapping in the power supply (A1), located on Receiver rear panel.

8. Make sure fuse is not blown or circuit card strapping is not damaged, and replace as required.

9. Inspect 3.6 V nickle cadmium battery (BT1), located on microcomputer circuit card assembly (A7A2), and replace as required.

NOTE

The battery should be replaced if there is any sign of damage, corrosion or loss of electrolyte.

5-11. LUBRICATION. No lubrication is required for the Receiver.

5-12. PERFORMANCE TESTS. The performance tests should be performed to determine that overall performance of the Receiver is satisfactory. Any substandard conditions found through these tests, should be corrected before placing the Receiver in normal operation. If discrepancies or malfunctions cannot be corrected, the troubleshooting procedures in paragraph 5-26 should be performed to isolate and correct the problem. Table 5-1 shows the frequency at which the performance tests should be conducted.

5-13. Power Supply Test. This procedure checks the dc output voltages of the Receiver power supply for correct levels and filtering.

1. Check fuse (F1) and power filter assembly (FL1) circuit card strapping for proper voltage input (see paragraph 2-6).

2. Connect female end of power cable to power filter assembly (FL1) input connector on Receiver rear panel.

3. Connect male end of power cable to ac power source.

4. Remove top cover of Receiver and power supply assembly (A1) to gain access to power supply.

5. Depress POWER PUSH/ON switch (S2) to on position.

6. Using digital voltmeter, measure unregulated dc power output potentials at test points indicated below.

NOTE

The test points for all unregulated DC power are located on the power rectifier (A1A1) accessed from the top of the power supply assembly (A2). Use chassis as ground in measuring all power.

TEST POINT	NOMINAL VOLTAGE	VOLTAGE RANGE
A1-TP1	+22 volts DC	+18 to +30 volts DC
A1-TP2	-22 volts DC	-18 to -30 volts DC
A1-TP3	+10 volts DC	+ 8 to +18 volts DC

7. Using digital voltmeter, measure regulated dc power output potentials at tests points indicated below.

NOTE

The test points for regulated power are located on the top of the power supply assembly. Use chassis as ground in measuring all dc power.

TEST POINT	NOMINAL VOLTAGE	VOLTAGE RANGE
TP1	-5 volts DC	-4.5 to -5.25 volts DC
TP2	+28 volts DC	+27 to +29 volts DC
TP3	+15 volts DC	+14.5 to +15.5 volts DC
TP4	-15 volts DC	-14.5 to -15.5 volts DC
TP5	+5 volts DC (analog)	+4.75 to +5.25 volts DC
TP6	+5 volts DC (digital)	+4.75 to + 5.25 volts DC

8. Using oscilloscope, measure AC ripple levels peak to peak at test points listed in step 7.

NOTE

The AC ripple at any test point should be no greater than 10 millivolts peak to peak.

9. Depress POWER PUSH/ON switch (S2) to off position.

NOTE

This concludes the power supply test, disconnect all test equipment.

5-14. Receiver Tuning Test. This test checks the operation of the Receiver via operation of the front panel controls, and monitoring from the front panel indicators.

1. Connect signal generator to ANTENNA connector J1 on Receiver rear panel as shown in Figure 5-1.

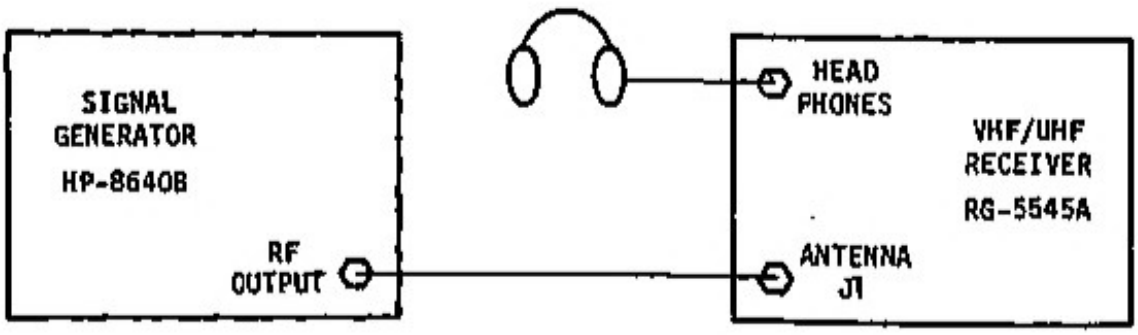


Figure 5-1. Receiver Tuning Test Set-up

2. Adjust signal generator output for 204.061 MHz, -60 dBm, with 1 kHz AM modulation at 30 percent.

3. Press REMOTE switch to local position (LED indicator off).

4. Press AM pushbutton key-switch (LED indicator on).

5. Press 10 kHz key-switch pushbutton (LED indicator on).

6. Press AGC FAST pushbutton key-switch (LED indicator on).

NOTE

If any other pushbutton key-switch indicators are on, press applicable key-switch and observe that indicator goes out.

7. Press numeric keys 2, 0, 4, . (decimal point), 0, 6, 0, 8, and 8 in sequence.

NOTE

If an incorrect digit is selected during frequency entry, press the CLR pushbutton key-switch to erase the digits entered and re-select the desired digits.

8. Press ENT/EXCL FREQ pushbutton key-switch and observe that frequency display changes to 204.06088 MHz and level meter deflects.

9. Connect headset to HEADPHONES jack.

10. Adjust associated (LSB/USB) headphones audio level controls and observe that level of 1 kHz tone changes, then adjust controls for comfortable audio level and remove headset.

11. Press TUNING rate SLOW pushbutton switch, then momentarily press TUNING slew switch lever upward, and observe that tens digit on frequency display increments to numeral 9 from previous setting of 8.

12. Momentarily press TUNING slew switch lever downward and observe that tens digit decrements to 8.

13. Press TUNING rate MED pushbutton switch, then press and hold the TUNING slew switch lever upward until a frequency of 204.09988 is reached.

NOTE

Observe that 1 kHz digit changes and that each time it cycles through numeral nine that it increments its total to 10 kHz digit. The tens and hundreds digits will not change.

14. Press TUNING rate FAST pushbutton switch, then press and hold TUNING slew switch lever upward until a frequency of 204.99988 is reached.

NOTE

Observe that 100 kHz digit changes while all other digits remain unchanged.

15. Press TUNING rate MED pushbutton switch and adjust TUNING control knob counter-clockwise to tune Receiver to a frequency of 204.06088 MHz.

NOTE

Observe that 1 kHz digit decrements its total to next lesser digit until frequency is reached. Verify also that the TUNING meter gradually indicates 0 as signal generator frequency is reached.

16. Press TUNING rate OFF pushbutton switch and adjust TUNING control in both directions, and observe that frequency display does not change.

17. Press TUNING slew switch lever in upward and downward directions and observe that frequency display remains unchanged.

18. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the receiver tuning test, disconnect all test equipment.

5-15. Scan Test. This test checks the ability of the Receiver to scan up or down over pre-set start and stop limits.

1. Depress POWER PUSH/ON switch to on and press REMOTE switch to obtain local control (remote LED indicator off).

2. Select lower frequency scan limit by pressing 4, 0, and 0 numeral pushbutton key-switches, then pressing SCAN DN pushbutton key-switch (LED indicator on).

3. Select upper frequency scan limit by pressing 8, 0 and 0 numeral pushbutton key-switches, then pressing SCAN UP pushbutton key-switch (LED indicator on).

4. Press SCAN UP pushbutton key-switch a second time and observe that associated LED indicator comes on and that a flashing 0 appears on the left most digit.

5. Press numeral pushbutton key-switch 1 and observe that tens digit in frequency display begins to increment very slowly.

6. Press numeral pushbutton key-switches 2 through 9 sequentially and observe that frequency display increments at progressively more rapid rates as pushbutton key-switches 2 through 9 are sequentially pressed, and that Receiver scans up from 400 MHz to 800 MHz, then skips back to 400 MHz and starts scan over again.

7. Press numeral pushbutton key-switch 0 and observe that scan stops but Receiver remains in scan mode.

8. Press SCAN ON pushbutton key-switch, then press numeral key 9 and observe that Receiver scans down from 800 MHz to 400 MHz, then skips back to 800 MHz and starts scanning down again.

9. Select slower scan rates by pressing numeral pushbutton key-switches 8 through 0 sequentially and observe that scan rate is progressively slower as numeral pushbutton key-switches 8 through 1 are selected, and that scan stops when numeral 0 is selected.

10. Press SCAN ON pushbutton key-switch, and observe that SCAN ON indicator goes off and Receiver is de-activated from scan mode.

11. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the scan test, disconnect all test equipment.

5-16. Scan With COR Threshold and AFC Test. This test checks the ability of the Receiver to stop scanning and hold on a signal level above a pre-set COR threshold, to center on that signal frequency, and to exclude frequencies from a COR threshold scan stop.

1. Connect signal generator to ANTENNA connector J1 on Receiver rear panel as shown in Figure 5-1.

2. Depress POWER PUSH/ON switch to on position and press REMOTE switch to obtain local control mode (remote LED indicator off).

3. Momentarily press COR THRESHOLD slew switch lever either up or down and release, then observe that associated COR THRESHOLD annunciator lights and LEVEL meter indicates some level.

NOTE

The COR THRESHOLD annunciator will remain activated for approximately two seconds and then extinguish unless the COR THRESHOLD switch is activated a second time.

4. With COR THRESHOLD annunciator on, press COR THRESHOLD slew switch lever either up (increase) or down (decrease) to adjust LEVEL meter reading to 20 dB.

5. Adjust signal generator output for 260.750 MHz at -20 dBm, then press AFC pushbutton key-switch and observe that associated LED indicator comes on.

6. Press numeral pushbutton key-switches 4, 5 and 0, then press SCAN UP pushbutton key-switch to enter upper scan limit.

7. Press numeral pushbutton key-switches 2, 0 and 0, then press SCAN DN pushbutton key-switch to enter lower scan limit.

8. Press SCAN UP pushbutton key-switch, then press numeral pushbutton key-switch 5 and observe that Receiver begins scanning up from 200 MHz.

NOTE

Observe that Receiver stops scanning at 260.750 MHz and remains at this frequency.

9. Press CLR pushbutton key-switch and observe that scanning resumes.

NOTE

Observe that scan is up to 450 MHz, then that it skips back to 200 MHz and starts scanning up, and it once again stops at 260.750 MHz.

10. Adjust signal generator level to -100 dBm and observe that after an approximate two second delay, scanning resumes as before but does not stop at 260.750 MHz.

11. Adjust signal generator level to -20 dBm and observe that scanning stops at 260.750 MHz.

12. Adjust signal generator frequency to 270.750 MHz and observe that after an approximate two second delay, Receiver scanning resumes and then stops at 270.750 MHz.

13. Press ENT/EXCL FREQ pushbutton key-switch and observe that scanning resumes and does not stop at 270.750 MHz on subsequent scans.

14. Press SCAN UP pushbutton key-switch to remove Receiver from scan mode.

15. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the COR threshold tests, disconnect all test equipment.

5-17. Channel Memory Test. This test checks the ability to store a full Receiver operating parameter set-up in channel memory, and to store, recall, or execute any channel for Receiver operation. The ability to scan active channels is also demonstrated in this test.

1. Depress POWER PUSH/ON switch to on position and press REMOTE switch to obtain local control (remote LED indicator off).

2. Press MEM pushbutton key-switch and observe that associated LED indicator comes on, MEMORY DISPLAY annunciator comes on, and a channel number is displayed.

3. Select channel numbers by pressing TUNING slew switch lever either up or down.

4. Press TUNING slew switch lever up and observe that channel numbers displayed increments upward.

5. Press TUNING slew switch lever down and observe that channel numbers displayed decrements down.

6. Select a memory channel that can be used to store a different Receiver operating parameter set-up, then press RCL pushbutton key-switch.

NOTE

The contents of the memory channel recalled will be transferred to the front panel without altering Receiver operation. The MEMORY DISPLAY will blink on and off to indicate that the front panel displays do not necessarily reflect Receiver operating conditions. Front panel controls may now be used to load the channel without affecting Receiver operation.

7. Press CW, 50 kHz and MGC pushbutton key-switches and observe that associated LED indicators come on.

8. Press RF GAIN slew switch lever up (increase) or down (decrease) to adjust LEVEL meter reading to 50 dB.

9. Press COR THRESHOLD slew switch lever up (increase) or down (decrease) to adjust LEVEL meter reading to 20 dB.

10. Press AFC pushbutton key-switch and observe that associated LED indicator comes on.

11. Press numeral pushbutton key-switches 2, 0, 5 . (decimal point), 6, 5, 6, 3 and 2 in sequence, then press ENT/EXCL FREQ pushbutton key-switch and observe that 205.65632 MHz is displayed.

12. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator comes on.

NOTE

Record all Receiver parameters as indicated on the front panel display and as entered in steps 7 through 12, including the channel number now displayed.

13. Press STO pushbutton key-switch and observe that Receiver front panel displays change to operating conditions that existed before when RCL pushbutton key-switch was pressed.

14. Press MEM pushbutton key-switch and observe that associated LED indicator goes off.

15. Connect signal generator as shown in Figure 5-1 and adjust for 205.65432 MHz at -20 dBm.

16. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator comes on and that channels are being scanned.

NOTE

The channel scan will be up from lowest active channel to highest active channel with an approximate 20 millisecond pause on each active channel. If any active channel has a COR threshold below the level of the signal generator, the scan will stop and hold on that channel. Each time the scan stops, press the CLR pushbutton key-switch to continue the scan until the channel stored in step 13 is reached. In addition, scanning should stop and hold channel just stored.

17. Press CHAN SCAN pushbutton key-switch and observe that associated LED indicator goes off.

18. Press MEM pushbutton key-switch and observe that associated LED indicator comes on and channel number stored in step 13 is displayed.

19. Press RCL pushbutton key-switch and observe that MEMORY DISPLAY flashes on and off and that Receiver parameters recorded after step 12 are displayed on front panel.

20. Press EXEC pushbutton key-switch and observe that MEMORY DISPLAY stops flashing and that all parameters in channel set-up are transferred to Receiver operation.

NOTE

Observe also that Receiver is removed from memory mode and MEMORY DISPLAY goes out.

21. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the memory tests, disconnect all test equipment.

5-18. RF Gain Level Test. This test checks that the RF/IF gain can be incremented in approximately 0.5 dB steps, over a 100 dB range, from the front panel of the Receiver.

1. Connect 50 ohm termination and RMS voltmeter to IF OUT connector J4 on Receiver rear panel as shown in Figure 5-2.

2. Connect signal generator to ANTENNA connector J1 on Receiver rear panel.

3. Depress POWER PUSH/ON switch to on position and press AM, 10 kHz and MGC pushbutton key-switches.

4. Press numeric pushbutton key-switches 6, 0 . (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

5. Press RF GAIN slew switch lever up and hold until LEVEL meter indicates 0.

6. Adjust signal generator output to 60.000 MHz, and -90 dBm CW.

7. Press RF GAIN slew switch lever down until RMS voltmeter reads approximately -10 dBm.

8. Observe reading on RMS voltmeter and press associated REL dB key.

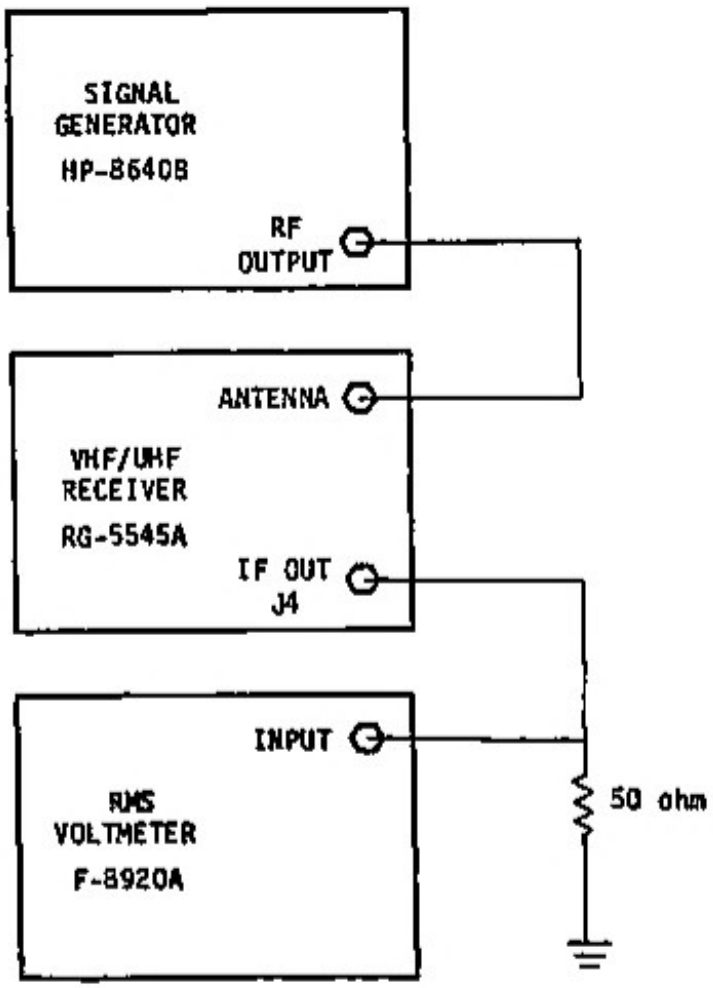


Figure 5-2. RF Gain Level Test

9. Press RF GAIN slew switch lever down 20 times and observe decrease in relative level of RMS voltmeter.

NOTE

Decrease in relative dB on RMS voltmeter shall be between 5 and 15 dB.

10. Adjust signal generator output to -20 dBm.

11. Press RF GAIN slew switch lever until RMS voltmeter reads 0 dB relative.

12. Press RF GAIN slew switch lever down 20 times and observe decrease in relative level of RMS voltmeter.

NOTE

Decrease in relative dB on RMS voltmeter shall be between 5 and 15 dB.

13. Press RF GAIN slew switch lever down until RMS voltmeter reads -30 dB relative.

14. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the RF gain level test, disconnect all test equipment.

5-19. IF Output Test. This test checks the IF outputs available at the rear panel. These outputs include: IF OUT connector J4, POST FL-IF connector J7, and PRE FL-IF connector J10.

1. Connect spectrum analyzer and signal generator as shown in Figure 5-3 with spectrum analyzer connected to IF OUT connector J4.

2. Depress POWER PUSH/ON switch to on position, press CW, 10 kHz, and AGC-FAST pushbutton key-switches.

3. Press numeric pushbutton key-switches 9, 0, . (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch and observe Receiver tunes to 90 MHz.

4. Adjust signal generator for 90.000 MHz and -107 dBm output.

5. Adjust spectrum analyzer controls to obtain set-up as follows:

RF Section: Center frequency 21.4 MHz
Scan width 20 kHz per division
Bandwidth 3 kHz
Input attenuation 20 dB

IF Section: Video filter 10 kHz
Scan time 5 msec per division
Log reference level 0 dBm

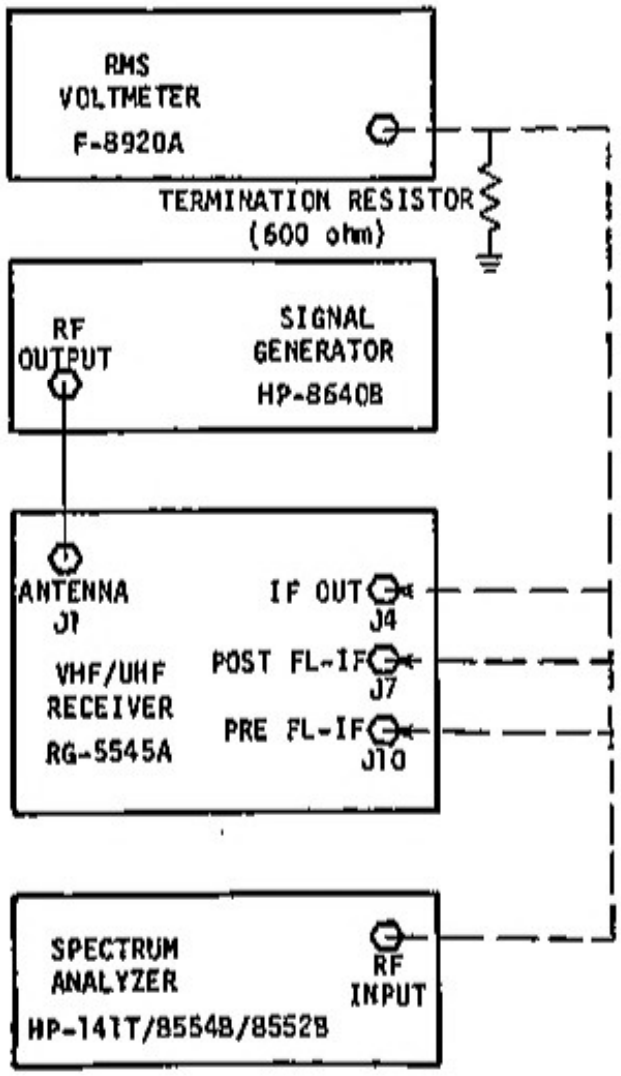


Figure 5-3. IF Output Test

6. Observe that spectrum analyzer indicates a level between -20 dBm and 0 dBm.

7. Repeat steps 4 through 6 for 20, 50 and 100/200/400 kHz (as applicable) bandwidths, however, adjust signal generator output level in step 4 for each bandwidth selected in accordance with the following:

20 kHz BW = -104 dBm
50 kHz BW = -100 dBm
100 kHz BW = -97 dBm
200 kHz BW = -94 dBm
400 kHz BW = -91 dBm

8. Reconnect spectrum analyzer to POST-FL IF connector J7.

9. Adjust signal generator output level to -50 dBm.

10. Observe that spectrum analyzer indicates a level between -20 dBm and -30 dBm.

11. Reconnect spectrum analyzer to PRE-FL IF connector J10.

12. Observe that spectrum analyzer indicates a level between -20 dBm and -30 dBm.

13. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the IF output test, disconnect all test equipment.

5-20. Video Output Test. This test checks the video outputs available at the rear panel which include: FM VIDEO connector J5 and VIDEO connector J11.

1. Connect signal generator and RMS voltmeter as shown in Figure 5-4 with RMS voltmeter connected to FM VIDEO connector J5.

2. Depress POWER PUSH/ON switch to on position and press FM, 10 kHz and AGC FAST pushbutton key-switches.

3. Press numeric pushbutton key-switches 2, 5, . (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

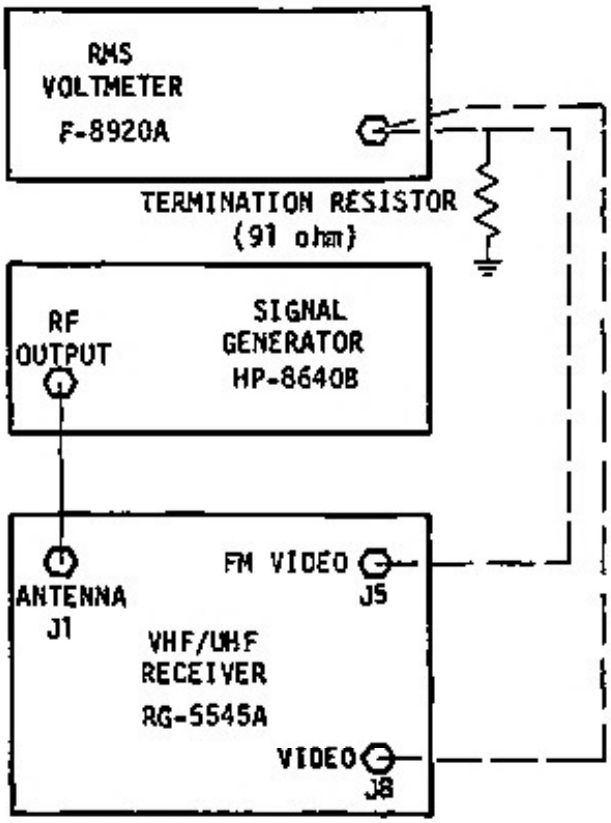


Figure 5-4. Video Output Test

4. Adjust signal generator for 25.000 MHz, -97 dBm with 400 Hz FM modulation at 5 kHz deviation.

5. Set RMS voltmeter for 93 ohm dBm reference.

6. Adjust FM VIDEO potentiometer R1 on Receiver rear panel fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

7. Adjust FM VIDEO potentiometer R1 clockwise until RMS voltmeter reads +5 dBm.

8. Disconnect RMS voltmeter from FM VIDEO connector J5 and re-connect to VIDEO connector J8.

9. Adjust VIDEO potentiometer R2 on Receiver rear panel fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

10. Adjust VIDEO potentiometer R2 clockwise until RMS voltmeter indicates less than -45 dBm.

11. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the video output test, disconnect all test equipment. The FM VIDEO potentiometer R1 and VIDEO potentiometer R2 may require re-adjustment when unit is installed in a typical system application.

5-21. Audio Output Test. This test checks the audio outputs available at the rear panel terminal board TB1 and the front panel HEADPHONES jack.

1. Obtain and connect test equipment as shown in Figure 5-5 with oscilloscope connected to HEADPHONES jack (tip to channel 1 and ring to channel 2) and signal generator no. 1 connected directly to ANTENNA connector J1 on Receiver rear panel.

2. Depress POWER PUSH/ON switch and press AM, 10 kHz, and AGC FAST pushbutton key-switches.

3. Adjust both (inner and outer) HEADPHONES audio level control fully counter-clockwise.

4. Press numeric pushbutton key-switches 2, 0, 4, . (decimal point), 0, 6, 0, 8 and 8, then press ENT/EXCL FREQ pushbutton key-switch.

5. Adjust signal generator output to 204.061 MHz, -60 dBm with 1 kHz AM modulation at 30 percent.

6. Adjust outer (USB) HEADPHONES audio level control clockwise while observing channel 1 oscilloscope trace.

7. Observe that 1 kHz signal on channel 1 changes amplitude as outer HEADPHONES audio level control is adjusted.

8. Adjust inner (LSB) HEADPHONES audio level control while observing channel 2 oscilloscope trace.

9. Observe that 1 kHz signal on channel 2 changes amplitude as inner HEADPHONES audio level control is adjusted.

10. Adjust signal generator output to 60.000 MHz, -60 dBm, with 1 kHz FM modulation and 3 kHz deviation.

11. On Receiver front panel, press FM and numeric pushbutton key-switches 6, 0, . (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

12. Observe that 1 kHz signal is displayed on both channels of oscilloscope.

13. Remove modulation from signal generator.

14. Press CW 1kHz pushbutton key-switch and observe that 1 kHz is displayed on both channels of oscilloscope.

15. Press CW 0 pushbutton key-switch and observe that 1 kHz signal disappears from both channels of oscilloscope.

16. Press TUNING rate SLOW pushbutton key-switch, then rotate TUNING control (knob) clockwise until frequency display on Receiver indicates 60.00100 MHz.

17. Observe that 1 kHz signal again is displayed on both channels of oscilloscope.

18. Disconnect oscilloscope and connect single signal generator to ANTENNA connector J1 on Receiver rear panel.

19. Connect RMS voltmeter between terminal board TB1 terminals 1 and 3 through isolation transformer as shown in Figure 5-5.

20. Press CW 1 kHz, 10 kHz and AGC SLOW pushbutton key-switches.

21. Press numeric pushbutton key-switches 2, 5, . (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

22. Adjust signal generator output for 25.000 MHz, -97 dBm, and remove modulation.

23. Set RMS voltmeter for 600 ohm dBm reference.

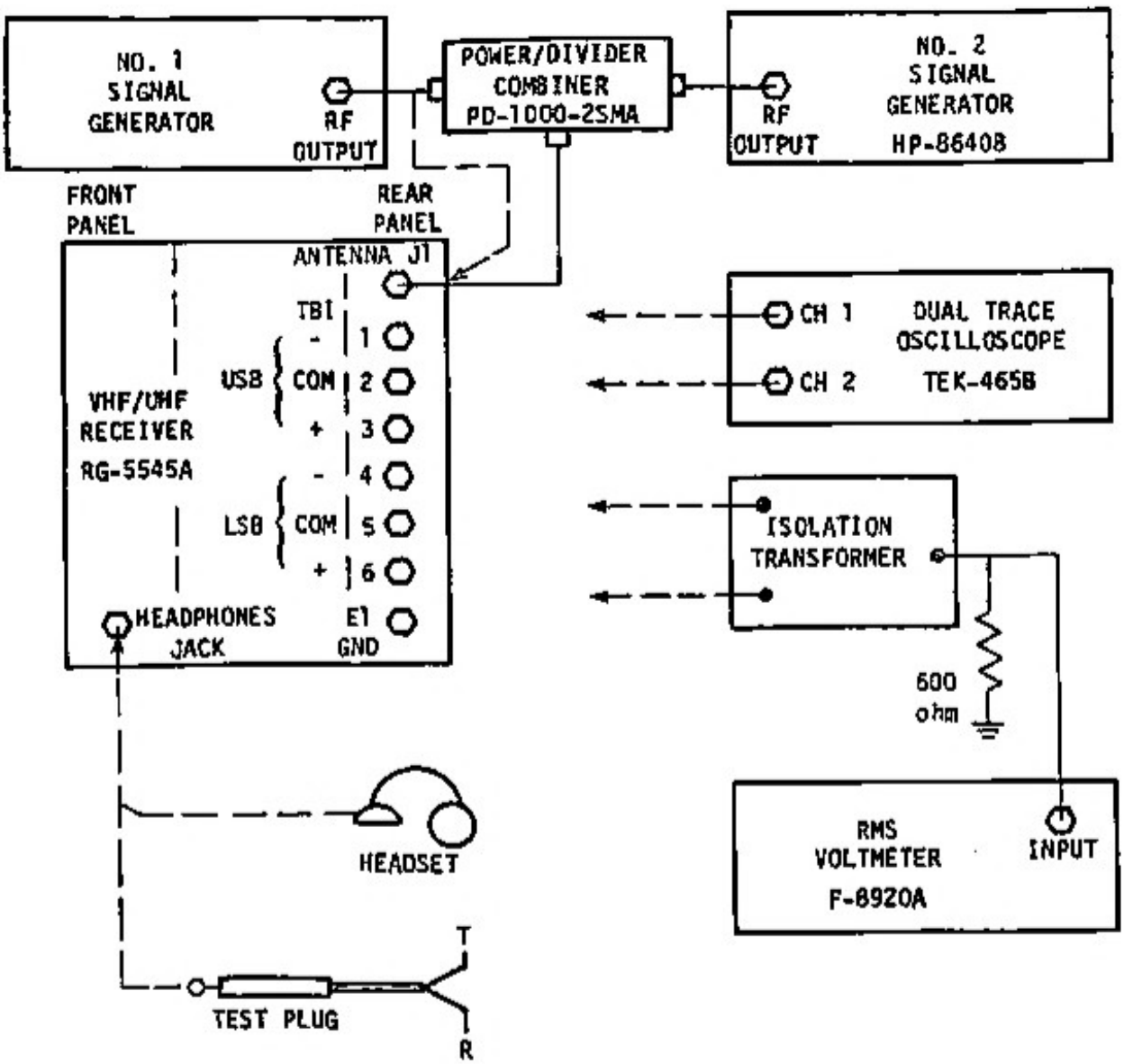


Figure 5-5. Audio Output Test

24. Adjust AUDIO 1 potentiometer R3 fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

25. Adjust AUDIO 1 potentiometer R3 clockwise until RMS voltmeter indicates +5 dBm.

26. Disconnect RMS voltmeter from between terminal board TB1 terminals 1 and 3, and reconnect between terminals 4 and 6.

27. Adjust AUDIO 2 potentiometer R4 fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

28. Adjust AUDIO 2 potentiometer R4 clockwise until RMS voltmeter indicates +5 dBm.

29. Disconnect RMS voltmeter from between terminals 4 and 6 and reconnect to the HEADPHONES jack tip without the isolation transformer.

30. Adjust outer (USB) HEADPHONES audio level control to the full clockwise position and observe that RMS voltmeter indicates at least +20 dBm, then reset control fully counter-clockwise.

31. Reconnect RMS voltmeter to the HEADPHONES jack ring without the isolation transformer.

32. Adjust inner (LSB) HEADPHONES audio level control to the full clockwise position and observe that RMS voltmeter indicates at least +20 dBm, then reset control fully counter-clockwise.

33. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the audio output test, disconnect all test equipment. AUDIO 1 potentiometer R3 and AUDIO 2 potentiometer R4 may require re-adjustment when unit is installed in a typical system application.

5-22. Reference Frequency Test. This test checks the ability of the Receiver to switch-select an external reference frequency.

CAUTION

The Receiver is equipped with an extremely accurate ($\pm 5 \times 10^{9}$) internal reference frequency that is factory calibrated beyond the tolerance range of ordinary frequency counters. Do not attempt to measure or adjust this 10 MHz or 1 MHz reference frequency output to the rear panel at 10 MHz REF OUT connector J11 and 1 MHz REF OUT connector J18.

1. Obtain and interconnect test equipment as shown in Figure 5-6, then turn synthesizer/function generator on and allow at least 30 minutes warm up time.

2. Depress POWER PUSH/ON switch to on position, then press EXT REF pushbutton key-switch and observe that associated LED indicator and REFERENCE UNLOCKED display flashes on and off.

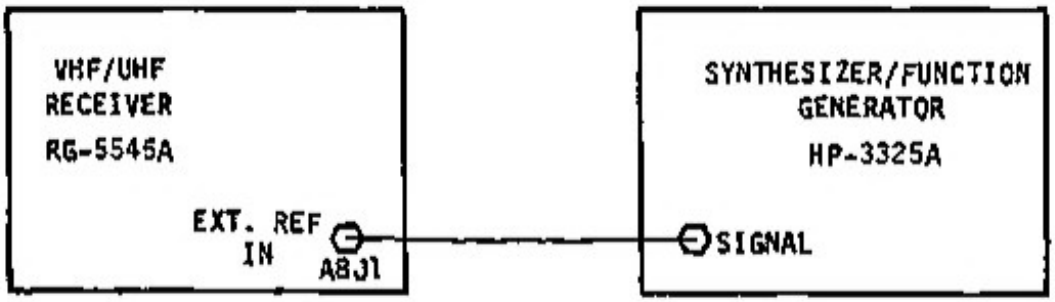


Figure 5-6. Reference Frequency Test

3. Set function generator to 1 MHz at 5 volts peak-to-peak and adjust frequency in 0.1 Hz steps until indicators quit flashing and extinguish.

4. Adjust function generator level to 50 millivolts peak-to-peak and observe that FREQUENCY UNLOCKED indicators remain off.

5. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the reference frequency test, disconnect all test equipment.

5-23. Remote Control Operation Test. This test checks the operation of the Receiver from a remote location using the remote computer/controller, when fitter with the IEEE-488C remote control interface circuit card assembly (A7A9), as may be applicable.

1. Obtain and interconnect remote computer/controller and signal generator to Receiver as shown in Figure 5-7.

2. Press REMOTE switch on Receiver front panel and observe that associated LED indicator is on, then set primary address switch (S1) located on rear panel to address 32 (first five positions from right to off.)

3. Initialize remote computer/controller and enter set-up program as listed in chart below, checking and editing entry as required, then execute program.

LINE NO.	STATEMENT	INSTRUCTION
100	WBYTE	@32,96: 1,2,3,4,5,6,7,8, 3, 10, 0 0, 125, -10
110	PRINT	"FREQUENCY MHz = 123.45678"
120	PRINT	"SCAN UP RATE = 3"
130	PRINT	"DETECTION MODE = 10"
140	PRINT	"BFO MODE kHz = 0"
150	PRINT	"GAIN MODE = 0"
160	PRINT	"GAIN dB = 125"
170	PRINT	"IFBW kHz = 10"
180	END	

4. Set Receiver controls to reflect settings entered above.

5. Adjust signal generator for 499.99999 MHz, -80 dBm with 1 kHz AM modulation at 50 percent.

6. Press REMOTE switch on Receiver front panel to obtain local control mode and observe that associated LED indicator is off.

7. Press AM, AGC FAST and 50 kHz pushbutton key-switches.

8. Press numeric pushbutton key-switches 4, 9, 9, . (decimal point), 9, 9, 9, 9 and 9, then press ENT/EXCL FREQ pushbutton key-switch and set reference source to internal.

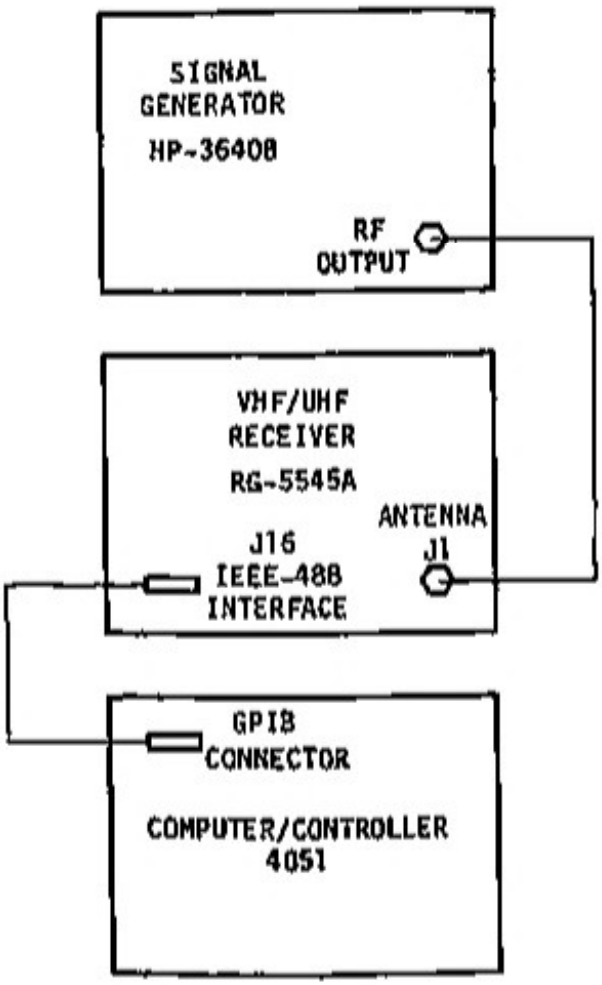


Figure 5-7. Remote Control Operation Test

9. Enter status program at remote computer/controller terminal as shown below, and edit entry as necessary, then execute program.

LINE	STATEMENT	INSTRUCTION
100	DIM	S(24)
110	WBYTE	@64, 96:
120	FOR I	=1 TO 24
130	RBYTE	S(I)
140	NEXT	I
150	PRINT	S
(Refer to note below before proceeding)		
160	END	

NOTE

After execution of line 150 PRINT S, then compare the computer's CRT display with the content shown in the status display chart below. If the CRT display does not agree with that shown in the status display chart, check program instruc-tions setup in step 3 and make corrections as required. If status program has been properly executed proceed with line entry 160 and END statement.

STATUS DISPLAY CHART

0 (RCVR ADDRESS)	0 (DATA ID)	4 (RCVR FREQ)	9 (RCVR FREQ)
9 (RCVR FREQ)	9 (RCVR FREQ)	9 (RCVR FREQ)	9 (RCVR FREQ)
9 (RCVR FREQ)	9 (RCVR FREQ)	0 (SCAN MODE/ RATE)	15 (DETECTION MODE)
0 (BFO MODE)	6 (GAIN MODE)	125 approx (GAIN)	17 (IFBW)
1 (REF SOURCE)	0 (CONTROL MODE)	108 approx (SIGNAL STRENGTH)	10 (IF SLOT 1)
17 (IF SLOT 2)	13 (IF SLOT 3)	10 (IF SLOT 4)	-59 (STATUS)

10. Recall status display chart for observation and compare contents of chart with CRT display and ascertain that both agree with each other.

11. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the remote control operation test, disconnect all test equipment. It should also be noted that control primary address switch assembly S1 must be reset for the particular system application.

5-24 Fast Scan Control Test. This test checks the operation of the Receiver in the fast scan control mode when directed by an optional Spectrum Surveillance Controller, Type RG-1342 (Spectrum Surveillance Controller).

1. Connect test setup with the Spectrum Surveillance Controller, spectrum display, signal generator, and the Receiver as shown in Figure 5-8.

2. Set up signal generator front panel controls as follows:

Output Level	-60 dBm
Range	256-128
Frequency	250.000 MHz
FM	Off
AM	Off

3. On Spectrum Surveillance Controller front panel, set REMOTE switch to LOCAL mode.

4. Adjust DISPLAY INTENSITY control in conjunction with the Spectrum Surveillance Controller BRIGHTNESS CONTROL as desired.

5. On Spectrum Surveillance Controller front panel, press BAND SCAN mode pushbutton key-switch to obtain BAND SCAN mode of operation on CRT Display.

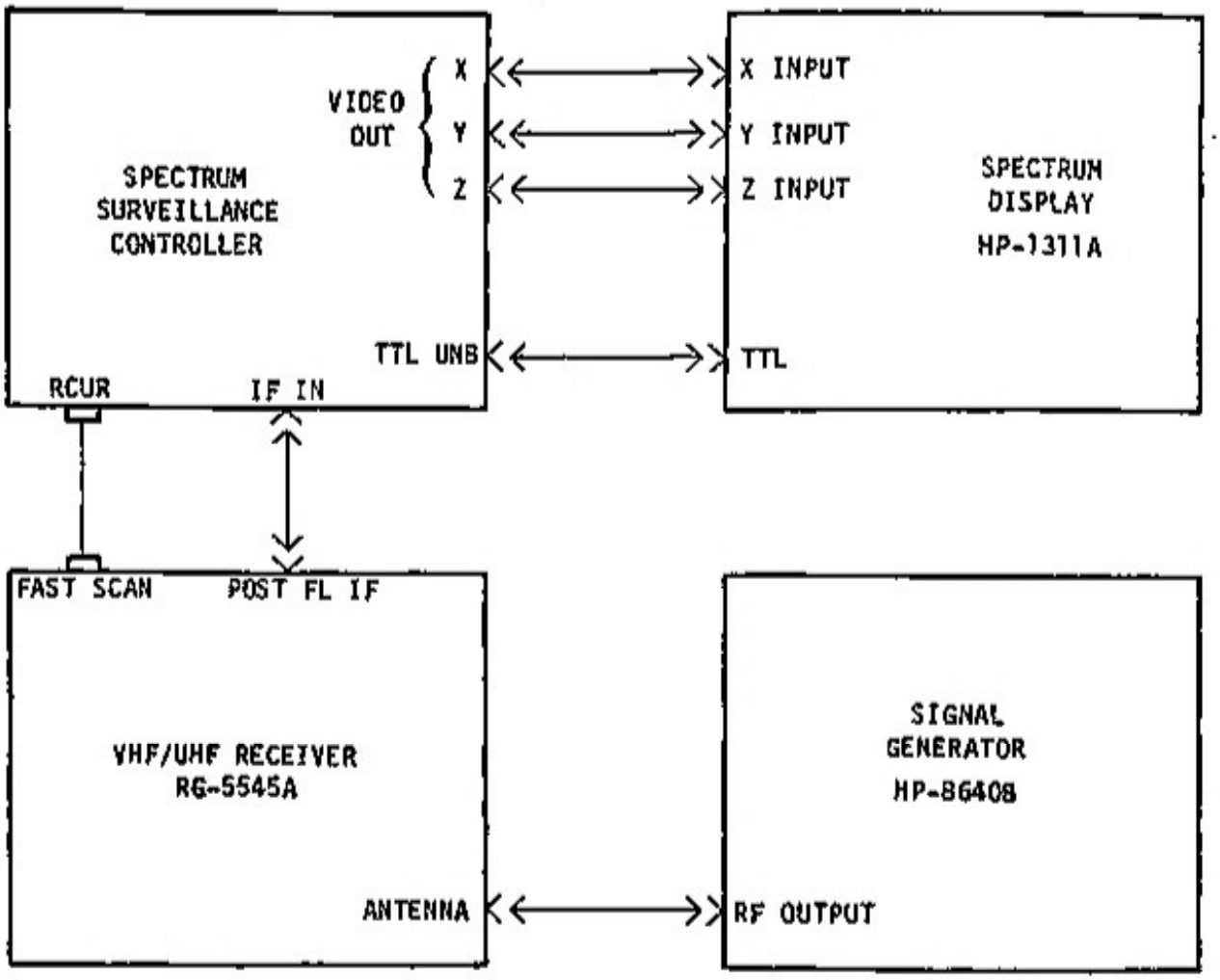


Figure 5-8. Fast Scan Mode Test Set-up

6. Set up Spectrum Surveillance Controller front panel controls to obtain a display as shown in Figure 5-9 as follows:

AVERAGING	Off
Scan time	80 msec
IFBW	100 kHz
Start Frequency	245.00000 MHz
Stop Frequency	255.00000 MHz

NOTE

The Receiver frequency should be blank and the FAST SCAN annunciator should be illuminated. Actuation of any control on the Receiver front panel should not have any effect on display. This concludes the fast scan test, disconnect all test equipment and turn power off.

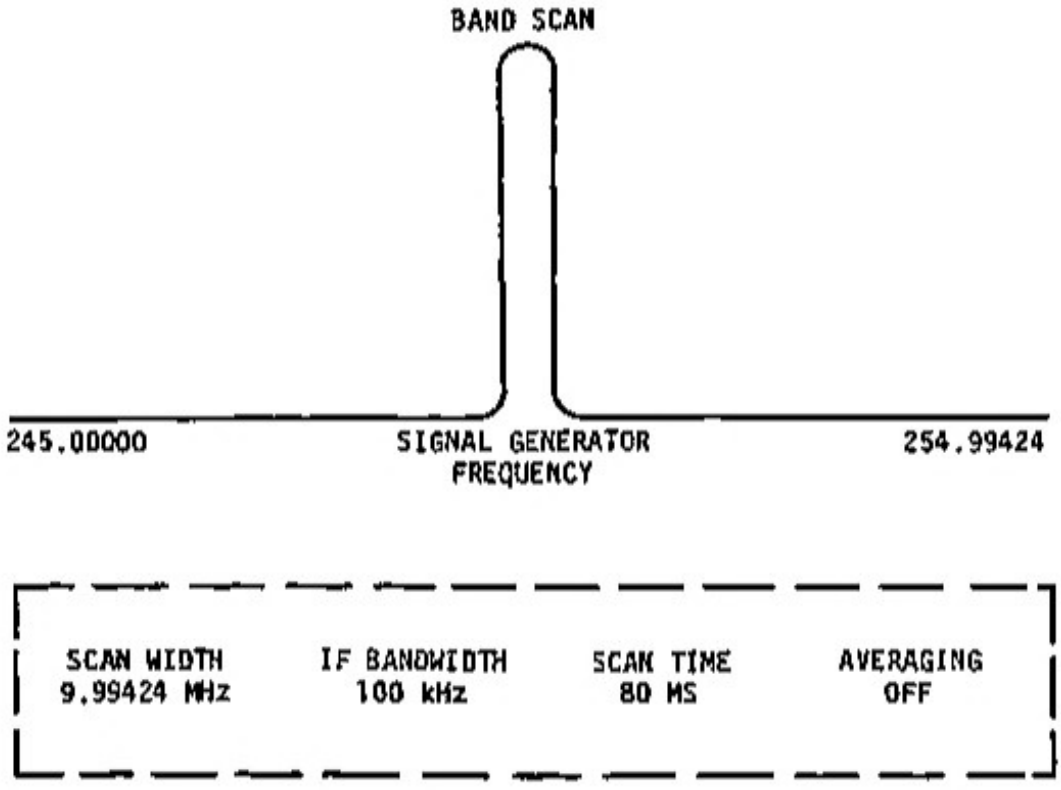


Figure 5-9. Band Scan Display

5-25. Memory Retention Test. This test checks the ability of the Receiver to retain its operating parameter settings after power interruption or power turn-off and on.

1. Depress POWER PUSH/ON switch to on position.

2. Set Receiver parameters as follows:

Frequency	450.00000 MHz
IF Bandwidth	10 kHz
Detection	AM
Gain	MGC

NOTE

Front panel indicators should indicate this above setting.

3. Depress POWER PUSH/ON switch off and on several times, ending sequence with switch on.

4. With power on, settings should remain as set in step 2 above.

5. Depress POWER PUSH/ON switch to off position.

NOTE

This concludes the memory retention test, disconnect all equipment.

5-26. TROUBLESHOOTING

5-27. This section contains troubleshooting procedures designed to isolate Receiver malfunctions to a replaceable major assembly/module and/or circuit

card/sub-assembly. Although troubleshooting of major assemblies/modules to the printed circuit card/sub-assembly level is provided in most cases, some require factory-only repair and/or replacement. These include: the tuner assembly (A3), 2nd LO module assembly (A4), IF control interface circuit card assembly (A6A1), receiver control interface circuit card assembly (A7A1), 1st LO synthesizer module assembly (A5), and reference generator module assembly (A8). The basic philosophy is to replace an entire module assembly/circuit card assembly or an easily accessible power supply or front panel component when malfunction occurs, thereby minimizing the system down-time. The procedures, contained in Table 5-3, should be used in conjunction with the performance tests of paragraph 5-12 to determine the cause of a malfunction. To correct a malfunction replace the sub-module or circuit card on which the malfunction has been isolated. When a malfunction occurs during normal service of the Receiver the following procedure is recommended.

1. Assure that all input and output cables are properly and securely con-nected at both the Receiver's rear panel and interfacing equipment (Figure 2-4).

2. Assure that all main chassis internal cables, module/assemblies and circuit card assemblies are connected properly (Figure 7-31).

3. Perform the power supply tests in paragraph 5-13.

4. Perform performance tests in paragraphs 5-14 through 5-25 as required.

5. Refer to the troubleshooting Table 5-3 and find the associated symptom as related to the malfunction or failure of the performance test.

6. Follow the procedures as set forth under possible cause and remedy in the troubleshooting table.

Table 5-3. Troubleshooting

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
1	No front panel indications when power is turned on.	1. AC power input or power supply module assembly (A1).	1. Check ac power input to Receiver. 2. Check voltage select card at rear panel for correct selection. 3. Check fuse F1. 4. Check dc outputs of power supply. Repair or replace as required.
2	Random or incorrect indications on the front panel.	1. One or more power supply outputs are absent or incorrect.	1. Check dc outputs of power supply. If all are present but incorrect, check ac input power and for proper selection through the voltage select card. 2. If some dc outputs are present and correct, but others are not, check internal components or power supply (A1). Repair or replace power supply.
3	Receiver frequency cannot be tuned from the keypad, tuning slew switch, or tuning control.	1. First LO synthesizer (A5). 2. Reference frequency (A8). 3. Second LO (A4).	1. Check for first LO level and frequency output at rear panel connector J3. 2. Check for 10 MHz reference frequency at rear panel J11. 3. Check for second LO level and frequency output at rear panel connector J6.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
3	(Cont.)	4. Receiver control (A7).	1. Replace A7A4. 2. Replace A7A2. 3. Replace A7A3. 4. Replace A7A6. 5. Replace A7A7.
4	Receiver frequency cannot be tuned from keypad but can be tuned from the tuning slew switch and tuning control.	1. Keyboard encoder (A2A2). 2. Front panel I/O control interface (A7A4).	1. Replace A2A2. 2. Replace A7A4.
5	Receiver frequency cannot be tuned from tuning slew switch and/or tuning knob but can be tuned through keypad.	1. Front panel interface (A7A4).	1. Replace A7A4.
6	Receiver will not scan or does not scan as programmed.	1. Microcomputer (A7A2).	1. Replace A7A2.
7	Scan will not stop and hold on a COR threshold.	1. Threshold is improperly set. 2. Converter (A7A8). 3. COR (A9A3).	1. Ascertain that signal level is above the preset COR threshold. 2. Replace A7A8. 3. Replace A9A3.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
8	Frequencies cannot be excluded from the scan stop.	1. Microcomputer (A7A2).	1. Replace A7A2.
9	Memory functions improperly.	1. Microcomputer (A7A2).	1. Replace A7A2.
10	No FM video output (from J5 on rear panel) when Receiver is tuned to frequency of input.	1. Cabling between power supply, audio video amplifier/COR (A9), J5, J7, J4 and J10 of rear panel, IF assembly (A6), tuner assembly (A3), first LO synthesizer assembly (A5), 2nd LO (A4), reference generator (A8), and receiver control (A7).	1. Check connections and continuity of cabling between units listed under Possible Cause.
		2. Audio video amplifier (A9A2) or control interface (A9A1).	2. If tuning meter on front panel does not indicate reading, go to next step. If tuning meter indicates reading, replace audio video amplifier (A9A2) or control interface (A9A1).
		3. IF filter amplifier (A6A3, A6A4, A6A5 or A6A6).	3. Switch to another IF bandwidth (thereby switching to a different IF filter amplifier). If there is still no FM VIDEO output, replace IF filter amplifier card which was originally connected.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
10	(Cont.)	4. No IF Output.	4. Measure IF output at J4 of rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately -10 dBm. If no or an improper signal is obtained, go to Item 2 of this table. If there is a proper signal, replace each IF filter amplifier (A6A3-A6A6), one at a time, until FM VIDEO output appears. If, after all four IF filter amplifiers have been replaced, the FM VIDEO still does not appear, go to next step.
		5. Preselector controller (A7A7).	5. Replace preselector controller (A7A7).
		6. Microcomputer control operation.	6. If step 5 above does not clear fault, in turn, replace microcomputer (A7A2), address decoder (A7A6), and converters card (A7A8) until fault is cleared.
11	No IF output (from J4 on rear panel) when Receiver tuned to frequency of input signal.	1. Variable Gain Amplifier (A6A2).	1. Measure post-filter IF output at J7 on rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately -10 dBm. If there is a correct signal, replace the variable gain amplifier (A6A2). If there is no correct signal, go to next step.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
11	(Cont.)	2. IF filter amplifier (A6A3, A6A4, A6A5, A6A6).	2. Measure pre-filter IF output at J10 at rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately 0 dBm. If there is a correct pre-filter IF output, replace the IF filter amplifier containing the switched in bandwidth filter.
12	No pre-filter IF ouput (from J10 on rear panel when Receiver tuned to frequency of input signal.	1. Reference generator (A8).	1. Check that the reference is at INT or, if at EXT, assure that an external reference is connected. Check for correct reference generator (A8) operation. Measure the reference error voltage, using the digital voltmeter (Item 1 of Table 5-2), at terminal 12 of TB1 on rear panel). This should be 0 ± 5.0 volts. If this is correct, replace reference generator (A8).
		2. 2nd LO (A4).	2. Measure 2nd LO signal into tuner (A3) terminal J3. Disconnect W2P3 from tuner (A3) terminal J3 and measure signal from this cable connector. Use the counter and RMS voltmeter (Items 12 and 9 of Table 5-2) to measure the frequency and amplitude. The frequency should be 640 MHz and the amplitude approximately 0 to + 5 dBm. If this signal is correct, reconnect W2P3 and go on to next step. If this signal is not correct, replace the 2nd LO card (A4).

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
12	(Cont.)	3. First LO synthesizer (A5).	3. Measure first LO synthesizer output at J3 on rear panel. Use the frequency counter and RMS voltmeter (Items 12 and 9 of Table 5-2) to measure the frequency and amplitude of this output. This should be equal to the tuned frequency plus 661.4 MHz with amplitude approximately -3 to + 5 dBm. If the correct signal is present, go to next step. If the correct signal is not present, replace the first LO synthesizer assembly (A5).
		4. Tuner (A3).	4. If steps (1), (2) and (3) do not clear fault, replace tuner assembly (A3).
		5. Preselector controller (A7A7).	5. If step (4) does not clear fault, replace preselector controller (A7A7).
		6. Microcomputer control operation.	6. If step (5) does not clear fault, replace microcomputer (A7A2), address decoder (A7A6), and converter (A7A8) until the fault is cleared.
13	No video output (from J8 on rear panel) when Receiver in FM mode and tuned to frequency of input signal.	1. Audio video amplifier (A9A2) or control interface (A9A1).	1. Check for output from FM VIDEO (J5 on rear panel). If output is obtained, replace audio/video amplifier (A9A2) or control interface (A9A1). If output is not obtained go to Item 1 of this table.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
14	No video output (from J8 on rear panel) when Receiver in AM mode and tuned to frequency signal of input signal.	1. No IF output.	1. Measure output at J4 at rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately 0 dBm. If no, or an improper signal is obtained, go to Item 2 of this table. If the correct signal is obtained, go to next step.
		2. Cabling between power supply (A1), audio video amplifier/ COR (A9), IF assembly (A6), and receiver control (A7).	2. Check connections and continuity of cabling between units listed in Possible Cause.
		3. Audio/Video Amplifier/COR (A9)	3. If (2) above does not clear fault, replace audio video amplifier/COR (A9).
		4. IF filter amplifiers (A6A3, A6A4, A6A5, A6A6)	4. Switch to another IF bandwidth (thereby switching to a different IF filter amplifier) If there is now a video output, replace IF filter amplifier (A6A3-A6A6) which was originally connected. If there is still no video output, go to next step.
		5. Preselector controller (A7A7).	5. Replace preselector controller card (A7A7).
		6. Microcomputer control operation.	6. If (5) above does not clear fault, replace microcomputer (A7A2), address decoder (A7A6), and converter (A7A8) until fault is cleared.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
15	No VIDEO output (from J8 at rear panel) when Receiver is in CW mode and tuned to frequency of input signal.	1. No IF output.	1. Measure IF output at J4 on rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately 0 dBm. If no or improper signal is obtained, go to Item 2 of this table. If there is a proper signal go to next step.
		2. Cabling between power supply (A1), audio video amplifier/ COR (A9) and IF (A6).	2. Check connections and continuity of cabling between units listed under Possible Cause.
		3. CW demodulator (A6A7).	3. If steps 1 and 2 do not clear fault, replace CW demodulator (A6A7).
		4. Audio video amplifier (A9A2) or control interface (A9A1).	4. Replace audio video amplifier (A9A2) or control interface (A9A1).
		5. Preselector controller (A7A7).	5. If step (4) above does not clear fault, replace preselector controller card (A7A7).
		6. Microcomputer control operation.	6. If step (5) does not clear fault, in turn replace microcomputer (A7A2), address decoder (A7A6), and converter (A7A8) until fault is cleared.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
16	Proper video output (from J8 or rear panel) but no or improper outputs from audio 1 or audio 2 at TB1 or headphones 1 or 2 (tip or ring) when Receiver is tuned to frequency of input signal.	1. Audio video amplifier (A9A2) or control interface (A9A1).	1. Replace audio video amplifier (A9A2) or control interface (A9A1).
17	No or incorrect push-button key-switch key LED indicator when a front panel key-switch is pressed (Slew and knob tuning indicates correctly on frequency display.	1. Cabling between power supply (A1), front panel (A2), and receiver control (A7).	1. Check connections and continuity of cabling between units listed in Possible Cause.
		2. Keyboard (A2A1).	2. Replace keyboard (A2A1).
		3. Keyboard decoder (A2A2).	3. If (2) above does not clear fault, replace keyboard decoder (A2A2).
		4. Display driver (A7A5).	4. If (3) above does not clear fault, replace display driver (A7A5).
18	Incorrect frequency display during slew tuning (keyswitches and knob tuning indicators operated correctly.)	1. Cabling between front panel (A2) and receiver control (A7).	1. Check connections and continuity of cabling within front panel (A2) (see Figure 7-2) and between front panel and receiver control (A7).
		2. Switches S2 and/or S3.	2. Replace switch S2 or S3 if faulty.

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
19	Incorrect frequency display during tuning control knob tuning (key switches and slew tuning indicators operate correctly).	1. Cabling between front panel (A2) and receiver control (A7).	1. Check connections and continuity of cabling within front panel (A2) (see Figure 7-2) and between front panel and receiver control (A7).
		2. Tuning control shaft encoder.	2. Replace tuning control shaft encoder if faulty.
20	No frequency display or annunciator display operation (keyswitches and LED displays operate correctly.)	1. Cabling between front panel (A2) and receiver control (A7).	1. Check connections and continuity of cabling within front panel (A2) (see Figure 7-2) and between front panel and receiver control (A7).
		2. Display (A2A3).	2. Replace display card (A2A3).
		3. Display driver (A7A5).	3. If (2) above does not clear fault, replace display driver (A7A5).
21	Incorrect operation of front panel keyswitches and slew tuning and control tuning indicators.	1. Cabling between power supply, (A1), front panel (A2), and receiver control (A7).	1. Check connections and continuity of cabling between units listed in Possible Cause.
		2. Front panel I/O control interface (A7A4).	2. Replace front panel I/O control interface (A7A4).
		3. Microcomputer (A7A2).	3. If (2) above does not clear fault, replace microcomputer (A7A2).
		4. Address decoder (A7A6).	4. If (3) above does not clear fault, replace address decoder (A7A6).

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
21	(Cont.)	5. Converter (A7A8).	5. If (4) above does not clear fault, replace converter (A7A8).
		6. Display driver (A7A5).	6. If (5) above does not clear fault, replace display driver (A7A5).
22	Faulty remote computer/controller operation.	1. Remote computer/controller.	1. Perform remote control operation performance test as described in paragraph 5-23 of the Performance Tests. If this test is satisfactory, fault lies in remote computer/controller, or in cabling from remote computer to IEEE-488C remote control interface connector J16 on Receiver rear panel. Assure sound connections and that remote computer is operating satisfactorily. If remote computer control performance test is unsatisfactory, go to next step.
		2. Cabling within Receiver between J16 (rear panel), receiver control (A7), power supply (A1) and connections within receiver control (A7).	2. Check connections and continuity of cabling between J16, receiver control (A7) and the power supply (A1) (see Figure 7-31). Check connections between receiver control (A7).
		3. IEEE-488C remote control interface (A7A9).	3. Replace IEEE-488C remote control interface (A7A9).
		4. Microcomputer (A7A2).	4. If (3) above does not clear fault, replace microcomputer (A7A2).

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
22	(Cont.)	5. Address decoder (A7A6).	5. If (4) above does not clear fault, replace address decoder (A7A6).
23	Faulty fast scan operation (when Spectrum Surveillance Controller used.)	1. Cabling within Receiver between J15 (rear panel), power supply and receiver control (A7), and connections within receiver control (A7).	1. Check connections and continuity of cabling between J15, receiver control (A7) and power supply (A1).
		2. IF output.	2. Measure IF output from J4 at rear panel (with Receiver tuned to input signal). If no signal, go to Item 2 of this Table. If there is a signal go to next step.
		3. Front panel I/O control interface (A7A4).	3. Replace front panel I/O control interface (A7A4).
		4. Microcomputer (A7A2).	4. If (3) above does not clear fault, replace microcomputer (A7A2).
		5. Address decoder (A7A6).	5. IF (4) above does not clear fault, replace address decoder (A7A6).
		6. Converter (A7A8).	6. If (5) above does not clear fault, replace converter (A7A8).
		7. Preselector controller (A7A7).	7. If (6) above does not clear fault, replace preselector controller (A7A7).

Table 5-3. Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
24	No memory retention of Receiver settings after power turned off and back on.	1. Microcomputer (A7A2).	1. Replace microcomputer (A7A2).

5-28. REMOVAL/REPLACEMENT

5-29. The Receiver circuits are subordinated as assemblies/module assemblies, or circuit card assemblies within an aluminum chassis with top and bottom covers. Access to the assemblies is achieved by removing the top and/or bottom cover, then performing the appropriate procedure for the assembly to be accessed as described below.

a. Power Supply Module Assembly (A1). The power supply module assembly is housed in its own compartment in the Receiver chassis. To gain access to the power supply module assembly circuits, remove six screws securing the top plastic cover and remove the cover. If circuit card assemblies or other components are to be removed from the compartment, their leads must be disconnected or unsoldered and the screws holding the component to the chassis removed.

b. Front Panel Assembly (A2). In addition to front panel controls, indicators, a keyboard decoder, tuning encoder and display are contained on the rear of the front panel assembly. To gain access to circuits on the rear of the assembly or to remove any assembly/component perform the procedures as follows:

1. Remove optional Spectrum Display (when fitted) from Receiver by loosening two captive screws securing unit and sliding out of compartment.

2. Remove two screws, located behind Spectrum Display front panel, from the front panel of the Receiver.

3. Remove four allen-head screws securing two handles and front panel to Receiver chassis, then disconnect P27 from A2P1, P29 from A2P3, and P31 from A2P5.

4. Disconnect assembly/component (as appropriate) to be removed, then remove screws and/or nuts securing assembly/component to the front panel and remove.

c. Tuner Assembly (A3). The tuner assembly comprises five sub-assemblies A3A1, A3A2, A3A3, A3A4 and A3A5. To remove any one or all of the sub-assemblies perform the procedures as follows:

NOTE

The Receiver must be positioned so that connectors and mounting screws can be removed from the bottom while the sub-assembly is removed from the top.

1. Remove connectors of sub-assembly input and output cables.

2. Remove mounting screws of sub-assembly from bottom of Receiver, then remove sub-assembly from top.

3. To gain access to sub-assembly circuits, remove screws (as appropriate) securing cover, and remove cover.

d. Second LO Module Assembly (A4). The second LO is contained in a module assembly with removable covers and is secured to the Receiver chassis with two screws. To gain access to this module assembly perform the procedures as follows:

1. Unscrew plug P4 from connector J2, disconnect plug P10 from connector J1, and plug P24 from module assembly.

2. Remove two screws from bottom of module assembly and remove module from top of Receiver.

NOTE

If adjustment or voltage measurements are to be made with the module assembly connected in the system, proceed with steps 3 through 5.

3. Remove six screws securing either cover to module assembly and remove cover, being careful not to misplace floating standoffs.

4. Turn Receiver bottom side up, then place module assembly on Receiver near its compartment with insulating pad between Receiver and module assembly.

5. Reconnect plugs removed in step 1.

e. First LO Synthesizer Module Assembly (A5). The first LO synthesizer is contained in a module assembly with a sealed cover and secured to the Receiver chassis with four knurled screws. The sealed cover should not be removed for any type of field maintenance. The module should be removed from the Receiver and returned to the factory for service. To remove the module from the Receiver, perform the procedures as follows:

1. Disconnect plug P4 from connector J1, plug P25 from connector J2, plug P2 from connector J3, and plug P12 from connector J4.

2. Remove four knurled screws from bottom of module assembly and remove module assembly from top of Receiver.

CAUTION

Do not attempt to remove the sealed cover. The unit must be returned to the factory for all servicing.

f. IF Assembly (A6). The IF assembly consists of an IF control interface (A6A1), and eight plug-in circuit card assemblies A6A2 through A6A9. The IF control interface (A6A1) is accessed from the bottom of the Receiver by removing a cover over the circuit card secured with six screws. The circuit cards are accessed from the top of the Receiver by removing a cover secured by four screws. The cards may be removed by using a circuit card puller (to pull them from the Receiver) and may be serviced in-circuit using a circuit card extender (see Table 5-2).

g. Receiver Control Assembly (A7). The Receiver control assembly consists of eight plug-in circuit cards, A7A1, A7A2, A7A4-A7A9. The circuit

cards are accessed from the top of the Receiver and may be removed by using a circuit card puller. The cards may be serviced in-circuit by using a circuit card extender (see Table 5-2).

h. Reference Generator Module Assembly (A8). The reference generator module assembly is contained in a compartment at the rear of the Receiver. To remove this module disconnect plug P7 from connector J2, plug P9 from connector J4 and plug P11 from connector J3, plug P15 from connector J6, plug P18 from connector J7, and plug P47 from connector J47, then remove the screws securing module assembly to the chassis and remove the module assembly.

i. Audio Video Amplifier/COR (A9). The audio video amplifier/COR assembly consists of three circuit card assemblies which include: audio video amplifier control interface (A9A1), audio video amplifier (A9A2), and COR (A9A7). The audio video amplifier (A9A2) is contained on the plug-in circuit card audio video control interface (A9A1) that is accessed from the top of the Receiver. The audio video amplifier and COR may be removed by using a circuit card puller and may be serviced in-circuit by using a circuit card extender.

5-30. ALIGNMENT PROCEDURES

5-31. The alignment procedures are designed to permit alignment of any one or all of the various functions in the Receiver; however, the adjustment in some functions interacts with other functions so that care must be taken when any one function alone is aligned. The alignment procedures require that external power be connected to the Receiver, that Receiver power be on, and that the power mode, bandwidth, AGC, and frequency be set as described in each procedure. Except where noted in each procedure, the circuit card assembly being adjusted must be extended for access to the adjusting controls. The extender card is listed in Table 5-2 under test equipment.

5-32. TUNER ASSEMBLY (A3) ADJUSTMENTS. The tuner assembly contains four sub-assemblies which require adjustment at the factory when performance charasteristics are not satisfactory, and/or when installed in the Receiver after replacement as a result of troubleshooting to ensure proper operation. These adjustments include: VHF preselector (A3A2), UHF preselector (A3A4), VHF tuner (A3A2), and UHF tuner (A3A4). These adjustments cannot be accomplished

using the receiver as a test bed. The technical complexity of inputs and outputs to the tuner assembly, fragility of interconnecting wiring, in accessibility of adjustments in the assembly, and chances of shorting electrical circuitry, all contribute to the necessity of using a test fixture, designed by the equipment manufacturer, in order that adjustments be made. For these reasons, if any of the above mentioned assemblies is suspected of malfunctioning, it is necessary to return the assembly to the factory for test, adjustments, repair, and/or other required maintenance. In such event, contact Racal Communications, Inc., to obtain disposition instructions for servicing.

5-33. SECOND LO MODULE ASSEMBLY (A4) ADJUSTMENTS. The second LO contains three sub-assemblies of which one, the 640 MHz oscillator circuit card assembly (A4A1) integrates a fine tuning trimmer capacitor C111. This adjustment is a factory adjustment which may not be implemented in the field due to this components in accessability.

5-34. FIRST LO SYNTHESIZER MODULE ASSEMBLY (A5) ADJUSTMENTS. The first LO synthesizer module assembly contains three sub-assemblies which require adjustment when performance characteristics are not satisfactory, and/or when installed in the Receiver after replacement as a result of troubleshooting to ensure proper operation. These adjustments include: VCO A (A5A1), VCO B (A5A5), and digiphase processor (A5A3). However, the only assembly that may be adjusted is the digiphase processor (A5A3). The VCO's A and B are sealed units, which must not be opened in the field and it should also be noted, that these adjustments cannot be accomplished using the receiver as a test bed. The technical complexity of inputs and outputs to the first LO synthesizer module assembly, fragility of interconnecting wiring, in acessibility of adjustments in the assembly and chances of shorting electrical circuitry all contribute to the necessity of using a test fixture, designed by the equipment mnaufacturer, in order that the adjustments be made. For these reasons, if either the VCO A or VCO B is suspected of malfunctioning it is necessary to return the assembly to the factory for test, adjustment, repair, and/or other required maintenance. In such event, contact Racal Communications, Inc. to obtain disposition instructions for servicing.

5-35. Digiphase Processor (A5A3) Adjustment. The digiphase processor must be extended from the Receiver to perform these adjustments.

1. Set Receiver front panel controls as follows:

Frequency	44.601 MHz
Detection Mode	CW (1 kHz)
IF Bandwidth	10 kHz

2. Connect signal generator to ANTENNA connector J1 on Receiver rear panel.

3. Adjust signal generator controls to obtain a frequency of 44.601 MHz and output level of -25 dBm.

4. Connect spectrum analyzer to IF OUT connector J4 on Receiver rear panel.

5. Adjust spectrum analyzer controls to obtain a 21.4 MHz center frequency and span of 10 kHz.

6. On digiphase processor, connect RMS voltmeter between TP1 and ground.

7. Adjust potentiometer R42 to obtain -4.5 VDC reading on RMS voltmeter.

8. Tune Receiver and signal generator to obtain a frequency of 484.601 MHz.

9. Adjust potentiometer R39 to obtain -3.0 VDC reading on RMS voltmeter.

10. Repeat step 1, then connect TP2 to ground and disconnect RMS voltmeter.

11. While observing spectrum analyzer, adjust potentiometer R42 to obtain minimum amplitude of 500 Hz and 1 kHz.

NOTE

This concludes the digiphase processor adjustment, disconnect all test equipment and install digiphase processor in the Receiver.

5-36. IF ASSEMBLY (A6). The IF assembly contains six sub-assemblies which require adjustment when performance characteristics are not satisfactory, and/or when installed into the Receiver after replacement as a result of troubleshooting, to ensure proper operation. These adjustments include: variable gain amplifier (A6A2), IF filter amplifiers (A6A3-A6A6), and CW demodulator (A6A7).

5-37. Variable Gain Amplifier Adjustments (A6A2). The variable gain amplifier must be extended from the Receiver for adjustment. Perform the following procedures for adjustment.

1. Adjust R95 to full clockwise position and potentiometer R81 to full counter-clockwise position.

2. Connect signal generator to ANTENNA connector J1 on Receiver rear panel and adjust for 21.4 MHz at -105 dBm level.

3. Adjust Receiver frequency to 21.400 MHz, mode to CW, and MGC with zero attenuation.

4. Connect spectrum analyzer to IF OUT connector J4 on Receiver rear panel.

5. Set spectrum analyzer controls to display 21.4 MHz signal at approximately -10 dBm.

6. Adjust R76 fully clockwise, then counter-clockwise until gain just begins to drop.

7. Adjust signal generator output level to -75 dBm.

8. Select AGC FAST and adjust potentiometer R37 for a -10 dBm display on spectrum analyzer.

9. Adjust signal generator output level to -50 dBm.

10. Disconnect spectrum analyzer from IF OUT connector J4 and connect to PRE-FL IF connector J10 on Receiver rear panel.

11. Adjust potentiometer R81 for -25 dBm ±1 dB, then adjust R95 until gain just begins to drop.

12. Disconnect spectrum analyzer from PRE FL IF J10 and reconnect to IF OUT J4.

13. Adjust signal generator from 0 dBm to -100 dBm and verify that output level remains at approximately -10 dBm, then readjust signal generator to -105 dBm and verify that output is at least -16 dBm.

NOTE

This concludes the variable gain amplifier adjustments, disconnect all test equipment and install variable gain amplifier in Receiver.

5-38. IF Filter Amplifier (A6A3-A6A6) Adjustments. The IF filter amplifier being adjusted must be extended from the Receiver for these adjustment procedures.

1. Select appropriate bandwidth on Receiver front panel for IF filter amplifier being adjusted, then press MGC pushbutton keyswitch (associated LED indicator lit) and set RF GAIN until level meter reads full scale.

2. Connect digital multimeter to A2TP1.

3. Adjust A2R12 for a 155 ± 1 millivolt indication on digital multimeter.

4. Connect signal generator to ANTENNA connector J1 on Receiver rear panel J1 and adjust for 21.40 MHz CW signal at -60 dBm.

5. Set Receiver frequency to 21.40 MHz, and mode to CW.

6. Connect spectrum analyzer to IF OUT connector J4 and adjust RF GAIN slew switch to obtain -10 dBm reading on spectrum analyzer.

7. Connect digital multimeter to pin 27/67 on the IF filter amplifier and set for dc volts.

8. Adjust R2 fully clockwise.

9. Adjust A2L3 for maximum dc indication on digital multimeter, then adjust A2L2 for maximum dc indication on digital multimeter.

10. Repeat step 9 as required to obtain maximum dc indication on digital multimeter.

11. Reconnect digital multimeter to pin 26/66 and re-adjust A2R2 for a 750 ±7 millivolt indication on the multimeter.

12. Disconnect digital multimeter from pin 26/66 and connect to pin 5 of U8.

13. Select FM mode and AGC SLOW at Receiver front panel.

14. Adjust OFF-CENTERED tuning screw, located inside discriminator housing to obtain a minimum digital multimeter indication.

15. Connect oscillator output of distortion analyzer to EXT FM input of signal generator.

16. Set output amplitude of distortion analyzer to 1 volt rms and signal generator to FM AC.

17. Adjust distortion analyzer frequency and signal generator peak deviation for IF filter amplifier being adjusted as shown below.

IF BANDWIDTH	OSCILLATOR FREQUENCY	GENERATOR DEVIATION
10 kHz	400 kHz	4 kHz
20 kHz	1 kHz	8 kHz
50 kHz	1 kHz	20 kHz
100 kHz	1 kHz	40 kHz
200 kHz	1 kHz	80 kHz
400 kHz	1 kHz	160 kHz

18. Connect FM VIDEO at plug P1 pin 22 to distortion analyzer input.

19. Adjust CENTER tuning screw, located on the discriminator housing, for minimum distortion indication.

20. Set distortion analyzer to input level, then adjust A3L2 for maximum voltage indication.

21. Adjust potentiometer R40 for a 400 millivolt rms indication on distortion analyzer.

22. Set signal generator to CW, then disconnect distortion analyzer from FM VIDEO at plug P1 pin 22.

23. Connect digital multimeter to FM DISCRIM pin 23 of plug P1 and adjust for dc volts.

24. Adjust potentiometer R53 for minimum dc indication on digital multimeter.

NOTE

An indication of 0 volts dc should be obtainable. This concludes the IF filter amplifier adjustments, disconnect all test equipment, and install the IF filter amplifier into the Receiver.

5-39. CW Demodulator Adjustments (A6A8). The CW Demodulator must be extended from the Receiver to perform these adjustment procedures.

1. Connect oscilloscope to pin 7/8 of U6 on CW demodulator.

2. Adjust variable coil L3 for a plus 5 to 10 volts dc indication on oscilloscope.

3. Disconnect oscilloscope from pin 8 of U6 and connect to TP1.

4. Adjust variable coil L7 for maximum amplitude of displayed 19.400 MHz signal.

5. Disconnect oscilloscope from TP1 and connect it to pin 8 of U21.

6. While selecting CW from Receiver front panel, adjust variable coil L15 for 5.0 volts dc and select CW 1 kHz, then verify that voltage reading is less than 12 volts dc.

7. Connect signal generator to the ANTENNA connector J1 on Receiver rear panel and adjust for 21.400 MHz, CW at -50 dBm output level.

8. Set Receiver frequency to 21.400 MHz, mode to CW 1 kHz and press AGC FAST pushbutton key-switch (associated LED indicator on).

9. Disconnect oscilloscope from pin 8 of U21 and reconnect to pin 7 of P1.

10. Alternately adjust trimmer capacitors C2 and C6 for maximum amplitude of the 2 MHz signal.

11. Disconnect oscilloscope from pin 7 of plug P1 and reconnect to pin 14 of plug P1.

12. Adjust potentiometer R107 for 1.75 volt indication on oscilloscope.

NOTE

This concludes the CW demodulator adjustments, disconnect all test equipment and install the CW demodulator into the Receiver.

5-40. RECEIVER CONTROL ASSEMBLY (A7) ADJUSTMENTS. The receiver control assembly contains a single sub-assembly which requires adjustment when

performance characteristics are not satisfactory, and/or when installed into the Receiver after replacement as a result of troubleshooting to ensure proper operation.

5-41. Converter (A7A8) Adjustments. The converter must be extended from the Receiver to perform these adjustments.

1. Connect a lead from pin 30 (ADC1) of plug P1 to pin 40 (ground) of plug P1 on converter.

2. Connect digital multimeter between pin 7 of U5B and ground.

3. Adjust potentiometer R13 for 2.50 ± 0.02 volt indication on digital multimeter.

4. Disconnect digital multimeter from U5B and ground and remove lead from between pin 30 and pin 40 of plug P1.

5. On front panel of Receiver, select MGC, then set RF GAIN control to minimum level, and adjust potentiometer R9 for full scale deflection on front panel LEVEL meter.

6. Connect digital multimeter between terminal E13 (AGC) on A3A1 and ground.

7. Adjust potentiometer R12 for a 12.8 ± 0.1 volt indication on digital multimeter.

8. Disconnect digital multimeter from between E13 and ground on A3A1.

9. Connect oscilloscope and digital multimeter between pin 38 (DAC 1A) of plug P1 and ground.

10. Connect signal generator to ANTENNA connector J1 on Receiver rear panel and adjust for 450.00000 MHz at -50 dBm.

11. Adjust Receiver frequency to 450.00000 MHz and select 100 kHz IF bandwidth.

12. Adjust potentiometer R7 to center voltage swing on oscilloscope, 0 volt indication on digital multimeter.

13. Adjust signal generator for 450.1000 MHz at -50 dBm.

15. Adjust potentiometer R10 for full scale deflection on Receiver front panel TUNING meter.

16. Disconnect oscilloscope and digital multimeter from between pin 38 and ground.

17. Connect digital multimeter to pin 5 (COR DAC) of plug P1 on COR circuit card assembly (A9A3).

18. On Receiver front panel, enable COR THRESHOLD and set COR threshold for maximum.

19. Adjust potentiometer R11 for a 12.8 $\pm$ 0.1 volt indication on digital multimeter.

NOTE

Potentiometers R1 through R4 are not used in this Receiver application. This concludes converter adjustments, disconnect all test equipment and install converter into the Receiver.

5-42. REFERENCE GENERATOR MODULE ASSEMBLY (A8) ADJUSTMENTS. The reference generator has one trimmer capacitor C17. This adjustment is for impedance matching and is a factory adjustment only. Adjustment of trimmer capacitor C17 may not be implemented in the field due to this components in accessability.

SECTION VII

ENGINEERING DRAWINGS

7-1. INTRODUCTION

7-2. This section contains engineering drawings for the Receiver, including a main chassis assembly interconnecting wiring diagram, and the schematic and logic diagrams of the various subassemblies and sub-subassemblies, as may be applicable.

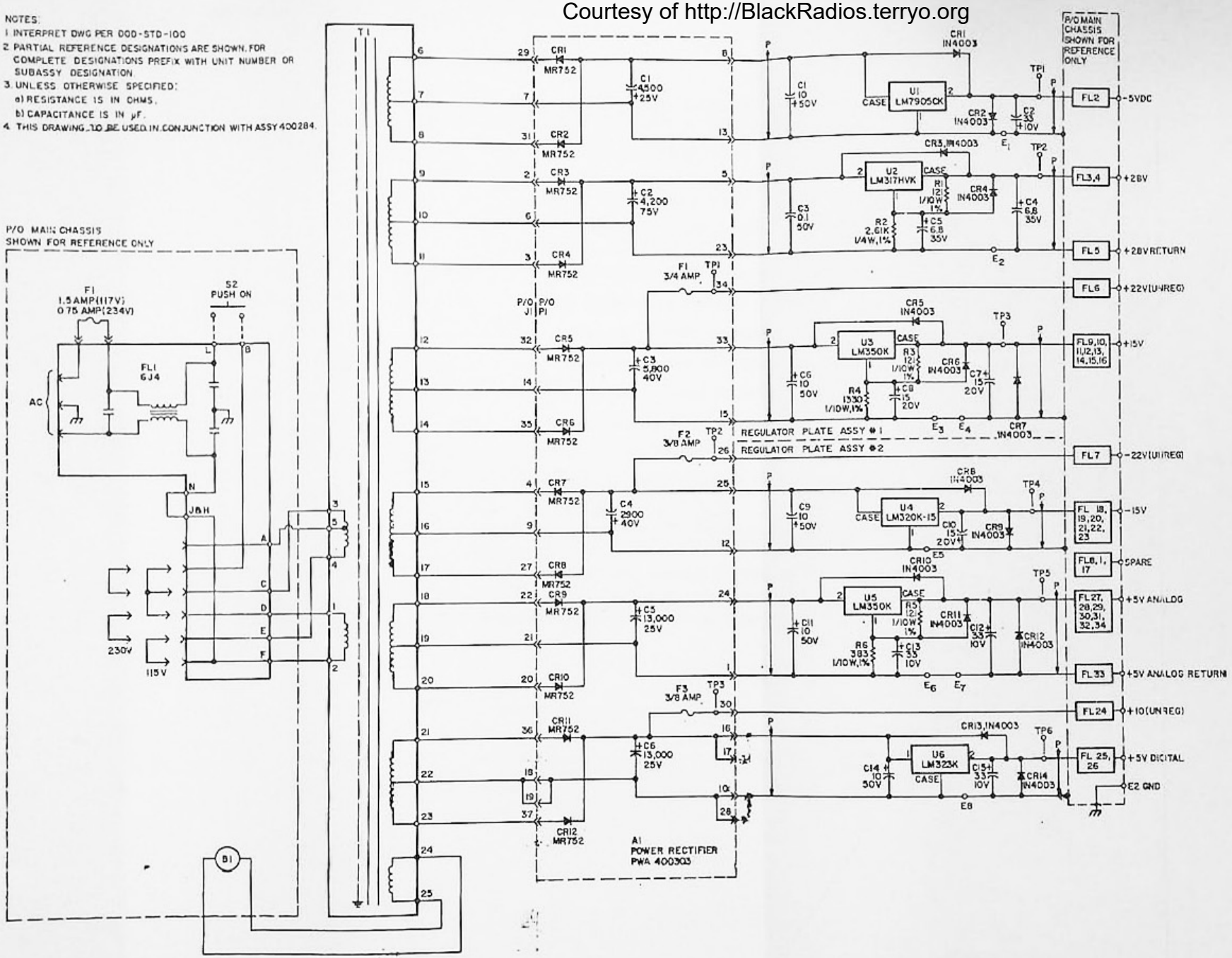
7-3. DRAWING INDEX

7-4. An index of those drawings contained in this section is provided below.

DRAWING INDEX

DRAWING INDEX (Cont.)

NOTES:
1. INTERPRET DWG PER 000-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS.
   b) CAPACITANCE IS IN μF.
4. THIS DRAWING TO BE USED IN CONJUNCTION WITH ASSY 400284.



400284	
HIGHEST REF DESIG	REF DESIG NOT USED
C15	
CR14	
R6	
TP6	
U6	
E8	

400303	
HIGHEST REF DESIG	REF DESIG NOT USED
C6	
CR12	
F3	
P1	
TP3	

Figure 7-1. Power Supply Module Assembly (A1) Schematic Diagram

NOTES:

1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 400211-2 & 400211-3
   CABLE 400240-2

4 FB DENOTES FERRITE BAND.

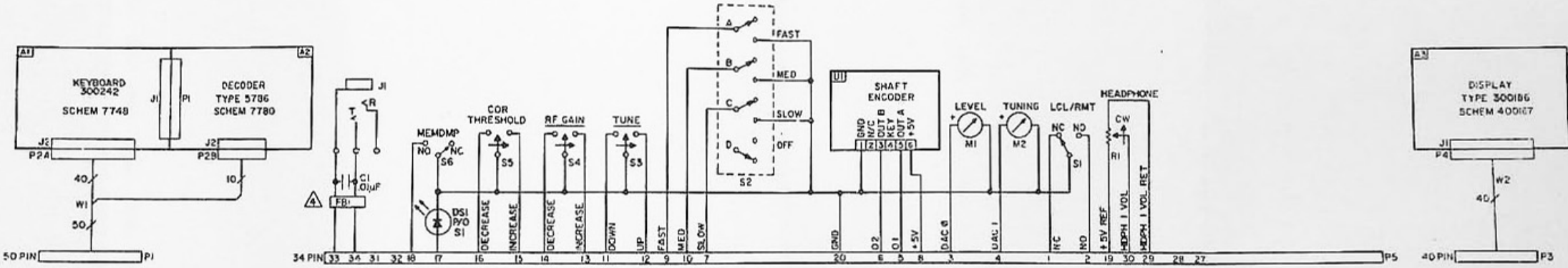
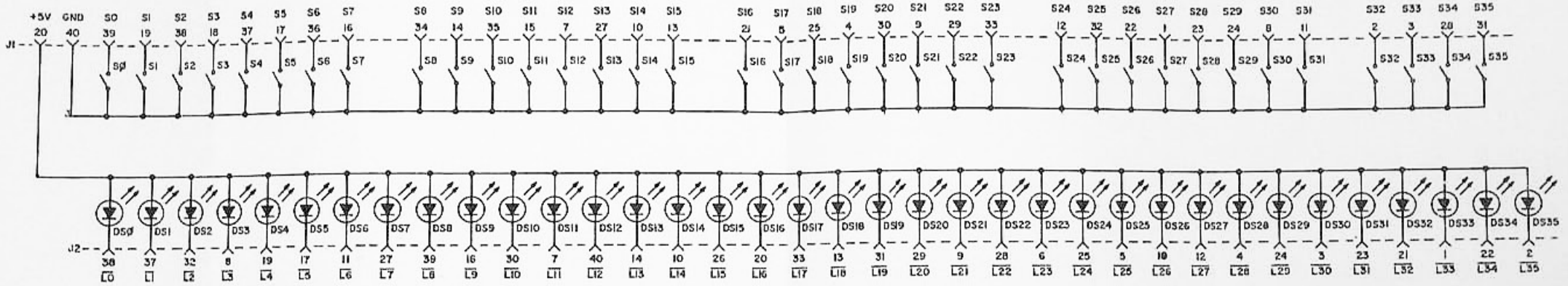


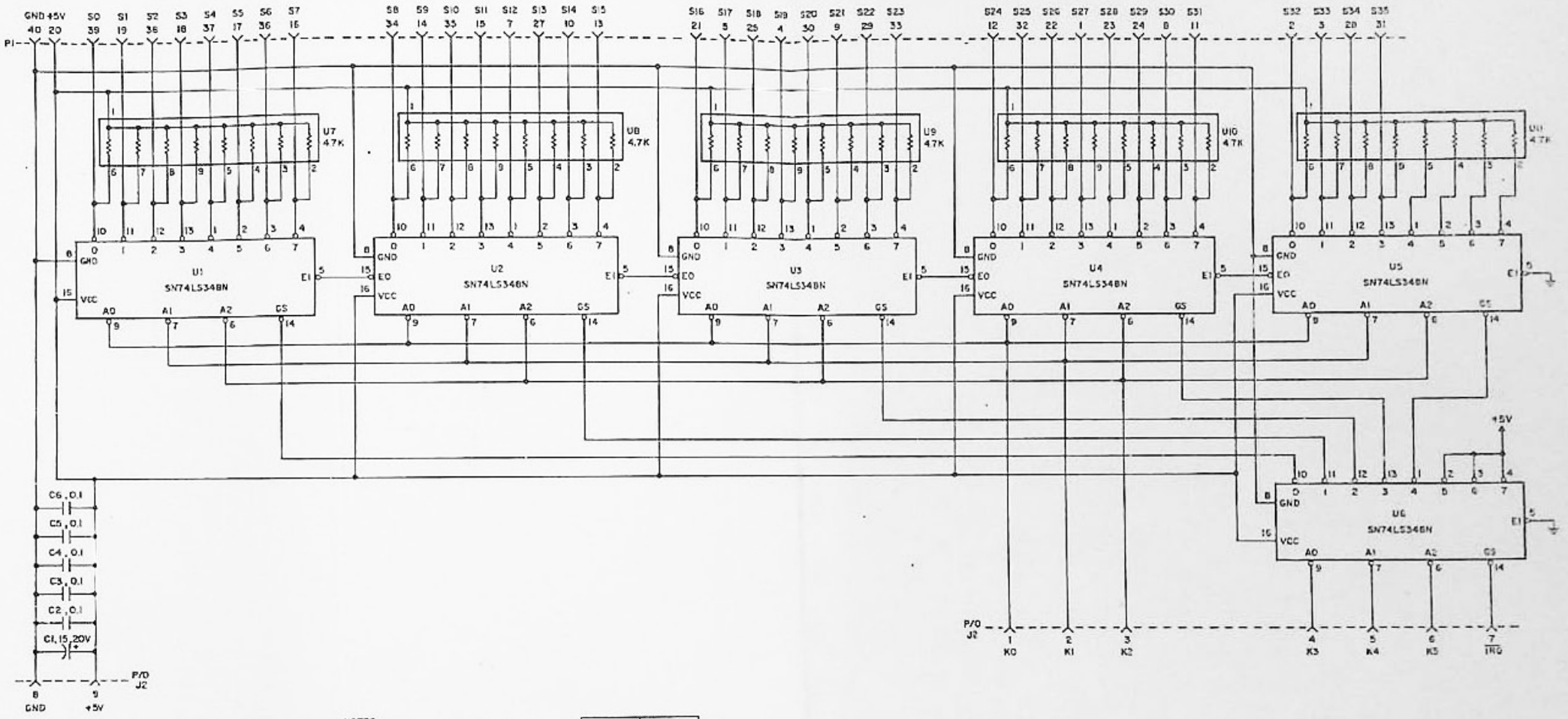
Figure 7-2. Front Panel Asssembly (A2) Schematic Diagram



NOTE: NOT ALL L.E.D's AND SWITCHES ARE INSTALLED.
REFER TO APPLICATION BLOCK FOR SPECIFIC ASSEMBLIES
AND THEIR RESPECTIVE SUB-ASSEMBLY PARTS LISTS.

HIGHEST REF DESIG	REF DESIG NOT USED
DS35	
J2	
S35	

Figure 7-3. Keyboard Assembly (A2A1) Schematic Diagram



NOTES
1. UNLESS OTHERWISE SPECIFIED:
   a) CAPACITANCE IS IN μF.
2. J1 IS P/O KEYBOARD (5755).

HIGHEST REF DESIG	REF DESIG NOT USED
C6	J1
J2	
P1	
U11	

Figure 7-4. Keyboard Decoder Circuit Card Assembly (A2A2) Schematic Diagram

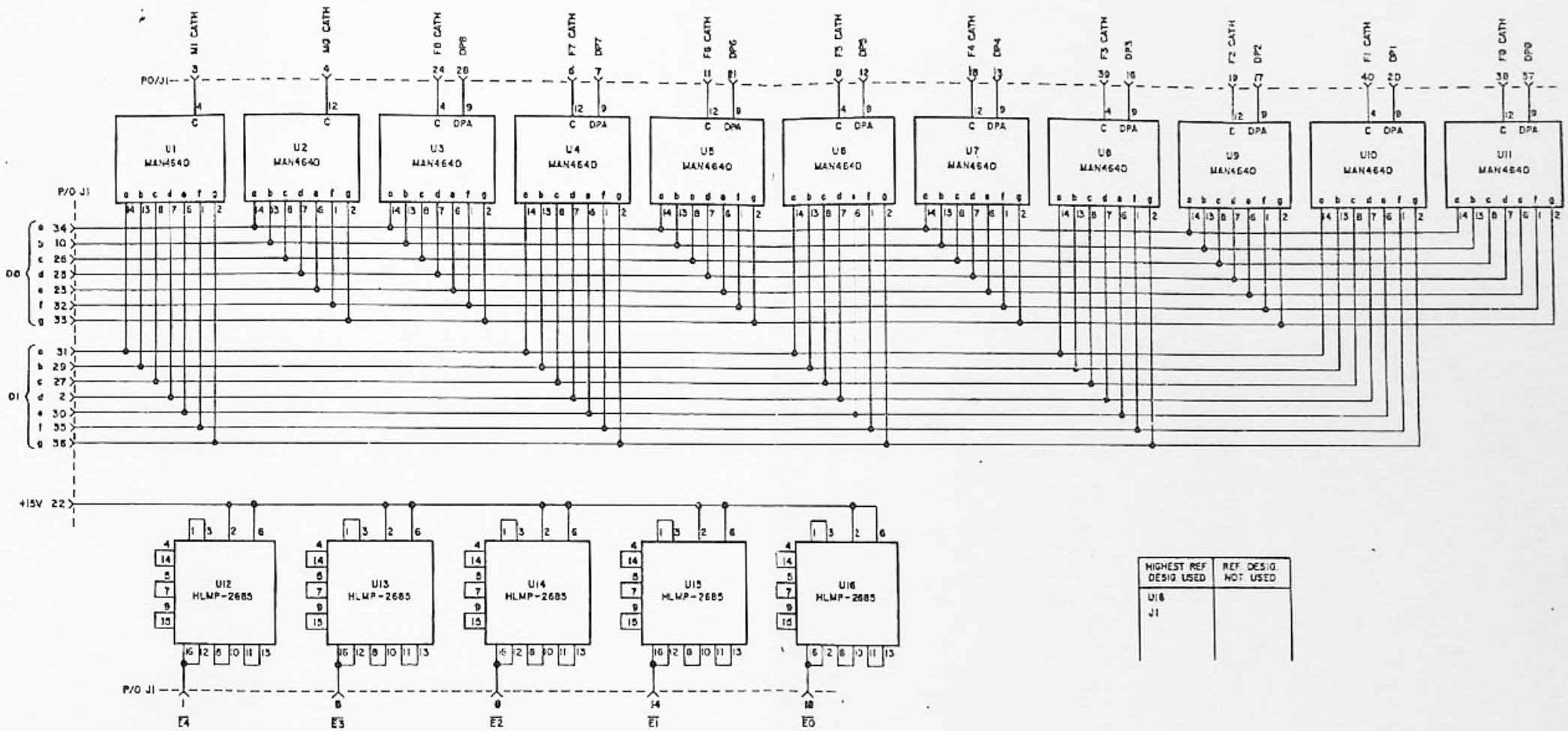


Figure 7-5. Display Circuit Card Assembly (A2A3) Schematic Diagram

NOTES:
1. INTERPRET DWG PER 000-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400205 WIRE LIST
4. LB DENOTES LOW BAND FREQUENCY RANGING FROM 20 MHz TO 500 MHz
   MB DENOTES MID BAND FREQUENCY RANGING FROM 500 MHz TO 1000 MHz
   HB DENOTES HIGH BAND FREQUENCY RANGING FROM 1000 MHz TO 1800 MHz
5. ATI IS USED ON -2 AND -3 ASSEMBLIES ONLY

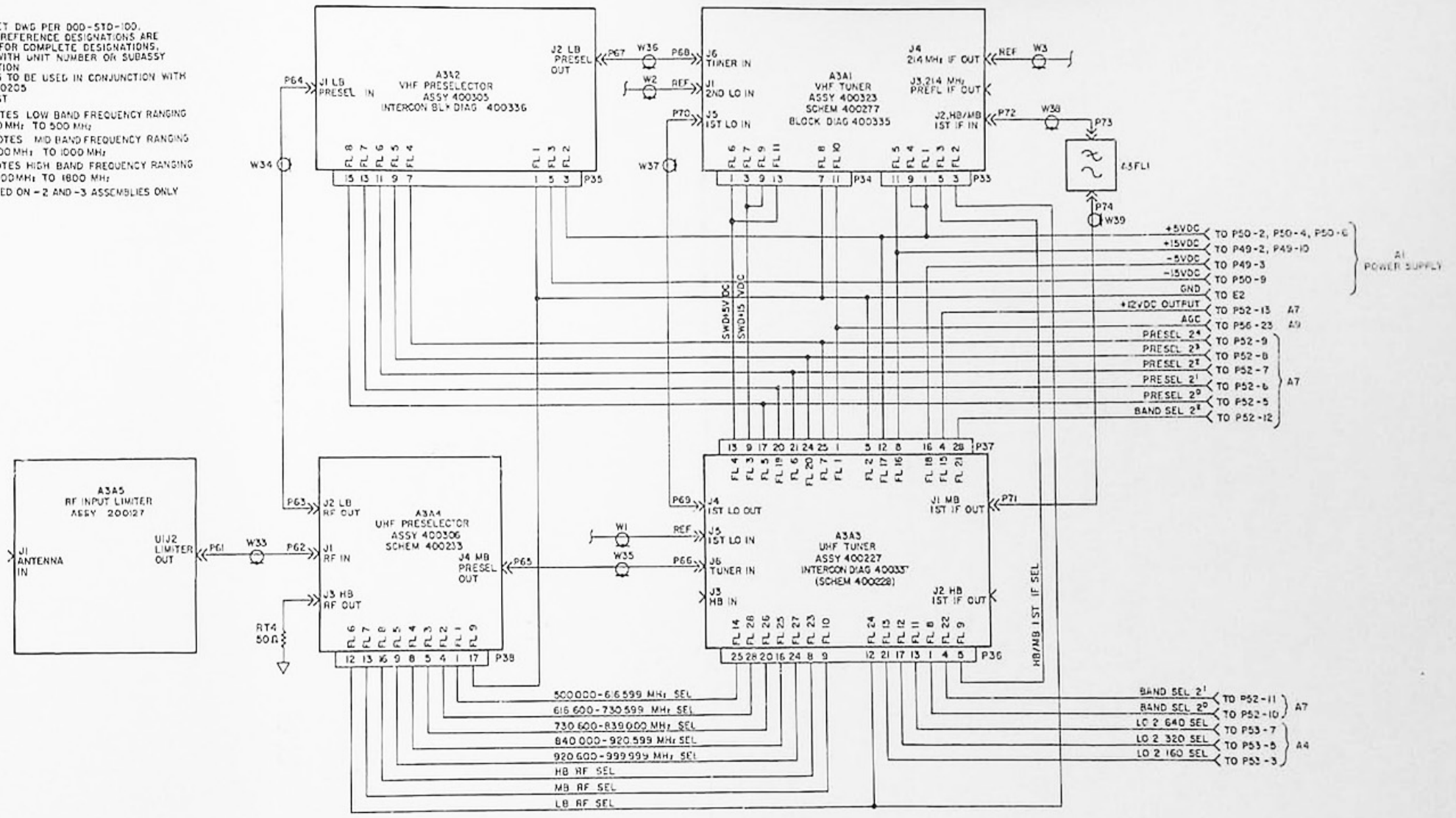


Figure 7-6. Tuner Assembly (A3) Interconnecting Wiring Diagram

NOTES

1. INTERPRET DWG PER DOD-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 400323
   SCHEMATIC 400277

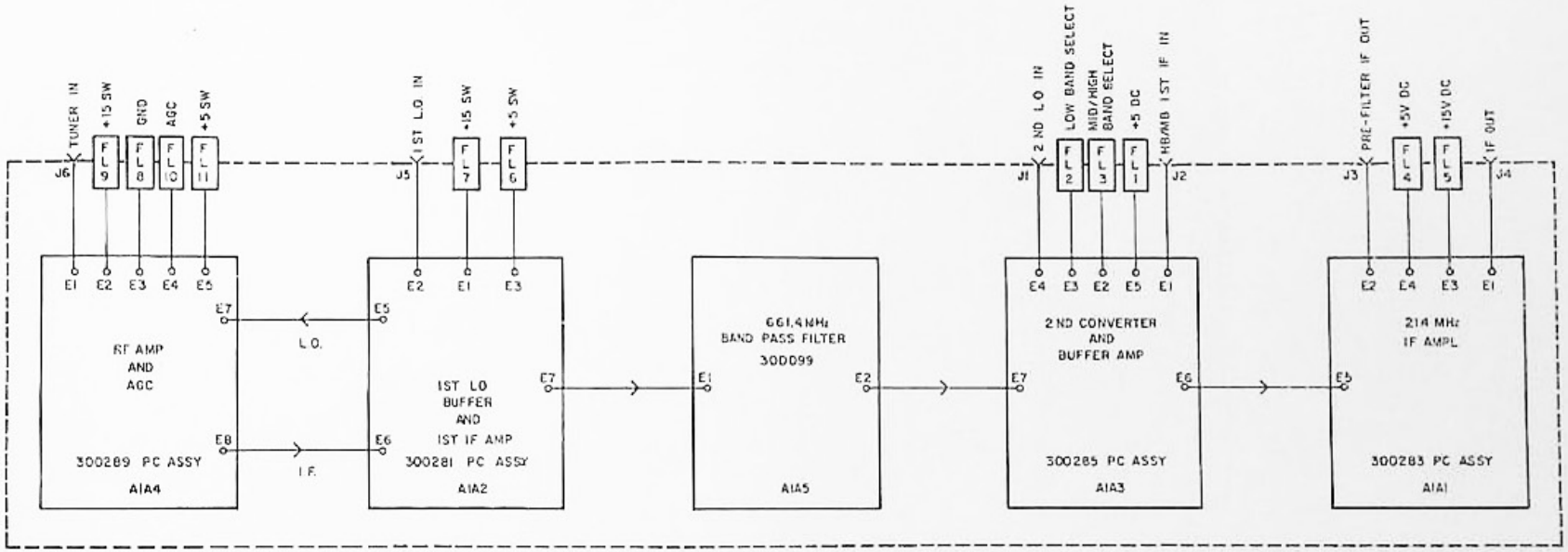


Figure 7-7. VHF Tuner Module Assembly (A3A1) Interconnecting Wiring Diagram

NOTES:
1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 300289, 300281, 300099, 300285, 300283
   PWB 300288, 300280, 200076, 300284, 300282
4. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4W, ±5%.
   b) 1% RESISTORS ARE 1/10W.
   c) CAPACITANCE IS IN pF.
   d) INDUCTANCE IS IN μH.

400323

HIGHEST REF DESIG	REF DESIG NOT USED
A5	
C6	
FL11	
J6	

A1 300283

HIGHEST REF DESIG	REF DESIG NOT USED
C6	E5 C1
FL1	
L3	
R1	
U3	

A2 300281

HIGHEST REF DESIG	REF DESIG NOT USED
C9	E7 E4
FL1	
L3	
R3	
U3	

A3 300285

HIGHEST REF DESIG	REF DESIG NOT USED
C11	C10
CR4	
L5	
R3	
U3	
W2	

A4 300289

HIGHEST REF DESIG	REF DESIG NOT USED
C16	E8 C15
CR5	E6
FL4	R17
L7	
Q1	
R20	
U6	

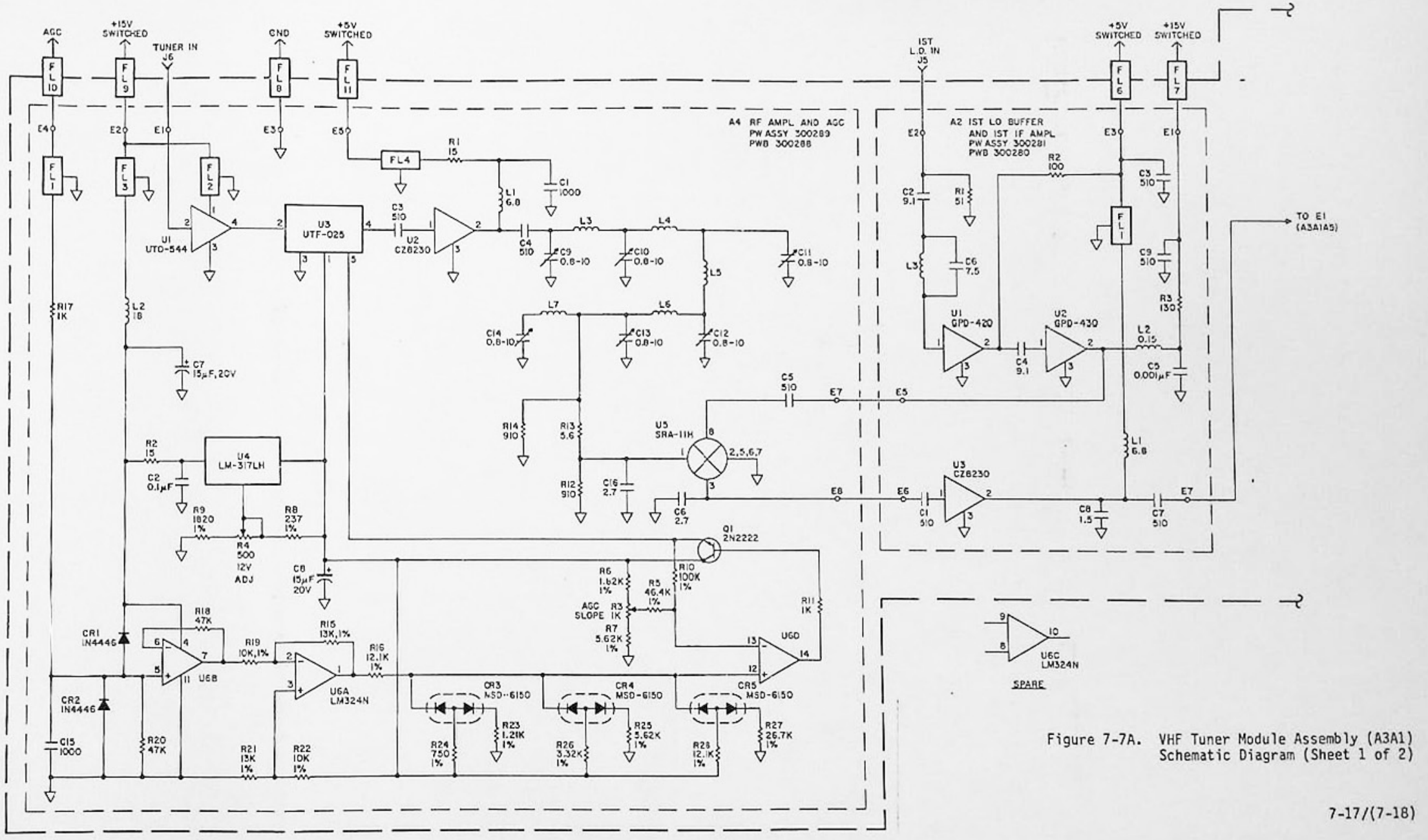


Figure 7-7A. VHF Tuner Module Assembly (A3A1) Schematic Diagram (Sheet 1 of 2)

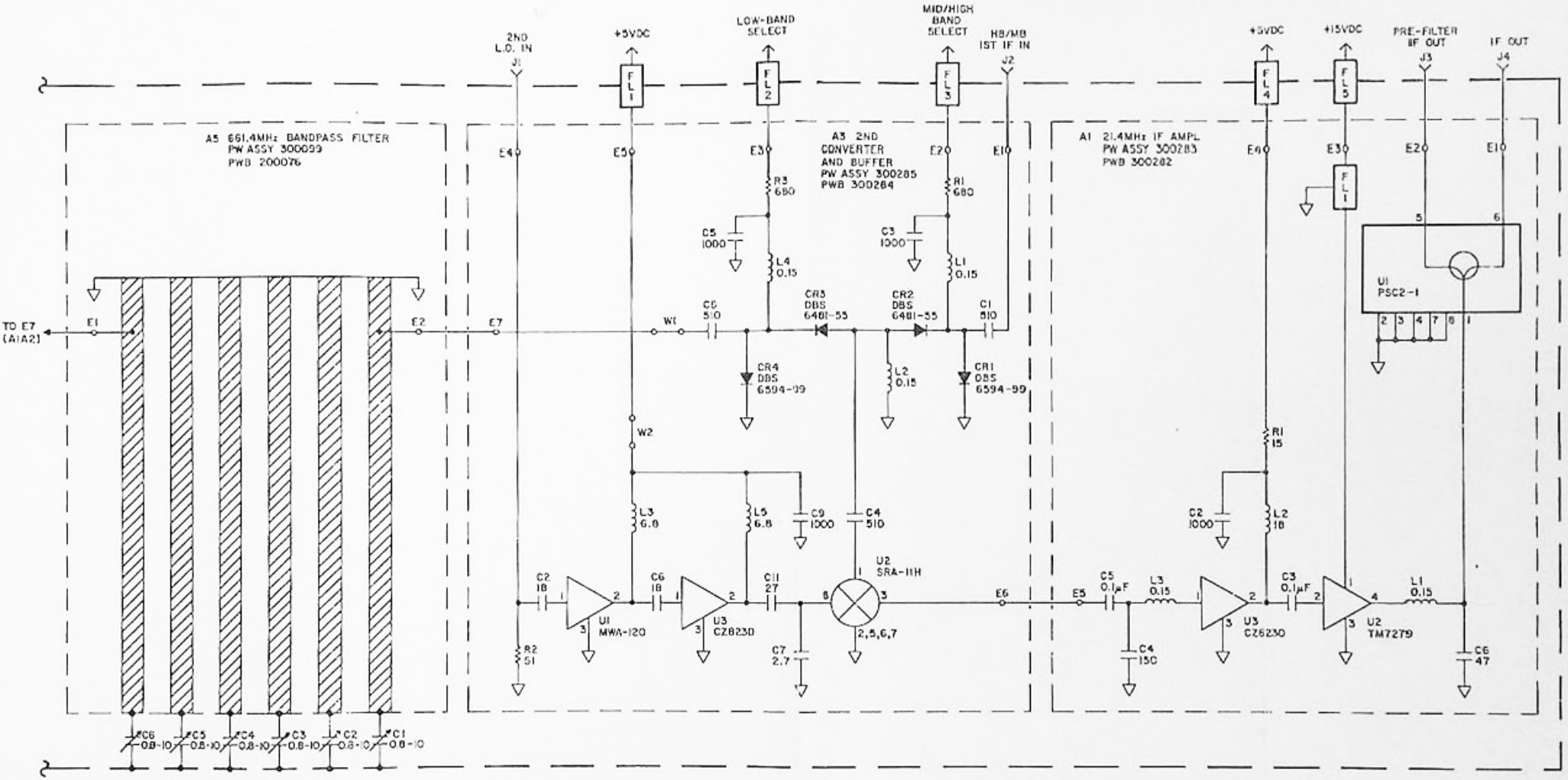
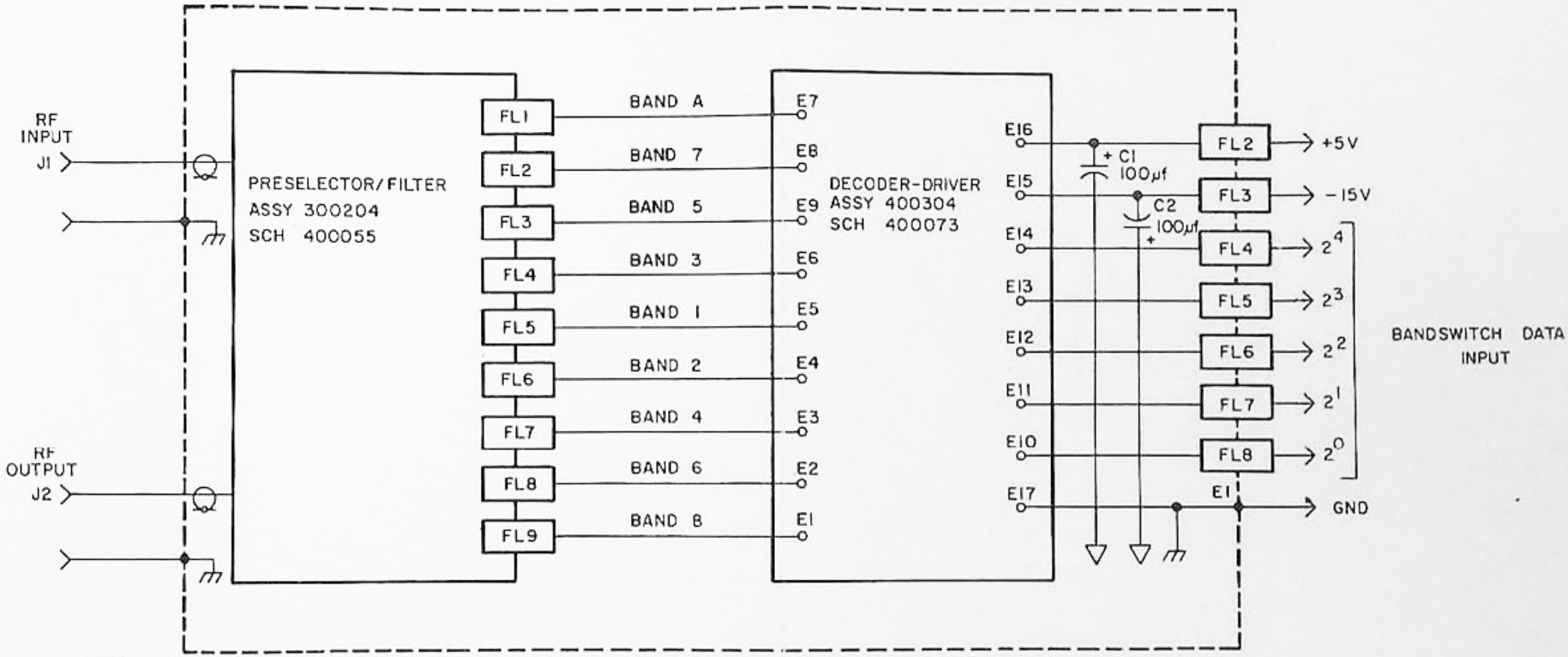


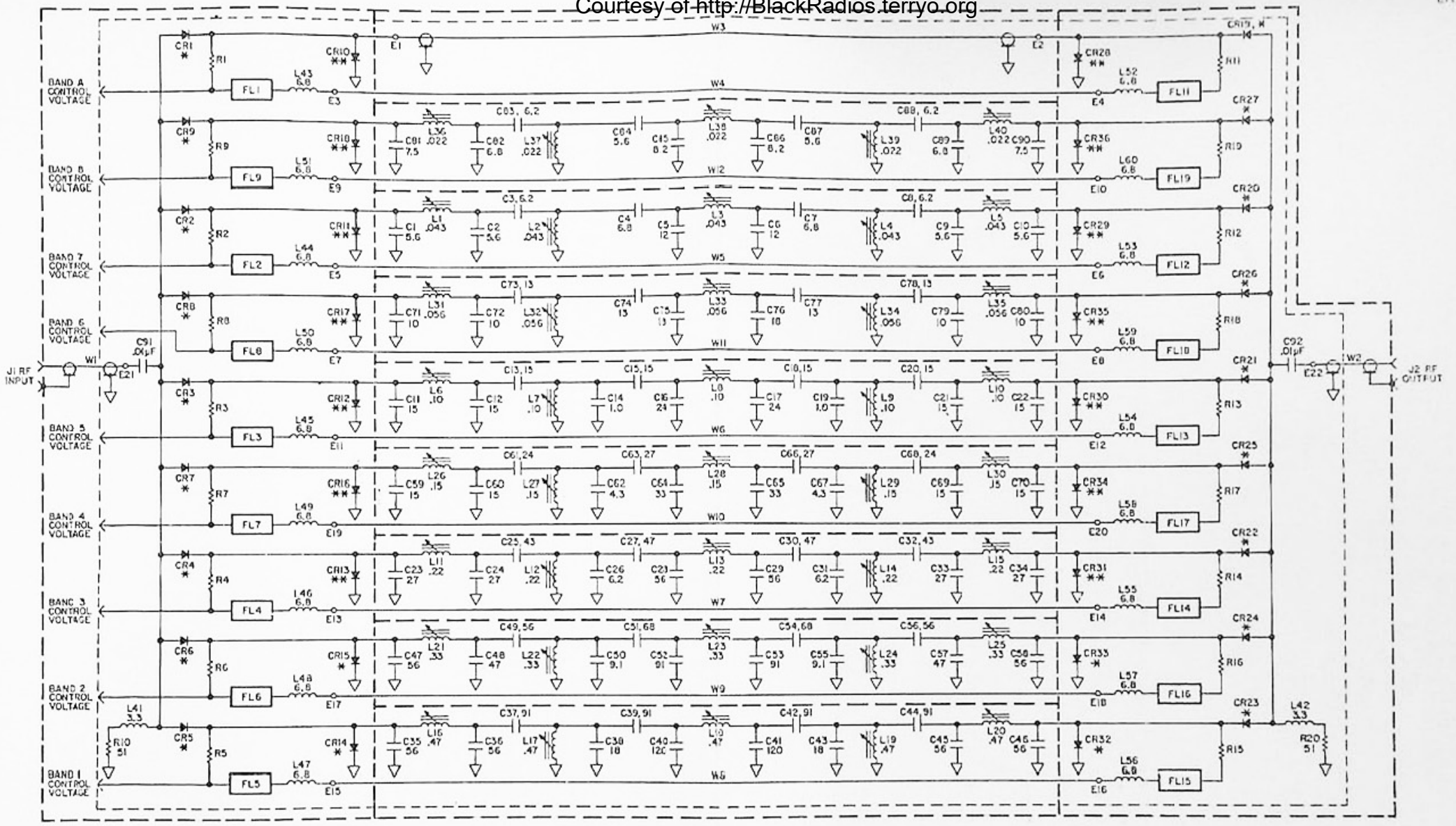
Figure 7-7A. VHF Tuner Module Assembly (A3A1) Schematic Diagram (Sheet 2 of 2)



NOTES:

1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400305

Figure 7-8. VHF (20-500 MHz) Preselector Module Assembly (A3A2) Interconnecting Wiring Diagram



NOTES:

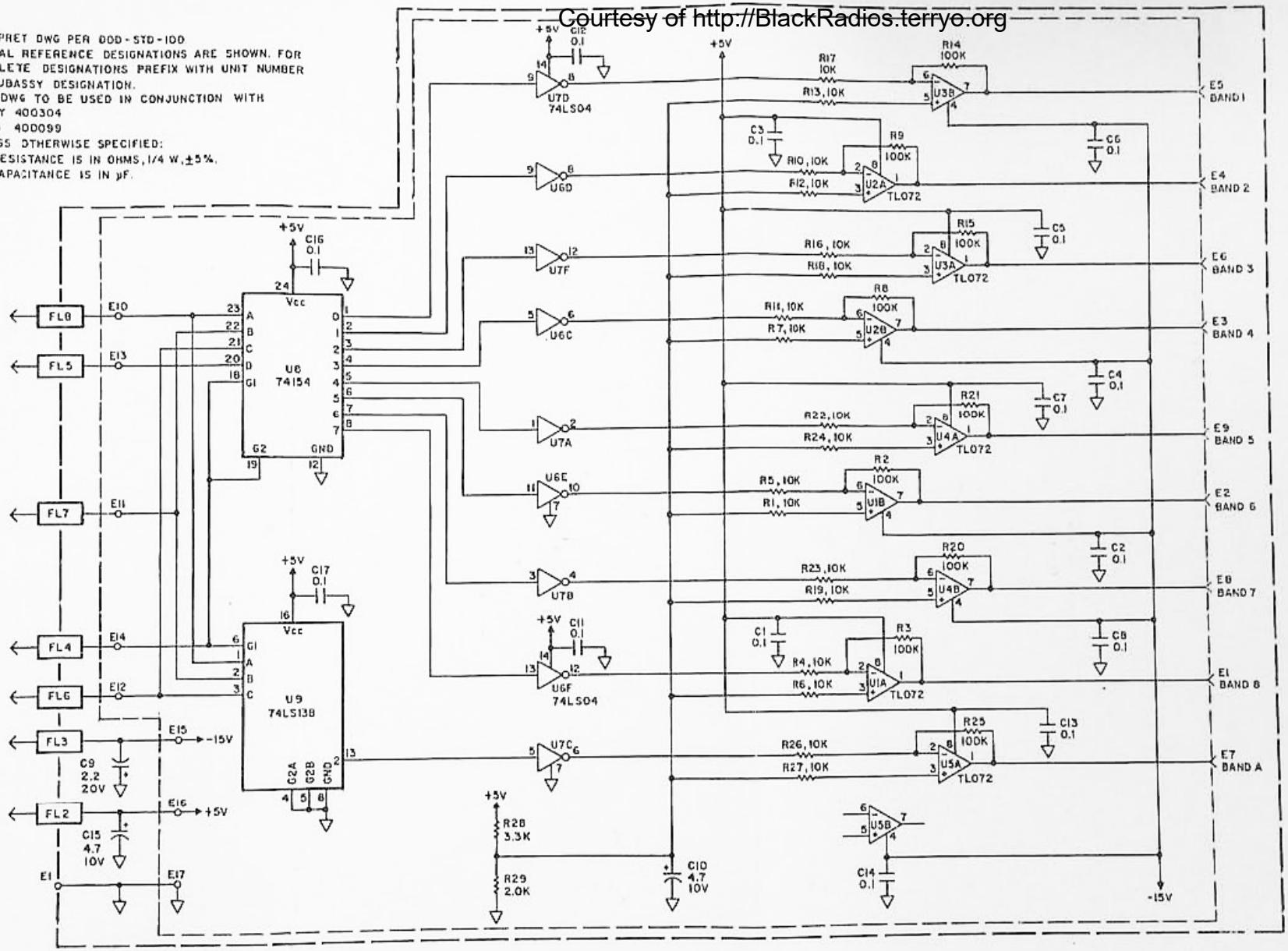
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS 680 OHMS, 1/4W ±5%
   b) CAPACITANCE IS IN pF
   c) INDUCTANCE IS IN µH.
2. DIODES MARKED * ARE DSB4036-95, DIODES MARKED ** ARE DSB6481-55.
3. INTERPRET THIS DRAWING PER DOD-STD-100.
4. THIS DRAWING TO BE USED IN CONJUNCTION WITH ASSEMBLY- 300204 & P.W.B-300016.
5. PARTIAL REFERENCE DESIGNATIONS SHOWN, FOR COMPLETE REF DESIGS - PREFIX WITH UNIT NUMBER OR SUBASSEMBLY DESIGNATIONS.

HIGHEST REF DESIG	REF DESIG NOT USED
C92	FL10
CR36	
E20	
FL19	
L60	
R20	
W20	

BAND	FREQUENCY (MHz)
1	20.0 - 28.6
2	28.6 - 39.6
3	39.6 - 62.6
4	62.6 - 100.6
5	100.6 - 144.6
6	144.6 - 220.6
7	220.6 - 334.6
8	334.6 - 500.6
A	THRU

Figure 7-8A. VHF (20-500) MHz Preselector Module Assembly (A3A2) Schematic Diagram

NOTES:
1. INTERPRET DWG PER 000-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 400304
   PWB 400099
4. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4 W, ±5%.
   b) CAPACITANCE IS IN µF.



HIGHEST REF DESIG	REF DESIG NOT USED
C17 E17 R28 U9	

Figure 7-9. VHF Preselector Decoder Driver Circuit Card Assembly (A3A2A2) Schematic Diagram

NOTES:
1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 400227
   SCHEM 400228, 400156

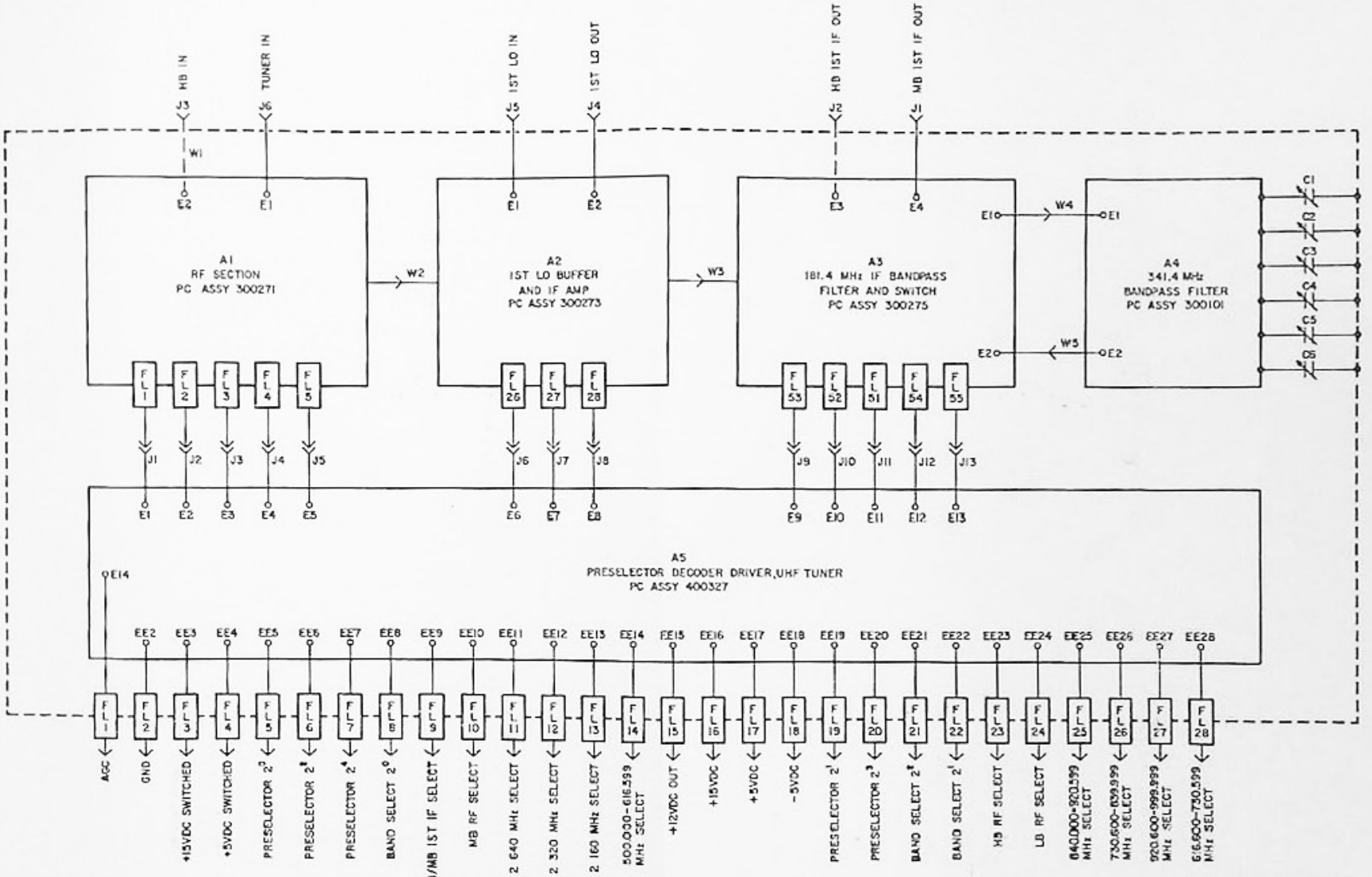


Figure 7-10. UHF Tuner Module Assembly (A3A3) Interconnecting Wiring Diagram

NOTES:
1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 300271, 300273, 300275, 300101
   PWB 300270, 300272, 300274, 200099
   SCHEM 400337, 400156
4. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4W, ±5%.
   b) CAPACITANCE IS IN pF.
   c) INDUCTANCE IS IN µH.

⑤ J3 WITH W1 AND J2 ARE USED WITH 1000 TO 1800 MHz TUNER.

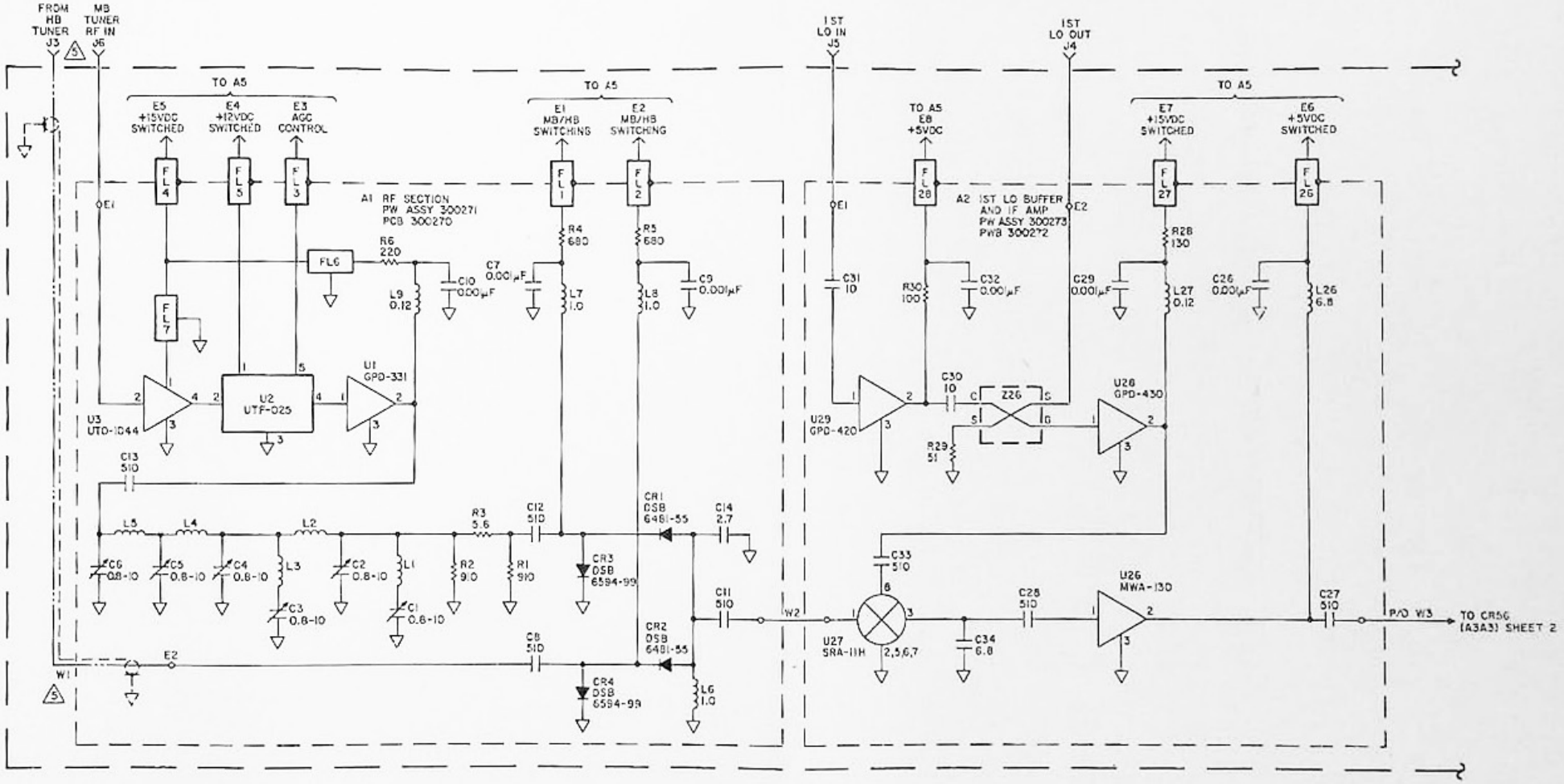


Figure 7-10A. UHF Tuner Module Assembly (A3A3) Schematic Diagram (Sheet 1 of 2)

400227

HIGHEST REF DESIG	REF DESIG NOT USED
C6 - J6 W5	J2 J3 W1

A1 300271

HIGHEST REF DESIG	REF DESIG NOT USED
C14 CR4 E2 FL7 L9 R6 U3	

A2 300273

HIGHEST REF DESIG	REF DESIG NOT USED
C26-C34 E2 FL26-FL28 L26-L27 R28-R30 U26-U29 Z26	

A3 300275

HIGHEST REF DESIG	REF DESIG NOT USED
C50-C70 CR51-CR60 E4 FL51-FL55 L51-L62 R51-R55 Z26	

A4 300101

HIGHEST REF DESIG	REF DESIG NOT USED
C2 E2	

NOT USED ON ASSY	
C15-C25 C35-C49 CR5-CR50 FL0-FL25 FL29-FL50	L10-L25 L28-L50 R7-R27 R31-R50 U4-U25 Z1-Z25

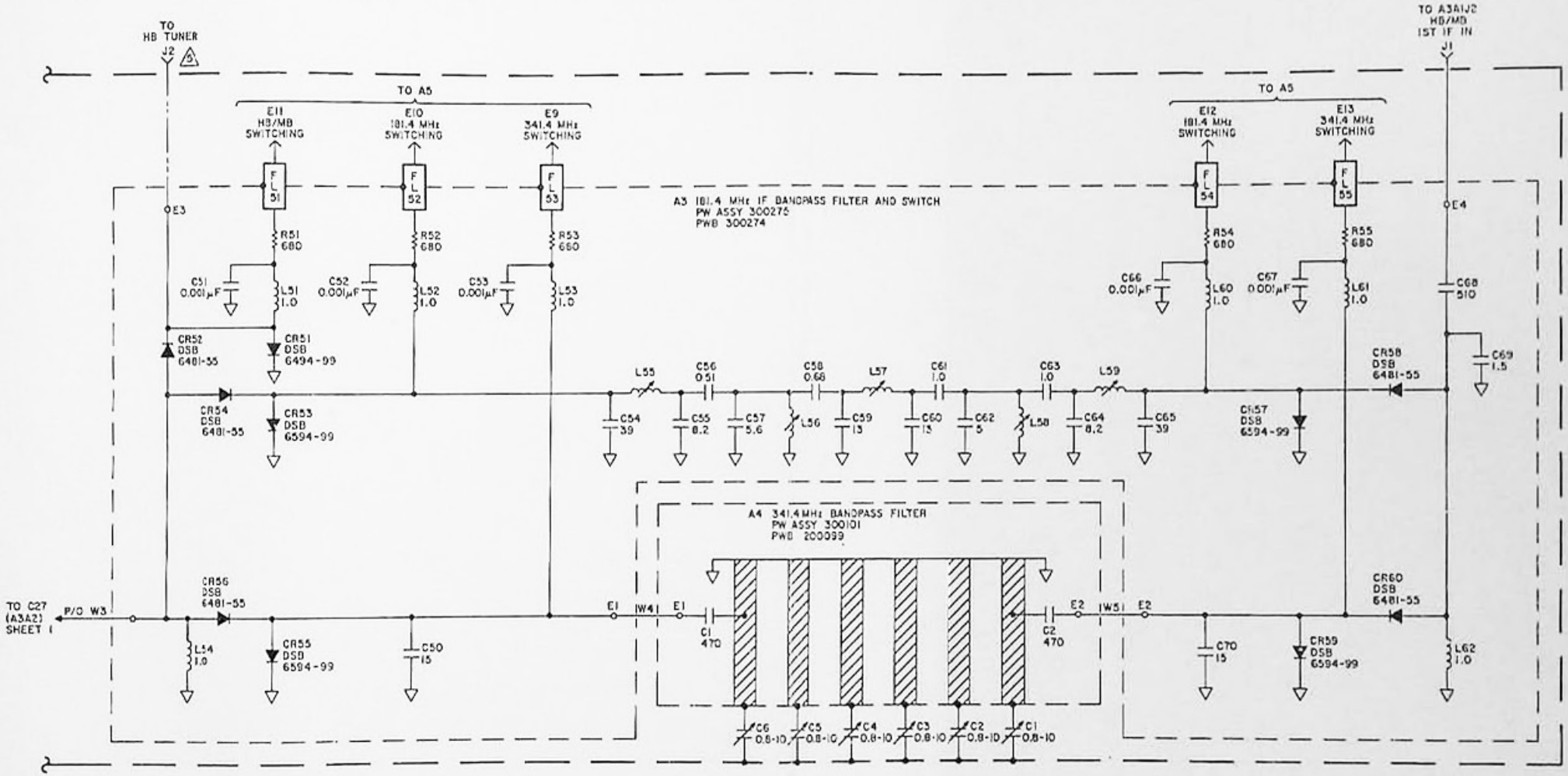
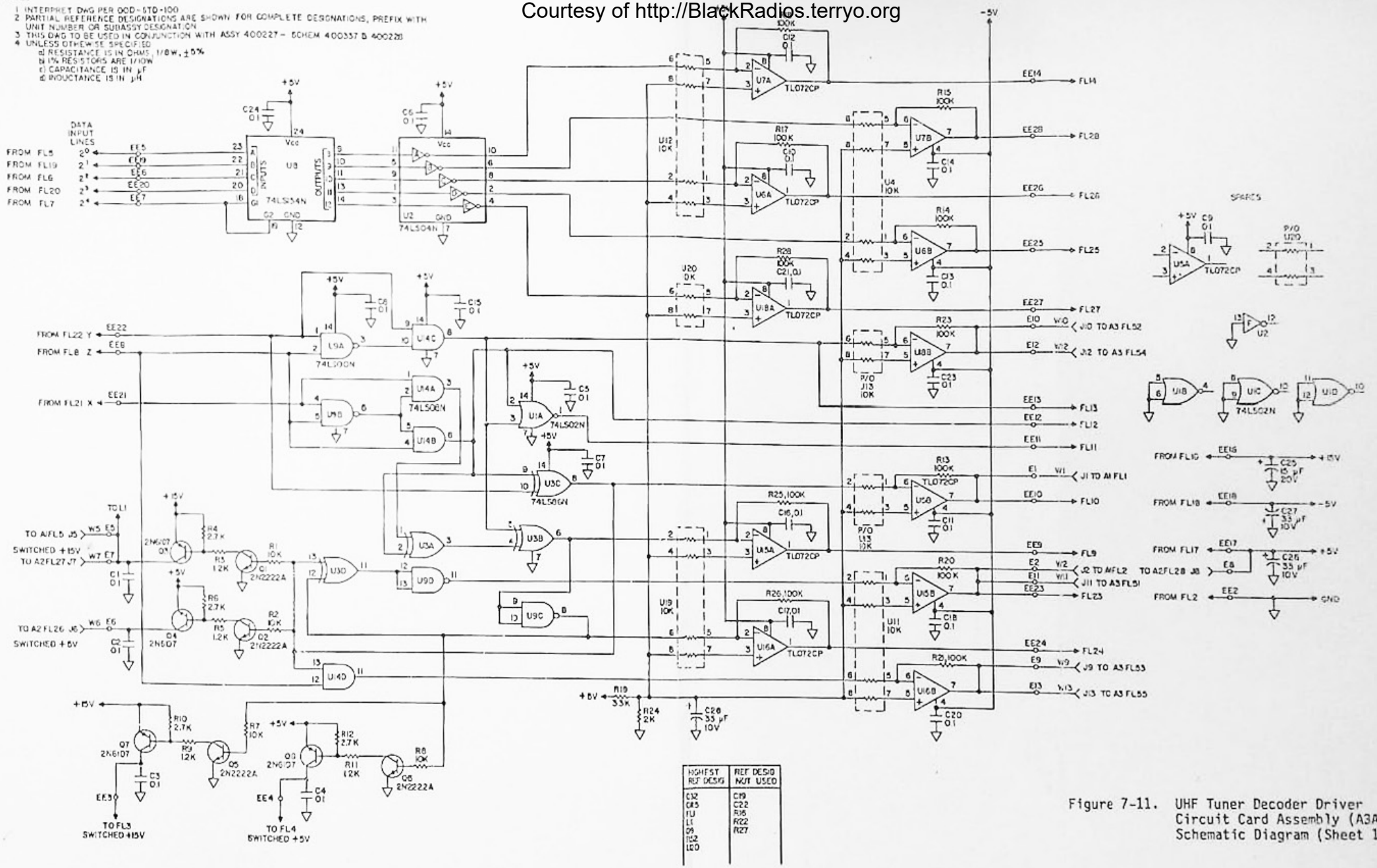


Figure 7-10A. UHF Tuner Module Assembly (A3A3) Schematic Diagram (Sheet 2 of 2)

NOTES

1. INTERPRET DWG PER DOD-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400227-, SCHEM 400337 & 400228
4. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE IS IN OHMS, 1/8W, ±5%
   b) 1% RESISTORS ARE 1/10W
   c) CAPACITANCE IS IN µF
   d) INDUCTANCE IS IN µH



HIGHEST REF DESIG	REF DESIG NOT USED
C32	C19
CR5	C22
FL1	R16
L1	R22
Q6	R27
R32	
U20	

Figure 7-11. UHF Tuner Decoder Driver Circuit Card Assembly (A3A3A5) Schematic Diagram (Sheet 1 of 2)

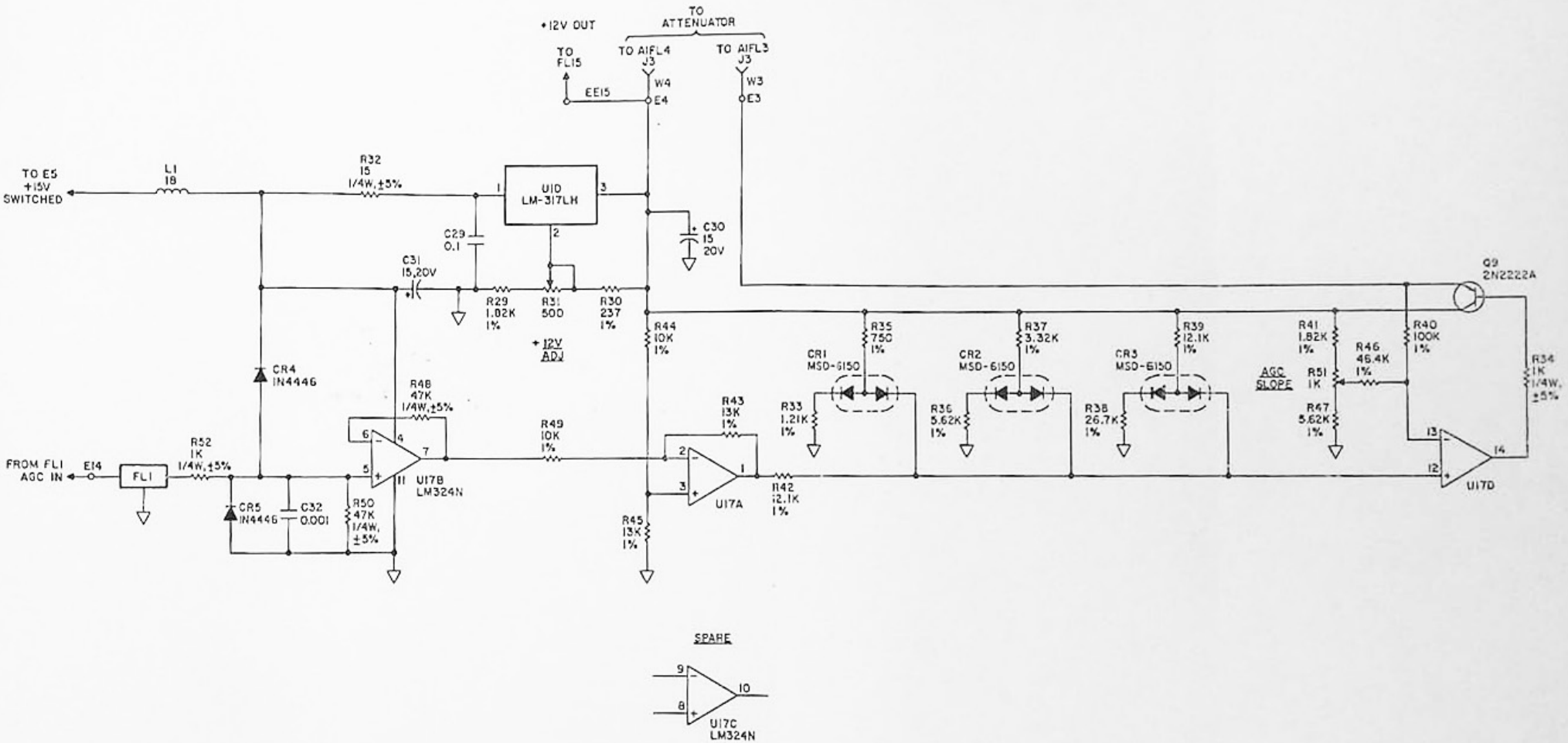
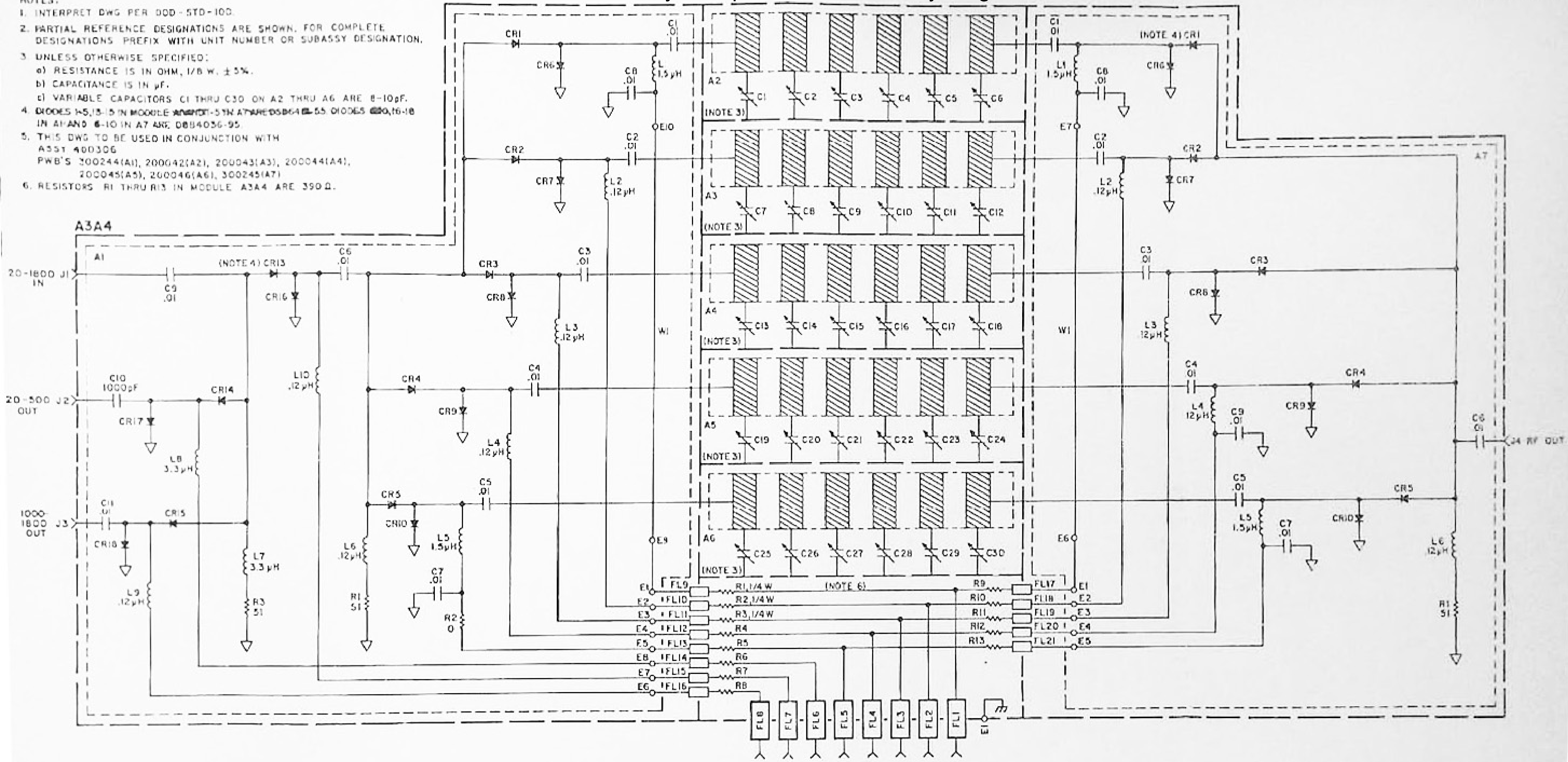


Figure 7-11. UHF Tuner Decoder Driver Circuit Card Assembly (A3A3A5) Schematic Diagram (Sheet 2 of 2)

NOTES:

1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHM, 1/8 W, ±5%.
   b) CAPACITANCE IS IN pF.
   c) VARIABLE CAPACITORS C1 THRU C30 ON A2 THRU A6 ARE 8-10pF.
4. DIODES 1-5,13-15 IN MODULE A1 AND 1-5 IN A7 ARE DSB6412-55. DIODES 6-10,16-18 IN A1 AND 6-10 IN A7 ARE DBB4036-95.
5. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400306 PWB'S 300244(A1), 200042(A2), 200043(A3), 200044(A4), 200045(A5), 200046(A6), 300245(A7)
6. RESISTORS R1 THRU R13 IN MODULE A3A4 ARE 390 Ω.



A3A4

HIGHEST REF DESIG	REF DESIG NOT USED
E1 FL21 J4 R13	

A3A4A1

HIGHEST REF DESIG	REF DESIG NOT USED
C11 R3 CR18 E10 L10	CR11,12

A3A4A2-A6

HIGHEST REF DESIG	REF DESIG NOT USED
C30	

A3A4A7

HIGHEST REF DESIG	REF DESIG NOT USED
C9 R1 CR10 E7 L6	

Figure 7-12. UHF Preselector (500-1000 MHz) Module Assembly (A3A4) Schematic Diagram

NOTES:
1. INTERPRET DWG PER 000-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400234, 300195, 300196, 300197 PWB 300104, 300105, 300107
4. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4 W, ±5%.
   b) CAPACITANCE IS IN μF.
   c) INDUCTANCE IS IN μH.
   d) ALL 1% RESISTORS ARE 1/10W

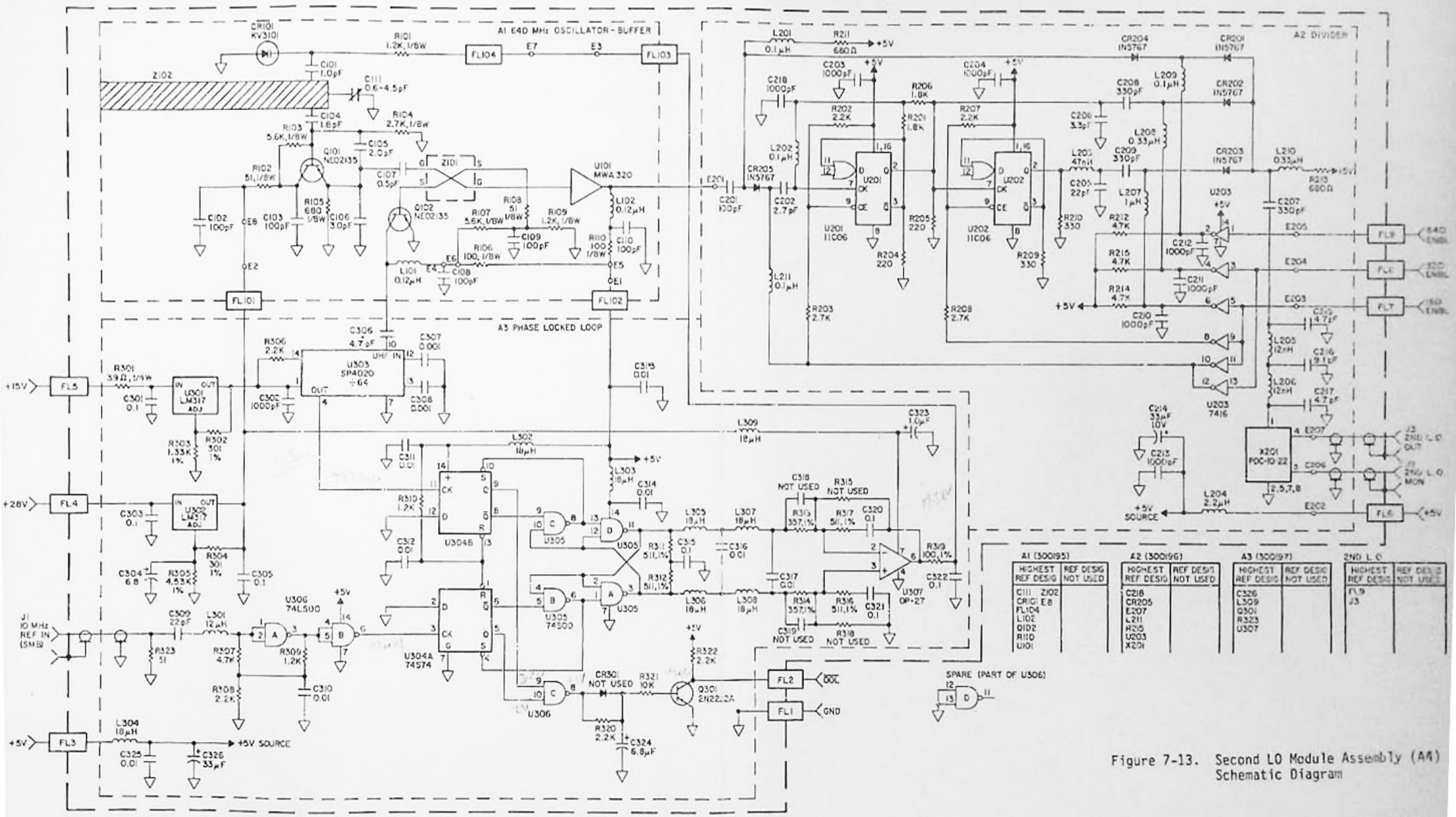
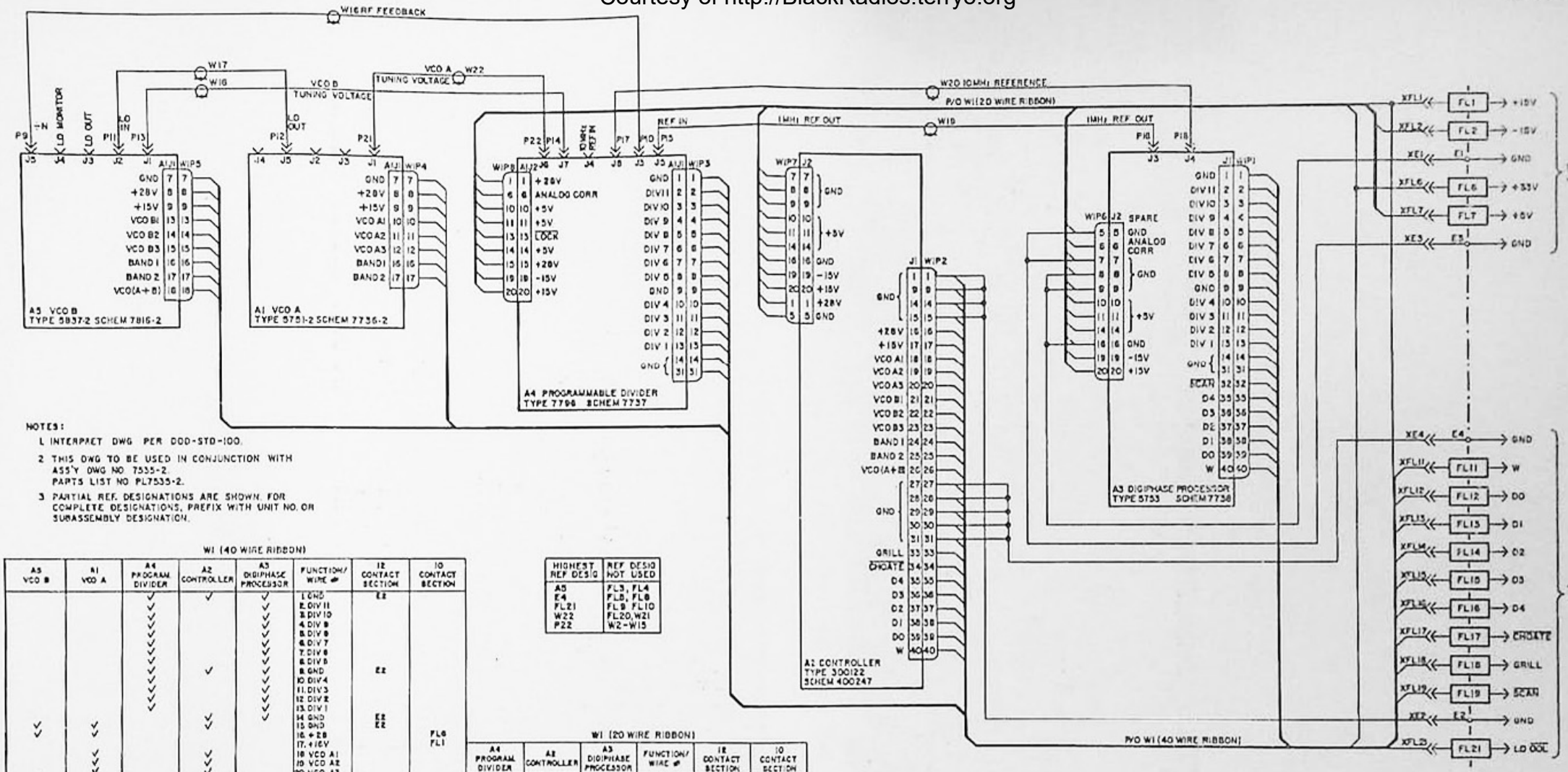


Figure 7-13. Second LO Module Assembly (A4) Schematic Diagram



NOTES:

1. INTERFACE DWG PER DOD-STD-100.
2. THIS DWG TO BE USED IN CONJUNCTION WITH ASS'Y DWG NO. 7535-2. PARTS LIST NO. PL7535-2.
3. PARTIAL REF. DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NO. OR SUBASSEMBLY DESIGNATION.

W1 (40 WIRE RIBBON)

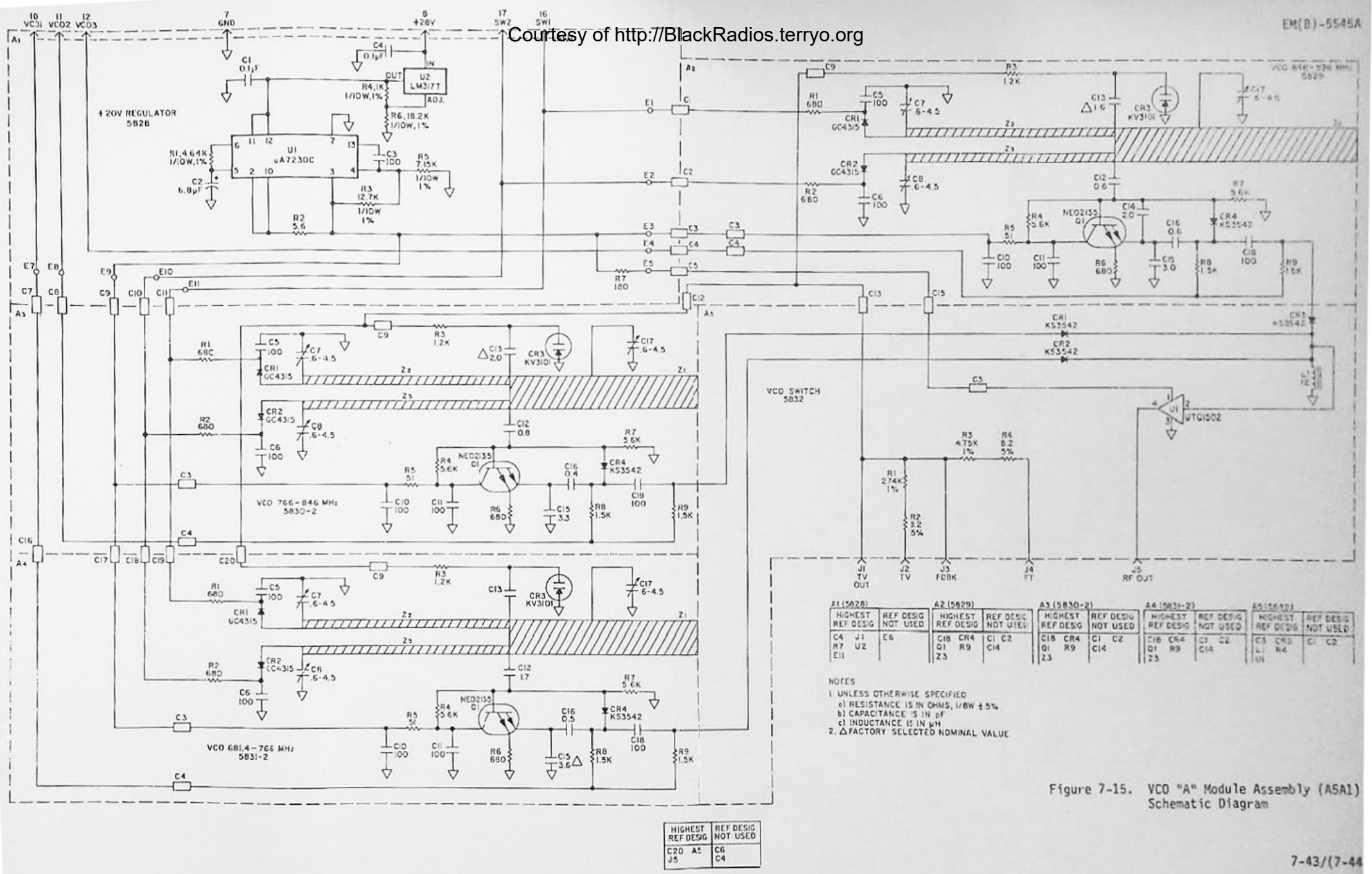
A5 VCO B	A1 VCO A	A4 PROGRAM. DIVIDER	A2 CONTROLLER	A3 DIGIPHASE PROCESSOR	FUNCTION/ WIRE #	J2 CONTACT SECTION	J0 CONTACT SECTION
		✓	✓	✓	1. GND	E2	
		✓		✓	2. DIV 11		
		✓		✓	3. DIV 10		
		✓		✓	4. DIV 9		
		✓		✓	5. DIV 8		
		✓		✓	6. DIV 7		
		✓		✓	7. DIV 6		
		✓		✓	8. DIV 5		
		✓	✓	✓	9. GND	E2	
		✓		✓	10. DIV 4		
		✓		✓	11. DIV 3		
		✓		✓	12. DIV 2		
		✓		✓	13. DIV 1		
			✓	✓	14. GND	E2	
✓	✓		✓		15. GND	E2	
					16. +28		FL6
					17. +15V		FL1
	✓		✓		18. VCO A1		
	✓		✓		19. VCO A2		
✓			✓		20. VCO A3		
✓			✓		21. VCO B1		
✓			✓		22. VCO B2		
✓			✓		23. VCO B3		
✓	✓		✓		24. BAND 1		
✓			✓		25. BAND 2		
			✓		26. VCO (A+B)		
			✓		27. GND	E4	
			✓		28. GND	E4	
			✓		29. GND	E4	
			✓		30. GND	E4	
		✓	✓	✓	31. GND	E4	
		✓	✓		32. SCAN	FL19	
			✓		33. GRILL	FL18	
			✓		34. CHDATE	FL17	
			✓	✓	35. D4	FL16	
			✓	✓	36. D3	FL15	
			✓		37. D2	FL14	
			✓		38. D1	FL13	
			✓	✓	39. D0	FL12	
			✓	✓	40. W	FL11	

HIGHEST REF DESIG	REF DESIG NOT USED
A5	FL3, FL4
E4	FL5, FL8
FL21	FL9 FL10
W22	FL20, W21
P22	W2-W15

W1 (20 WIRE RIBBON)

A4 PROGRAM. DIVIDER	A2 CONTROLLER	A3 DIGIPHASE PROCESSOR	FUNCTION/ WIRE #	J2 CONTACT SECTION	J0 CONTACT SECTION
✓	✓		1. +28V		
			2. SPARE		
			3. VARACTOR		
			4. SPARE		
	✓	✓	5. GND		E3
✓	✓	✓	6. ANLG CORR		
	✓	✓	7. GND		E3
	✓	✓	8. GND		E1
	✓	✓	9. GND		E1
✓	✓	✓	10. +5V		
✓	✓	✓	11. +5V		
			12. N/U		
✓		✓	13. LOCR	FL21	
✓	✓	✓	14. +5V		FL7
			15. +28V		FL6
	✓	✓	16. GND		E1
			17. N/U		
			18. N/U		
✓	✓	✓	19. -15V		FL8
✓	✓	✓	20. +15V		FL1

Figure 7-14. First LO Synthesizer Module Assembly (A5) Interconnecting Wiring Diagram



A1 (5828) HIGHEST REF DESIG	A1 (5828) REF DESIG NOT USED
C4 J1 R7 U2 E11	E6

A2 (5829) HIGHEST REF DESIG	A2 (5829) REF DESIG NOT USED
C18 CR4 Q1 R9 Z3	C1 C2 C14

A3 (5830-2) HIGHEST REF DESIG	A3 (5830-2) REF DESIG NOT USED
C18 CR4 Q1 R9 Z3	C1 C2 C14

A4 (5831-2) HIGHEST REF DESIG	A4 (5831-2) REF DESIG NOT USED
C18 CR4 Q1 R9 Z3	C1 C2 C14

A5 (5832) HIGHEST REF DESIG	A5 (5832) REF DESIG NOT USED
C3 CR3 L1 R4 U1	C1 C2

HIGHEST REF DESIG	REF DESIG NOT USED
C20 A5 J5	C6 C4

Figure 7-15. VCO "A" Module Assembly (A5A1) Schematic Diagram

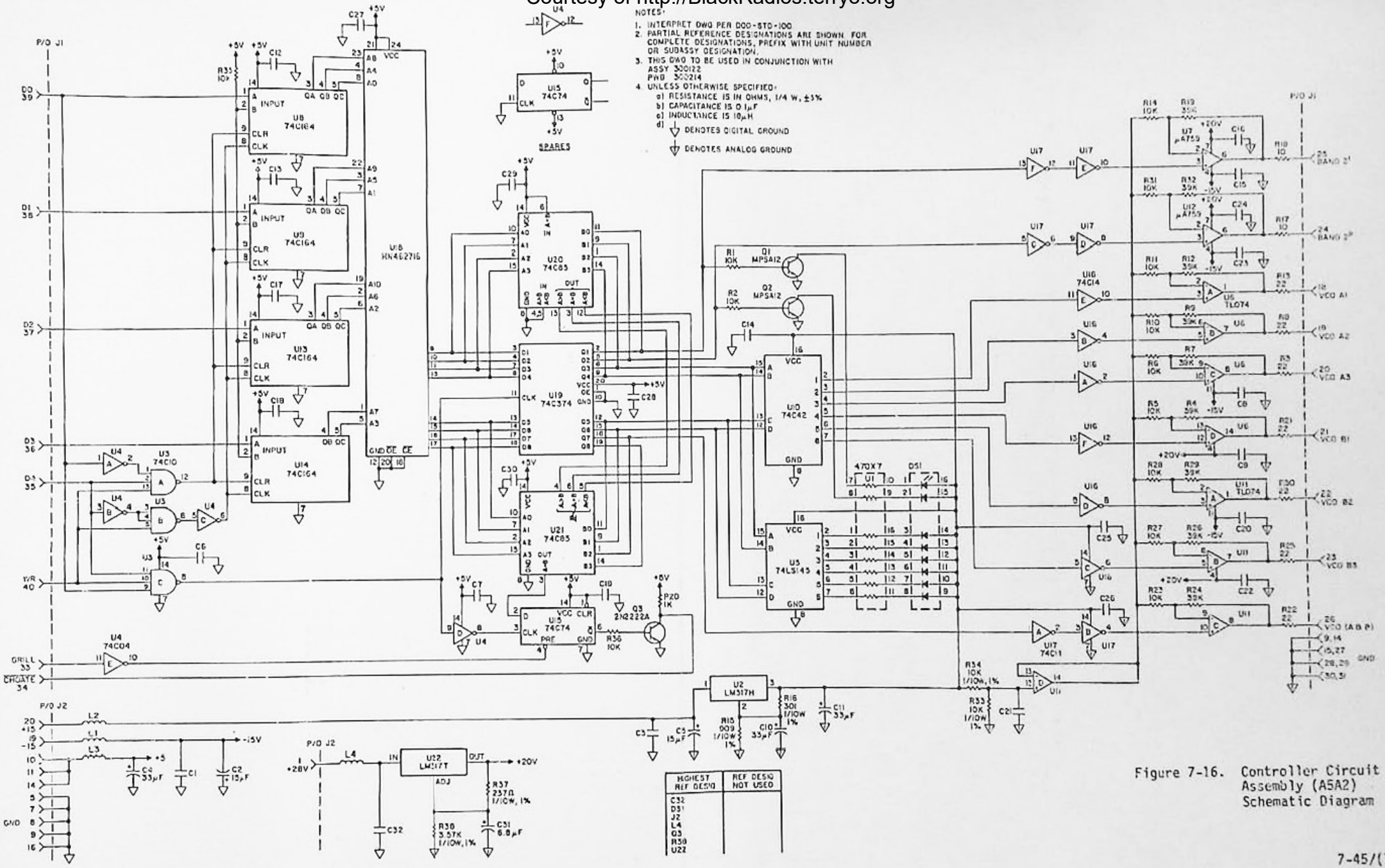
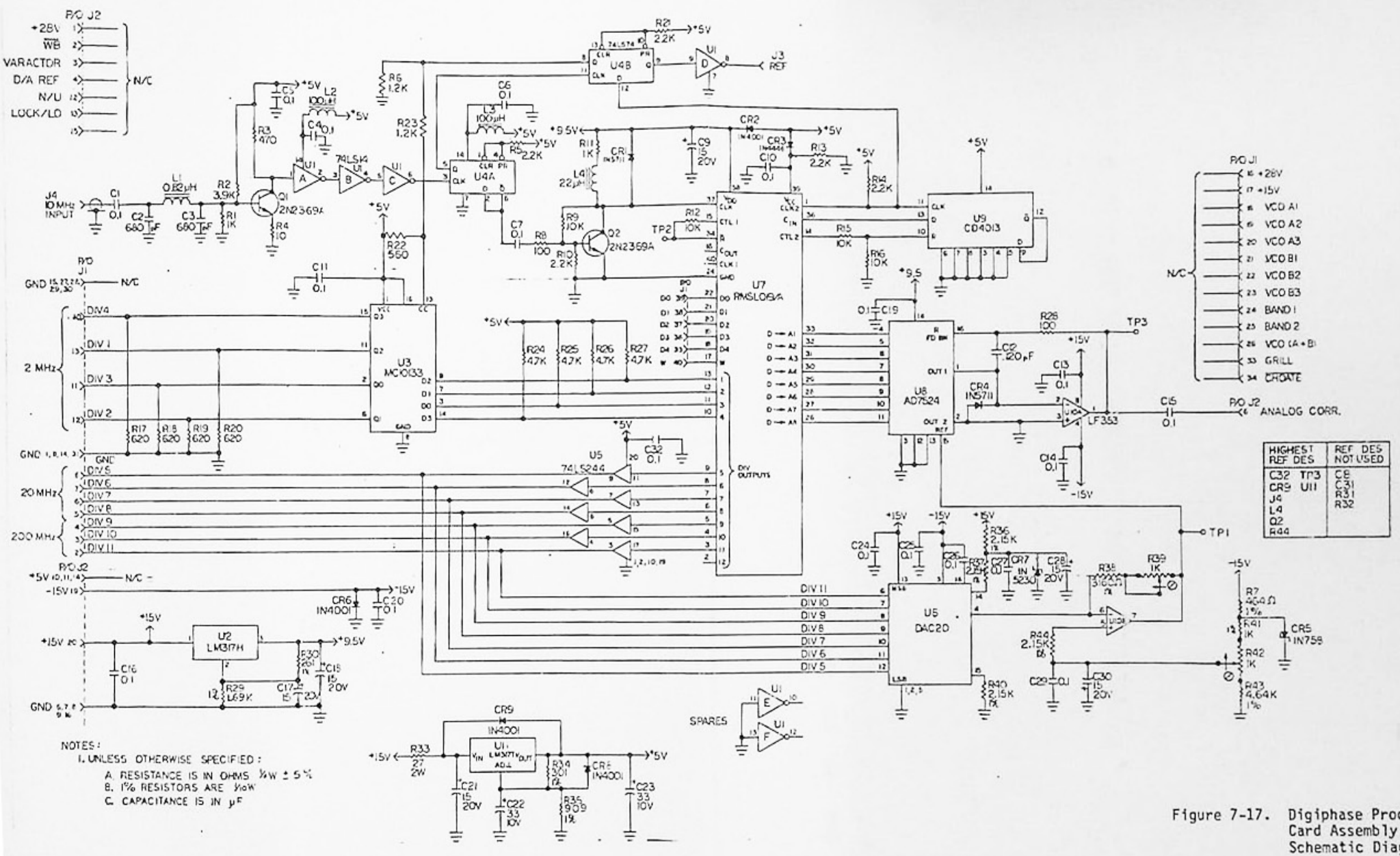


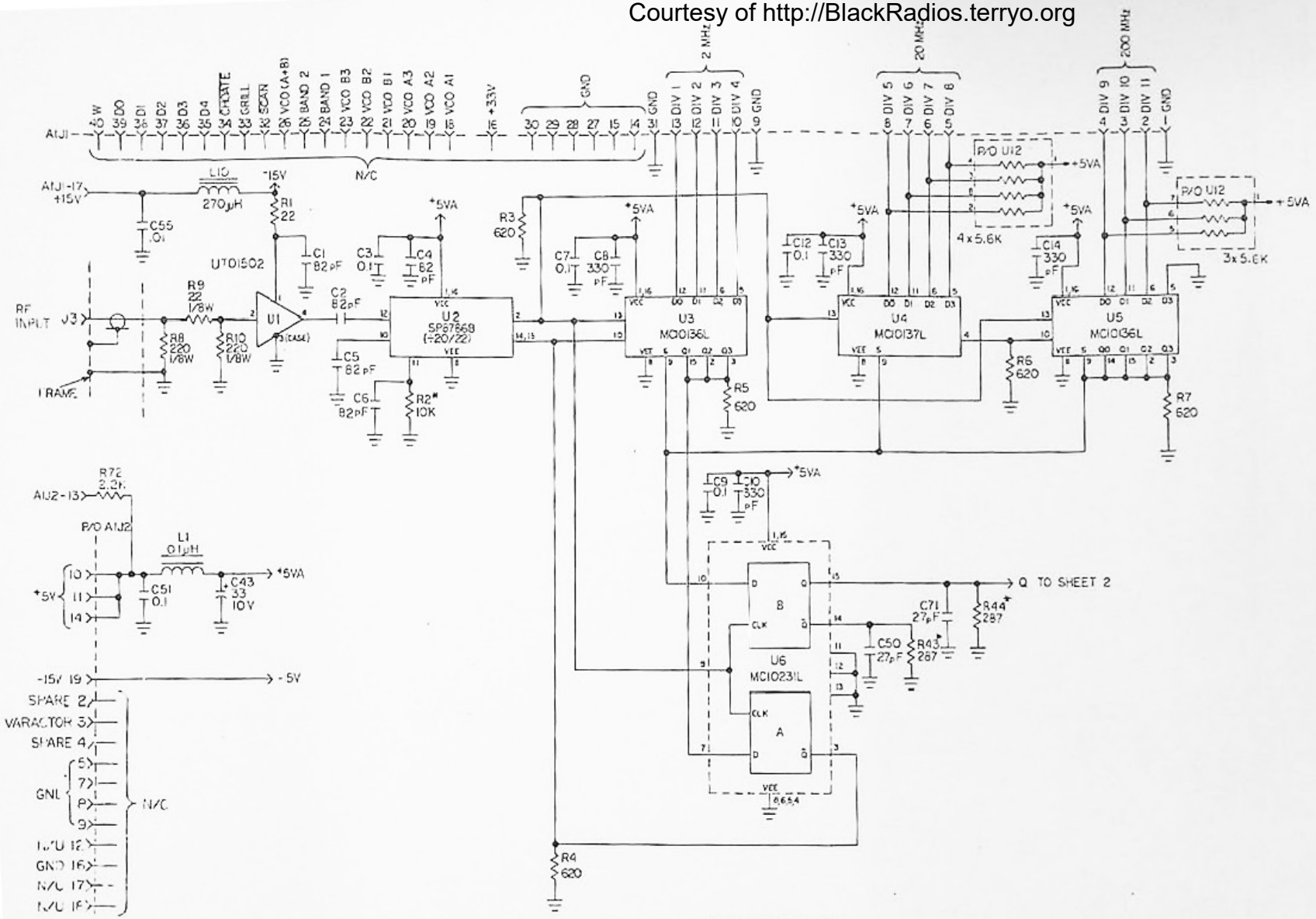
Figure 7-16. Controller Circuit Card Assembly (A5A2) Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTANCE IS IN OHMS ¼W ± 5%
   - B. 1% RESISTORS ARE ⅛W
   - C. CAPACITANCE IS IN μF

Figure 7-17. Digiphase Processor Circuit Card Assembly (A5A3) Schematic Diagram



NOTES:

1. RESISTANCE MARKED WITH '*' IS IN OHMS ½cW ±1% ALL OTHERS IN OHMS ¼W ±5%
2. UNLESS OTHERWISE SPECIFIED:
   A. CAPACITANCE IS IN µF

HIGHEST REF. DES.	REF. DES. NOT USED
C77	C11, C15, C16, C17, C18, C49, C56-C70
CR6	
J8	
L14	
Q3	C74, L2
R73	R11, R12, R42, R71, R46-R69
U12	

Figure 7-18. Programmable Divider Circuit Card Assembly (A5A4) Schematic Diagram (Sheet 1 of 2)

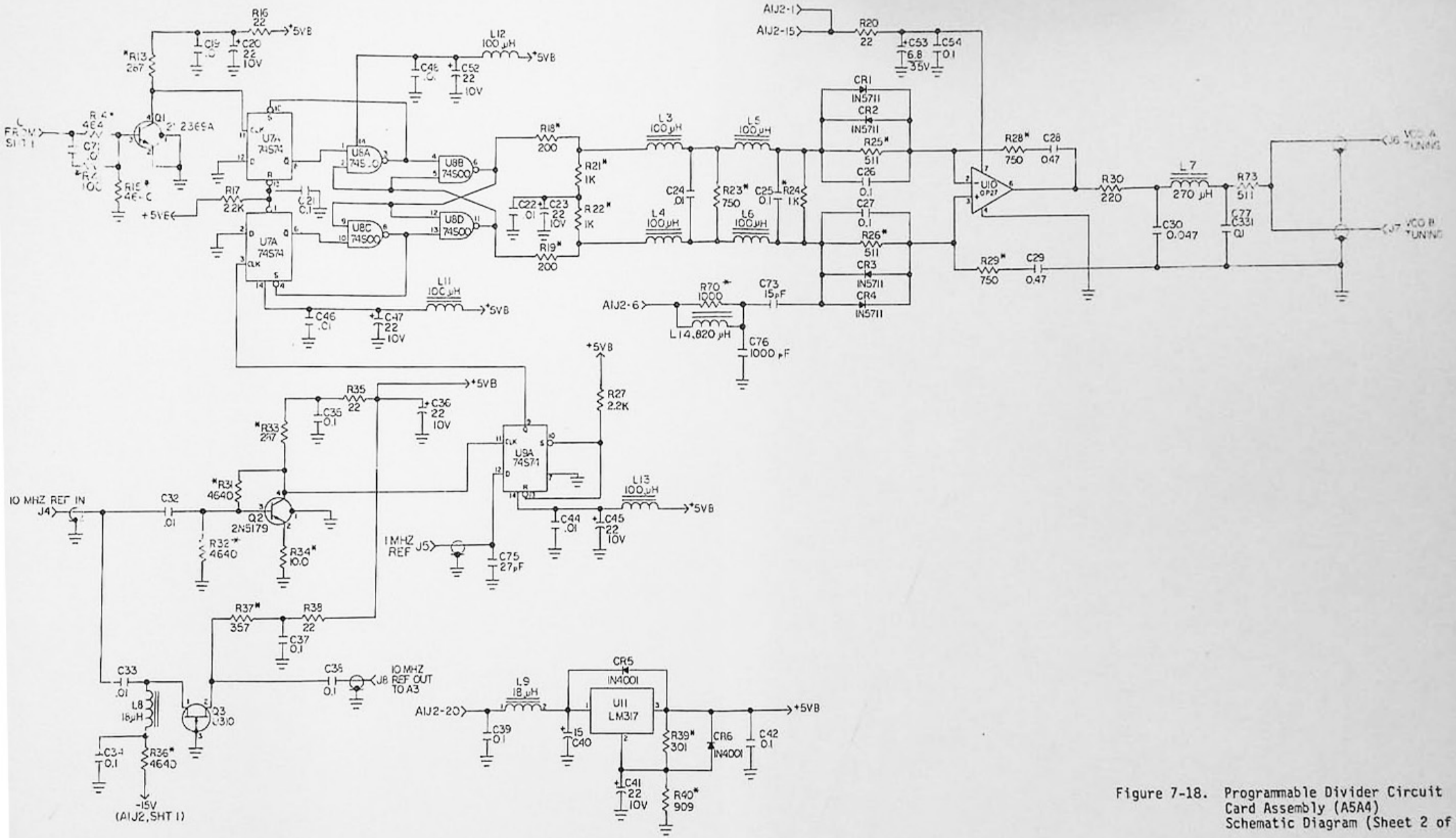


Figure 7-18. Programmable Divider Circuit Card Assembly (A5A4) Schematic Diagram (Sheet 2 of 2)

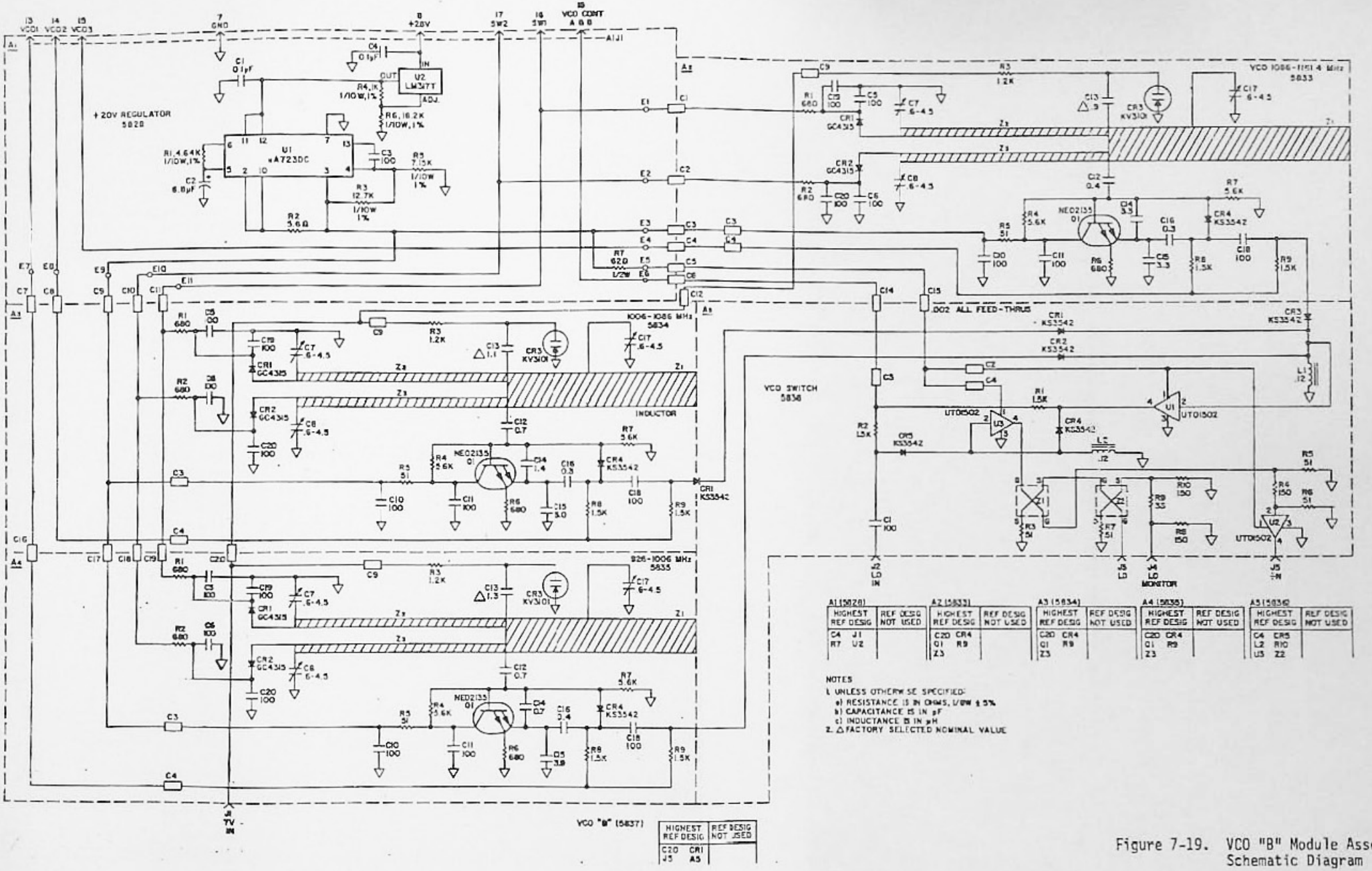
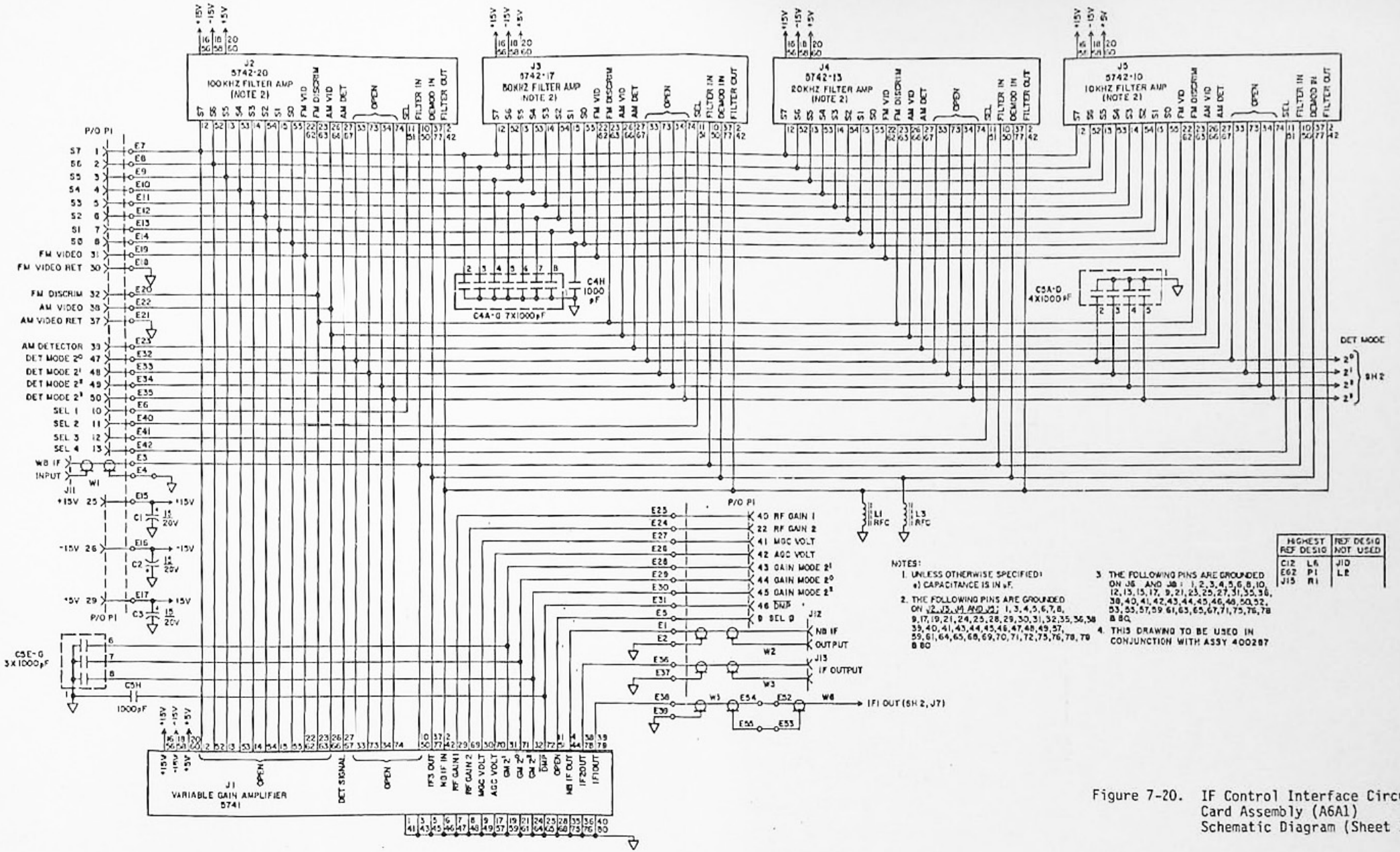


Figure 7-19. VCO "B" Module Assembly (A5A5) Schematic Diagram



HIGHEST REF DESIG	REF DESIG NOT USED
C12 L6	J10
E62 P1	L2
J15 R1	

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   a) CAPACITANCE IS IN μF.
2. THE FOLLOWING PINS ARE GROUNDED ON J2, J3, J4 AND J5: 1, 3, 4, 5, 6, 7, 8, 9, 17, 19, 21, 24, 25, 28, 29, 30, 31, 32, 35, 36, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 49, 57, 59, 61, 64, 65, 68, 69, 70, 71, 72, 75, 76, 78, 79 & 80.
3. THE FOLLOWING PINS ARE GROUNDED ON J6 AND J8: 1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 15, 17, 9, 21, 23, 25, 27, 31, 35, 36, 38, 40, 41, 42, 43, 44, 45, 46, 48, 50, 52, 53, 55, 57, 59, 61, 63, 65, 67, 71, 75, 76, 78 & 80.
4. THIS DRAWING TO BE USED IN CONJUNCTION WITH ASSY 400287

Figure 7-20. IF Control Interface Circuit Card Assembly (A6A1) Schematic Diagram (Sheet 1 of 2)

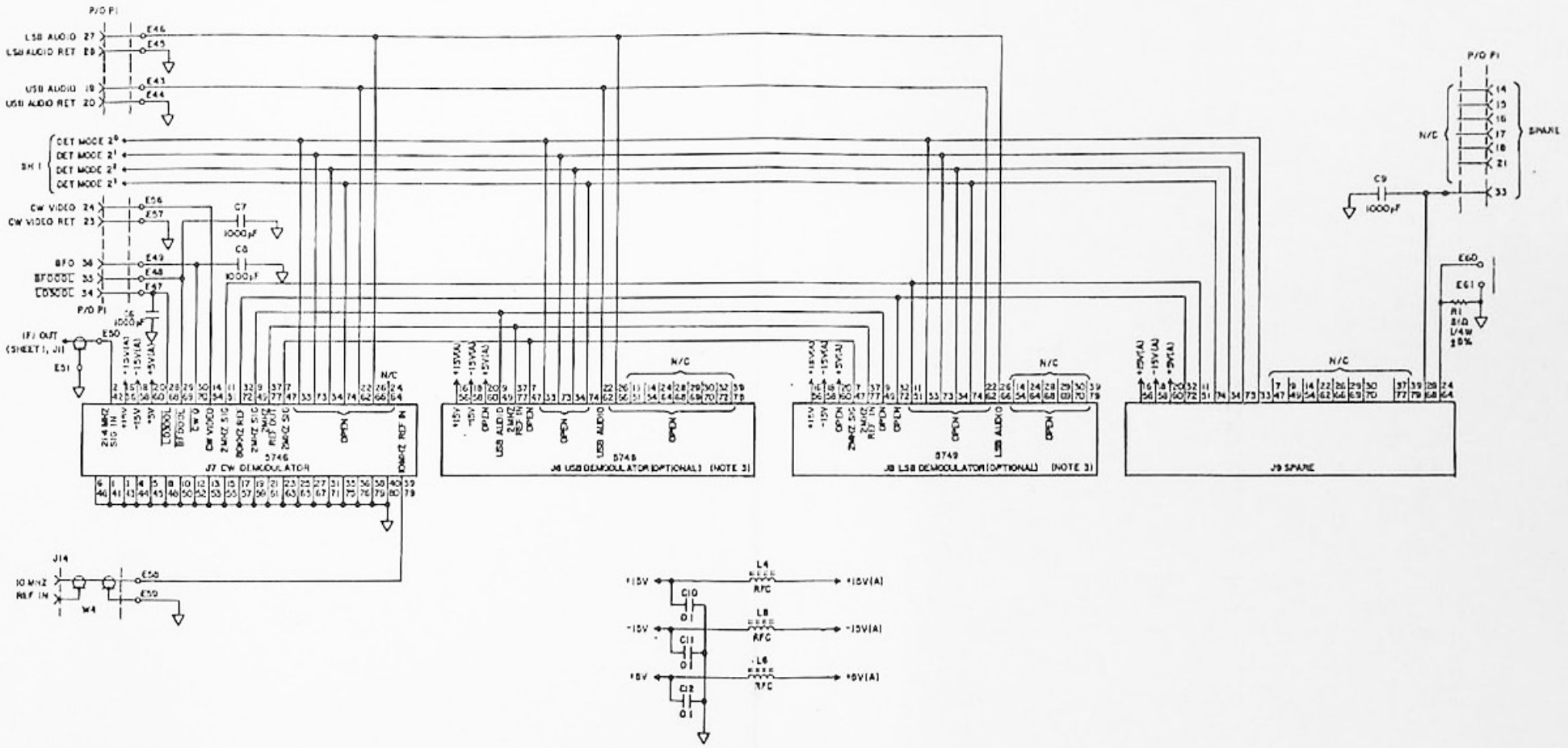
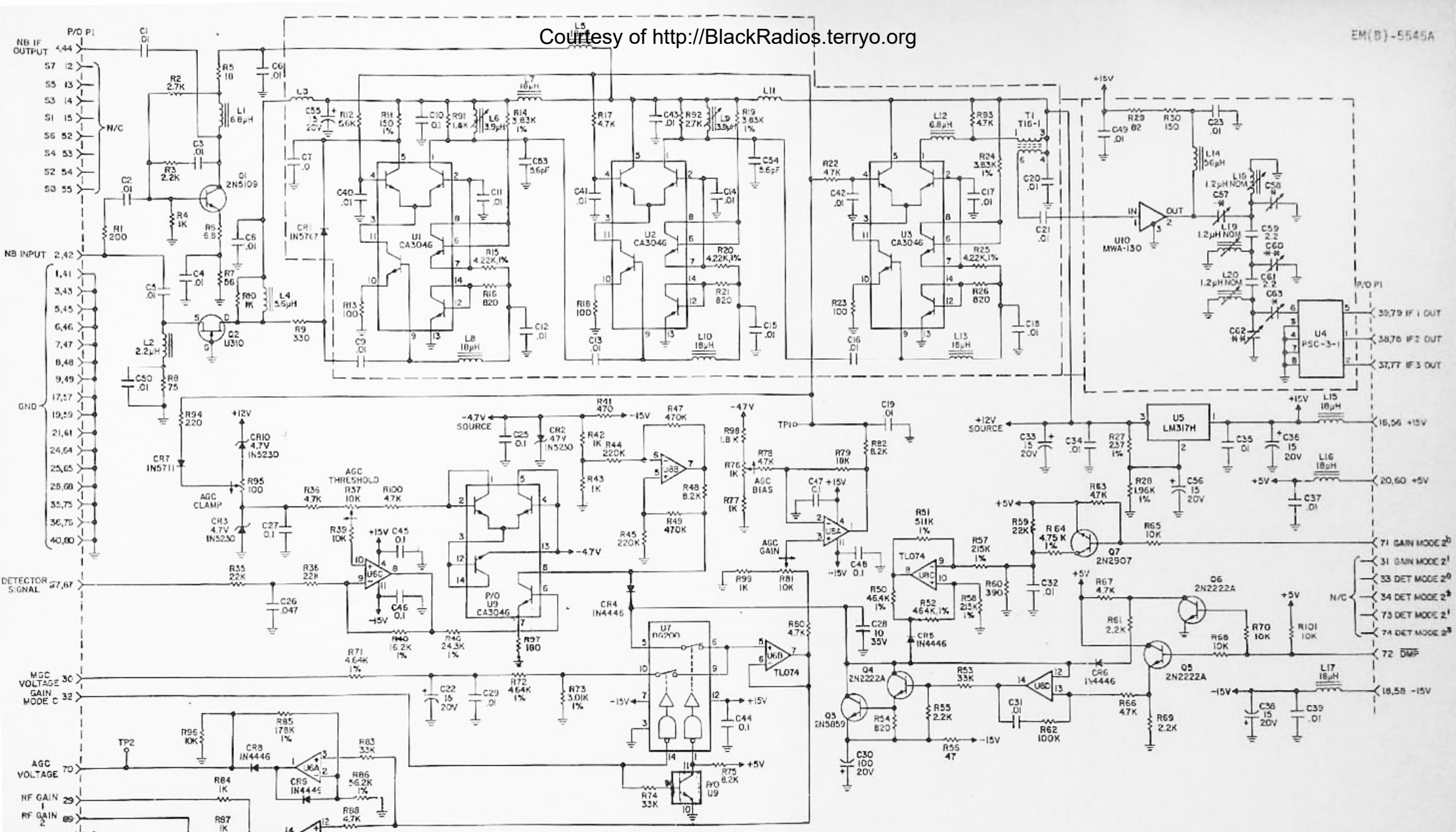


Figure 7-20. IF Control Interface Circuit Card Assembly (A6A1) Schematic Diagram (Sheet 2 of 2)



NOTES

1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4 W ±5% - 1% RESISTORS ARE 1/10W.
   b) CAPACITANCE IS IN µF.
2. * DENOTES 2.5 - 27 pF.
   ** DENOTES 6.0 - 60 pF.

HIGHEST REF DESIG	REF DESIG NOT USED
C63 Q3	R84 - R34
CR10 R101	C24
T1	C51
U10 TP2 P1 J10	

Figure 7-21. Variable Gain Amplifier Circuit Card Assembly (A6A2) Schematic Diagram

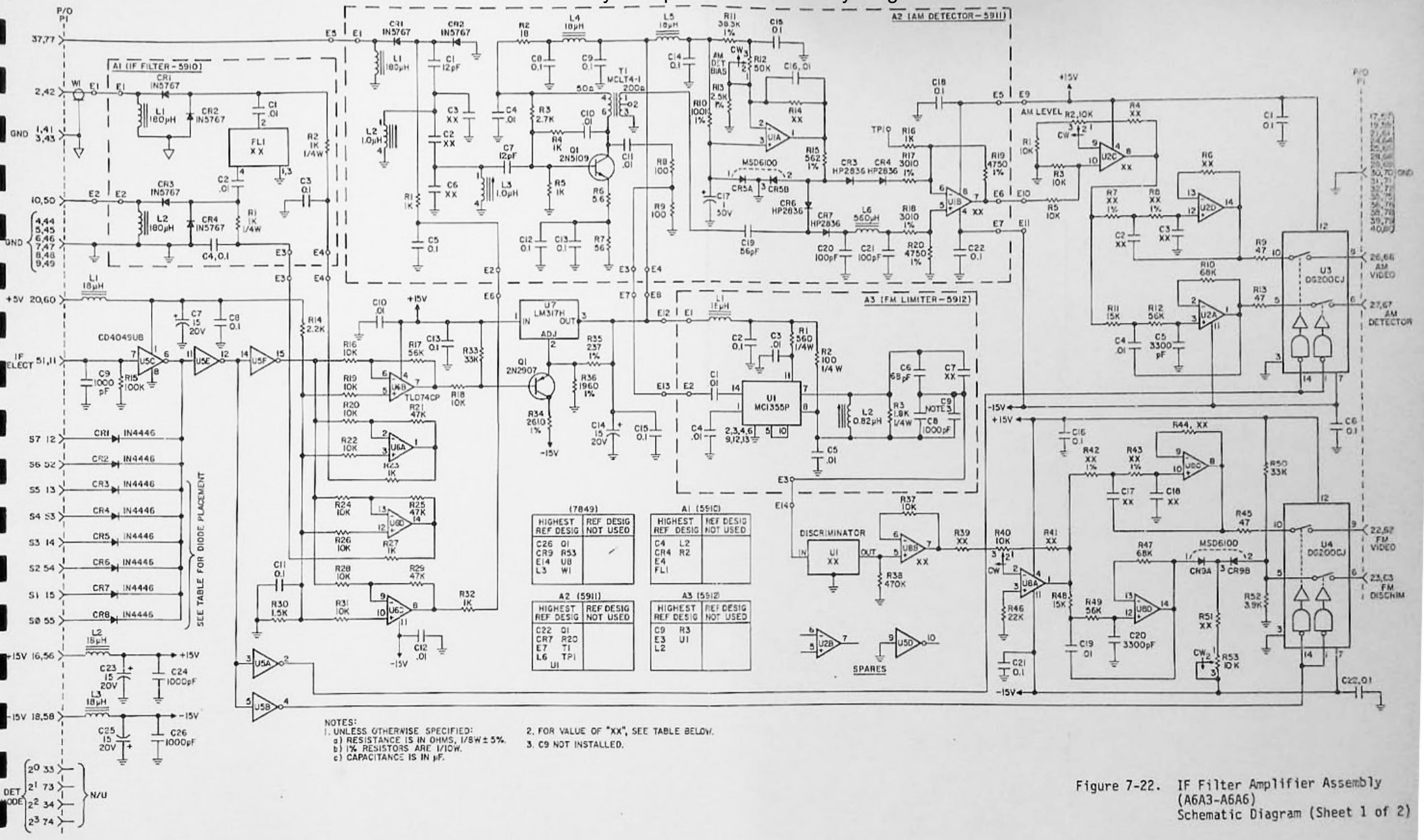


Figure 7-22. IF Filter Amplifier Assembly (A6A3-A6A6) Schematic Diagram (Sheet 1 of 2)

DASH NO.	BANDWIDTH	C2	C3	C17	C18	CR3	CR4	CR5	CR6	CR7	CR8	R4	R6	R7	R8	R39	R41	R42	R43	R44	R51	U1	U2 U8	A1FL1	A2C2	A2C3 A2C6	A2R14	A2U1	A3C7
-10	10 kHz	3300 pF	1000 pF	3300 pF	1000 pF	✓	N/U	✓	✓	✓	✓	10K	2.2K	4220	17.8K	4.7K	68K	4220	17.8K	22K	12K	3629 -10	TL074	3628 -10	10pF	47pF	30.1K	TL072	18pF
-13	20kHz	3300 pF	1000 pF	3300 pF	1000 pF	✓	N/U	✓	✓	N/U	N/U	↕	12K	2150	9090	10K	68K	2150	9090	12K	↕	3629 -13	↕	3628 -13	↕	↕	↕	↕	18pF
-17	50 kHz	1000 pF	330 pF	1000 pF	330 pF	✓	N/U	✓	N/U	N/U	N/U	↕	12K	2870	11.0K	4.7K	39K	2870	11.0K	12K	↕	3629 -17	↕	3628 -17	↕	↕	↕	↕	N/U
-20	100kHz	1000 pF	330 pF	1000 pF	330 pF	✓	N/U	N/U	✓	N/U	✓	10K	6.8K	1470	5620	10K	39K	1820	6810	6.8K	12K	3629 -20	TL074	3628 -20	10pF	47pF	30.1K	TL072	↕
-23	200kHz	1000 pF	330 pF	1000 pF	330 pF	✓	N/U	N/U	N/U	✓	N/U	6.8K	3.3K	681	2670	4.7K	24K	715	3240	3.3K	15K	9822 -23	LF347	9821 -23	2.2pF	43pF	40.2K	NE 5532	↕
-26	400kHz	330 pF	100 pF	330 pF	100 pF	N/U	✓	✓	✓	✓	✓	6.8K	5.6K	1020	4530	10K	30K	1020	4530	5.6K	18K	9822 -26	LF347	9821 -26	2.2pF	43pF	40.2K	NE 5532	N/U

Figure 7-22. IF Filter Amplifier Assembly (A6A3-A6A6) Schematic Diagram (Sheet 2 of 2)

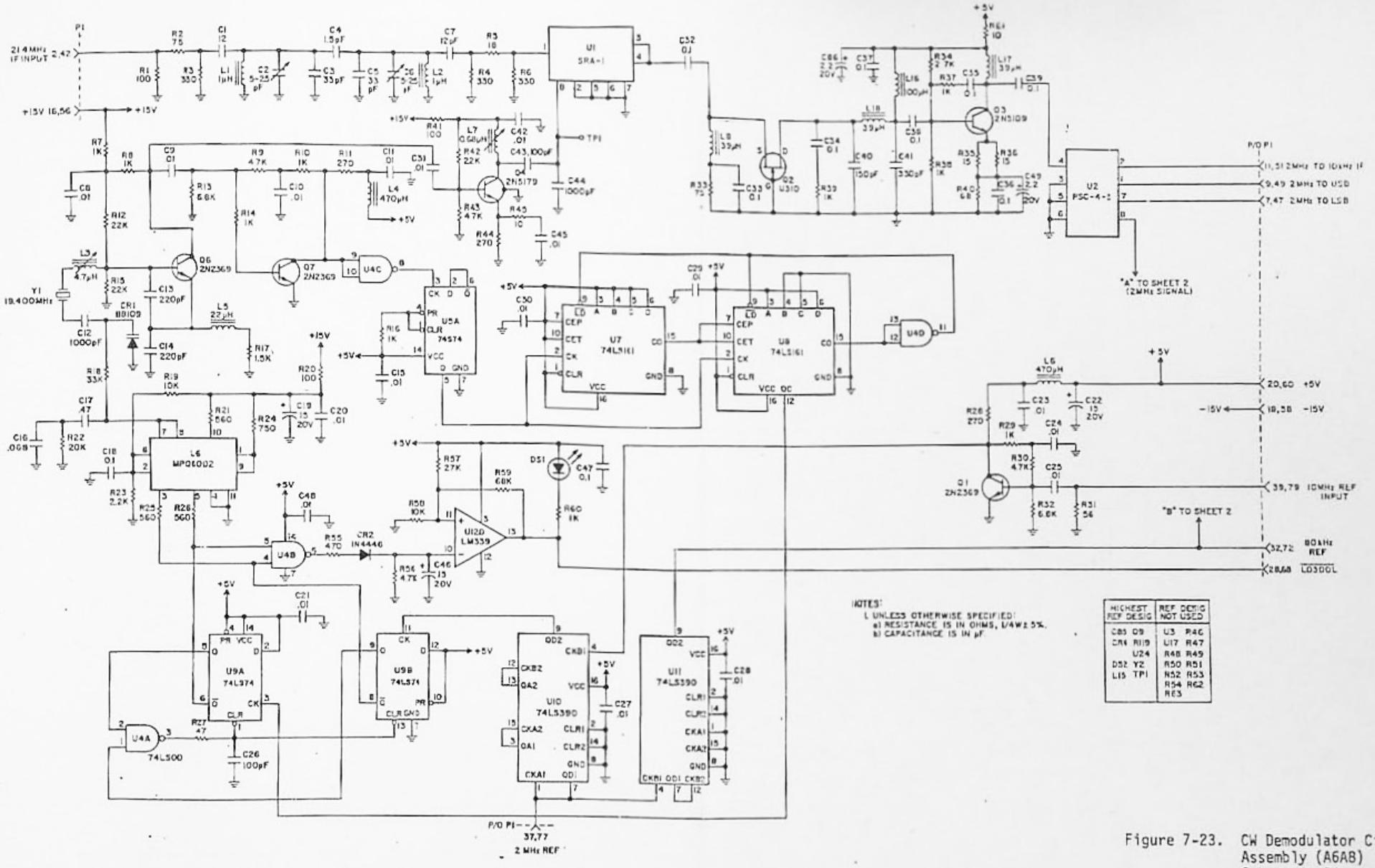


Figure 7-23. CW Demodulator Circuit Card Assembly (A6A8) Schematic Diagram (Sheet 1 of 2)

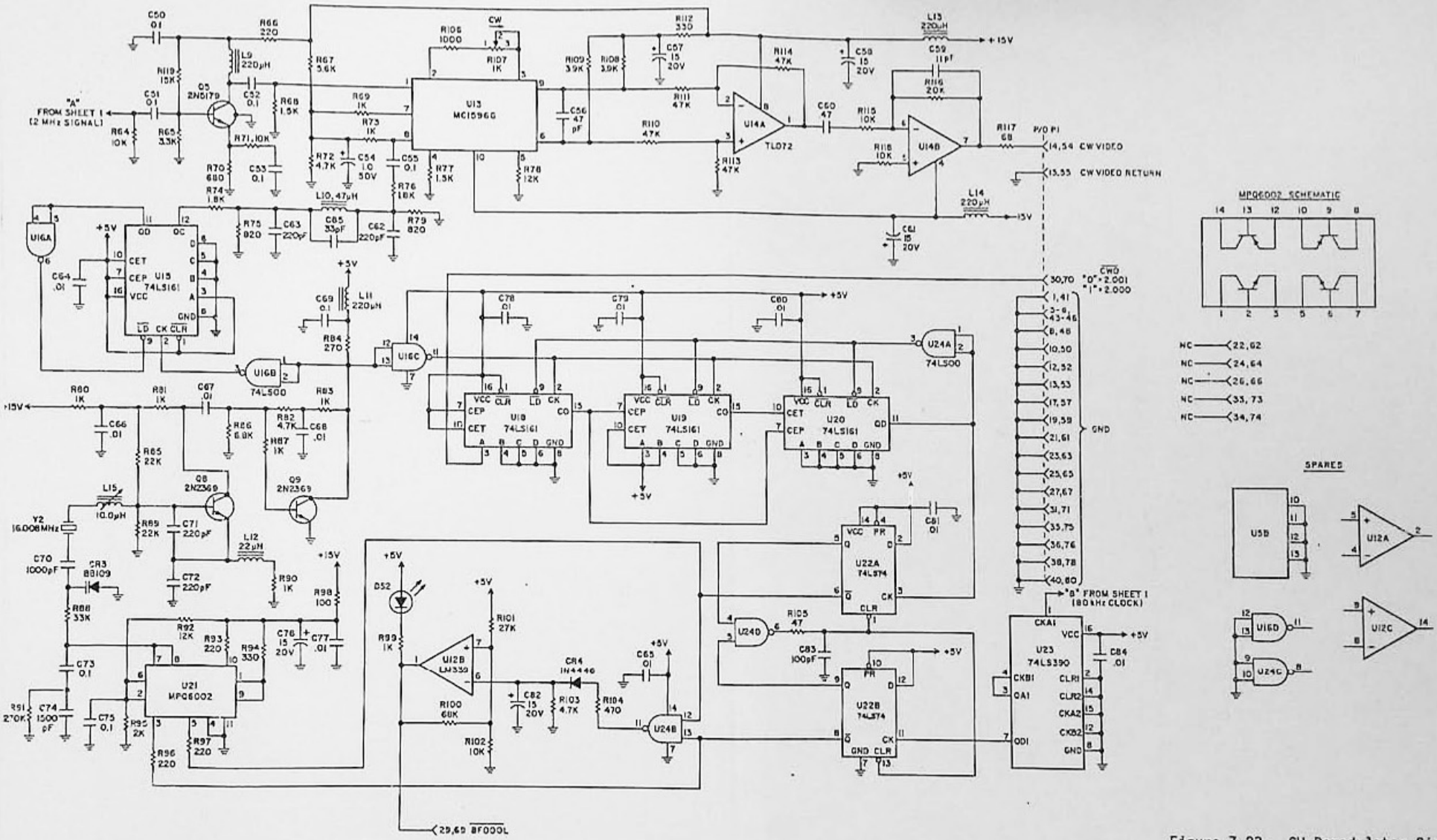


Figure 7-23. CW Demodulator Circuit Card Assembly (A6A8) Schematic Diagram (Sheet 2 of 2)

NOTES:
1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400213 PWB 400248 WIRE LIST 400309
4. LEGEND:
   - — — — DENOTES WIRE WRAP
   - ——— DENOTES P.C. TRACK

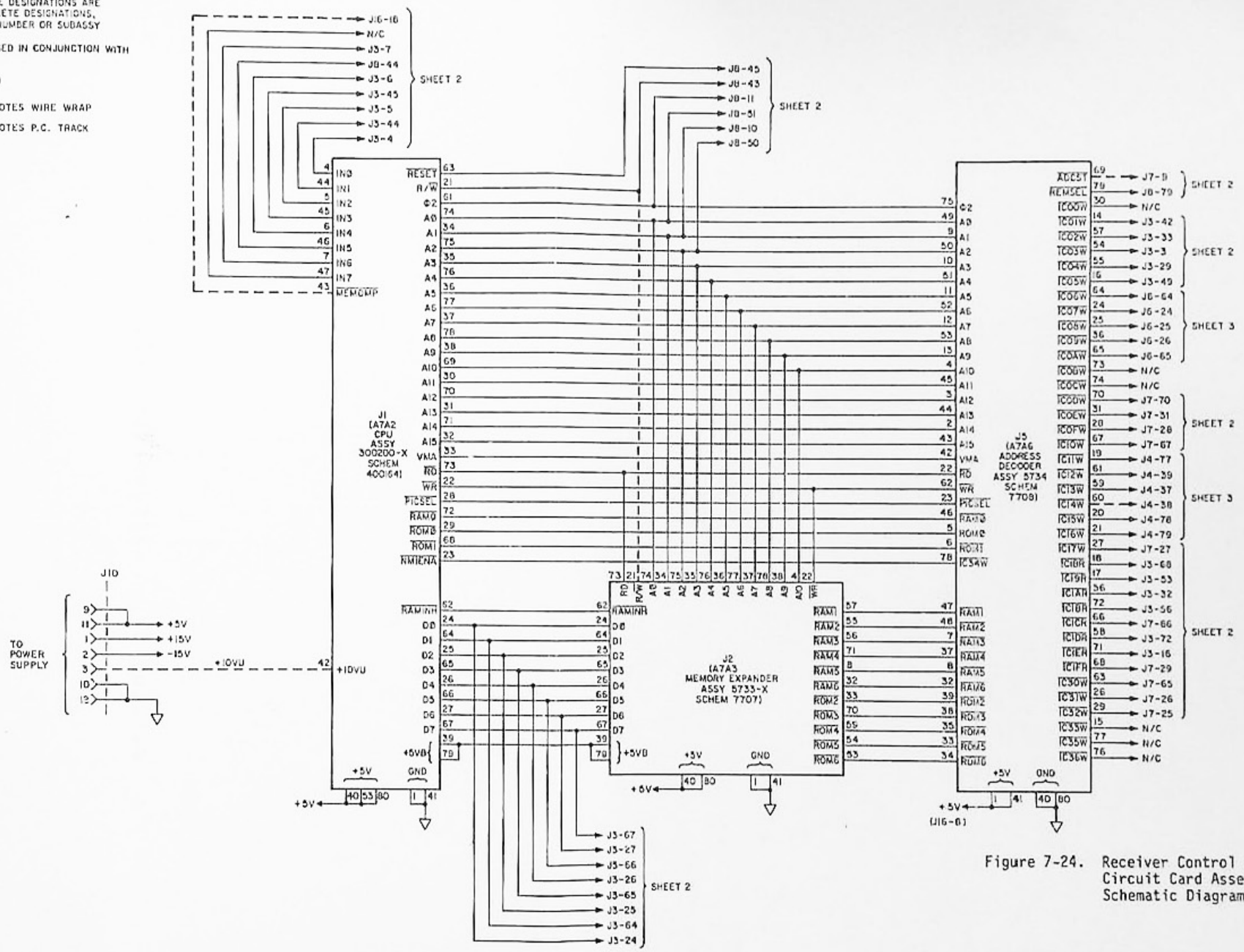


Figure 7-24. Receiver Control Interface Circuit Card Assembly (A7A1) Schematic Diagram (Sheet 1 of 3)

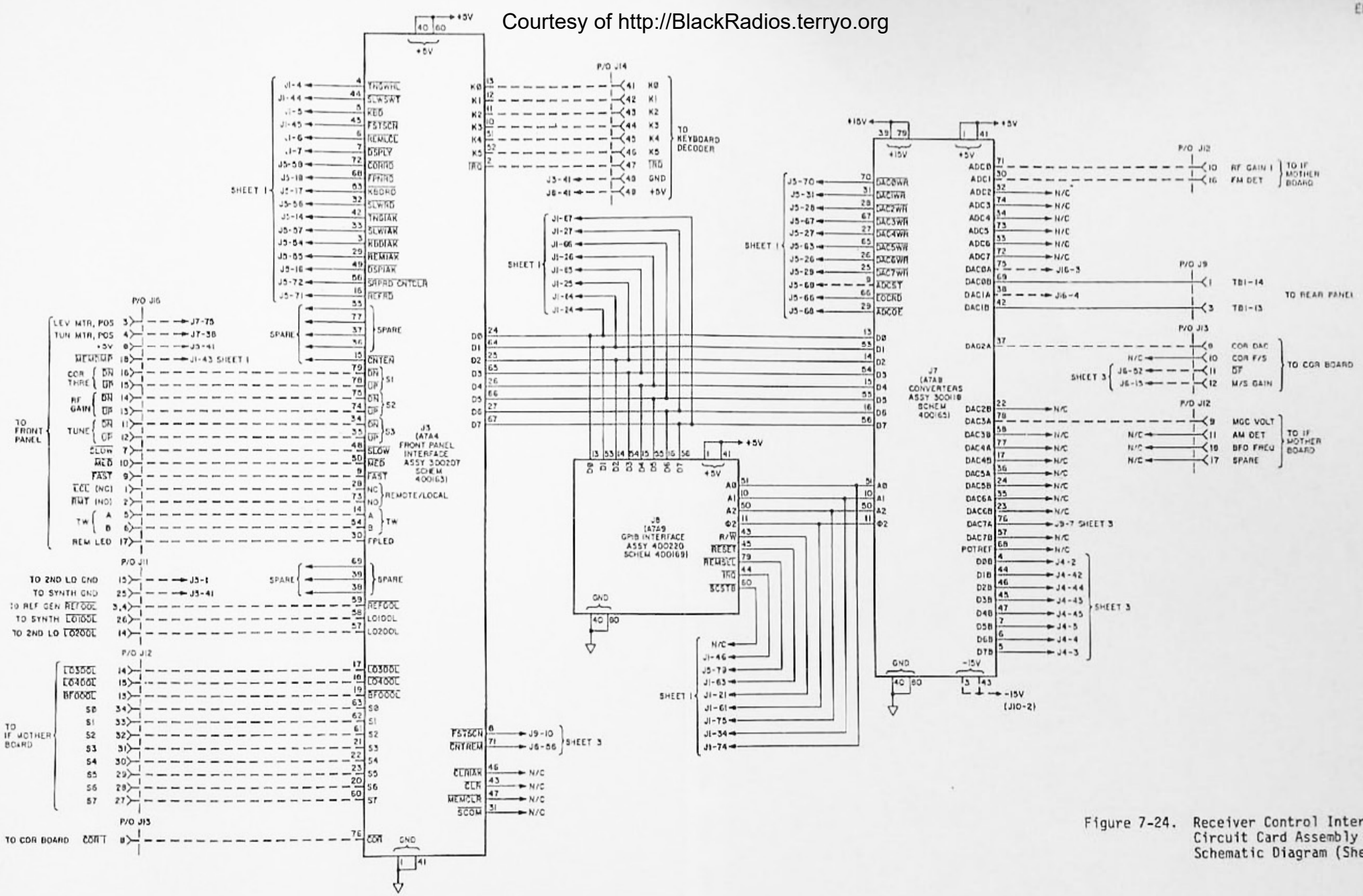


Figure 7-24. Receiver Control Interface Circuit Card Assembly (A7A1) Schematic Diagram (Sheet 2 of 3)

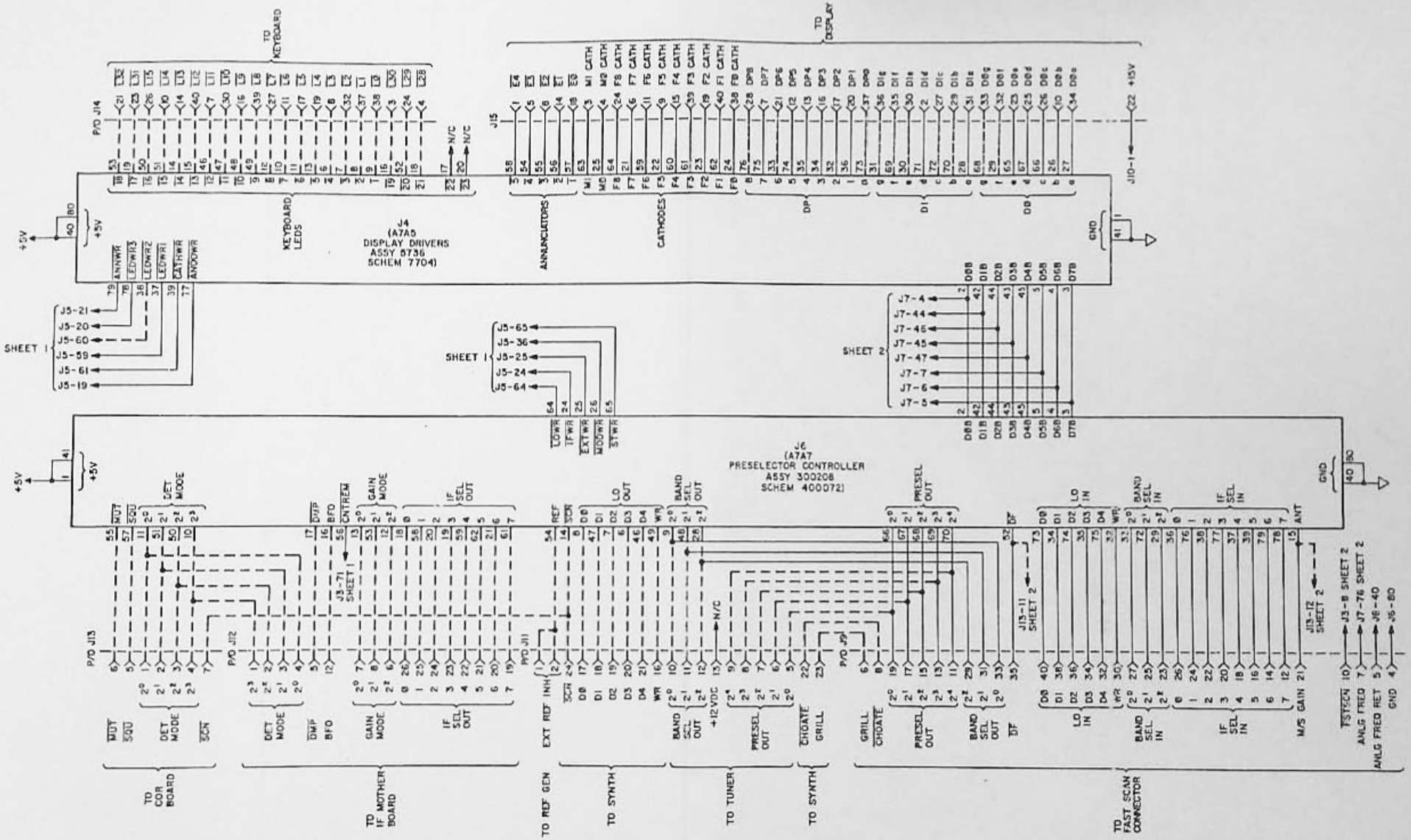


Figure 7-24. Receiver Control Interface Circuit Card Assembly (A7A1) Schematic Diagram (Sheet 3 of 3)

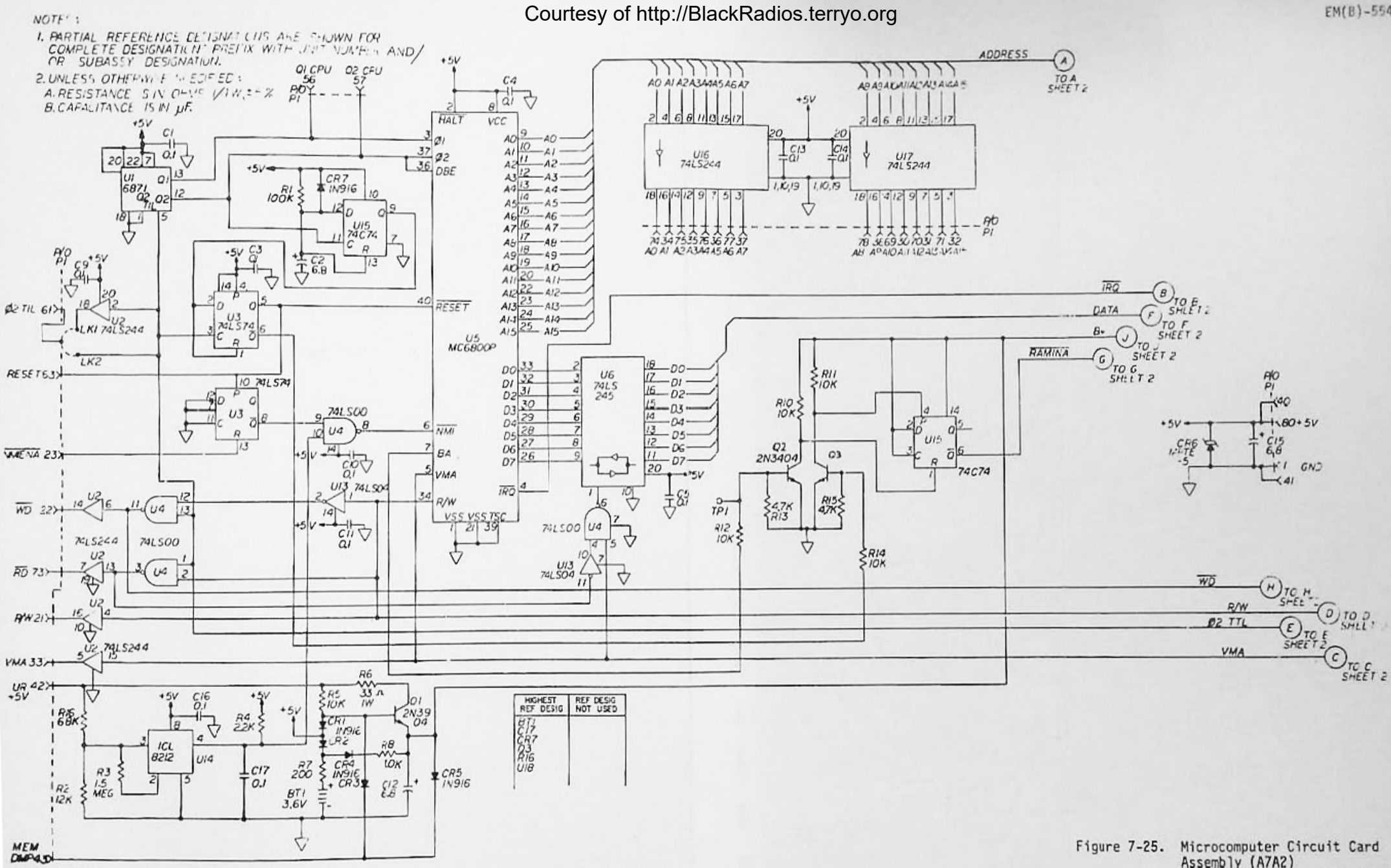


Figure 7-25. Microcomputer Circuit Card Assembly (A7A2) Schematic Diagram (Sheet 1 of 2)

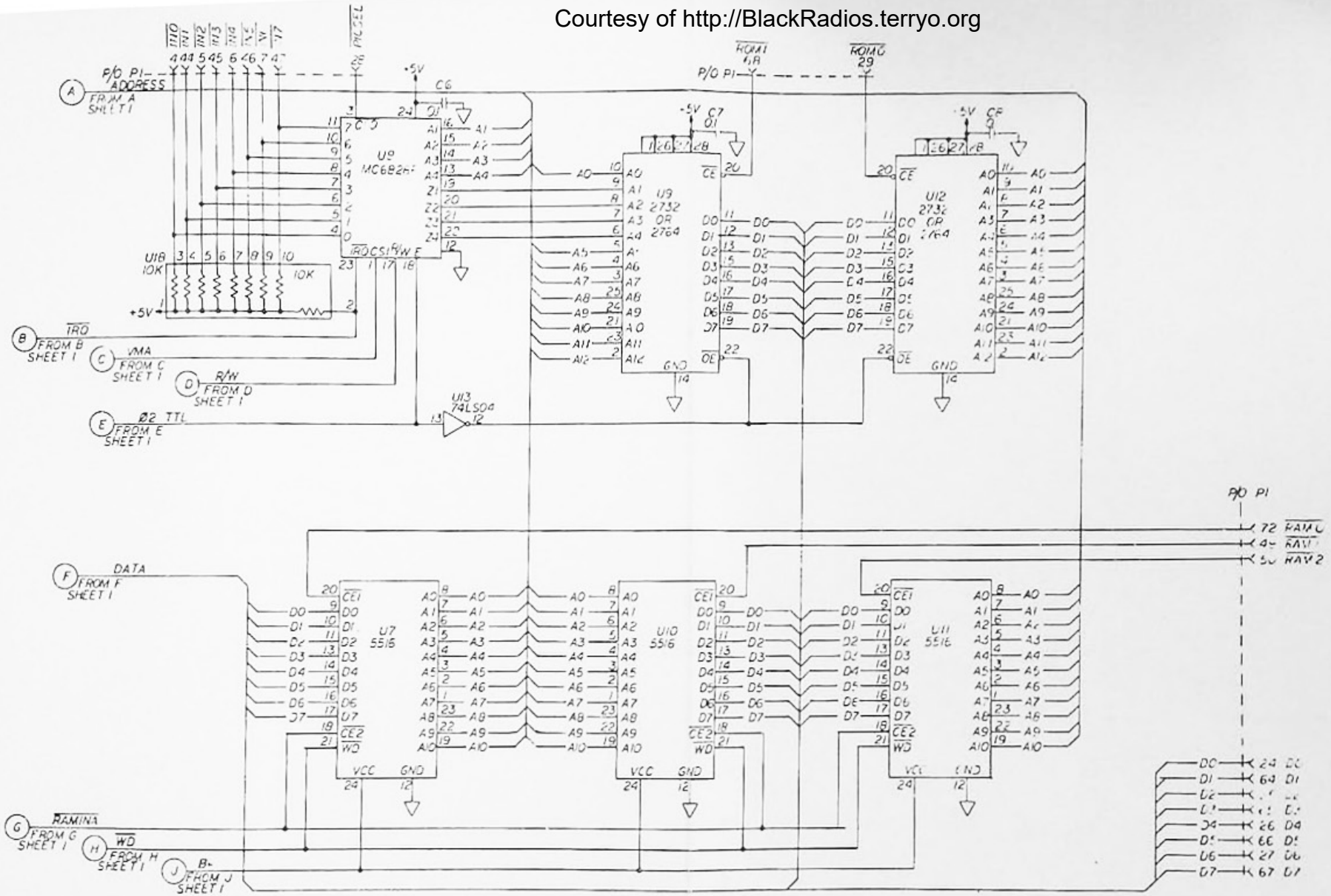


Figure 7-25. Microcomputer Circuit Card Assembly (A7A2) Schematic Diagram (Sheet 2 of 2)

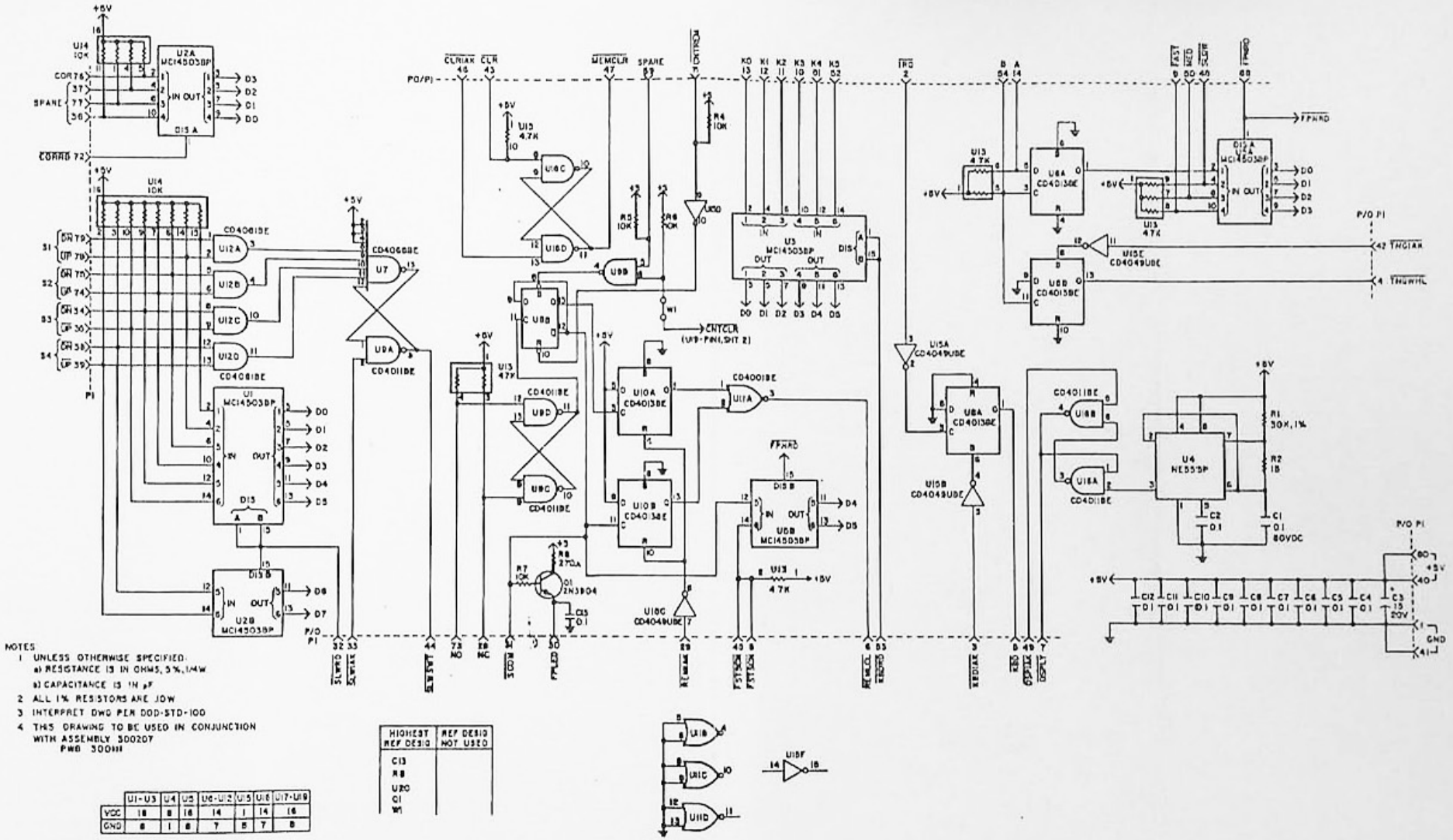


Figure 7-26. Front Panel I/O Control Interface Circuit Card Assembly (A7A4) Schematic Diagram (Sheet 1 of 2)

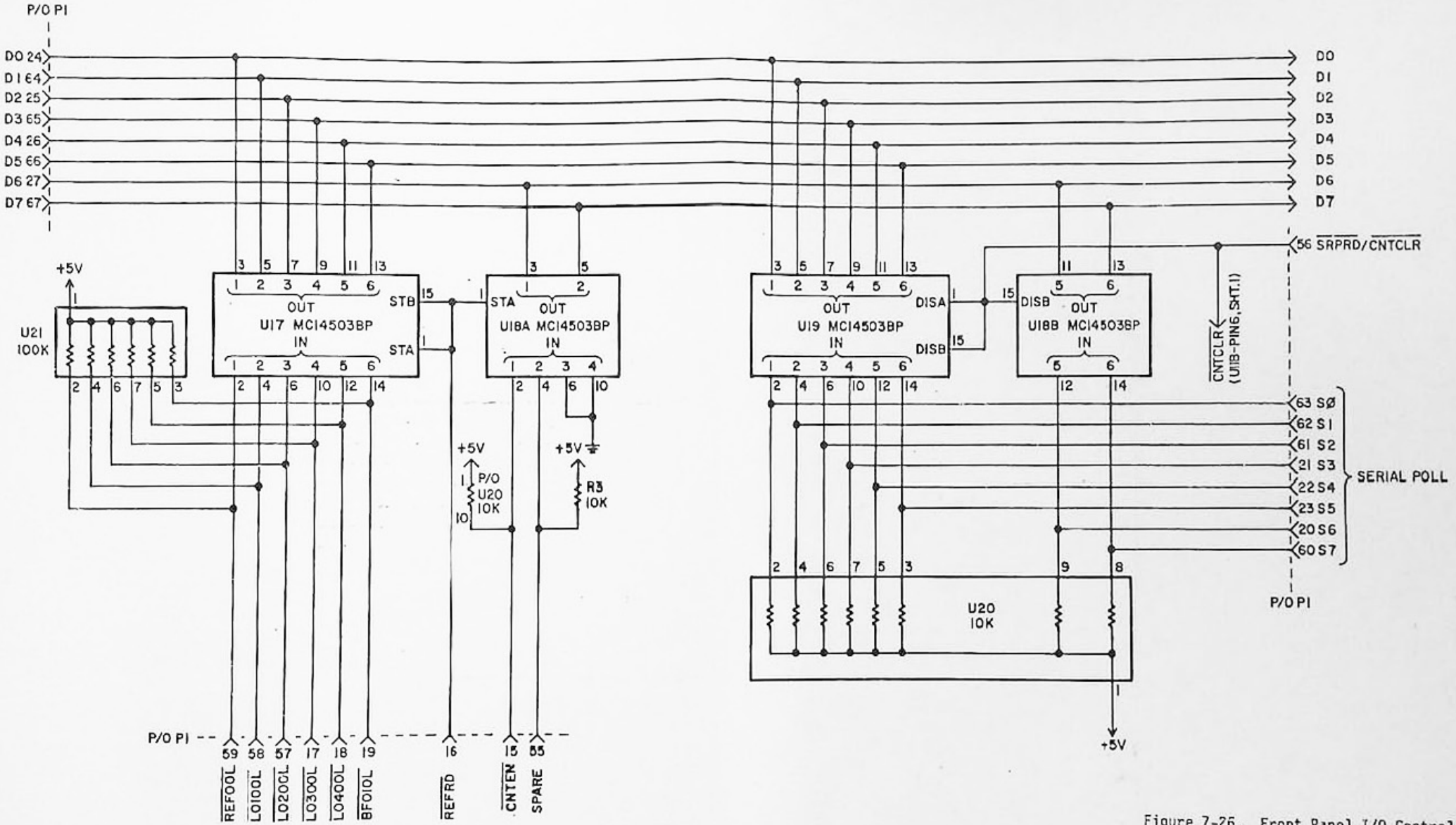
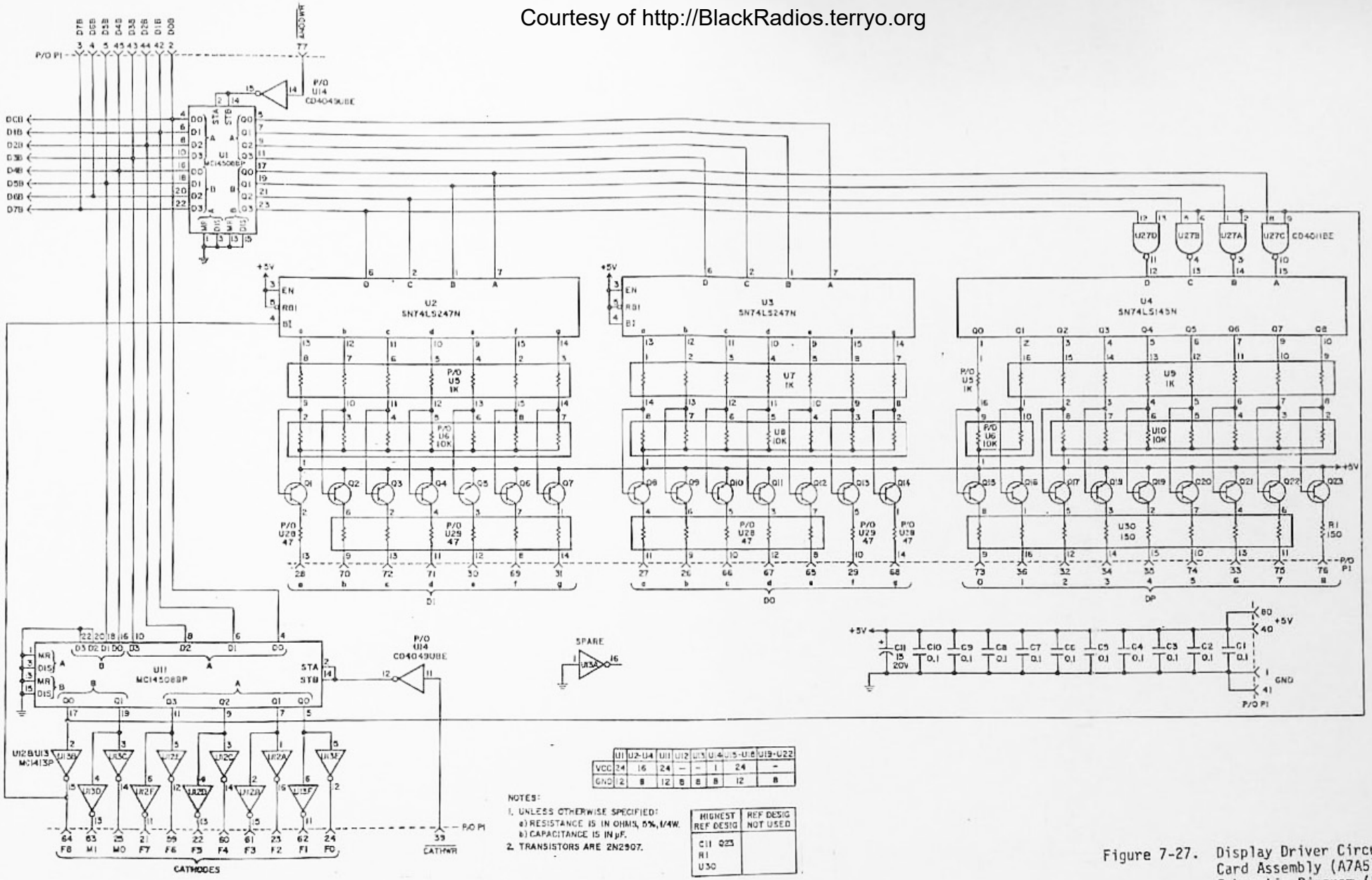


Figure 7-26. Front Panel I/O Control Interface Circuit Card Assembly (A7A4) Schematic Diagram (Sheet 2 of 2)



	U1	U2-U4	U11	U12	U13	U14	U15-U18	U19-U22
VCC	24	16	24	–	–	1	24	–
GND	12	8	12	8	8	8	12	8

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 5%, 1/4W.
   b) CAPACITANCE IS IN μF.
2. TRANSISTORS ARE 2N2907.

HIGHEST REF DESIG	REF DESIG NOT USED
C11 Q23 R1 U30	

Figure 7-27. Display Driver Circuit Card Assembly (A7A5) Schematic Diagram (Sheet 1 of 2)

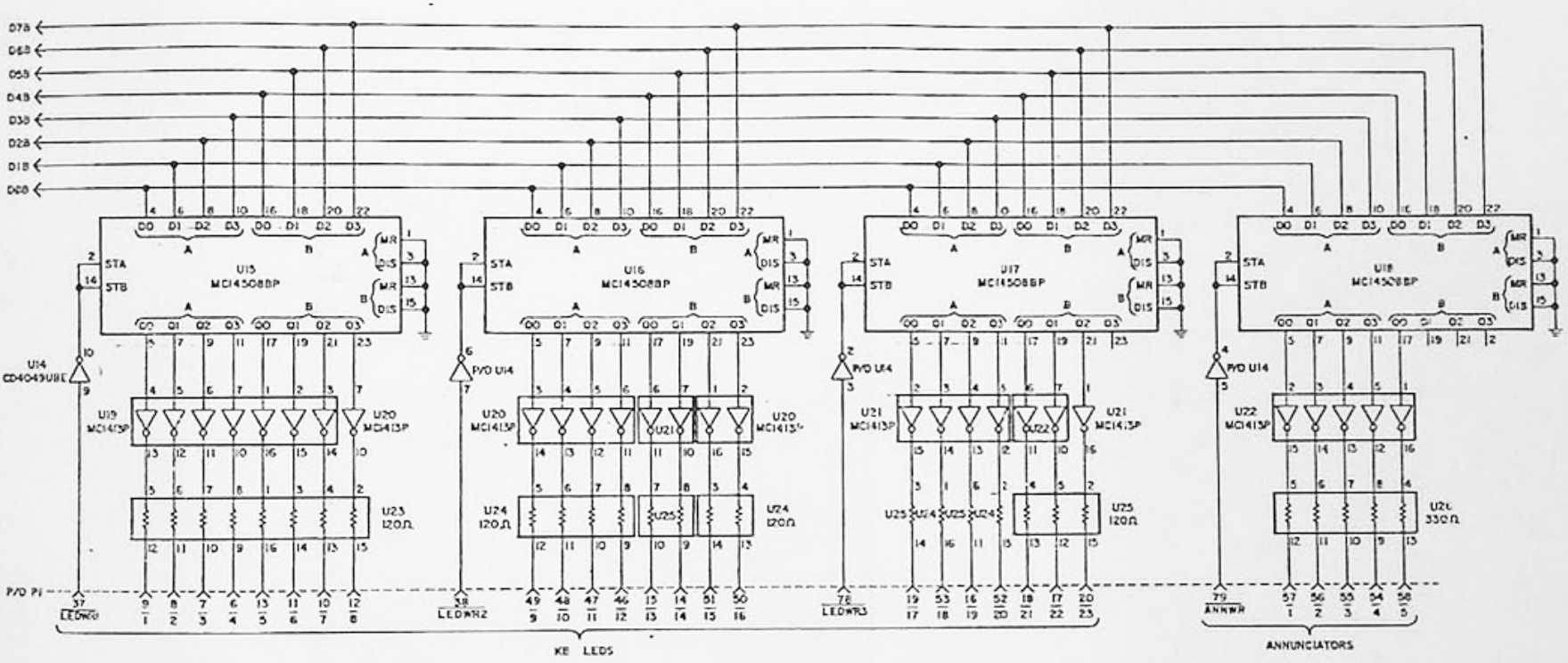


Figure 7-27. Display Driver Circuit Card Assembly (A7A5) Schematic Diagram (Sheet 2 of 2)

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
2. UNLESS OTHERWISE SPECIFIED
   A. RESISTANCE IS IN OHMS, 1/4 W, ±2%.
   B. CAPACITANCE IS IN μF.

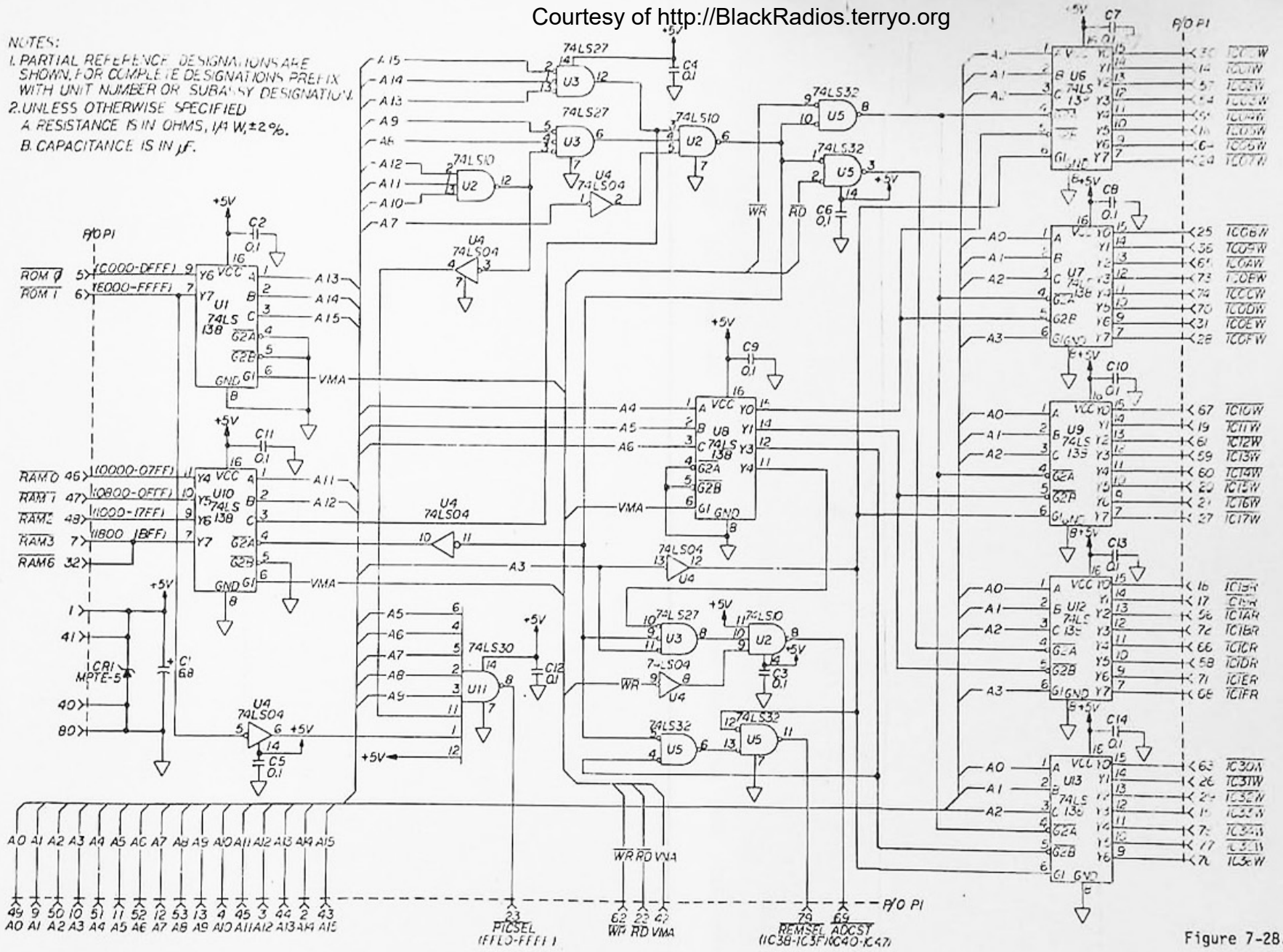
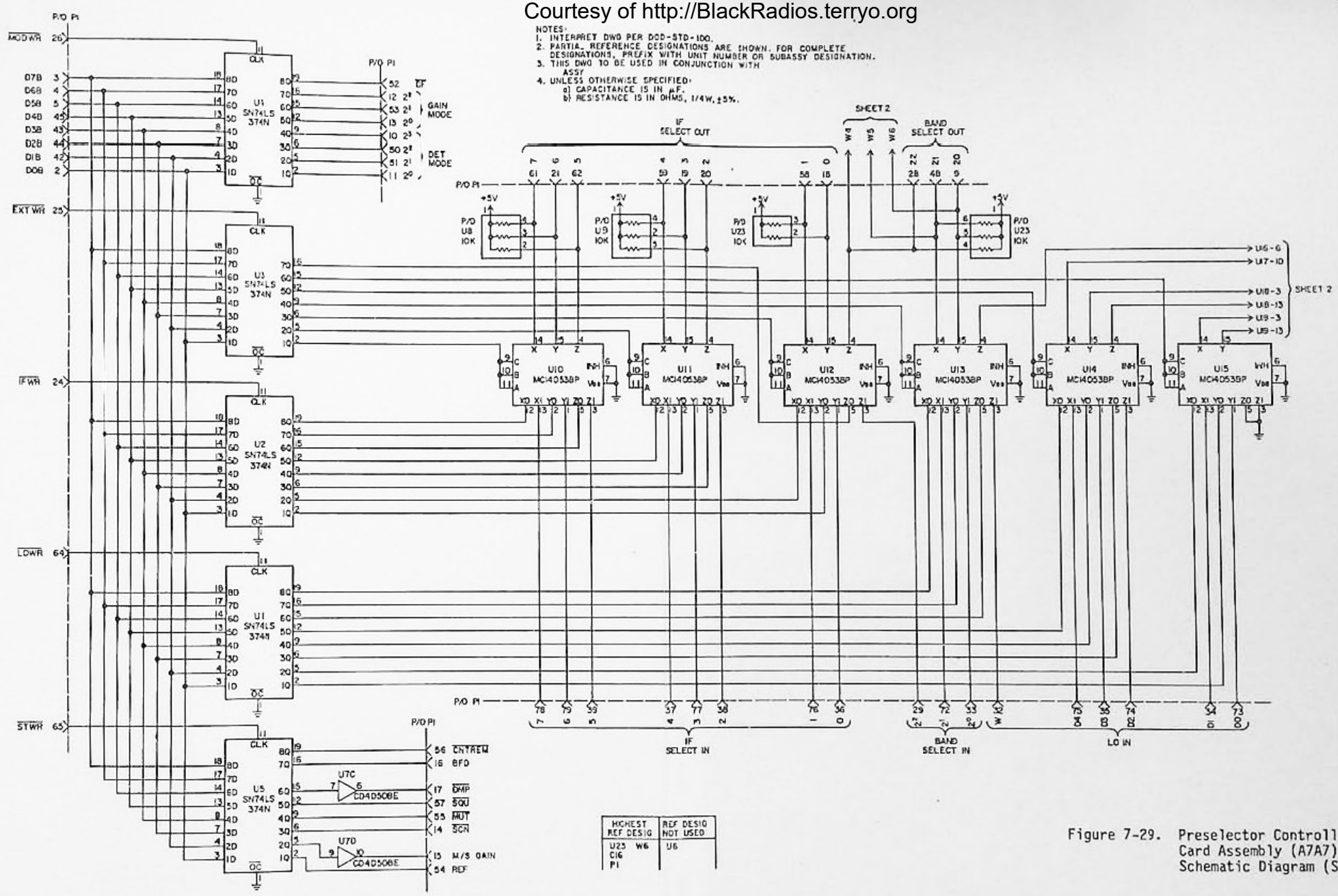


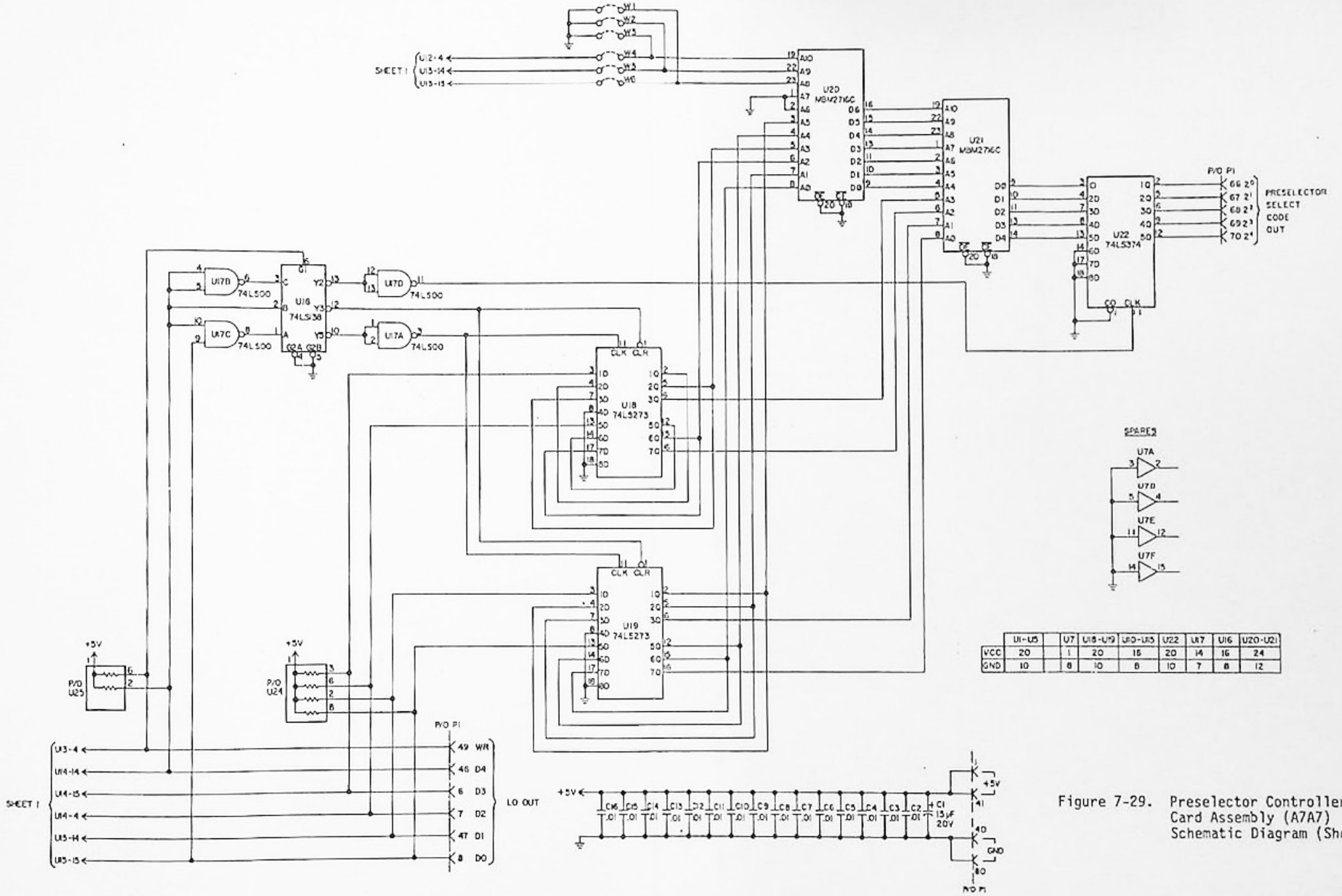
Figure 7-28. Address Decoder Circuit Card Assembly (A7A6) Schematic Diagram

NOTES:
1. INTERPRET DWG PER DOD-STD-100.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY
4. UNLESS OTHERWISE SPECIFIED:
   a) CAPACITANCE IS IN μF.
   b) RESISTANCE IS IN OHMS, 1/4W, ±5%.



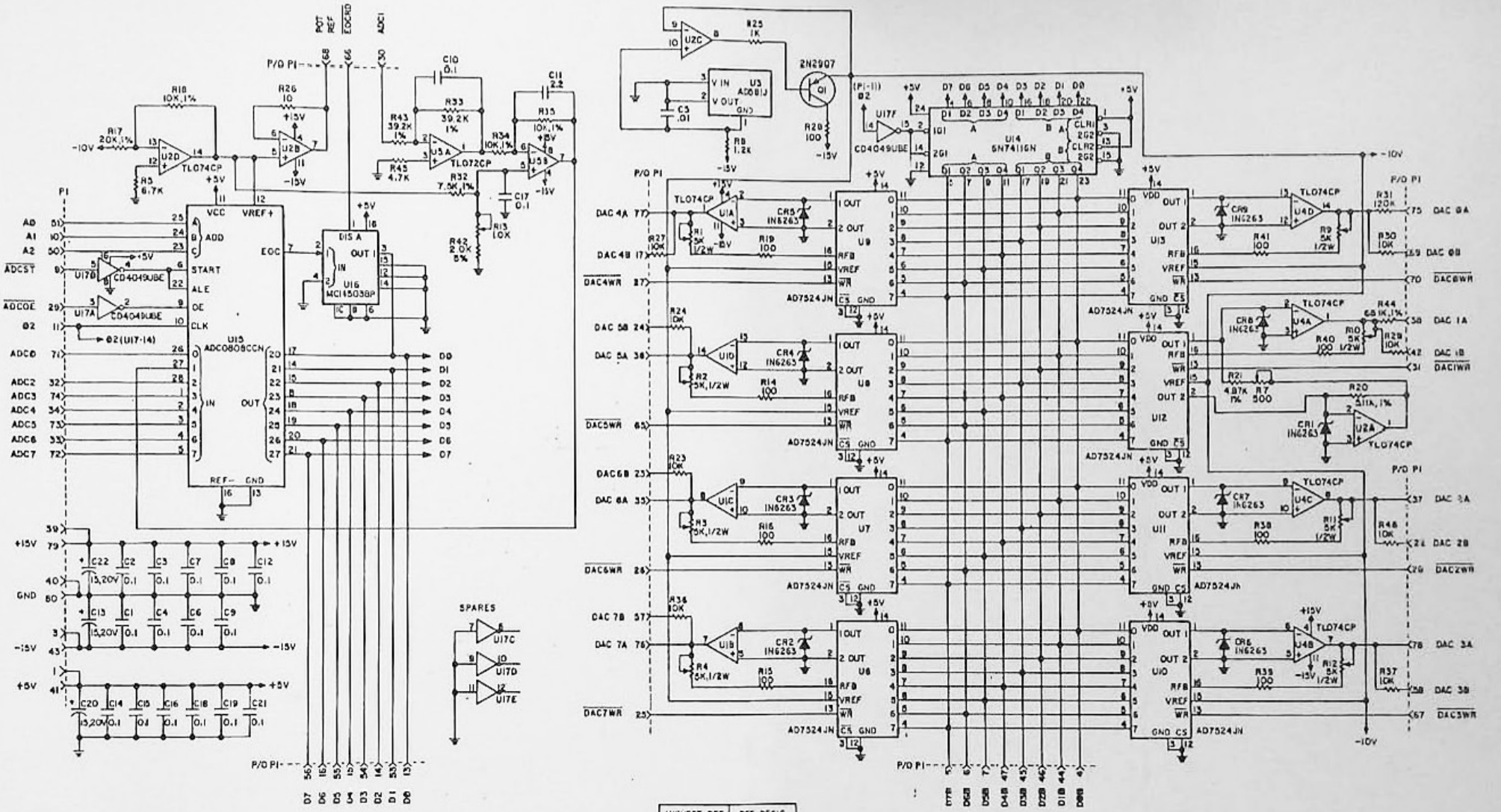
HIGHEST REF DESIG	REF DESIG NOT USED
U23 W6 C16 P1	U6

Figure 7-29. Preselector Controller Circuit Card Assembly (A7A7) Schematic Diagram (Sheet 1 of 2)



	U1-U5	U7	U18-U19	U13-U15	U22	U17	U16	U20-U21
VCC	20	1	20	16	20	14	16	24
GND	10	8	10	8	10	7	8	12

Figure 7-29. Preselector Controller Circuit Card Assembly (A7A7) Schematic Diagram (Sheet 2 of 2)



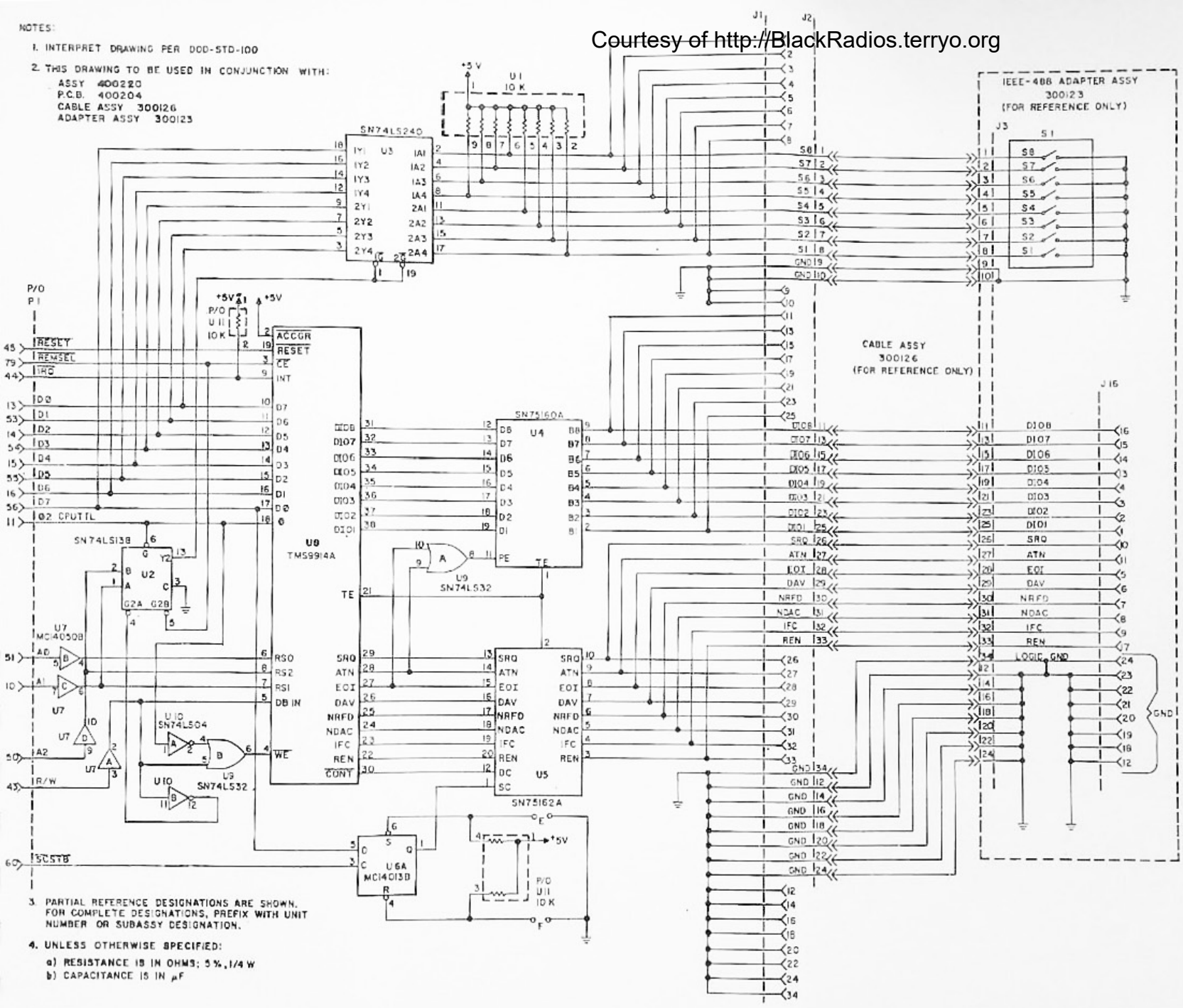
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 5%, 1/4W
   b) CAPACITANCE IS IN μF.
2. ALL 1% RESISTORS ARE .10W

HIGHEST REF DESIG USED	REF DESIG NOT USED
R46	R6, R22
C22	
CR9	
U17	
Q1	

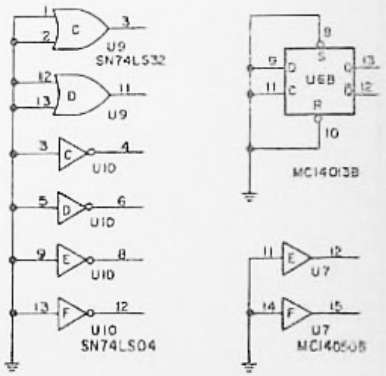
Figure 7-30. Converter Circuit Card Assembly (A7A8) Schematic Diagram

NOTES:

1. INTERPRET DRAWING PER DOD-STD-100
2. THIS DRAWING TO BE USED IN CONJUNCTION WITH:
   ASSY 400220
   P.C.B. 400204
   CABLE ASSY 300126
   ADAPTER ASSY 300123
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
4. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS; 5%, 1/4 W
   b) CAPACITANCE IS IN μF



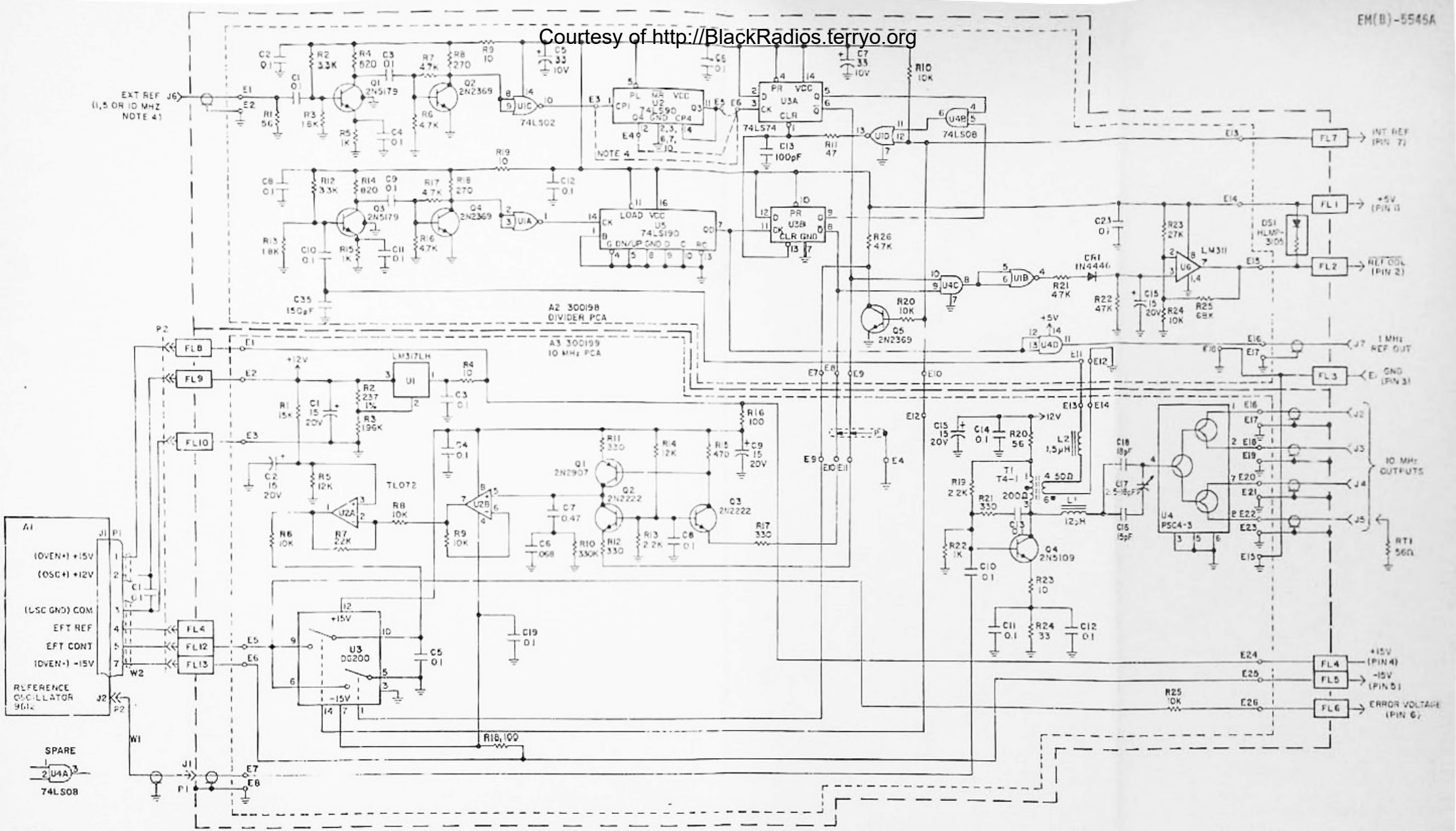
SPARES



HIGHEST REF DESIG	REF DESIG NOT USED
C 11	
J 2	
P 1	
U 11	

	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11
VCC	1	16	20	20	22	14	1	40	14	14	1
GND	—	8	10	10	11	7	8	20	7	7	—

Figure 7-31. IEEE-488C Remote Control Interface Circuit Card Assembly (A7A9) Schematic Diagram (Optional)



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4W ±5%
   b) CAPACITANCE IS IN µF
2. INTERPRETE DWG PER DOD-STD-100
3. THIS DWG USED IN CONJUNCTION WITH ASSEMBLY DWG 400251.
4. STRAP AS FOLLOWS.

EXT REF FREQ	U2 INSTALLED	JUMPER
1MHZ	NO	E3-E6
5MHZ	YES	E5-E6
10MHZ	YES	E4-E6

400251

HIGHEST REF DESIG	REF DESIG NOT USED
A3 DS1	
C1	
FL13	
J7	
P3	
W1	

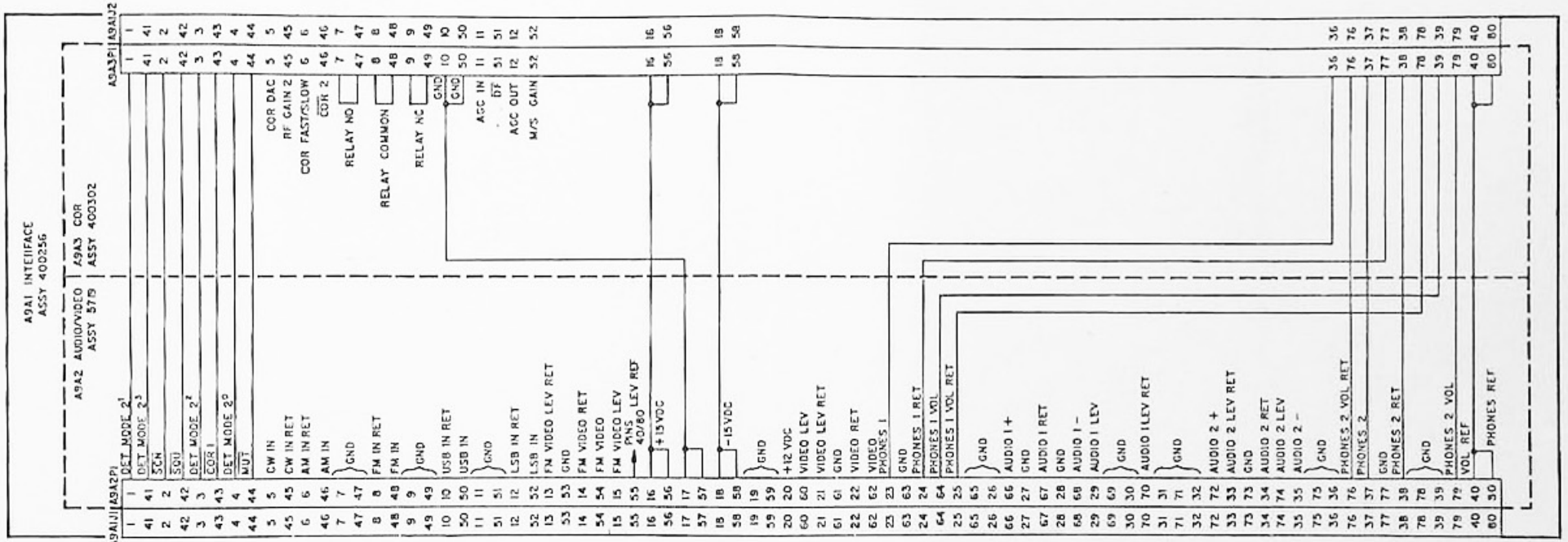
A2 (300198)

HIGHEST REF DESIG	REF DESIG NOT USED
C35 U6	C14
CR1	C17-22
E18	
Q5	
R26	

A3 (300199)

HIGHEST REF DESIG	REF DESIG NOT USED
C19 U4	
E26	
L2	
Q4	
R25	
T1	

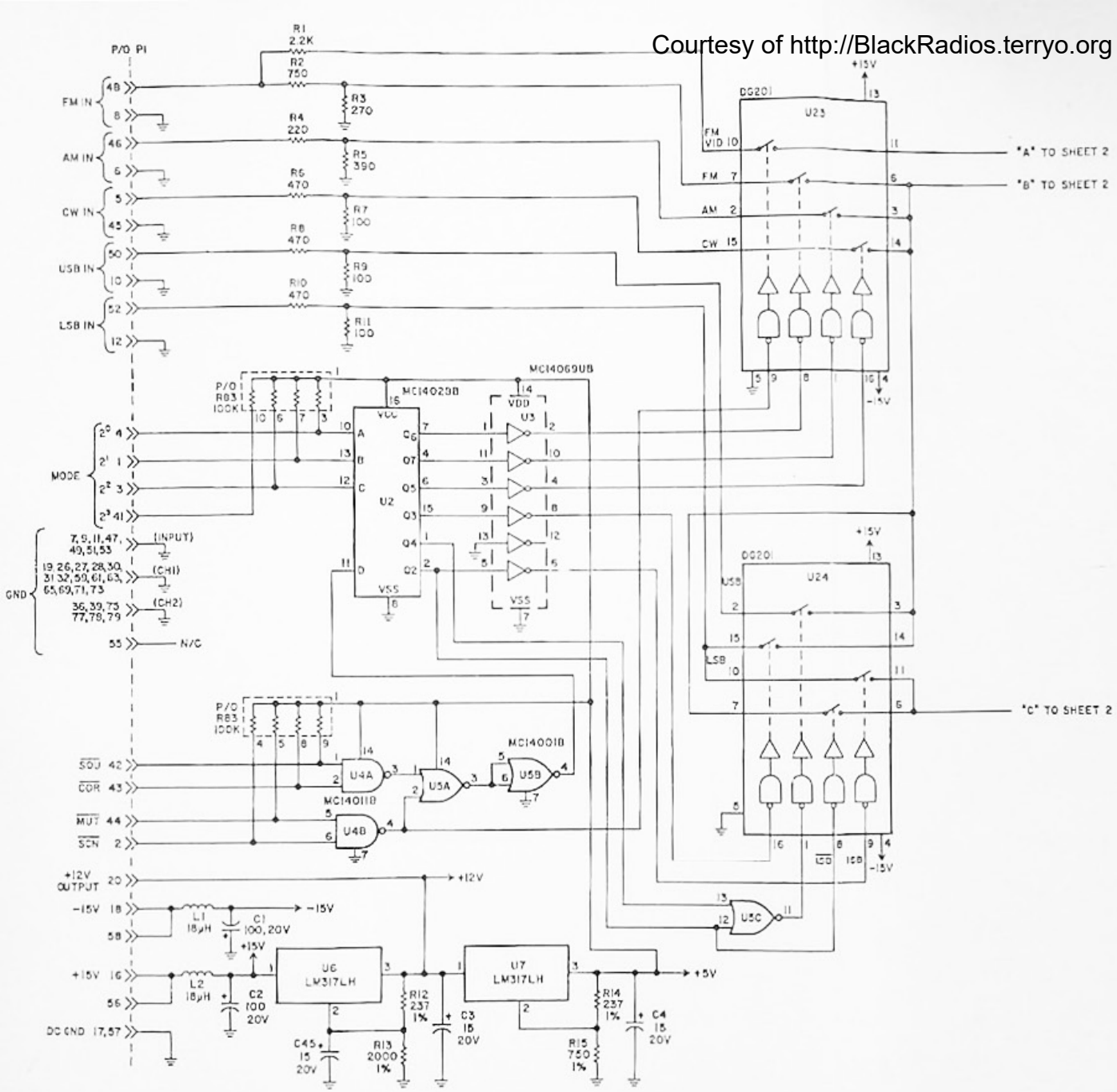
Figure 7-32. Reference Generator Module Assembly (A8) Schematic Diagram



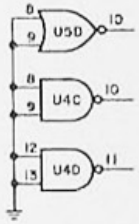
NOTES:

1. INTERPRET DWG PER DOD STD 100.
2. THIS DWG TO BE USED IN CONJUNCTION WITH
   ASSY 400256, 5719, 400302
   PWB 400300, 5719, 400301

Figure 7-33. Audio Video Control Interface Circuit Card Assembly (A9A1) Schematic Diagram



SPARES



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTANCE IS IN OHMS, 1/4W ± 5%.
   b) CAPACITANCE IS IN μF.
   c) 1% RESISTORS ARE 1/10W.
* 2. FOR 5719 USE LF356, FOR 5719-2 USE LF357

HIGHEST REF DESIG	REF DESIG NOT USED
R83	R25 R26
C45	R35 R48
U24	R59
L2	U1

Figure 7-34. Audio Video Amplifier Circuit Card Assembly (A9A2) Schematic Diagram (Sheet 1 of 2)

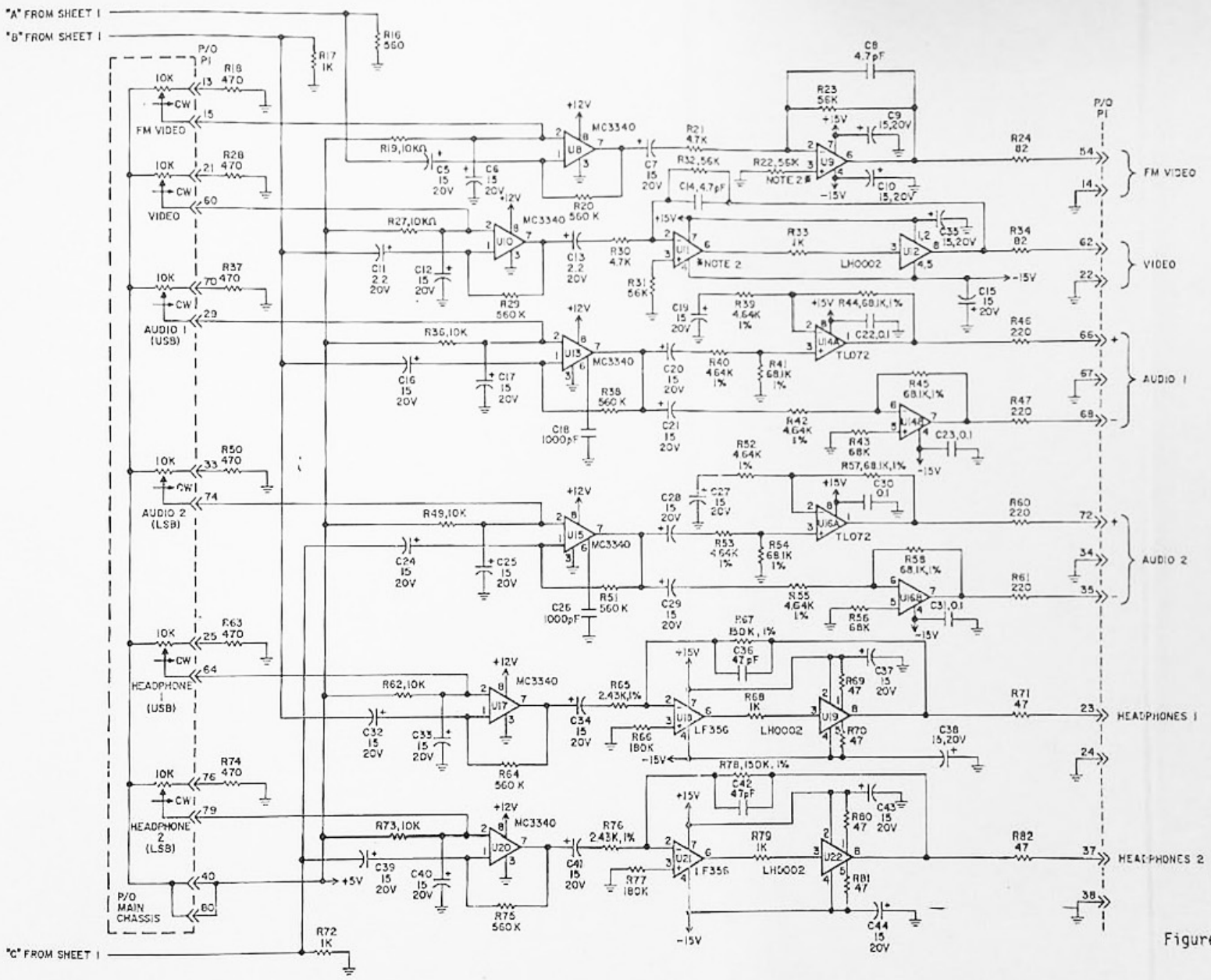


Figure 7-34. Audio Video Amplifier Circuit Card Assembly (A9A2) Schematic Diagram (Sheet 2 of 2)

NOTES:

1. INTERPRET DRAWING PER DOD-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION.
3. THIS DRAWING TO BE USED IN CONJUNCTION WITH
   ASSY 400302
   PWB 400301
4. UNLESS OTHERWISE SPECIFIED:
   a. RESISTANCE IS IN OHMS, 1/4 W, ± 5%.
   b. CAPACITANCE IS IN µF.

REF DESIG	NOT USED
C16	C7
CR2	
K1	
L2	
P1	
Q5	
R29	
U4	

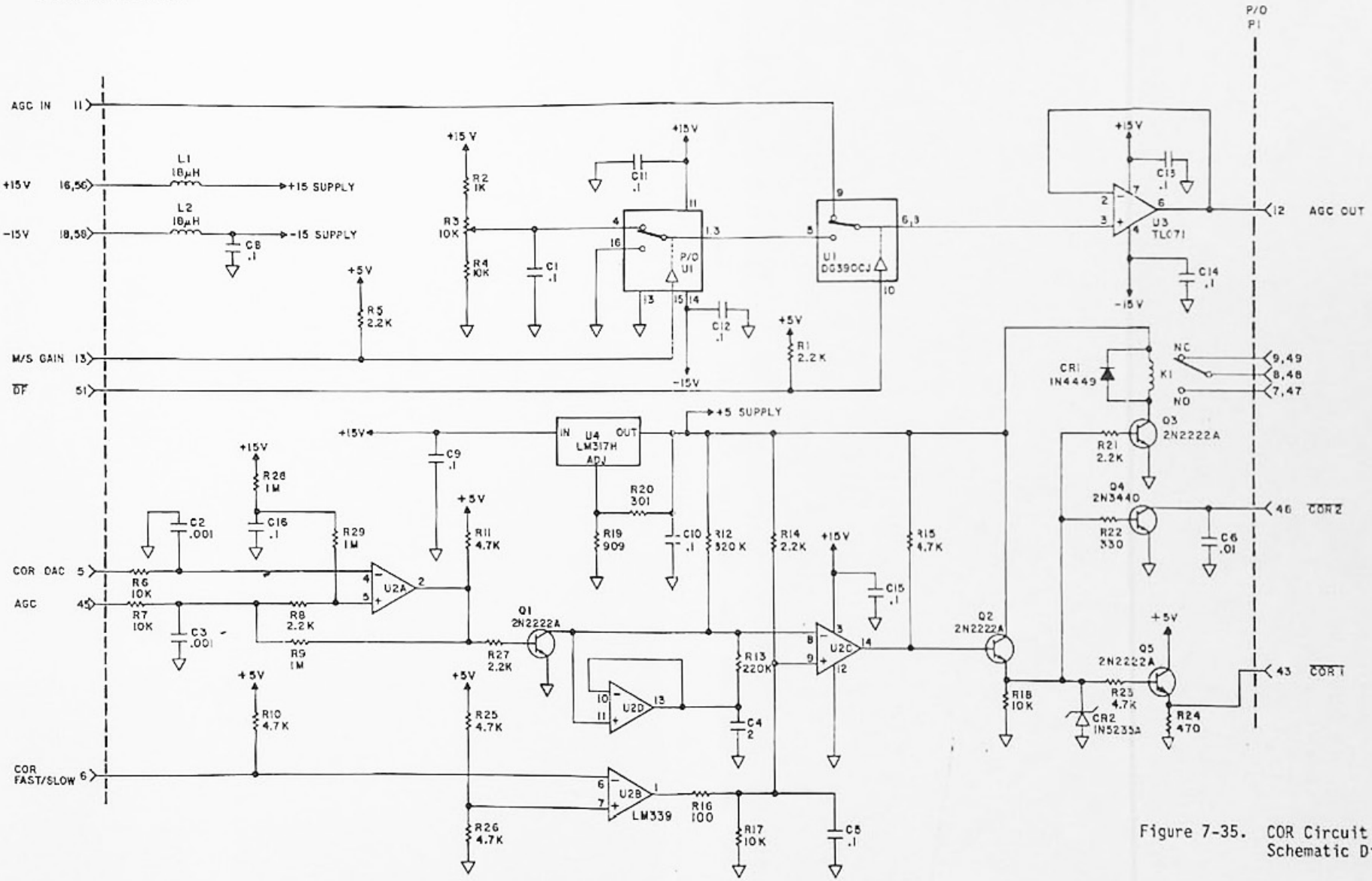


Figure 7-35. COR Circuit Card Assembly (A9A3) Schematic Diagram

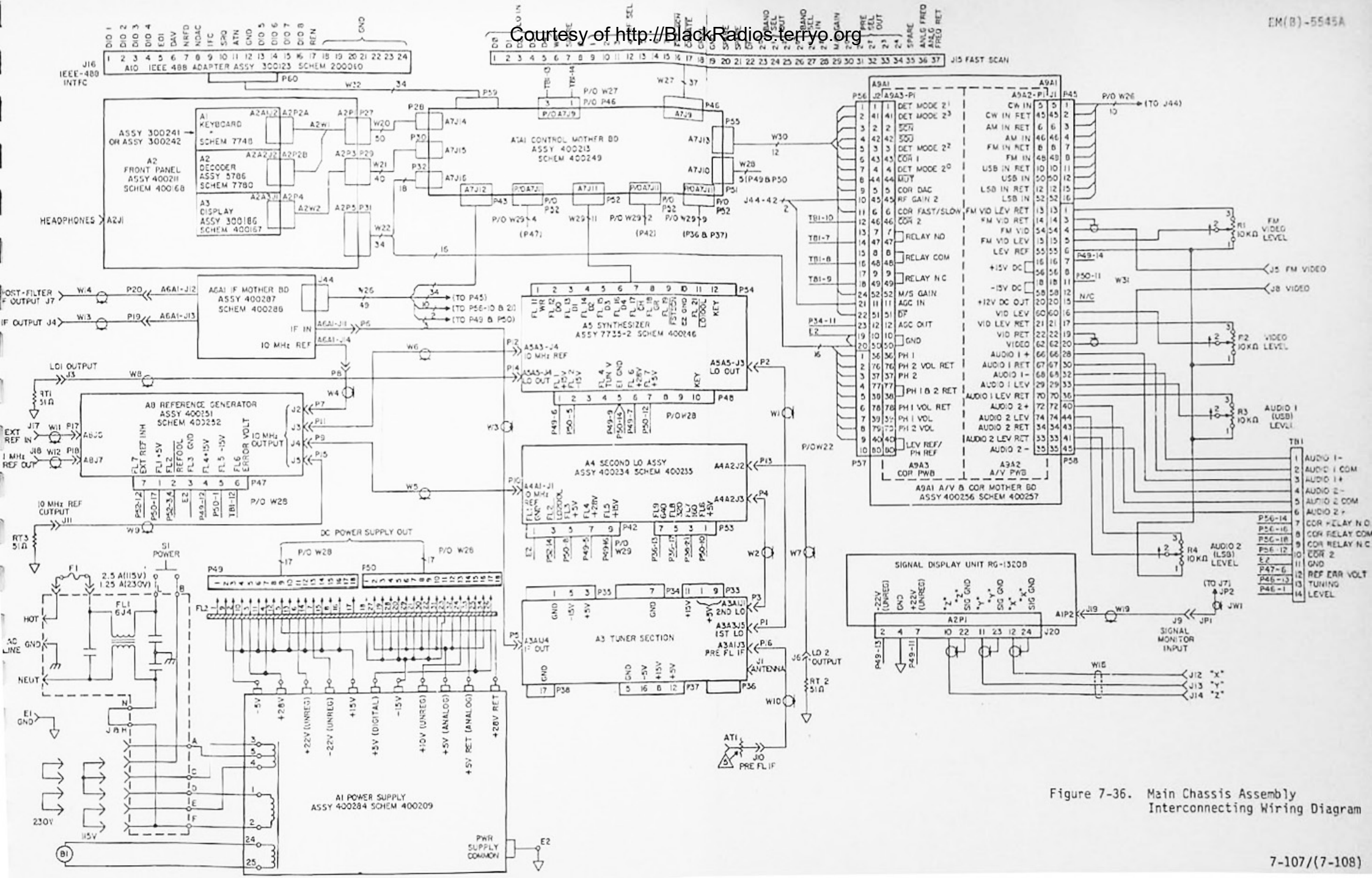


Figure 7-36. Main Chassis Assembly Interconnecting Wiring Diagram

SECTION VIII

DIFFERENCE DATA SHEETS

8-1. INTRODUCTION

8-2. Installation, operation, and maintainance instructions for the type models included in this section are the same as the instructions for the VHF/UHF Receiver, Type RG-5545A, except for the specific differences noted by the applicable difference data sheet. Section I through VII contains information for VHF/UHF Receiver, Type RG-5545A, part number 400205-1.

8-3. INDEX OF DIFFERENCE DATA SHEETS

8-4. Type models covered by difference data sheets are as follows:

DIFFERENCE DATA SHEET

VHF/UHF RECEIVER TYPE RG-5545A(DF)

The instructions contained in the preceding sections of this equipment manual are applicable to this type model except for the differences cited in this difference data sheet.

1. SCOPE OF DIFFERENCE DATA SHEET

2. This section provides information on the differences between the standard spectrum surveillance VHF/UHF Receiver Type RG-5545A, part number 400205-1 and the VHF/UHF Receiver Type RG-5545A(DF), part number 400205-3, hereinafter referred to as the DF version. This difference data, when used with the technical manual for the standard receiver will provide a technical manual for the DF version.

3. INTRODUCTION

4. The DF version of the Receiver is both functionally and physically identical except for four front panel pushbuttons (see Figure 1), the removal of the 100 kHz IF filter amplifier, the function of an AGC attenuation circuit already contained in the standard version and EPROM programming changes.

5. FRONT PANEL PUSHBUTTONS. Four pushbuttons on the DF version front panel are different from the standard version. Figure 1 shows the front panel of the DF version and the location of the four changed pushbuttons. Three of the pushbuttons, blank and unused on the standard version are labeled; MODE, REJ and DF for the DF version. These three pushbuttons provide for communication between the DF receiver and an external (external to the receiver) system computer used in the direction finding (DF) system. The fourth pushbutton, labeled 100 kHz in the standard version, is no longer labeled and is blank and unused in the DF version. This blank unused pushbutton is the result of the DF version not being equipped with a 100 kHz IF filter amplifier (see paragraph 6).

6. 100 kHz IF FILTER AMPLIFIER. The DF version of the receiver does not contain a 100 kHz IF amplifier or the 100 kHz pushbutton to select the filter. This circuit, contained on plug-in module A6A3, type 5742-20 is removed and not present in the DF version. All references, contained in the standard version manual, to this module, its circuits, operation and function should be deleted for the DF version. The absence of this circuit does not affect the operation or function of the DF version in any other way except its inability to select and use the 100 kHz IF filter.

7. AGC 20 dB ATTENUATION. The DF version of the receiver uses a circuit to obtain a zero gain or 20 dB attenuation to the gain of the RF signal through the tuner assembly. This is accomplished through a circuit contained on the COR module (A9A3). This circuit, shown in Figure 7-36 of the standard manual and in Figure 2 for convenience to the user, functions differently in the DF version. In normal operation an AGC signal from the variable gain amplifier circuit card assembly is routed through CMOS select switch U1 and amplifier U3 to the tuner

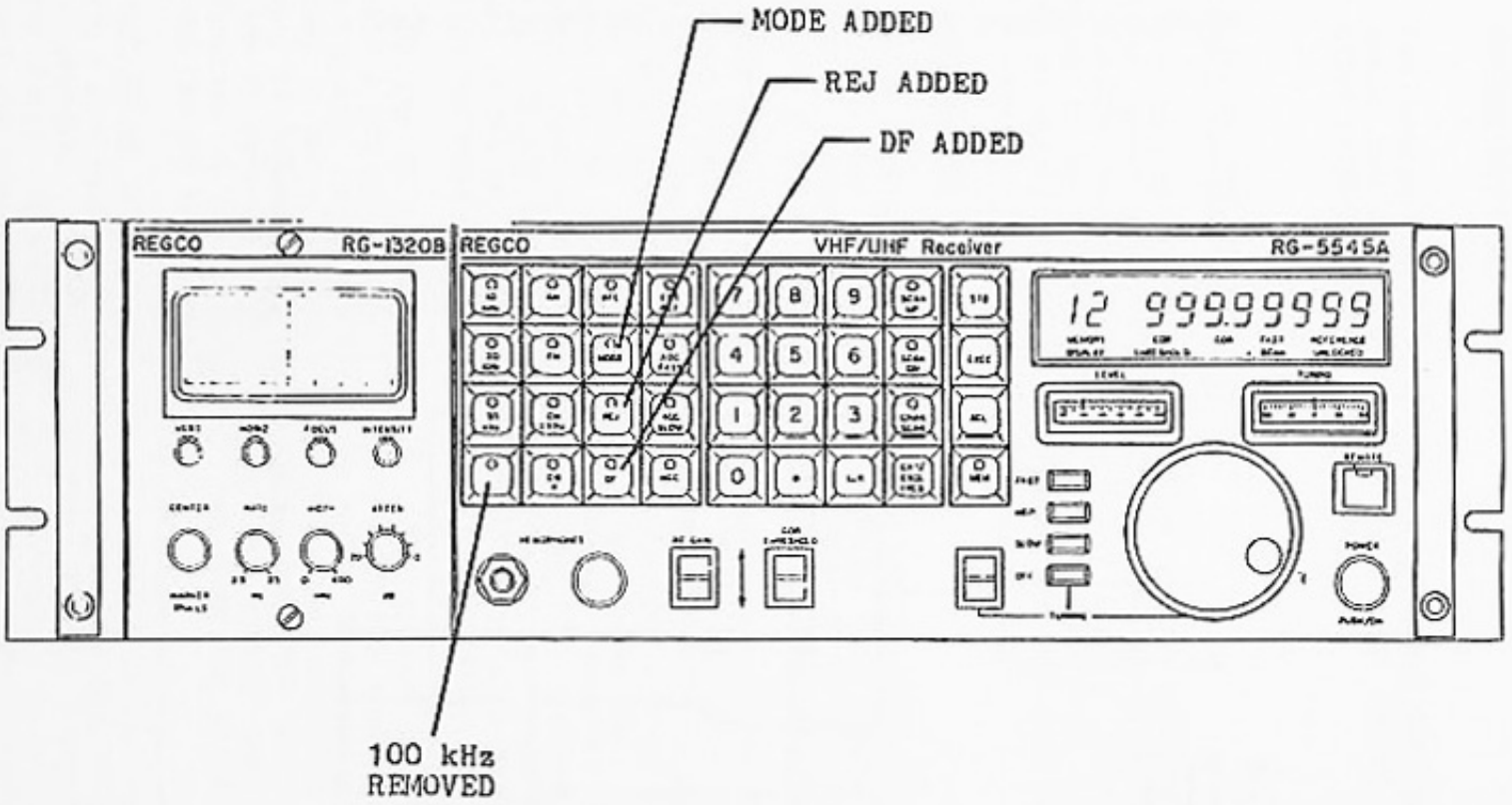


Figure 1. DF Version Front Panel Differences

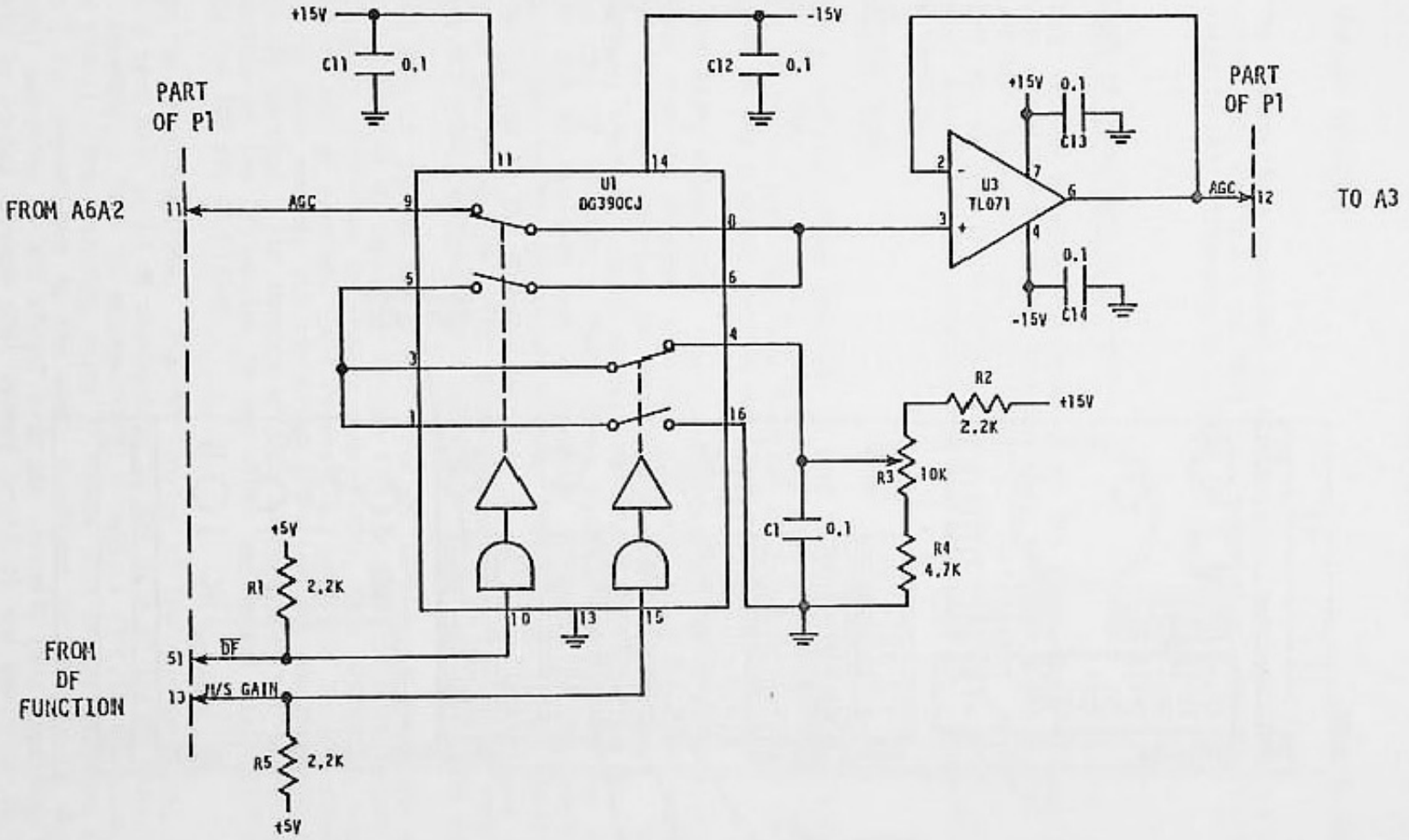


Figure 2. Direction Finding AGC Control, Schematic Diagram

assembly variable attenuator. In the DF version, the DF system computer can control the CMOS switch to select either a 20 dB attenuating signal or a zero attenuating signal. This is accomplished through the DF select and the M/S GAIN select control lines to the CMOS switch. These control lines are controlled by the DF system computer.

8. AGC 20 dB Attenuation Adjustment. Provision is made in the 20 dB attenuation circuit for adjustment. This potentiometer (R3) should be adjusted to provide 20 dB of attenuation to the RF signal through the tuner assembly. To accomplish this adjustment perform the following procedures.

a. Connect the 50 ohm termination and RMS voltmeter to the IF OUT connector J4 on the receiver rear panel as shown in Figure 3.

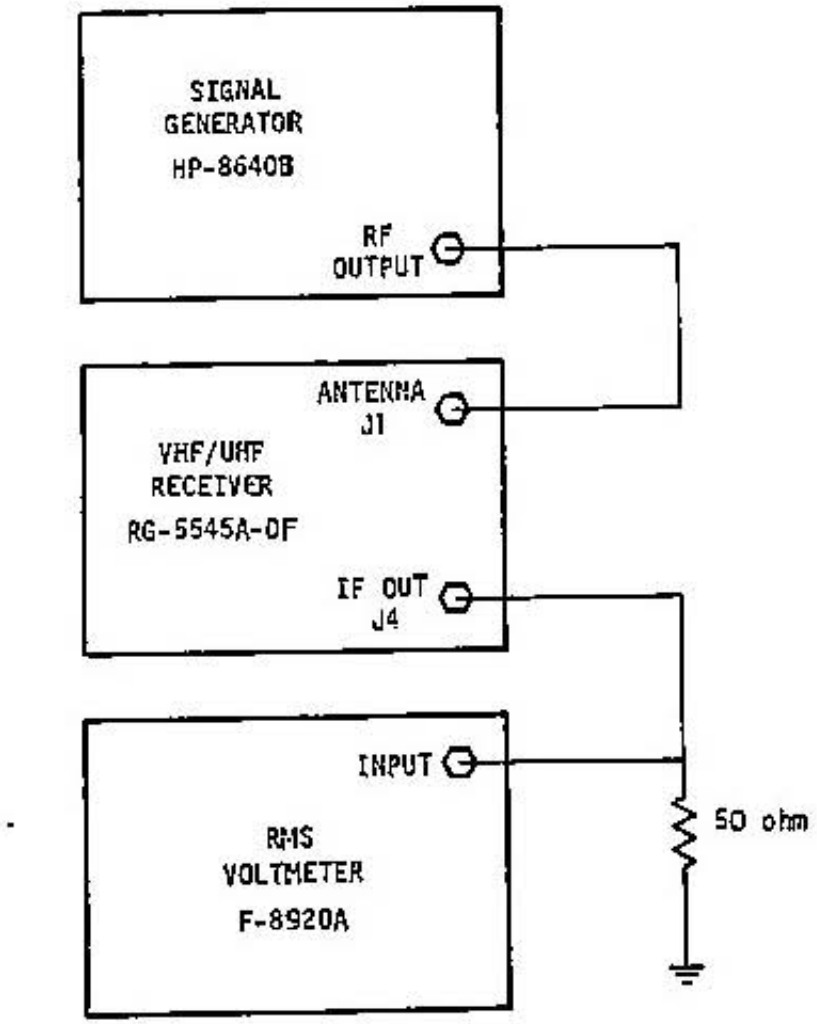


Figure 3. AGC 20 dB Attenuation Adjustment Set-up

b. Connect the signal generator to ANTENNA-J1 on the rear panel as shown in Figure 3.

c. Turn power on to the receiver and to the test equipment.

d. Tune receiver frequency to 450.000 MHz and adjust the signal generator for 450.000 MHz at -50 dBm.

e. Select the M/S GAIN mode (zero gain to the tuner for the DF Receiver).

f. Note the reading on the RMS voltmeter, then press its REL dB key.

g. Disable the M/S GAIN and note the decrease in relative dB on RMS voltmeter.

h. Decrease in relative dB shall be 20 dB. If it is not adjust R3 and repeat steps 5 through 8 until decrease in relative dB is 20 dB.

i. This concludes the 20 dB attenuator adjustment, turn all power off and disconnect the test equipment.

9. PROGRAMMING. The DF version of the receiver has programming changes that are different from the standard version. These programming changes provide for communication between the DF system computer and the DF receiver microcomputer. The MODE, REJ and DF pushbuttons on the DF receiver front panel provides for control signals from the receiver to the system computer. The programming changes are accomplished in the EPROM set, part number 5733-6 which replaces part number 5733-5 in the standard version.

DIFFERENCE DATA SHEET

VHF/UHF RECEIVER TYPE RG-5545A(MOD)

The instructions contained in the preceding sections of this equipment manual are applicable to this type model except for the differences cited in this difference data sheet.

1. SCOPE OF DIFFERENCE DATA SHEET

2. The information presented herein identifies and describes the differences between a standard VHF/UHF Receiver, Type RG-5545A, part number 400205-1, and a VHF/UHF Receiver, Type RG-5545A (MOD), part number 400205-4 (hereinafter referred to as the standard and modified receiver respectively), manufactured by Racal Communications, Inc. (RACOMINC) of Rockville, Maryland. The difference data provided is a direct result of the addition of standard options and various equipment modifications unique to this application for the New Zealand Navy program only.

3. INTRODUCTION

4. This difference data provides technical information for the associated equipment modifications, circuit changes, and receiver deployment of the modified receiver. In addition, parts lists and schematic diagrams for the equipment modifications addressed are appended to the rear of this document. This difference data, when used with the technical manual for the standard receiver, will provide a technical manual for the modified receiver.

5. The following features are provided as options to the standard receiver configuration and are unique to this modified receiver application. These include: a 400 kHz intermediate frequency (IF) bandwidth, independent sideband (ISB) demodulation, a pulse IF blanker, a narrow band 400 kHz spectrum analysis display, and enhanced quieting. It should also be noted that the following additional features, including continous wave/beat frequency oscillator (CW/BFO) and carrier operated relay/automatic frequency control (COR/AFC), unique to this application, are already presented in the standard RG-5545A VHF/UHF receiver equipment manual which forms a part of this document.

6. EQUIPMENT MODIFICATIONS

7. The standard receiver was modified to provide the following: a 400 kHz IF bandwidth (when selected) , centered at 21.4 MHz, supplied to the modified receiver rear panel IF OUT connector J4; ISB demodulation of the lower sideband (LSB) and upper sideband (USB) of frequencies produced by an amplitude-modulated signal; and, a 216 MHz IF pulse blanking circuit. In addition, the modified receiver hardware configuration does not incorporate the IEEE-488C remote control interface circuit card assembly (A7A9) to accomodate remote control operation.

8. To implement the equipment modifications to the standard receiver, the standard 100 kHz IF filter amplifier (A6A3) was replaced with a 400 kHz IF filter amplifier (A6A3), in addition to incorporating low-noise IF filters within the IF filter amplifiers (A6A3-A6A6), part numbers 4600013-1, 4600007-1, 4600006-1 and 4600004-1 respectively, and discriminators; part numbers 4600024-1, 4600023-1, 4600022-1, and 4600021-1 respectively. In addition, an LSB demodulator (A6A9), USB demodulator (A6A7), and IF blanker (A11) circuit card assembly were added; the IEEE-488C remote control interface was removed; and the IF filter amplifiers (A6A4-A6A6) have been replaced in the modified receiver by IF filter amplifiers (A6A4-A6A6), type numbers G5742-17-1, G5742-13-1, and G5742-10-1 respectively.

9. CIRCUIT CHANGES

10. The following paragraphs describe those circuits that were added, replaced, and/or changed to implement the equipment modifications.

11. 400 kHz IF FILTER AMPLIFIER (A6A3). The modified receiver utilizes a 400 kHz IF filter amplifier, type number G5742-26-1, in place of the 100 kHz IF filter amplifier (A6A3), type number 5742-20 used in the standard receiver. In addition, the corresponding 100 kHz pushbutton key-switch used in the standard receiver has been replaced with a 400 kHz pushbutton key-switch. It should also be noted that all references contained in the standard RG-5545A VHF/UHF receiver equipment manual to the 100 kHz IF filter amplifier and associated pushbutton key-switch should be superseded by the 400 kHz IF filter amplifier and associated pushbutton key-switch. Refer to Figure B-2 for circuit details and Table B-1 for component listing in Appendix B, as appropriate.

12. USB DEMODULATOR CIRCUIT CARD ASSEMBLY (A6A7). The USB demodulator circuit card assembly used in the modified receiver provides a demodulated upper sideband audio output, which is applied for further processing to the audio video amplifier/COR assembly (A9). The USB demodulator consists of three single-stage amplifiers, a 2 MHz high pass filter, a demodulator/mixer, and a two-stage output amplifier. Refer to Figure C-2 for circuit details and Table C-1 for replaceable component listing in Appendix C, as appropriate.

13. LSB DEMODULATOR CIRCUIT CARD ASSEMBLY (A6A9). The LSB demodulator circuit card assembly used in the modified receiver provides a demodulated lower sideband audio output, which is applied for further processing to the audio video amplifier/COR assembly (A9). The LSB demodulator consists of three single-stage amplifiers, a 2 MHz low pass filter, a demodulator/mixer, and a two-stage output amplifier. Refer to Figure D-2 for circuit details and Table D-2 for replaceable component listing, in Appendix D, as appropriate.

14. IF BLANKER CIRCUIT CARD ASSEMBLY (A11). The IF blanker circuit card assembly is used to prevent IF AGC from being "captured" by a radar pulse signal intercepted by the modified receiver. With the presence of a high power, radar transmitted pulse in the receiving vicinity of the modified receiver, it is necessary to protect the RF input circuitry from damage due to excessive RF input power, and to prevent the presence of extraneous receiver output data information caused by the radar pulse, since information about the radar output is of no further value to the modified receiver. For the intended design function of the modified receiver, it is therefore not necessary to obtain information from a radar pulse that has been transmitted as source data. The

operating frequency of the radar signals mainly to be protected against is 216 MHz, therefore frequency band 6 (144.6 MHz-220.6 MHz) and frequency band 7 (220.6 MHz-335.6 MHz) are affected. It should be noted that for the operating frequency of 216 MHz, the modified receiver functions are blanked, made inoperative, during the transmitting pulsing time of the radar unit. If the radar pulse were allowed to penetrate the threshold of the IF AGC, due to the long decay time of that circuit, the IF AGC would not be sensitive to other input signals, therefore at any time the radar signals would be allowed to initiate the IF AGC, the AGC circuit would not be free to operate on other incoming signals. This process is accomplished by reducing the saturated output of the VHF tuner (A3A1), limited in the clamping input circuit or IF blanker to +18 dBm, by 110 dB. The net blanked output of the IF blanker is -92 dBm which is below the AGC threshold of the IF AGC.

15. The IF blanker has been designed for physical and electrical insertion between the wideband IF output, 21.4 MHz, from IF OUT connector J4 of the VHF tuner (A3A1), and the wideband IF input, 21.4 MHz, to connector J11, of the IF control interface (A6A1), via interconnecting cabling W41 and W42 respectively. It should also be noted that concurrent with, but approximately five microseconds in advance of a radar pulse, an IF blanking pulse, is generated by the transmitting radar unit. The blanking pulse is +16 volts, nominal, 3 microseconds $\pm$ 1 microsecond pulse width, with rise and fall times of approximately 150 nanoseconds. The repetition rate of the blanking pulse is 1520 $\pm$ 20% pulses per second, randomly varied by a pulse generator. The leading edge of this blanking pulse is used to control the blanking function. A 75 ohm, coaxial IF BLANK input (BNC) connector, mounted on the modified receiver rear panel, is used to receive this signal.

16. The IF blanker consists of a blanking trigger termination circuit, a voltage comparator, a multivibrator, an output operational amplifier, a buffer amplifier, a blanking time select switch, and a 21.4 MHz IF pass circuit. Refer to Figure E-2 for circuit details and Table E-1 for replaceable component listing, in Appendix E, as appropriate.

17. NARROWBAND 400 kHz SPECTRUM ANALYSIS DISPLAY. The narrowband 400 kHz spectrum analysis display, Spectrum Display Unit, Type RG-13208, is a plug-in option to the standard receiver, and is used in this modified receiver application. Refer to the Spectrum Display Unit, Type RG-13208 equipment manual provided under separate cover, which forms a part of this document, for technical support of the narrowband 400 kHz spectrum analysis display.

18. RECEIVER DEPLOYMENT

19. The following paragraphs address the installation, operation, theory of operation, and maintenance of the modified receiver.

20. INSTALLATION. The physical installation of the modified and standard receiver is identical with the following exceptions. The modified receiver is equipped to provide ancillary equipment interconnection at the modified receiver rear panel for a blanking pulse to control the IF blanker (A11). This is accomplished through implementing the proper interconnection at the IF BLANK input connector. In addition, interconnection to the IEEE-488 INTERFACE connector J16 is not required for this application. The following paragraph provides a general description of this connector.

21. IF BLANK Connector. The IF BLANK connector provides a BNC connection for access to the leading edge of a blanking pulse when utilizing the IF blanking control function. This connector will mate with any standard male type BNC connector.

22. OPERATION. Operation of the modified receiver is identical to that of the standard receiver, except that a 400 kHz IF bandwidth is now selectable at the modified receiver front panel, and remote control operation utilizing the IEEE-488C remote control interface circuit card assembly (A7A9) is not used in this application. In addition, an ISB, USB, and LSB pushbutton key-switch has been added. Refer to Section III of the standard RG-5545A VHF/UHF receiver equipment manual for ISB/USB and ISB/USB operating instructions.

23. THEORY OF OPERATION. The theory of operation for each of the standard module assemblies/circuit card assemblies of the modified and standard receivers is identical except where previously identified and discribed as a result of the circuit changes. These descriptions may be referenced in the standard RG-5545A VHF/UHF receiver technical manual, which forms a part of this document, for support of the modified receiver. However, the module asemblies/circuit card assemblies unique to this modified configuration are included herein. The following paragraphs provide a functional description of circuit operation for the USB demodulator (A6A7), the LSB demodulator (A6A9), and the IF blanker (A11) circuit card assemblies, unique to this application, which are keyed to block diagrams at the major circuit level. (Refer to applicable schematic diagrams in Appendices C, D, and E as appropriate.)

24. USB Demodulator Circuit Card Assembly (A6A7). As shown in Figure 1, the USB demodulator circuit comprises six functional circuits which include; three single stage amplifiers, a filter, a demodulator/mixer, and a two-stage amplifier. The 2 MHz IF (A6A8) is connected to amplifier stage Q1 which provides approximately 20 dB of gain. The amplifier's output signal is routed to filter FL1 which eliminates signals below 2 MHz. The filtered output, through amplifier stage Q2 provides approximately 10 dB of gain to drive one input to the demodulator/mixer U1. The second input to this mixer is the 2 MHz reference from the CW demodulator (A6A8) and is applied through amplifier stage Q3 which provides 3 dB of gain. The mixer output signal, containing the demodulated upper sideband, drives operational amplifier stages U2A and U2B which provide the USB audio output. The output is then routed to the audio video amplifier/COR assembly (A9) for further processing. Potentiometer R26 adjusts the gain of mixer U1.

25. LSB Demodulator Circuit Card Assembly (A6A9). As shown in Figure 1, the LSB demodulator is identical to the USB demodulator except that filter FL1 in the LSB demodulator eliminates the upper sideband (frequency above 2 MHz, so that its output is the LSB audio signal. This signal output is also routed to the audio video amplifier/COR assembly (A9) for further processing. Potentiometer R26 adjusts the gain of mixer U1.

26. IF Blanker Circuit Card Assembly (A11). As shown in Figure 2, the IF blanker circuit consists of seven circuits which include; a blanking trigger termination circuit, a voltage comparator, a multivibrator, an output operational amplifier, a buffer amplifier/current booster, a blanking time select switch, and a 21.4 MHz IF pass circuit. The blanking trigger input is applied to J1, where switch SW1, when physically activated, provides the

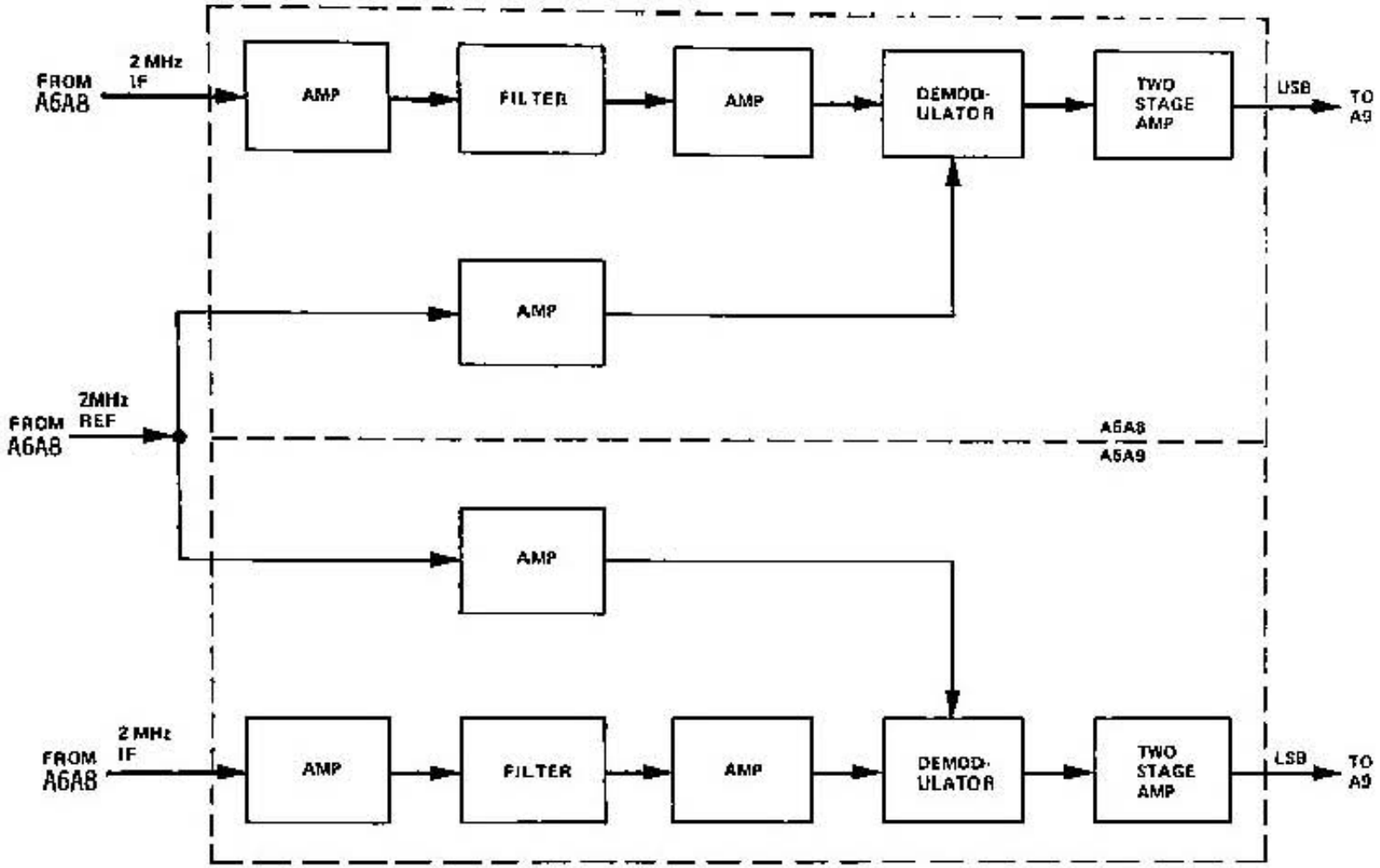


Figure 1. USB and LSB Demodulators (A6A7 and A6A9) Functional Block Diagram

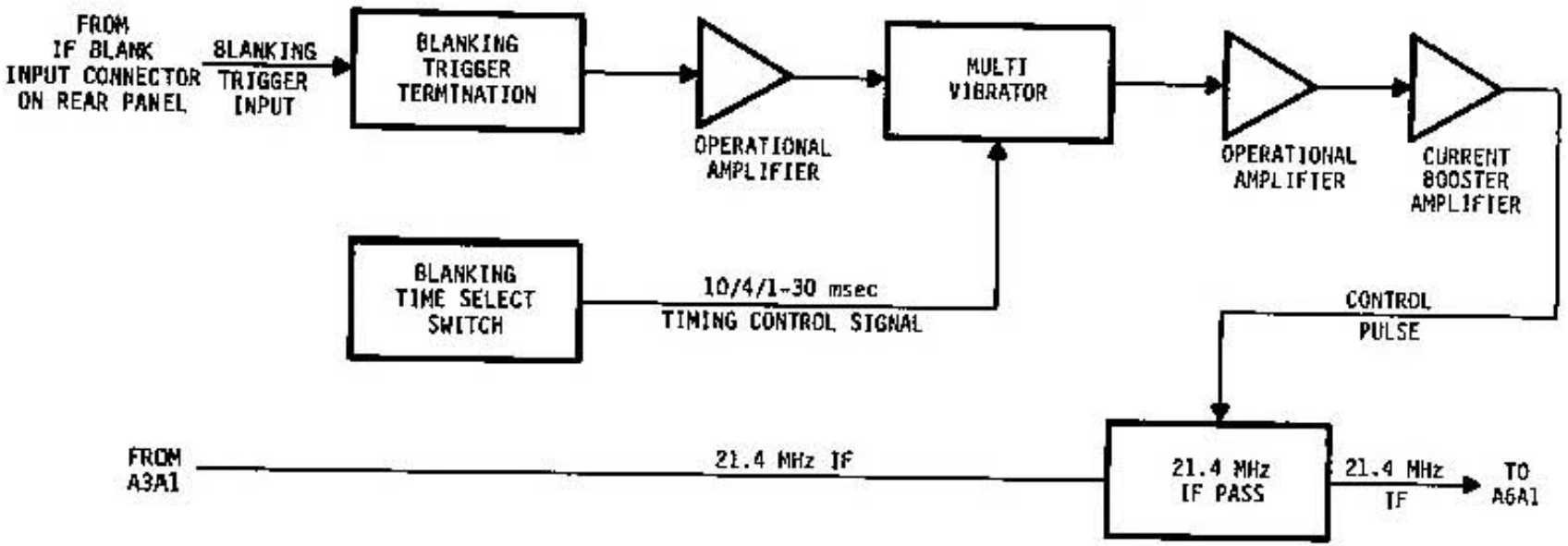


Figure 2. IF Blanker (A11) Functional Block Diagram

required 75 ohm impedance termination for the 75 ohm incoming coaxial line. In the open position, that switch provides an impedance termination of 2 K ohms. The 2 K termination would be used for applications that would require the IF blanking function to respond to limited (reduced) blanking input levels where the termination is not critical. The blanking trigger input is fed through an operational amplifier, U1, into a low impedance multivibrator, U2. For expanded application purposes, the blanking control output of that multibrator is controlled by a BLANKING TIME SELECT switch, SW2, which must be manually set by removing the top cover of the modified receiver, making the adjustment, and then, replacing the top cover. The switch offers blanking times of 4 microseconds; 10 microseconds; and, by adjusting potentiometer R21, a variable time between one and 30 microseconds. The output of the multivibrator is fed into another operational amplifier, U3, and then to current booster, U4. Feedback from the current booster is returned to control the operational amplifier, U3, via R11. The output of the current booster, U4. Feedback from the current booster is returned to control the operational amplifier, U3, via R11. The output of the current booster provides the switching control pulse required to interrupt the 21.4 MHz IF signal flow from the VHF tuner (A3A1) to the IF control interface (A6A1). That output is present for verification and testing at test point TP1 on the IF blanker. The operational amplifier, U3, is inverting, with loop gain approximated by the formula:

$$\frac{R11 + R10}{R10} = 5.7$$

When the multivibrator, U2, is in the OFF state, the output level at TP1 is -10 volts dc. Whenever the blanking trigger input is present at J1, the multivibrator, U2, is placed into the ON state, in turn causing the voltage level of TP1 to become +10 volts dc. This 20 volt swing, and loop gain of U3 of 5.7, shows that the input voltage of U3 is approximately 3.5 volts dc. That output is fed through both R22 and R23. In the +10 volt state, this control pulse conducts diodes CR4 and CR5, allowing the flow of the 21.4 IF frequency to pass to the IF control interface (A6A1). In the -10 volt state, diodes CR4 and CR5 are reverse-biased, diodes CR3 and CR10 are conducting, and the 21.4 MHz IF signal is gated off.

27. MAINTENANCE. Maintenance of the modified receiver is the same as for the standard receiver with the following exceptions. Refer to Section V of the standard RG-5545A VHF/UHF receiver equipment manual in conjunction with the performance tests, adjustments, and troubleshooting presented hereunder.

28. Audio Output Test - This test checks the audio outputs available at the rear panel terminal block (TB1) and the front panel HEADPHONES jack.

1. Connect test equipment as shown in Figure 3 with oscilloscope connected to HEADPHONES jack (tip to channel 1 and ring to channel 2), and signal generator no. 1 connected directly to ANTENNA connector J1 on Receiver rear panel.

2. Depress Receiver POWER PUSH/ON switch to on, then press AM, 10 KHz, and AGC FAST pushbutton key-switches.

3. Adjust both inner and outer HEADPHONES (LSB/USB) audio level gain controls fully counter-clockwise.

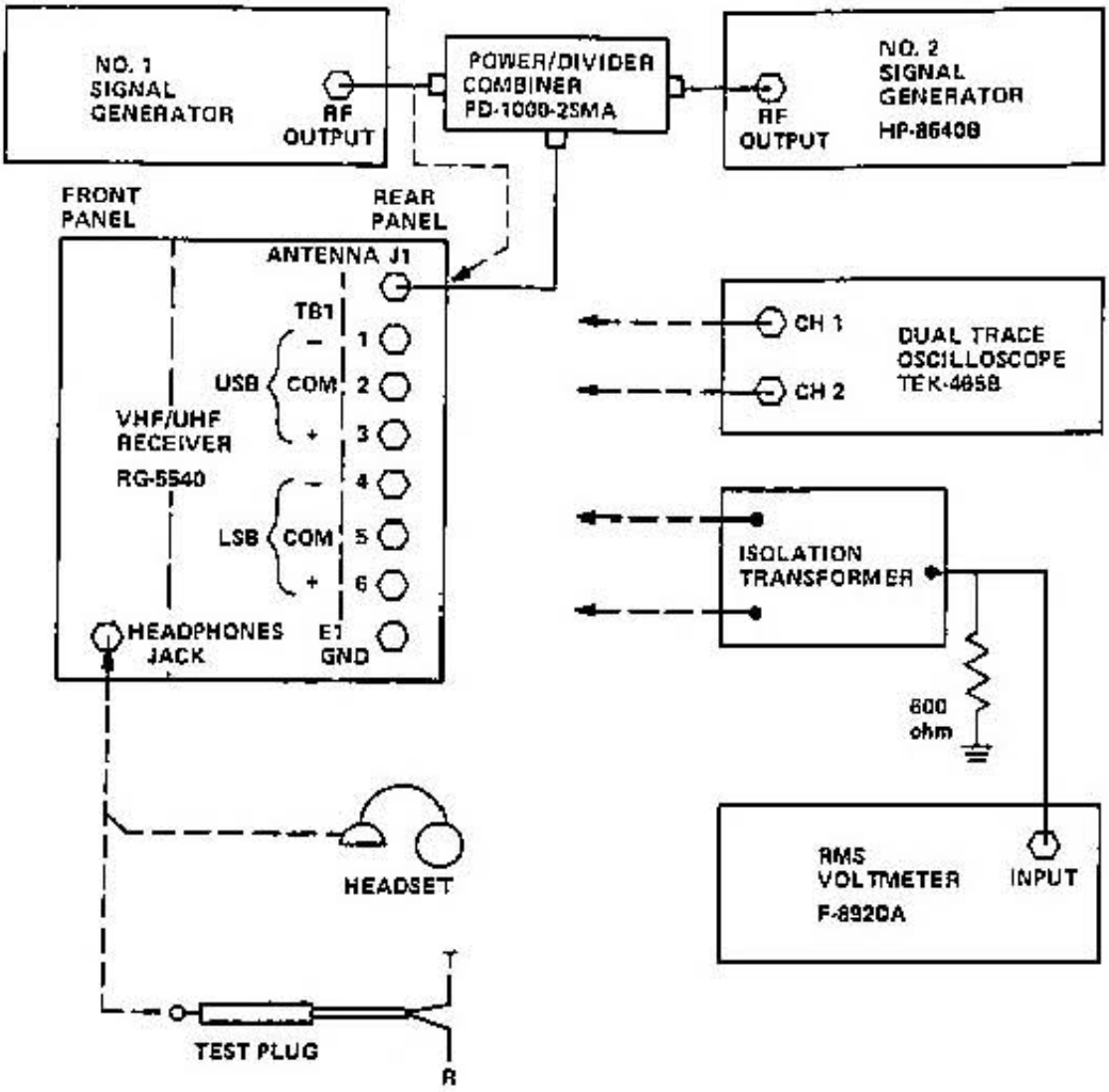


Figure 3. Audio Output Test

4. Press numeric pushbutton keys 2, 0, 4,. (decimal point), 0, 6, 0, 8 and 8, then press ENTER/EXCL FREQ pushbutton key-switch.

5. Adjust signal generator output to 204.061 MHz, -60 dBm with 1 kHz AM modulation at 30 percent.

6. Adjust inner HEADPHONES (USB) audio level gain control clockwise while observing channel 1 oscilloscope trace.

7. Observe that 1 kHz signal on channel 1 changes amplitude as outer (USB) audio level gain control is rotated.

8. Adjust outer HEADPHONES (LSB) audio level gain control while observing channel 2 oscilloscope trace.

9. Observe that 1 kHz signal on channel 2 changes amplitude as outer (LSB) audio level gain control is adjusted.

10. Adjust signal generator output to 60.000 MHz, -60 dBm, with 1 kHz FM modulation and 3 kHz deviation.

11. On Receiver front panel, press FM pushbutton key-switch and numeric pushbutton key-switches 6, 0,. (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

12. Observe that 1 kHz signal is displayed on both channels of oscilloscope.

13. Remove modulation from signal generator.

14. Press CW 1 KHz pushbutton key-switch and observe that 1 kHz is displayed on both channels of oscilloscope.

15. Press CW 0 pushbutton key-switch and observe that 1 kHz signal disappears from both channels of oscilloscope.

16. Press TUNING rate SLOW pushbutton key-switch, then adjust TUNING control knob clockwise until frequency display on Receiver indicates 60.00100 MHz.

17. Observe that 1 kHz signal again is displayed on both channels of oscilloscope.

18. Refer to Figure 3 and connect two signal generators through power combiner to ANTENNA connector J1 on Receiver rear panel, then tune Receiver to 60.00000 MHz.

19. Adjust signal generator no. 1 to 60.00200 MHz at -60 dBm.

20. Adjust signal generator no. 2 to 59.99900 MHz at -60 dBm.

21. Press AGC SLOW pushbutton key-switch, then LSB.

22. Observe that 1 kHz signal is displayed on both channels of oscilloscope.

23. Press USB pushbutton key-switch and observe that 2 kHz signal is displayed on oscilloscope.

24. Press ISB pushbutton key-switch and observe that 2 kHz signal is displayed on channel 1 and 1 kHz signal is displayed on channel 2.

25. Adjust USB (inner) audio level gain control and observe that amplitude of channel 1 changes but channel 2 does not.

26. Adjust LSB (outer) audio level gain control and observe that amplitude of channel 2 changes but channel 1 does not.

27. Disconnect oscilloscope and connect a signal generator to ANTENNA connector J1 on Receiver rear panel, then connect RMS voltmeter between terminals 1 and 3 of terminal block (TB1) through isolation transformer as shown in Figure 3.

28. Press CW 1 KHz, 10 KHz and AGC SLOW pushbutton key-switches.

29. Press numeric pushbutton key-switches 2, 5,. (decimal point), 0, 0 and 0, then press ENT/EXCL FREQ pushbutton key-switch.

30. Adjust signal generator output for 25.000 MHz, -97 dBm and modulation off.

31. Set RMS voltmeter for 600 ohm dBm reference.

32. On Receiver rear panel, adjust AUDIO 1 control R3 fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

33. On Receiver rear panel, adjust AUDIO 1 control R3 clockwise until RMS voltmeter indicates +5 dBm.

34. Disconnect RMS voltmeter from between terminals 1 and 3, of terminal block (TB1), then reconnect between terminals 4 and 6.

35. On Receiver rear panel, adjust AUDIO 2 control R4 fully counter-clockwise and observe that RMS voltmeter indicates less than -45 dBm.

36. On Receiver rear panel, adjust AUDIO 2 control R4 clockwise until RMS voltmeter indicates +5 dBm.

37. Disconnect RMS voltmeter from between terminals 4 and 6 and reconnect to HEADPHONES jack tip without isolation transformer.

38. Adjust USB audio level (inner) gain control to full clockwise position and observe that RMS voltmeter indicates at least +20 dBm, then reset gain control fully counter-clockwise.

39. Reconnect RMS voltmeter to HEADPHONES jack ring without the isolation transformer.

40. Adjust LSB audio level (outer) gain control to full clockwise position and observe that RMS voltmeter indicates at least +20 dBm, then reset gain control fully counter-clockwise.

NOTE

This concludes the audio output test, disconnect all test equipment and depress Receiver POWER PUSH/ON switch to off. The AUDIO 1 control R3 and AUDIO 2 control R4 may require re-adjustment when unit is installed in system.

29. LSB Demodulator (A6A9) Adjustments - The LSB demodulator must be extended from the Receiver to perform these adjustment procedures.

1. Set Receiver frequency to 30.000 MHz, mode to LSB, AGC to FAST and IF bandwidth to 20 kHz.

2. Connect signal generator to ANTENNA connector J1 on Receiver rear panel.

3. Adjust signal generator for 29.9990 MHz at -50 dBm output level.

4. Using oscilloscope, monitor pin 37 of plug P1 for 2.000 MHz TTL waveform and pin 7 for 2.001 MHz at 200 millivolts peak to peak.

5. Connect oscilloscope to pin 26 of plug P1 and adjust potentiometer R26 for a 1.75 volt peak-to-peak sine wave, then verify that frequency is 1 kHz.

6. Connect RMS voltmeter to LSB (ring) on HEADPHONES jack.

7. Set signal generator to 30.0 MHz at -50 dBm.

8. Set Receiver frequency to 29.99900 MHz.

9. Adjust LSB (outer) HEADPHONES audio level gain control for +10 dBm reading on RMS voltmeter with 600 ohm reference.

10. Press dBm/REL pushbutton on RMS voltmeter and observe that meter indicates 0.00 dB relative.

11. Slowly tune Receiver between 29.99980 and 299660 MHz while observing RMS voltmeter indication.

12. Set Receiver frequency where peak indication occurs, then reset dBm/REL pushbutton to set peak for new reference.

13. Slowly tune Receiver between 29.99980 and 29.99660 MHz and assure that dB level is not more than 3 less down (from peak in step 12) over the tuned range.

NOTE

This concludes the LSB demodulator adjustments, disconnect all test equipment and install LSB demodulator card in Receiver.

30. USB Demodulator (A6A7) Adjustments - The USB Demodulator must be extended from the Receiver to perform these adjustment procedures.

1. Set Receiver frequency to 30.000 MHz, mode to USB, AGC to FAST, and IF bandwidth to 20 kHz.

2. Connect signal generator to ANTENNA connector J1 on Receiver rear panel.

3. Adjust signal generator for 30.0010 MHz at -50 dBm output level.

4. Using oscilloscope, monitor pin 37 of plug P1 for 2.000 MHz TTL waveform and pin 9 for 1.999 MHz at 200 millivolts peak-to-peak.

5. Connect oscilloscope to pin 22 and adjust potentiometer R26 for a 1.75 volt peak-to-peak sine wave, then verify that frequency is 1 kHz.

6. Connect RMS voltmeter to USB (tip) on HEADPHONES jack.

7. Set signal generator to 30.0 MHz at -50 dBm.

8. Set Receiver frequency to 30.00100 MHz.

9. Adjust USB (inner) HEADPHONES audio level gain control for +10 dBm reading on RMS voltmeter with 600 ohm reference.

10. Press dBm/REL pushbutton on RMS voltmeter and observe that meter indicates 0.00 dB relative.

11. Slowly tune Receiver between 30.00020 and 30.00340 MHz while observing RMS voltmeter indication.

12. Set Receiver frequency where peak indication occurs, then reset the dBm/REL pushbutton to set peak for new reference.

13. Slowly tune Receiver between 30.00020 and 30.00340 MHz and assure that dB level is not more than 3 dB less (from peak in step 12) over tuned range.

NOTE

This concludes the USB demodulator adjustments, disconnect all test equipment and install the USB demodulator in the Receiver.

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
1	No VIDEO output (from J8 of rear panel) when Receiver tuned to input signal.	1. USB demodulator (A6A7).	1. Check for VIDEO output at connector J8 rear panel with Receiver in CW mode and tuned to a CW input signal. If there is no output go to Item 3 of this table. If there is an output, replace USB demodulator (A6A7).
2	No VIDEO output (from J8 at rear panel) when Receiver is in LSB mode and tuned to frequency of input signal.	1. LSB demodulator (A6A9).	1. Check for VIDEO output at connector J8 on rear panel with Receiver in CW mode and tuned to a CW input signal. If there is no output, go to Item 3 of this table. If there is an output, replace LSB demodulator (A6A9).
3	No VIDEO output (from J8 at rear panel) when Receiver is in CW mode and tuned to frequency of input signal.	1. No IF output.	1. Measure IF output at connector J4 at rear panel (use RMS voltmeter, Item 9 of Table 5-2). This should be approximately -10 dBm. If no or improper signal is obtained, go to Item 2 of Table 5-3 in Section V of standard manual. If there is a proper signal go to next step.
		2. Cabling between power supply assembly (A1), audio video amplifier/COR assembly (A9) and IF assembly (A6).	2. Check connections and continuity of cabling between units (see Figure 7-31) listed under Possible Cause column.
		3. CW demodulator (A6A8).	3. If steps 1 and 2 do not clear fault, replace CW demodulator (A6A8).

Troubleshooting (Cont.)

ITEM	SYMPTOM	POSSIBLE CAUSE	REMEDY
		4. Audio video amplifier/COR assembly (A9).	4. If step 3 does not clear fault, check connections between audio video control interface (A9A1) and audio video amplifier (A9A2). If defective, replace audio video control interface (A9A1). If not defective, replace audio video amplifier (A9A2).
		5. Preselector controller (A7A7).	5. If step 4 above does not clear fault, check connections to preselector controller (A7A7) at receiver control interface (A7A1). If defective, return Receiver to manufacturer for receiver control interface repair and/or replacement. If not defective replace preselector controller (A7A7).

APPENDIX A

MAIN CHASSIS ASSEMBLY

Type Number: 400205-4

Interconnecting Wiring Diagram: Figure A-1

Table A-1. Main Chassis Assembly, Type 400205-4
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
A-1		Main Chassis Assembly	54805	400205-4	1	
	A1	. Power Supply Module	54805	400284	1	
		. . Assembly				
	A1A1	. . Power Rectifier Circuit	54805	400303	1	
		. . . Card Assembly				
	A2	. Front Panel Assembly	54805	400211-3	1	
	A2A1	. . Keyboard Assembly	54805	300242	1	
	A2A2	. . Keyboard Decoder Circuit	54805	5786	1	
		. . . Card Assembly				
	A2A3	. . Display Circuit Card	54805	300186	1	
		. . . Assembly				
		. Rear Panel Assembly*	54805	400205-4	1	
	A3	. Tuner Assembly	54805		1	
	A3A1	. . VHF Tuner Module Assembly	54805	400323	1	
	A3A2	. . VHF (20-500 MHz) Prese-	54805	400305	1	
		. . . lector Module Assembly				
	A3A3	. . UHF Tuner Module Assembly	54805	400227	1	
	A3A4	. . UHF Preselector Module	54805	400306	1	
		. . . Assembly				
	A3A5	. . RF Input Limiter	54805	200127	1	
	A4	. Second LO Synthesizer	54805	400234	1	
	A4A1	. . 640 MHz Oscillator	54805	300195	1	
	A4A2	. . Divider Circuit Card	54805	300196	1	
		. . . Assembly				
	A4A3	. . Phase-Locked-Loop Circuit	54805	300197	1	
		. . . Assembly				
	A5	. First LO Synthesizer	54805	400245	1	
	A5A1	. . VCO "A" Module Assembly	54805	5751-2	1	
	A5A2	. . Controller Circuit Card	54805	300122	1	
		. . . Assembly				
	A5A3	. . Digiphase Processor	54805	5753	1	
		. . . Circuit Card Assembly				

Table A-1. Main Chassis Assembly, Type 400205-4
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	A5A4	. . Programmable Divider . . . Circuit Card Assembly	54805	7796	1	
	A5A5	. . VCO "B" Module Assembly	54805	5837-2	1	
	A6	. IF Assembly	54805			
	A6A1	. . IF Control Interface . . . Circuit Card Assembly	54805	400287	1	
	A6A2	. . Variable Gain Amplifier . . . Circuit Card Assembly	54805	5741	1	
	A6A3	. . 400 kHz IF Filter . . . Amplifier Assembly	23386	G5742-26-1	1	
	A6A4	. . 50 kHz IF Filter . . . Amplifier Assembly	23386	G5742-17-1	1	
	A6A5	. . 20 kHz IF Filter . . . Amplifier Assembly	23386	G5742-13-1	1	
	A6A6	. . 10 kHz IF Filter . . . Amplifier Assembly	23386	G5742-10-1	1	
	A6A7	. . USB Demodulator Circuit . . . Card Assembly	54805	5748	1	
	A6A8	. . CW Demodulator Circuit . . . Card Assembly	54805	5746	1	
	A6A9	. . LSB Demodulator Circuit . . . Card Assembly	54805	5749	1	
	A7	. Receiver Control Assembly	54805			
	A7A1	. . Receiver Control Inter- . . . face Circuit Card . . . Assembly	54805	400213	1	
	A7A2	. . Microcomputer Circuit . . . Card Assembly	23386	4100078	1	
	A7A3	. . Not Used				
	A7A4	. . Front Panel I/O Inter- . . . face Circuit Card . . . Assembly	54805	300207	1	

Table A-1. Main Chassis Assembly, Type 400205-4
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	A7A5	. . Display Driver Circuit . . . Card Assembly	54805	5736	1	
	A7A6	. . Address Decoder Circuit . . . Card Assembly	23386	4100081	1	
	A7A7	. . Preselector Controller . . . Circuit Card Assembly	54805	300208	1	
	A7A8	. . Converter Circuit Card . . . Assembly	54805	300118	1	
	A7A9	. . Not Used				
	A8	. Reference Generator Module . . Assembly	54805	400251	1	
	A8A1	. . Reference Oscillator . . . Module Assembly, 10 MHz	54805	A9812-1	1	
	A8A2	. . Divider Circuit Card . . . Assembly	54805	300198	1	
	A8A3	. . 10 MHz Buffer Circuit . . . Card Assembly	54805	300199	1	
	A9	. Audio/Video Assembly	54805			
	A9A1	. . Audio Video Control . . . Interface Circuit . . . Card Assembly	54805	400256	1	
	A9A2	. . Audio Video Amplifier . . . Circuit Card Assembly	54805	5719	1	
	A9A3	. . COR Circuit Card Assembly	54805	400302	1	
	A10	. Not Used				
	A11	. IF Blanker Circuit Card . . Assembly	23386	4100096-501	1	
	AT1	. 6.0 dB Pad, BNC, . . Male to BNC Female	SOLI-TRON	9470001	1	
		. Screen, Fan Blower	54805	300173	1	
	E1	. Not Used				
	E2-3	. Terminal, Ground	71279	160-2381-01-05-00	2	

Table A-1. Main Chassis Assembly, Type 400205-4
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	FL1-34	. Filter, EMI, Feedthrough	00779	859619-1	34	
	RT1-3	. Terminal, BNC	54805	35650-51	3	
	W1	. Cable Assembly, RF Coax	54805	300250-1	1	
	W1-J	. Cable Assembly, RF Coax	54805	300259	1	
	W2	. Cable Assembly, RF Coax	54805	300250-2	1	
	W3	. Cable Assembly, RF Coax	54805	300251	1	
	W4	. Cable Assembly, RF Coax	54805	300252	1	
	W5	. Cable Assembly, RF Coax	54805	300253-1	1	
	W6	. Cable Assembly, RF Coax	54805	300253-2	1	
	W7	. Cable Assembly, RF Coax	54805	300255-1	1	
	W8	. Cable Assembly, RF Coax	54805	300255-2	1	
	W9	. Cable Assembly, RF Coax	54805	300254-1	1	
	W10	. Cable Assembly, RF Coax	54805	300255-3	1	
	W11	. Cable Assembly, RF Coax	54805	300254-2	1	
	W12	. Cable Assembly, RF Coax	54805	300254-3	1	
	W13	. Cable Assembly, RF Coax	54805	300256-1	1	
	W14	. Cable Assembly, RF Coax	54805	300256-2	1	
	W15-17, 24, 25	. Not Used				
	W18	. Cable Assembly, RF Coax	54805	300257	1	
	W19	. Cable Assembly, RF Coax	54805	300258	1	
	W20	. Cable Assembly, Ribbon	54805	300228	1	
	W21	. Cable Assembly, Ribbon	54805	300229	1	
	W22	. Cable Assembly, Ribbon	54805	300230	1	
	W23	. Wiring Harness Assembly	54805	300262	1	
	W26	. Cable Assembly, Ribbon	54805	300260	1	
	W27	. Cable Assembly, Ribbon	54805	300231	1	
	W28	. Wiring Harness Assembly	54805	300263	1	
	W29	. Wiring Harness Assembly	54805	300264	1	
	W30	. Cable Assembly, Ribbon	54805	300261	1	
	W31	. Wiring Harness Assembly	54805	300265	1	
	W32	. Not Used				

*NOTE: Part of Main Chassis Assembly; subordinated for convenience of parts listing.

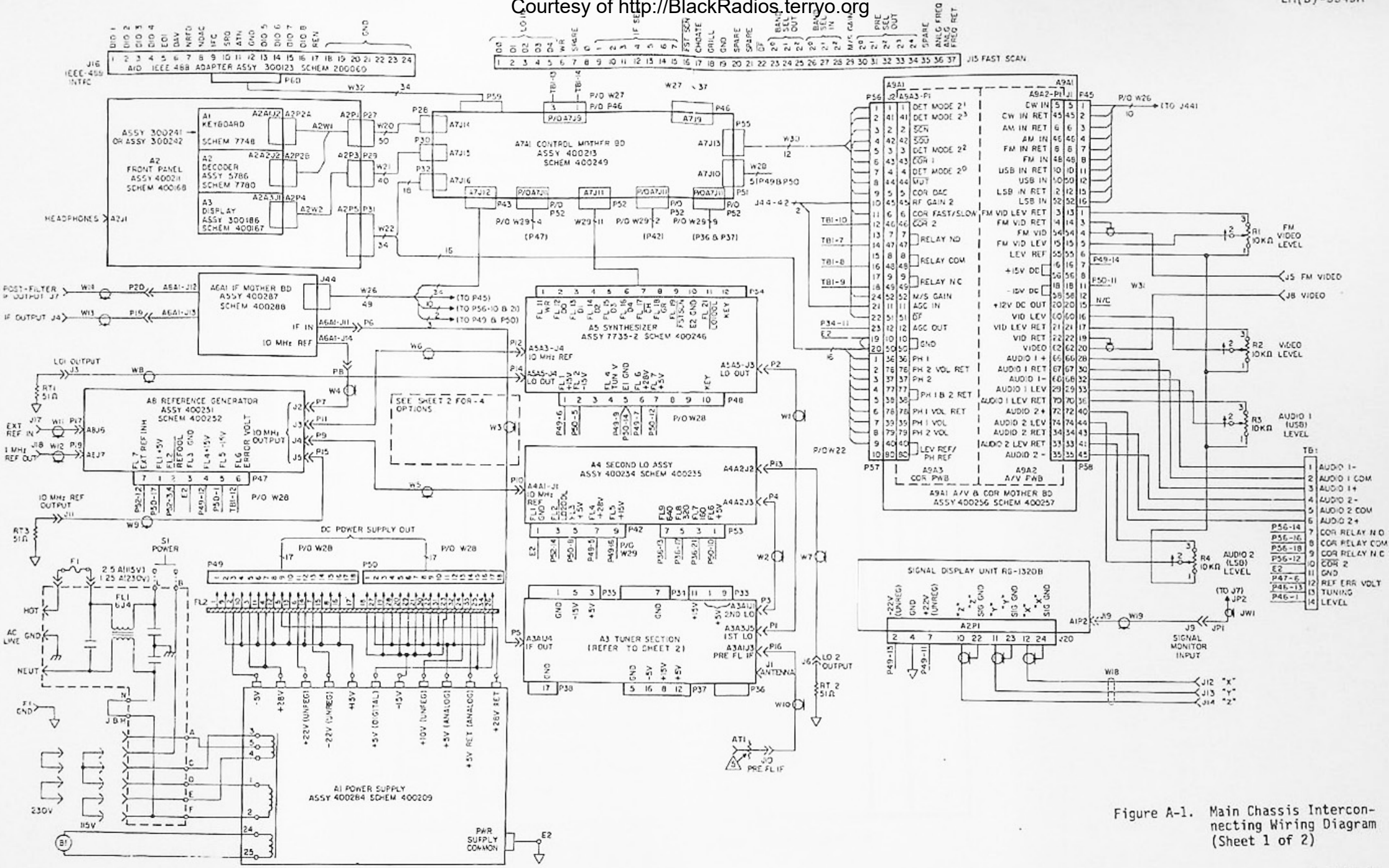


Figure A-1. Main Chassis Interconnecting Wiring Diagram (Sheet 1 of 2)

NOTES
1. INTERPRET DWG PER DOD-STD-100
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT NUMBER OR SUBASSY DESIGNATION
3. THIS DWG TO BE USED IN CONJUNCTION WITH ASSY 400205 WIRE LIST
4. LB DENOTES LOW BAND FREQUENCY RANGING FROM 20 MHz TO 500 MHz
   MB DENOTES MID BAND FREQUENCY RANGING FROM 500 MHz TO 1000 MHz
   HB DENOTES HIGH BAND FREQUENCY RANGING FROM 1000 MHz TO 1800 MHz
△2 ATI IS USED ON -2 AND -3 ASSEMBLIES ONLY

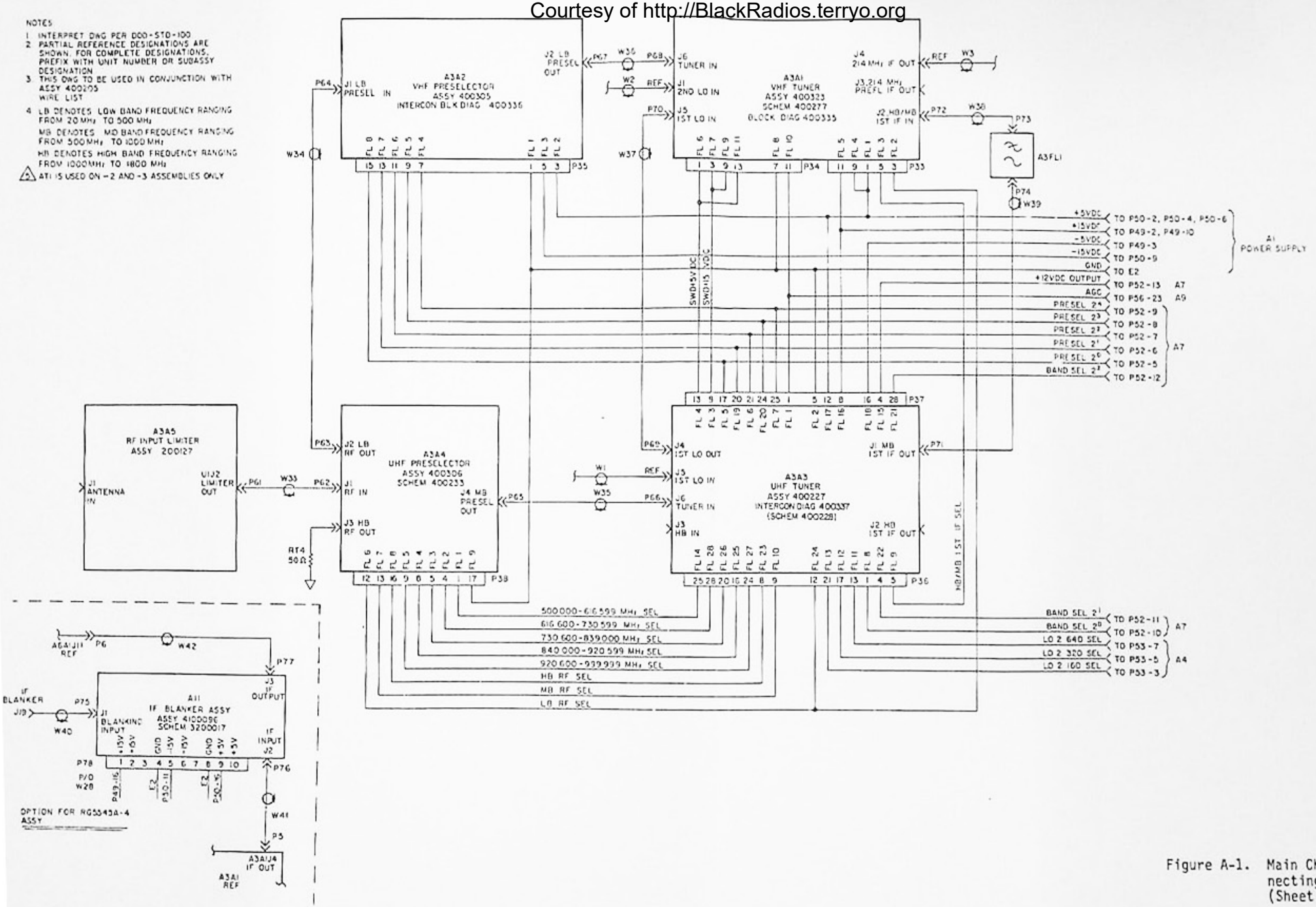


Figure A-1. Main Chassis Interconnecting Wiring Diagram (Sheet 2 of 2)

APPENDIX B

400 kHz IF FILTER AMPLIFIER CIRCUIT CARD ASSEMBLY (A6A3)

Type Number: G5742-26-1 (400 kHz)

Schematic Diagram: Figure B-2

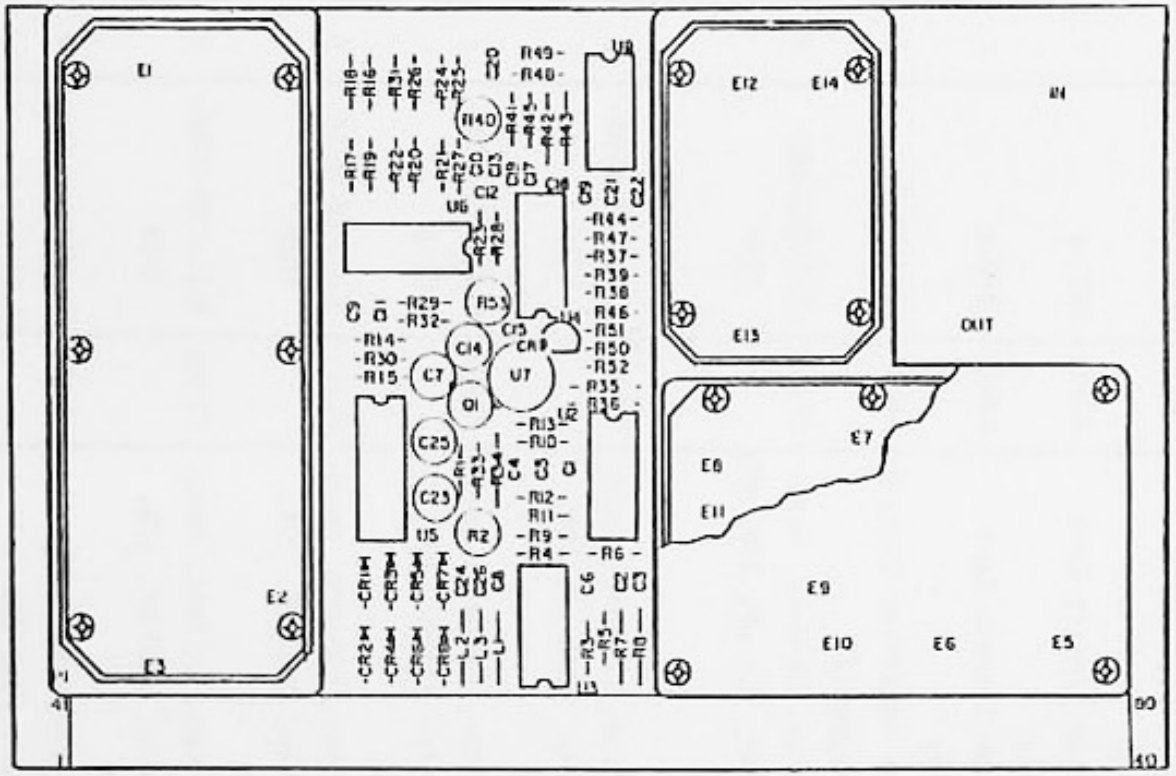


Figure B-1. 400 kHz IF Filter Amplifier Circuit Card Assembly (A6A3)
Component Location Diagram

Table 8-1. 400 kHz IF Amplifier Assembly, Type G5742-26-1 (A6A3)
Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
B-1	A6A3	400 kHz IF Filter Amplifier . Assembly	54805	G5742-26-1	1	
	A1	. IF Filter Circuit Card . . Assembly	54805	5910-26-1	1	
	A2	. AM Detector Circuit Card . . Assembly	54805	5911-1	1	
	A3	. FM Limiter Circuit Card . . Assembly	54805	5912-2	1	
	A4	. IF Filter Amplifier Circuit . . Card Assembly	34805	7849-26-1	1	
	C1,6,8, 11,13, 15, 16, 21,22,	. . Capacitor, Ceramic, Mono- . . . lithic, 0.1 uF, 20%, 50V	72982	8121-050-651-104M	9	
	C9,24 26	. . Capacitor, Ceramic, Mono- . . . lithic, 1000 pF, 10%, . . . 100V	72982	8121-100-X7R0-102K	3	
	C2,17	. . Capacitor, Ceramic, Mono- . . . lithic, 330 pF, 10%, . . . 100V	72982	8101-100-X7R0-331K	2	
	C4,10, 12,19, 3,18	. . Capacitor, Ceramic, Mono- . . . lithic, 0.01 uF, 10%, . . . 100V	72982	8121-100-X7R0 103K	6	
	C5,20	. . Capacitor, Ceramic, Mono- . . . lithic, 3300 pF, 10%, . . . 100V	72982	8121-100-X7R0-332K	2	
	C7,14, 23,25	. . Capacitor, Electrolytic, . . . 15 uF, 20%, 20V	31433	T368B156M020A5	4	
	CR1,2,6, 8,4,5,7	. . Diode	81349	1N4446	7	
	CR3	. . Not Used				
	CR9	. . Diode, Dual	04713	MSD6100	1	

Table B-1. 400 kHz IF Amplifier Assembly, Type G5742-26-1 (A6A3)
Replacement Parts List (Cont.)

FIG. & INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	E1-14	. . Terminal, Pin Connector	71279	460-2946-02-03-00	14	
	L1-3	. . Coil, Fixed, 18 uH	81349	MS75084-15	3	
	P1	. . Connector, 80 Pin	22526	65002-240	1	
	Q1	. . Transistor, PNP	81349	2N2907	1	
	R1,3,5, 16,18-20,22, 24,26, 28,31, 37,39,	. . Resistor, Fixed, Composi- . . . tion, 10 K, 5%, 1/8W	81349	RCR05G103JS	14	
	R2,40,53	. . Resistor, Variable, 10K	19701	8014EMB103E1	3	
	R4	. . Resistor, Fixed, Composi- . . . tion, 6.8K, 5%, 1/8W	81349	RCR05G682JS	1	
	R6	. . Resistor, Fixed, Film, . . . 5.62K, 1%, 1/10W	81349	RN55C5621F	1	
	R7	. . Resistor, Fixed, Film, . . . 1.02K, 1%, 1/10W	81349	RN55C1021F	1	
	R9,13,45	. . Resistor, Fixed, Composi- . . . tion, 47 ohms, 5%, 1/8W	81349	RCR05G470JS	3	
	R10,47	. . Resistor, Fixed, Composi- . . . tion, 68K, 5%, 1/8W	81349	RCR05G683JS	2	
	R11,48	. . Resistor, Fixed, Composi- . . . tion, 15K, 5%, 1/8W	81349	RCR05G153JS	2	
	R12,17, 49	. . Resistor, Fixed, Composi- . . . tion, 5%, 1/8W	81349	RCR05G563JS	3	
	R14	. . Resistor, Fixed, Composi- . . . tion, 2.2K, 5%, 1/8W	81349	RCR05G222JS	1	
	R15	. . Resistor, Fixed, Composi- . . . tion, 100K, 5%, 1/8W	81349	RCR05G104JS	1	
	R21,25, 29,8	. . Resistor, Fixed, Composi- . . . tion, 47K, 5%, 1/8W	81349	RCR05G473JS	4	

Table B-1. 400 kHz IF Amplifier Assembly, Type G5742-26-1 (A6A3) Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	R23,27, 32	. . Resistor, Fixed, Composition, 1K, 5%, 1/8W	81349	RCR05G102JS	3	
	R30	. . Resistor, Fixed, Composition, 1.5K, 5%, 1/8W	81349	RCR05G152JS	1	
	R33,50	. . Resistor, Fixed, Composition, 33K, 5%, 1/8W	81349	RCR05G333JS	2	
	R34	. . Resistor, Fixed, Film, 2.61K, 1%, 1/10W	81349	RN55C2611F	1	
	R35	. . Resistor, Fixed, Film, 237 ohms, 1%, 1/10W	81349	RN55C2370F	1	
	R36	. . Resistor, Fixed, Film, 1.96K, 1%, 1/10W	81349	RN55C1961F	1	
	R38	. . Resistor, Fixed, Composition, 470K, 5%, 1/8W	81349	RCR05G474JS	1	
	R41	. . Resistor, Fixed, Composition, 30K, 5%, 1/8W	81349	RCR05G303JS	1	
	R42	. . Resistor, Fixed, Film, 1.02K, 1%, 1/10W	81349	RN55C1021F	1	
	R43	. . Resistor, Fixed, Film, 4.7K, 1%, 1/10W	81349	RN55C4701F	1	
	R44	. . Resistor, Fixed, Composition, 5.6K, 5%, 1/8W	81349	RCR05G560JS	1	
	R46	. . Resistor, Fixed, Composition, 22K, 5%, 1/8W	81349	RCR05G223JS	1	
	R51	. . Resistor, Fixed, Composition, 12K, 5%, 1/8W	81349	RCR05G123JS	1	
	R52	. . Resistor, Fixed, Composition, 3.9K, 5%, 1/8W	81349	RCR05G392JS	1	
	U1	. . Integrated Circuit, Discriminator	54805	4600024-1	1	
	U2,8	. . Integrated Circuit, Quad Operational Amplifier	23386	LF347	2	
	U3,4	. . Integrated Circuit, Dual MOSFET Switch	17856	OG-200CJ	2	

Table B-1. 400 kHz IF Amplifier Assembly, Type G5742-26-1 (A6A3)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	U5	. . Integrated Circuit, . . . Hex Inverter	02735	CD4049UB	1	
	U6	. . Integrated Circuit, Quad . . . Operational Amplifier	01295	TL074CP	1	
	U7	. . Integrated Circuit, . . . Adjustable Regulator	27014	LM317H	1	
	XU1	. . Not Used				
	XU2-4,6	. . Socket, Integrated . . . Circuit, 14 Pin*	06776	ICL-143-S6-T	5	
	XU5	. . Socket, Integrated . . . Circuit, 16 Pin*	06776	ICL-163-S6-T	1	
	XU7	. . Transipad*	13103	7717-220AP	1	
	W1	. Cable Assembly	54805		1	

*NOTE: These components are not shown on illustration.

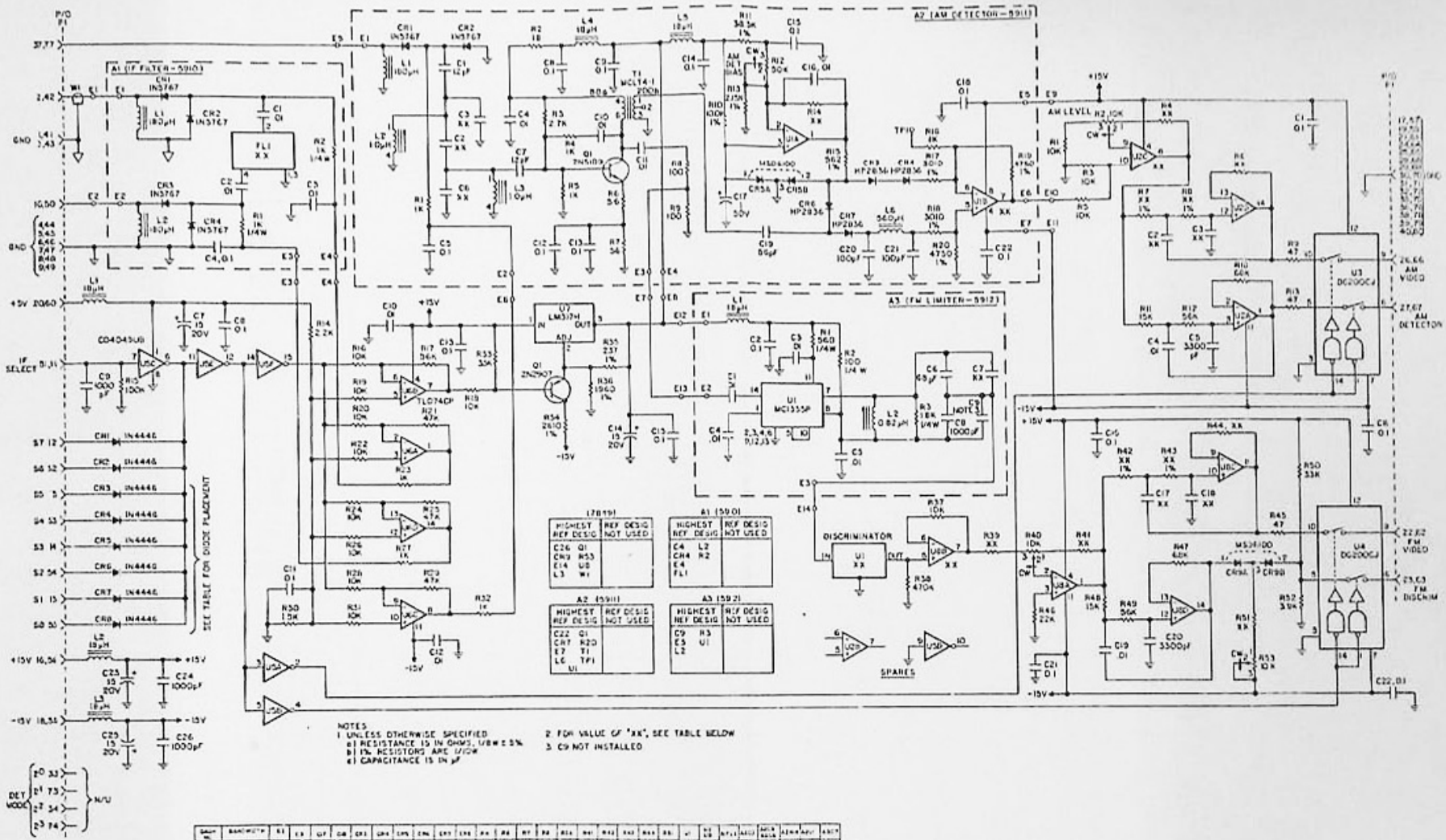


Figure B-2. 400 kHz IF Filter Amplifier Circuit Card Assembly (A6A3) Schematic Diagram

APPENDIX C

USB DEMODULATOR CIRCUIT CARD ASSEMBLY (A6A7)

Type Number: 5748

Schematic Diagram: Figure C-2 (7732)

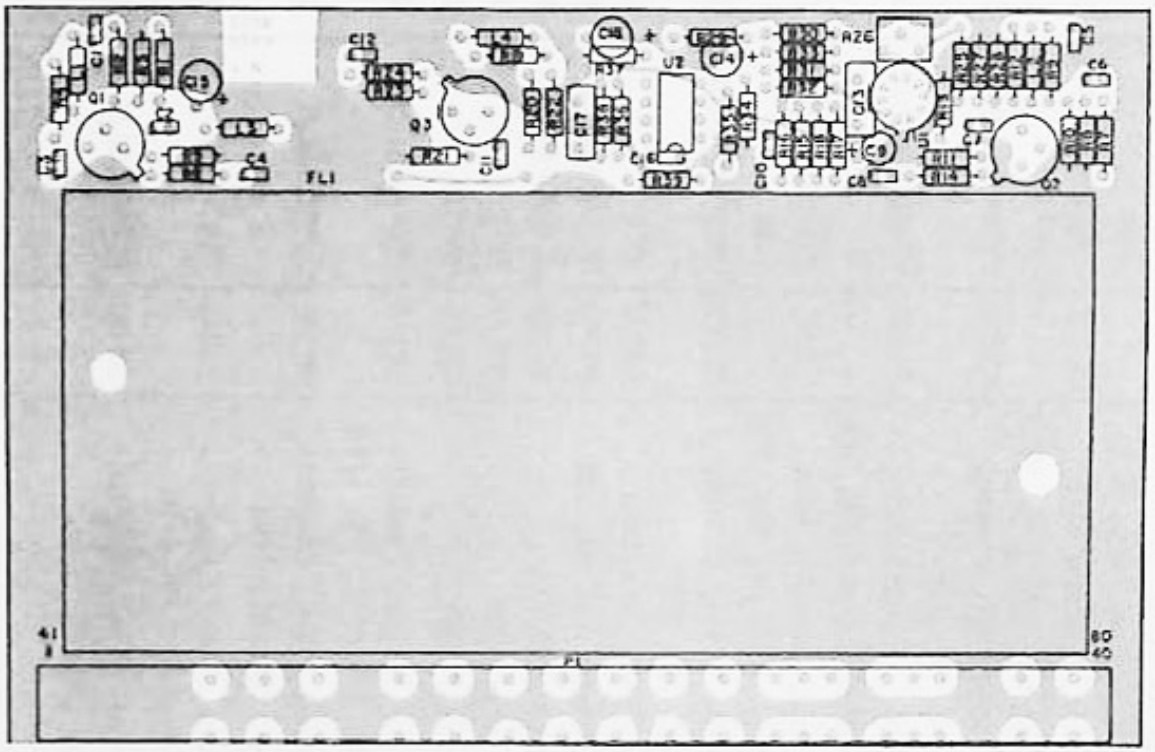


Figure C-1. USB Demodulator (A6A7) Component Location

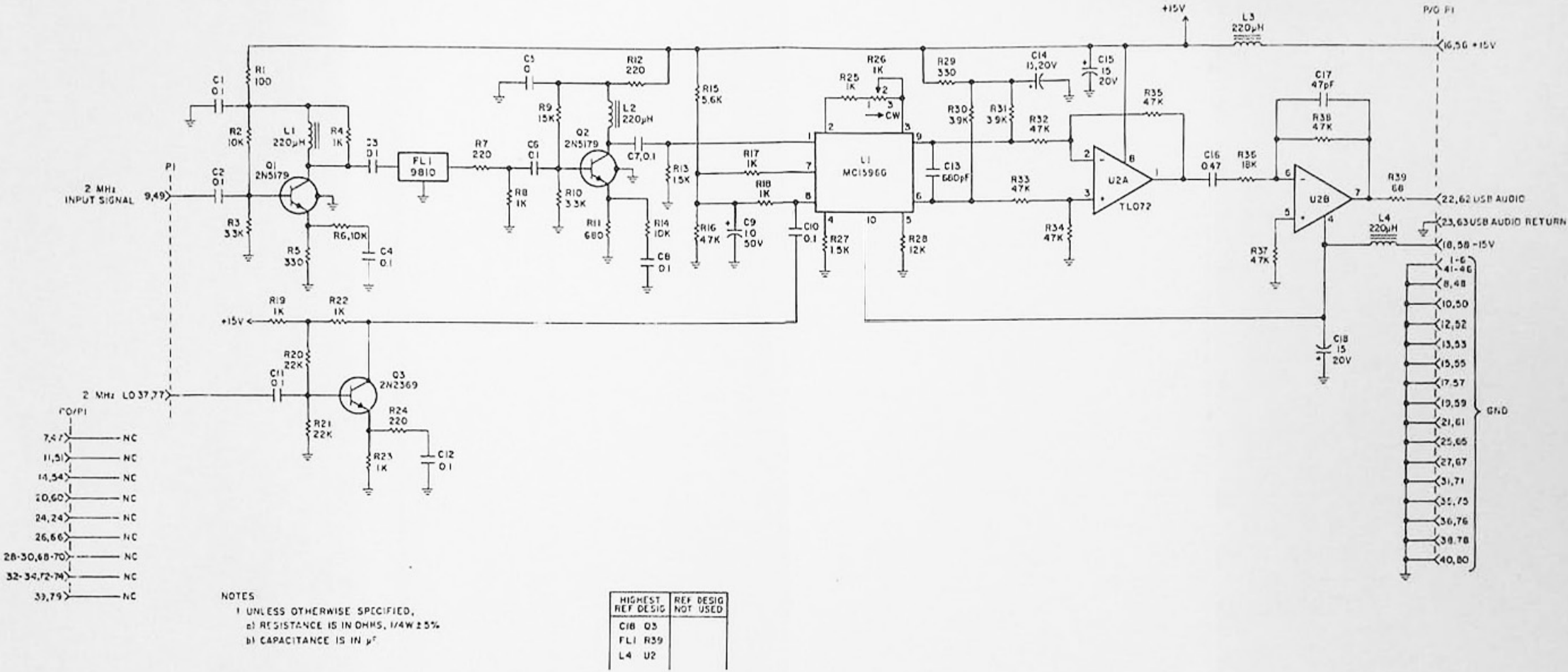
Table C-1. USB Demodulator Circuit Card Assembly (A6A7), Type 5748, Replacement Parts List

FIG. & INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
C-1	A6A7	USB Demodulator Circuit Card Assembly	54805	5748	1	
	C1-8, I0-12	. Capacitor, Ceramic, Mono- . . lithic 0.1 μF, 20%, 50V	72982	8121-050-651-104M	11	
	C9	. Capacitor, Electrolytic, . . Tantalum, 1 μF, 20%, 50V	31433	T368A105M050A9	1	
	C13	. Capacitor, Mica, Dipped, . . 680 pF, 5%, 500V	81349	CM06FD681J03	1	
	C14-15 18	. Capacitor, Electrolytic, . . Tantalum, 15 μF, 20%, 20V	31433	T368B156M020AS	3	
	C16	. Capacitor, Ceramic, Mono- . . lithic, 0.47 μF, 20%, 20V	72982	8121-050-651-474M	1	
	C17	. Capacitor, Mica, Dipped, . . 47 pF, 5%, 500V	81349	CM05FD470J03	1	
	FL1	. Filter, USB, Equalized	54805	9810	1	
	L1-4	. Coil, Fixed, 220 μH, 10%	81349	MS75085-11	4	
	P1	. Connector, 80 Pin	22526	65002-240	1	
	Q1-2	. Transistor, NPN	80131	2N5179	2	
	Q3	. Transistor, NPN	80131	2N2369	1	
	R1	. Resistor, Fixed, Composi- . . tion, 100 ohms, 5%, 1/4W	81349	RCR07G101JS	1	
	R2,6 14	. Resistor, Fixed, Composi- . . tion, 10K, 5%, 1/4W	81349	RCR07G103JS	3	
	R3,10	. Resistor, Fixed, Composi- . . tion, 3.3K, 5%, 1/4W	81349	RCR07G332JS	2	
	R4,8, 17-19 22-23, 25	. Resistor, Fixed, Composi- . . tion, 1K, 5%, 1/4W	81349	RCR07G102JS	8	
	R5,29	. Resistor, Fixed, Composi- . . tion, 330 ohms, 5%, 1/4W	81349	RCR07G331JS	2	
	R7,12, 24	. Resistor, Fixed, Composi- . . tion, 220 ohms, 5%, 1/4W	81349	RCR07G221JS	3	

Table C-1. USB Demodulator Circuit Card Assembly (A6A7), Type 5748
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	R9	. Resistor, Fixed, Composi- . . tion, 15K, 5%, 1/4W	81349	RCR07G153JS	1	
	R11	. Resistor, Fixed, Composi- . . tion, 680 ohms, 5%, 1/4W	81349	RCR07G681JS	1	
	R13,27	. Resistor, Fixed, Composi- . . tion, 1.5K, 5%, 1/4W	81349	RCR07G152JS	1	
	R15	. Resistor, Fixed, Composi- . . tion, 5.6K, 5%, 1/4W	81349	RCR07G562JS	1	
	R16	. Resistor, Fixed, Composi- . . tion, 4.7K, 5%, 1/4W	81349	RCR07G472JS	1	
	R20-21	. Resistor, Fixed, Composi- . . tion, 22K, 5%, 1/4W	81349	RCR07G223JS	1	
	R26	. Resistor, Variable, . . 1K, 20%, 1/2W	19701	8014EMU1102E	1	
	R28	. Resistor, Fixed, Composi- . . tion, 12K, 5%, 1/4W	81349	RCR07G123JS	1	
	R30-31	. Resistor, Fixed, Composi- . . tion, 3.9K, 5%, 1/4W	81349	RCR07G392JS	1	
	R32-35, 37-38	. Resistor, Fixed, Composi- . . tion, 47K, 5%, 1/4W	81349	RCR07G473JS	6	
	R36	. Resistor, Fixed, Composi- . . tion, 18K, 5%, 1/4W	81349	RCR07G183JS	1	
	R39	. Resistor, Fixed, Composi- . . tion, 68 ohms, 5%, 1/4W	81349	RCR07G680JS	1	
	U1	. Integrated Circuit, Bal- . . anced Modulator/Demodu- . . lator	04713	MC1596G	1	
	U2	. Integrated Circuit, Dual . . Operational Amplifier	01295	TL072CP	1	
	XU1	. Socket, 10 Pin, Round*	91506	805-9-2G10	1	
	XU2	. Socket, 8 Pin, DIP*	06776	ICL-083-S6-T	1	

*NOTE: This component is not shown on illustration.



NOTES

1. UNLESS OTHERWISE SPECIFIED,
   a) RESISTANCE IS IN OHMS, 1/4W ±5%
   b) CAPACITANCE IS IN µF

HIGHEST REF DESIG	REF DESIG NOT USED
C18 Q3	
FL1 R39	
L4 U2	

Figure C-2. USB Demodulator Circuit Card Assembly (A6A7) Schematic Diagram

APPENDIX D

LSB DEMODULATOR CIRCUIT CARD ASSEMBLY (A6A9)

Type Number: 5749

Schematic Diagram: Figure D-2 (7733)

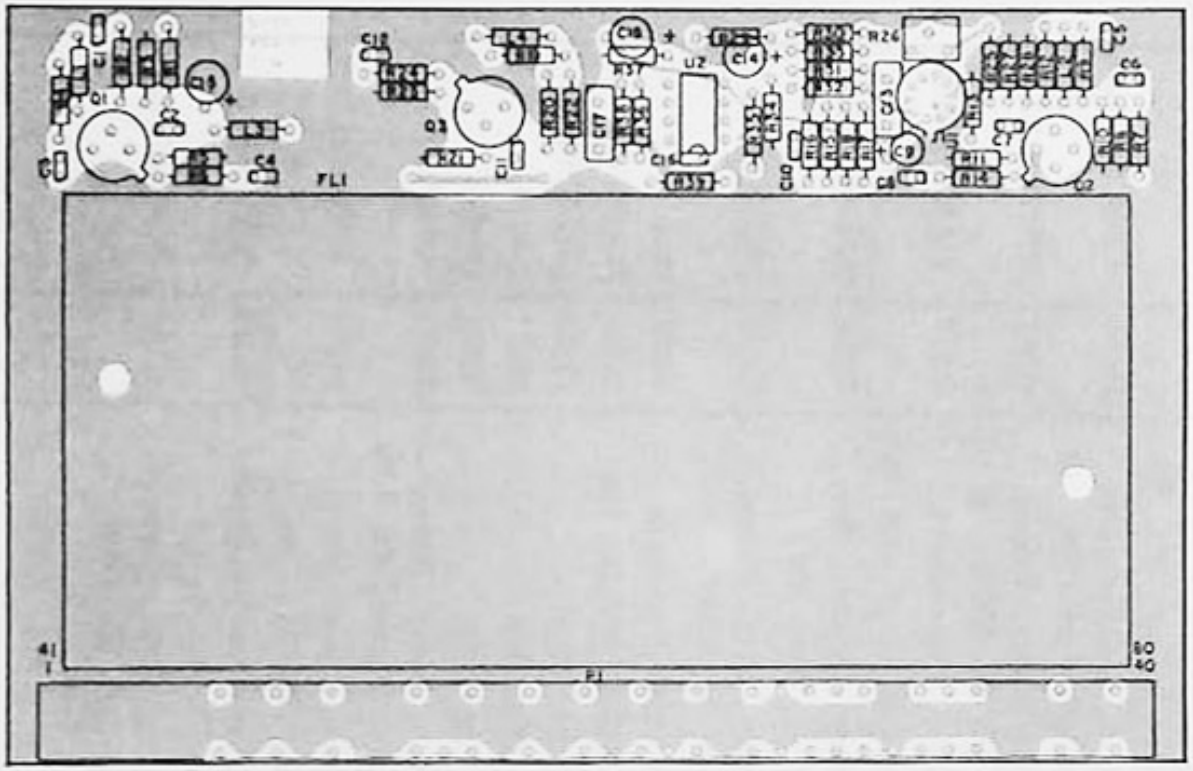


Figure D-1. LSB Demodulator (A6A9) Component Location

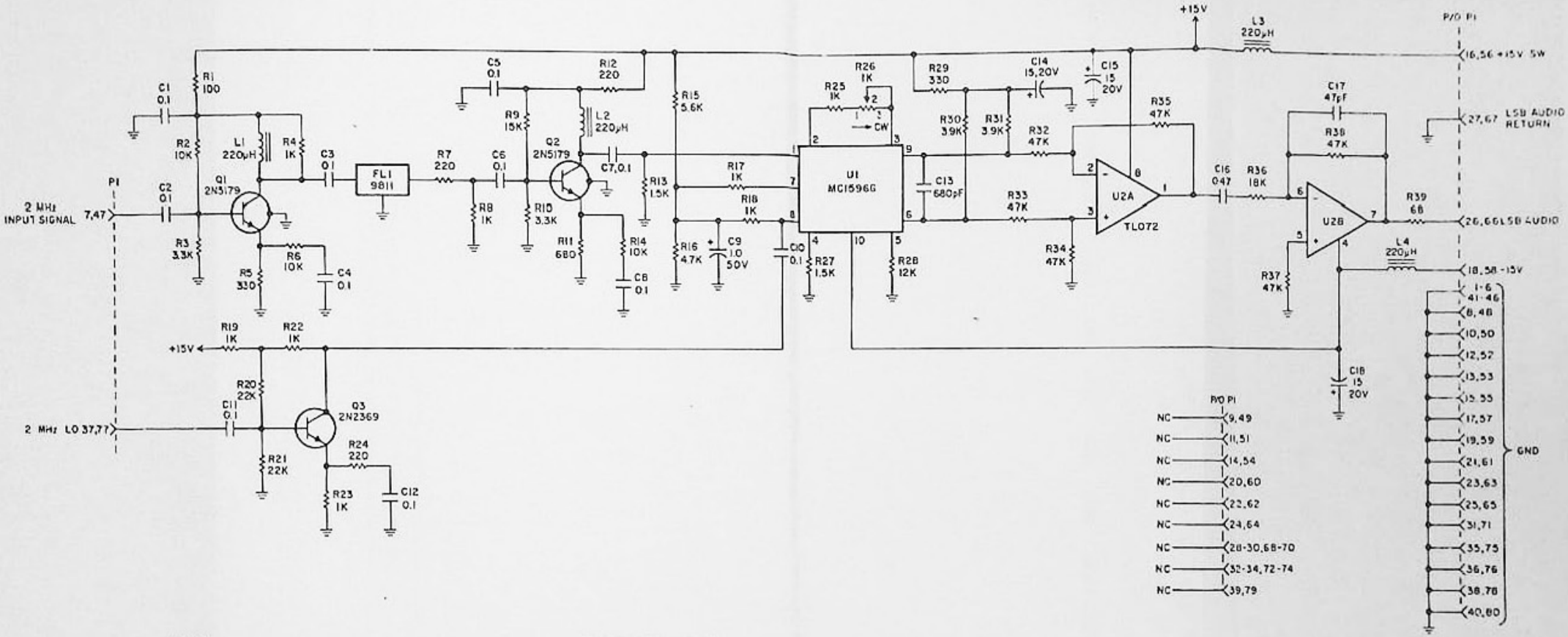
Table D-1. LSB Demodulator Circuit Card Assembly (A6A9), Type 5749 Replacement Parts List

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
D-1	A6A9	LSB Demodulator Circuit . Card Assembly	54805	5749		
	C1-8, 10-12	. Capacitor, Ceramic, Mono- . . lithic, 0.1 μF, 20%, 50V	72982	8121-050-651-104M		
	C9	. Capacitor, Electrolytic, . . Tantalum, 1 μF, 20%, 50V	31433	T368A105M050AS		
	C13	. Capacitor, Mica, Dipped, . . 680 pF, 5%, 500V	81349	CM06FD681J03		
	C14-15, 18	. Capacitor, Electrolytic, . . Tantalum, 15 μF, 20%, 20V	31433	T368B156M020AS		
	C16	. Capacitor, Ceramic, Disc, . . 0.47 μF, 20%, 50V	72982	8131-050-651-474M		
	C17	. Capacitor, Mica, Dipped, . . 47 pF, 5%, 500V	81349	CM05FD470J03		
	FL1	. Filter, LSB, Equalized	54805	9811		
	L1-4	. Coil, Fixed, 220 μH, 10%	81349	MS75085-11		
	P1	. Connector, 80 Pin	22526	65002-240		
	Q1-2	. Transistor, NPN	80131	2N5179		
	Q3	. Transistor, NPN	80131	2N2369		
	R1	. Resistor, Fixed, Composi- . . tion, 100 ohms, 5%, 1/4W	81349	RCR07G101JS		
	R2,6, 14	. Resistor, Fixed, Composi- . . tion, 10K, 5%, 1/4W	81349	RCR07G103JS		
	R3,10	. Resistor, Fixed, Composi- . . tion, 3.3K, 5%, 1/4W	81349	RCR07G332JS		
	R4,8, 17-19, 22-23, 25	. Resistor, Fixed, Composi- . . tion, 1K, 5%, 1/4W	81349	RCR07G102JS		
	R5,29	. Resistor, Fixed, Composi- . . tion, 330 ohms, 5%, 1/4W	81349	RCR07G221JS		
	R7,12, 24	. Resistor, Fixed, Composi- . . tion, 220 ohms, 5%, 1/4W	81349	RCR07G221JS		
	R9	. Resistor, Fixed, Composi- . . tion, 15K, 5%, 1/4W	81349	RCR07G221JS		

Table D-1. LSB Demodulator Circuit Card Assembly (A6A9), Type 5749
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	R11	. Resistor, Fixed, Composi- . . tion, 680 ohms, 5%, 1/4W	81349	RCR07G153JS		
	R13,27	. Resistor, Fixed, Composi- . . tion, 1.5K, 5%, 1/4W	81349	RCR07G681JS		
	R15	. Resistor, Fixed, Composi- . . tion 5.6K, 5%, 1/4W	81349	RCR07G562JS		
	R16	. Resistor, Fixed, Composi- . . tion, 4.7K, 5%, 1/4W	81349	RCR07G472JS		
	R20-21	. Resistor, Fixed, Composi- . . tion, 22K, 5%, 1/4W	81349	RCR07G223JS		
	R26	. Resistor, Variable, . . 1K, 20%, 1/2W	19701	8014EMU102E1		
	R28	. Resistor, Fixed, Composi- . . tion, 12K, 5%, 1/4W	81349	RCR07G123JS		
	R30-31	. Resistor, Fixed, Composi- . . tion, 3.9K, 5%, 1/4W	81349	RCR07G392JS		
	R32-35, 37-38	. Resistor, Fixed Composi- . . tion, 47K, 5%, 1/4W	81349	RCR07G473JS		
	R36	. Resistor, Fixed, Composi- . . tion, 18K, 5%, 1/4W	81349	RCR07G183JS		
	R39	. Resistor, Fixed, Composi- . . tion, 68 ohms, 5%, 1/4W	81349	RCR07G680JS		
	U1	. Integrated Circuit, Bal- . . anced Modulator/Demodu- . . lator	04713	MC1596G		
	U2	. Integrated Circuit, Dual . . Operational Amplifier	01295	TL072CP		
	XU1	. Socket, 10 Pin, Round*	91506	8059-2G10		
	XU2	. Socket, 8 Pin, DIP*	06776	ICL-083-S6-T		

*NOTE: This component is not shown on illustration.



NOTES:

1. UNLESS OTHERWISE SPECIFIED;
   a) RESISTANCE IS IN OHMS, 1/4W ±5%.
   b) CAPACITANCE IS IN μF.

HIGHEST REF DESIG	REF DESIG NOT USED
C18 Q3	
FL1 R39	
L4 U2	

Figure D-2. LSB Demodulator Circuit Card Assembly (A6A9) Schematic Diagram

APPENDIX E

IF BLANKER CIRCUIT CARD ASSEMBLY (A11)

Type Number: 4100096-501

Schematic Diagram: Figure E-2 (3200017)

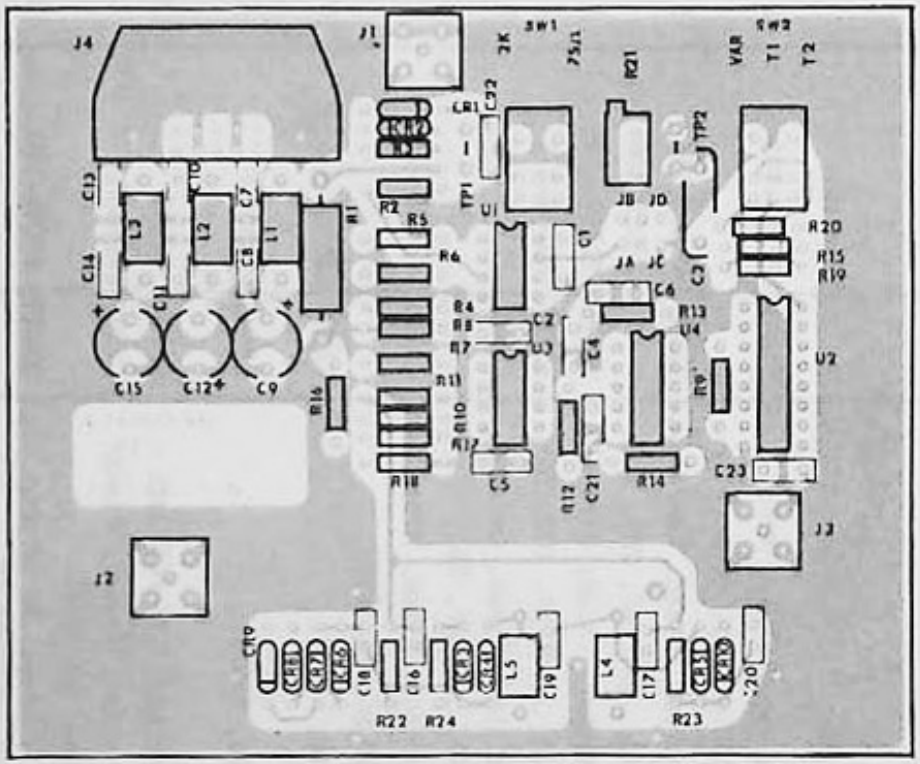


Figure E-1. IF Blanker Circuit Card Assembly (A11) Component Location Diagrams

Table E-1. IF Blanker Circuit Card Assembly (A11)
Replacement Parts List

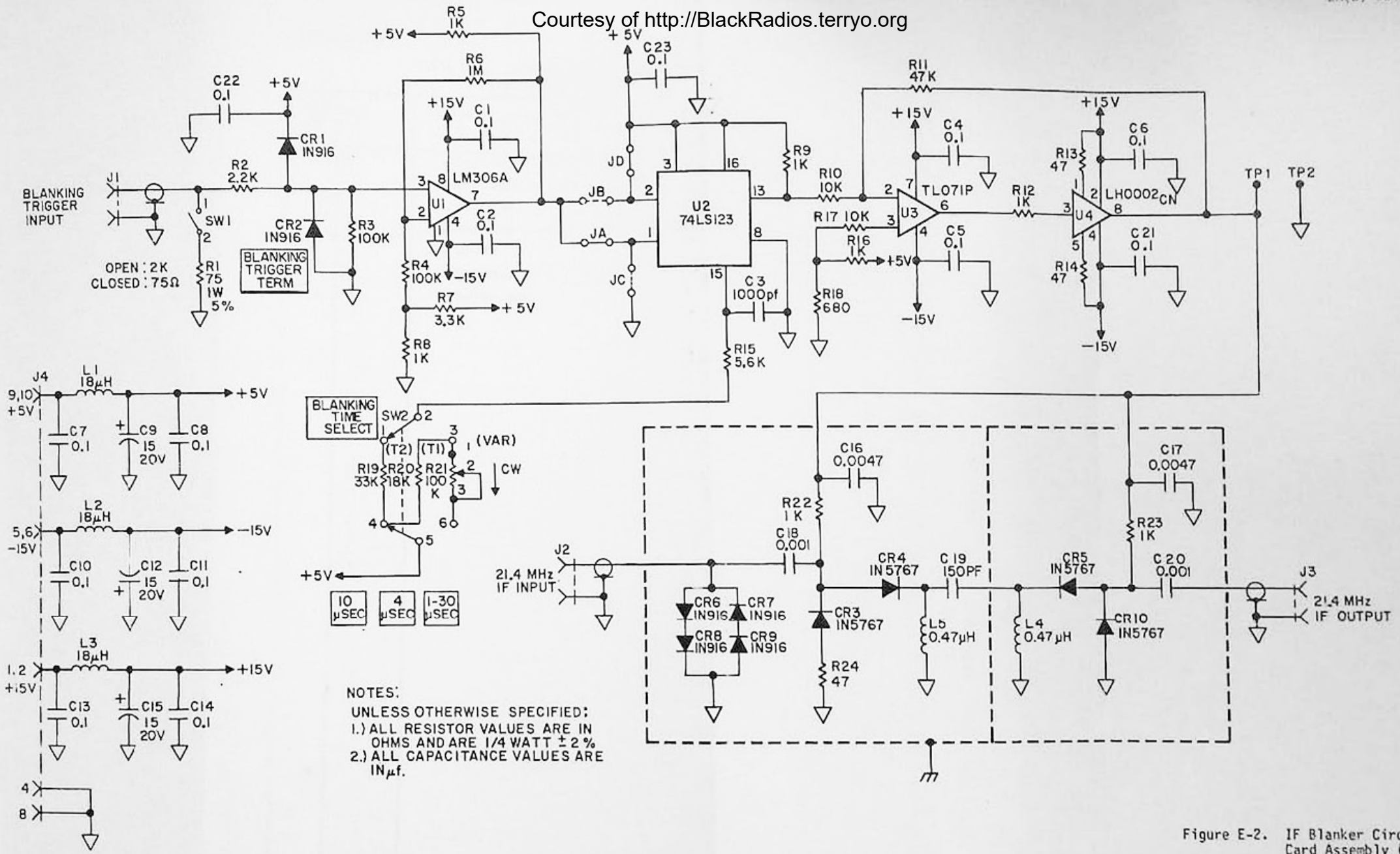
FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
E-1	A11	IF Blanker Circuit Card . Assembly	23386	4100096-501	1	
	C1,2, 4-8, 10,11, 13,14, 21,22, 23	. Capacitor, Fixed, Ceramic, . . Z5U, 0.1 μF, 20%, 50V	23386	21795-104	14	
	C3	. Capacitor, Fixed, Mica, . . 1000 pF, 2%, 500V	23386	22373-102	1	
	C9,12, 15	. Capacitor, Fixed, Tantalum, . . Z5U, .0047 μF, 20%, 50V	23386	25062-156 25062-156	3	
	C16,17	. Capacitor, Fixed, Ceramic,	23386	21789-472	2	
		. . Z5U, .0047 μF, 20%, 50V	23386	21789-472	2	
	C18,20	. Capacitor, Fixed, Ceramic, . . NP0, .001 μF, 5%	23386	21361-102	2	
	C19	. Capacitor, Fixed, Mica, . . 150 pF, 2%, 500V	23386	22372-151	1	
	CR1-2, 6-9	. Diode, 1N916	23386	35514	6	
	CR3-5, 10	. Diode, 1N5767	23386	36021	4	
	J1-3	. Connector, SMB PCB Jack	23386	60044	3	
	J4	. Connector, Header, Right . . Angle 10 Cont.	23386	61238	1	
	L1-3	. Coil, Fixed, RF 18 μH, . . 10%, MS75084-15	23386	43062-180	3	
	L4-5	. Coil, Fixed, RF .47 μH, . . 10%, MS75083-9	23386	43062-R47	2	
	R1	. Resistor, Fixed, Film, . . 2.2K, 2% 1/4W	23386	12161-222	1	
	R2-3	. Resistor, Fixed, Film, . . 2.2K, 2%, 1/4W	23386	12161-222	2	

Table E-1. IF Blanker Circuit Card Assembly (A11)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	R4	. Resistor, Fixed, Film, . . 1K, 2%, 1/4W	23386	12161-102	1	
	R5,8, 9,12, 16,22, 23	. Resistor, Fixed, Film, . . 1K, 2%, 1/4W	23386	12161-102	7	
	R6	. Resistor, Fixed, Film, . . 1M, 2%, 1/4W	23386	12161-104	1	
	R7	. Resistor, Fixed, Film, . . 3.3K, 2%, 1/4W	23386	12161-332	1	
	R10,17	. Resistor, Fixed, Film, . . 10K, 2%, 1/4W	23386	12161-103	2	
	R11	. Resistor, Fixed, Film, . . 47 ohm, 2%, 1/4W	23386	12161-473	1	
	R13,14, 24	. Resistor, Fixed, Film, . . 47 ohm, 2%, 1/4W	23386	12161-470	3	
	R15	. Resitor, Fixed, Film, . . 5.6K, 2%, 1/4W	23386	12161-562	1	
	R18	. Resistor, Fixed, Film, . . 33K, 2%, 1/4W	23386	12161-681	1	
	R19	. Resistor, Fixed, Film, . . 18K, 2%, 1/4W	23386	12161-333	1	
	R20	. Resistor, Fixed, Film, . . 18K, 2%, 1/4W	23386	12161-183	1	
	R21	. Resistor, Variable, PCB, . . Cermet Lin Mulit-turn . . 100K, 10%, 1/2W	23386	16110-104	1	
	S1	. Switch Toggle PCB DPDT	23386	50025	1	
	S2	. Switch, Toggle, PCB, DPDT . . 3 POS	23386	50024	1	
	TP1-2	. Test Point	23386	70125	2	
	U1	. Integrated Circuit, LM306, . . Voltage Comparator	23386	365029	1	

Table E-1. IF Blanker Circuit Card Assembly (A11)
Replacement Parts List (Cont.)

FIG.& INDEX NO.	REF. DESIG.	COMPONENT DESCRIPTION 1 2 3 4 5 6 7	FSCM	MFR. PART NO.	QTY.	USABLE ON CODE
	U2	. Integrated Circuit, 74LS123 . . Dual Retrig. Mono Multi- . . vibrator	23386	36885-123	1	
	U3	. Integrated Circuit, TL071, . . OP-AMP	23386	36985	1	
	U4	. Integrated Cricuit, LH002, . . Buffer Amp.	23386	36663	1	



NOTES:

UNLESS OTHERWISE SPECIFIED:

1.) ALL RESISTOR VALUES ARE IN OHMS AND ARE 1/4 WATT ± 2 %

2.) ALL CAPACITANCE VALUES ARE IN μf.

Figure E-2. IF Blanker Circuit Card Assembly (A11) Schematic Diagram